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A Low Voltage Low Power Highly Linear CMOS Quadrature Mixer Using Transconductance Cancellation Technique

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Abstract — This paper presents a low voltage low power high linearity quadrature mixer for software defined radio applications in a 90nm CMOS technology. A 7-dB improvement of input-referred 3rd-order intermodulation point (IIP₃) is achieved by using a differential g_m'' (the second derivation of transconductance) canceling technology. The negative value of g_m'' in saturated pseudo differential transistor (PDT) is compensated by the positive value of PDT in subthreshold region. The even-order distortion is eliminated by differential PDTs. The mixer consumes a dc power of only 3.8 mW under 1V supply. The conversion gain with 10 samples is 3.6~7.2 dB in the frequency range of 0.3~6 GHz. The IIP₃ is 7.9~12.3 dBm 0.3~6 GHz, whereas the single-sideband noise figure (SSB NF) is 11.1~14.7 dB.

Index Terms — Mixer, low voltage, low power, high linearity, pseudo differential transistor (PDT), CMOS; software defined radio (SDR).

I. INTRODUCTION

Since the energy-efficiency software radio is still a great challenge in a long time. The most practical solution is reconfigurable RF front-ends can be widely programmed to operate with all present and future standards [1], [2]. The RF front-end must be very flexible, to serve all communication standards in a cost-efficiency way. These standards include wireless local personal networks (e.g. Bluetooth), wireless local area networks (e.g. WLAN 802.11a, b, g, j, n), cellular networks (e.g. GSM, UMTS), digital broadcasting (e.g. DAB, DVB-TH), and positioning systems (e.g. GPS). As the required receiver needs to deal with the signals with input frequency from tens of MHz up to several GHz, nonlinearity may cause many problems, such as harmonic distortions, gain compression, blocking, cross modulation and inter-modulation, etc. The even-order distortion can easily be reduced by using differential signal process, but it is very difficult to reduce the odd-order distortions. The 3rd-order inter-modulation distortion IM₃ is the most dominant nonlinearity component. The linearity performance of mixer is expressed by the input-referred 3rd-order inter-modulation point (IIP₃) divided by the DC power consumption P_{DC} (IIP₃/P_{DC}). The IIP₃ is usually proportional to P_{DC}. Therefore, it is a great challenge to increase IIP₃/P_{DC} for low power SDR systems.

In order to maximize the IIP₃/P_{DC}, some linearity improvement techniques are employed [3]-[5]. Most of them are based on negative feedback circuit using degeneration by resistors and inductors. Although the IIP₃ is enhanced by this method, it suffers from gain reduction. The passive mixer can provide high IIP₃, but it suffers from the large conversion loss. Single-ended multiple gated transistors (MGTR) can be used to cancel the g_m'' in amplifier [6], however, it suffer from high even-order distortion. A transconductance linearization technique called differential multiple gated transistors (DMGTR) has been used to improve the IIP₃/P_{DC} in programmable gain amplifier design [7]. The negative value of g_m'' which degrades the linearity in fully differential transistors (FDT) can be compensated with a positive value of g_m'' in pseudo differential transistors (PDT). However, for FDT, there must be four-stage components stacked from power supply to ground, including tail current source, g_m stage, switch stage, and load. This makes low-voltage low-power design unattainable.

In this paper, a low voltage low power IIP₃ improved quadrature down-conversion mixer with differential PDTs working in saturated and subthreshold region is present. With differential PDTs, high even-order distortion and large power consumption issues in previous work [6], [7] can be solved. To our best knowledge, this is the first paper simultaneously achieving low voltage low power high linearity performances with proposed differential PDTs.

II. MIXER DESIGN

Generally, the non-linearity of mixer is mostly caused by the input transconductance cell. Unlike the large signal distortion caused by gain compression which can be eliminated by the automatic gain control (AGC) loop, the small signal non-linearity will greatly affect the quality of wanted signal. The g_m'' which is inversely proportional to the IIP₃ is introduced to evaluate the small signal non-linearity [8]. The IIP₃ of the device can be improved by reducing g_m'' effectively.

The schematic of proposed quadrature mixer is shown in Fig.1. The input transconductance cell consists of two PDTs, M₁-M₄. M₁ and M₂ is biased in saturation region by v_{b1} , while the M₃ and M₄ is biased in the subthreshold region by v_{b2} . M₅-M₁₂ are switch cells connected to quadrature LO and IF. The I

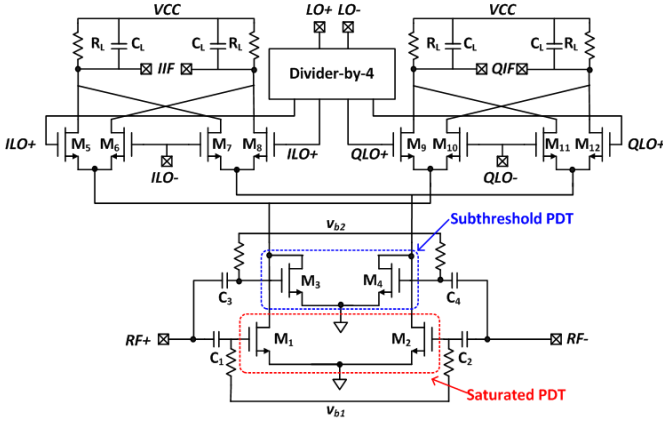


Fig. 1. Schematic of proposed quadrature mixer

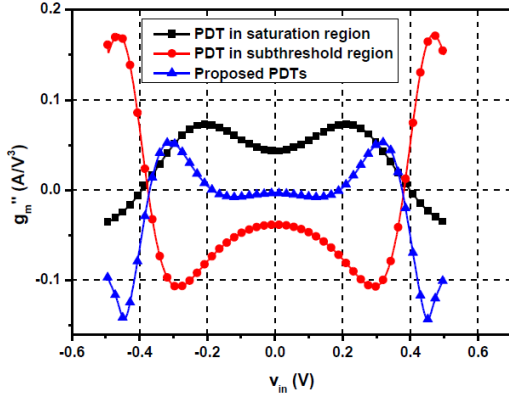


Fig. 2. g_m'' versus differential input voltage in the PDTs

and Q switch cells share one transconductance cell to decreasing the power consumption. The load R_L and C_L is designed to achieve proper gain as well as filtering the high frequency harmonics at the IF frequency. Neglecting channel-length modulation effect, the drain current I_D of M_1 and M_2 shows square law to V_{GS} , $I_D = (\mu_n C_{ox}/2) \times (W/L) \times (V_{GS} - V_{TH})^2$. For small signal linearity consideration, while $v_{in}=0$, the g_m'' is given as:

$$g_m''|_{\Delta v_{in}=0} = \frac{-3}{4\sqrt{I_{SS}}} \left(\mu_n C_{ox} \frac{W}{L} \right)^{\frac{3}{2}} < 0 \quad (1)$$

where the v_{in} equals to $v_{RF+} - v_{RF-}$. The μ_n and C_{ox} is process related parameters. I_{SS} is the total current of PDT M_1 and M_2 .

Then assume the voltages at the PDT M_3 and M_4 are $v_{b2} \pm \Delta v_{in}/2$, where v_{b2} is bias voltage and Δv_{in} is small signal voltage. Since the current of MOSFET in subthreshold region is $I_D = I_0 e^{(v_{GS}/\xi V_T)}$, where $\xi > 1$ is a non-ideal factor, I_0 is a parameter related to process, V_T is thermal voltage. For small signal linearity consideration, while $v_{in}=0$, the g_m'' is given as:

$$g_m''|_{\Delta v_{in}=0} = \frac{I_0}{4(\xi V_T)^3} e^{\frac{v_b}{\xi V_T}} > 0 \quad (2)$$

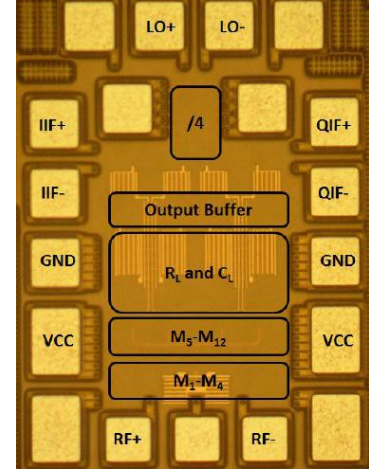


Fig. 3. Microphotograph of quadrature mixer

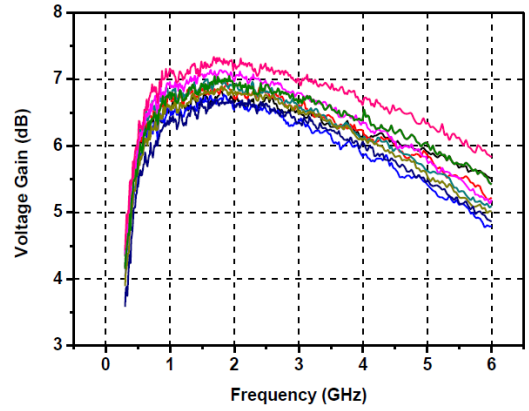


Fig. 4. Measured voltage gain (10 samples)

According to equation (1) and (2), by adjusting W/L and bias voltage v_{b1} and v_{b2} in PDT, g_m'' can be set to nearly zero. Consequently, the highest IIP₃ can be achieved. Compared to the previous work [6]-[9], transconductance cancellation condition can be easily established by hand calculation instead of simulation.

The transistor size of M_1 and M_2 is set to be $15\mu\text{m}/0.1\mu\text{m}$, and the size of M_3 and M_4 is $38\mu\text{m}/0.1\mu\text{m}$. The current of saturation PDT is 3.5 mA, while the current of subthreshold PDT is 80 μA . And, the g_m'' for saturation PDT and subthreshold PDT is approximate $-0.04\text{A}/\text{V}^3$ and $0.04\text{A}/\text{V}^3$.

Fig.2 shows the simulated g_m'' versus differential input voltage in the PDTs. In small signal operation region, the negative value of g_m'' which degrades the linearity in saturation PDT can be compensated with a positive value of g_m'' in subthreshold PDT. Since the performance of mixer mainly depend on saturation PDT, the linearity is greatly improved by this method without sacrificing other performance like NF, gain, and power consumption.

III. IMPLEMENTATION AND MEASUREMENT RESULTS

The mixer was fabricated in a low-cost 90-nm CMOS process. The microphotograph of the fabricated LNA is shown

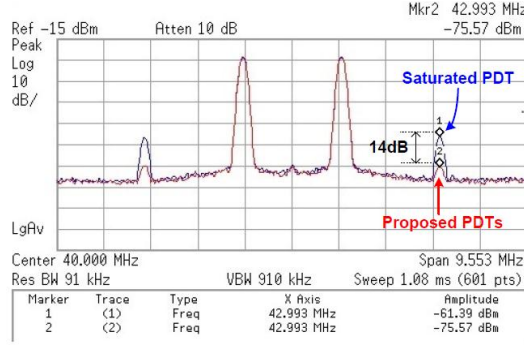


Fig. 5. Measured result of two-tone intermodulation test

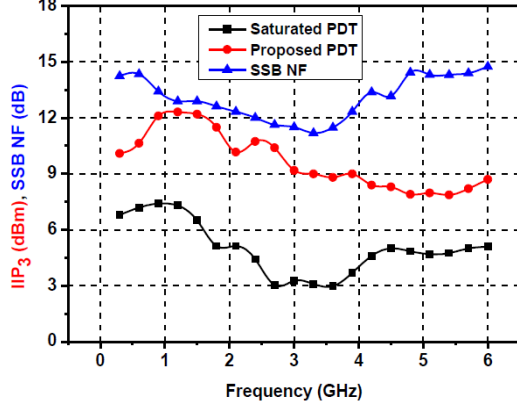


Fig. 6. Measured IIP₃ improvement and SSB NF

in Fig. 3. All pins are ESD-protected using PN diodes. The dimension of the chip including PAD is 640 μ m \times 450 μ m. The VCC is feed to the chip symmetrically to decrease the imbalance of I and Q mixer. A divider-by-4 circuit is designed to convert the differential LO signal to the quadrature signals. The total DC power consumption is 3.8 mW under 1V supply.

Fig.4 shows the measure voltage gain with 10 samples. The maximum gain is 7.2 dB at 1.7 GHz, and the minimum gain is 3.6 dB at 300MHz. The 3dB gain bandwidth for each sample can easily cover the interested 300MHz to 6GHz frequency range. The gain reduction in low frequency band is caused by the on-chip BIAS-T at input. The capacitors in BIAS-T can't be designed large enough for the area limitation. Because of C_{gs} and C_{gd} , the gain drops at high frequency. Fig.5 shows the measurement result of two-tone intermodulation test. With a similar fundamental power, the proposed mixer decrease the IM_3 power up to 14 dB, and the corresponding IIP₃ improvement is 7 dB. Fig.6 shows the IIP₃ improvement and SSB NF measurement results. At least 3.1 dB IIP₃ improvement is obtained in the frequency range 0.3-6GHz, the maximum IIP₃ improvement is 7.1 dB at 2.7GHz. The measured SSB NF is 11.1-14.7 dB at 0.3-6GHz. The measured performance of is summarized in Table I. Other previously published papers are also included for comparison. The mixer's figure of merit (FOM) can be expressed as [9]:

$$FOM = 10 \log \left(10^{G/20} \times 10^{(IIP_3 - 10)/20} / (10^{NF/10} \times P) \right) \quad (3)$$

TABLE I
PERFORMANCE COMPARISONS

Reference	This Work	[9]	[10]	[11]
Frequency range(GHz)	0.3-6	0.5-7.5	0.2-2	2-11
Voltage gain(dB)	3.6-7.2	5.7	19	6.9
IIP ₃ (dBm)	7.9-12.3	-5.7	11	6.5
SSB NF(dB)	11.1-14.7	15	6.5	15.5-20
I _{DD} (mA)/V _{DD} (V)	3.8/1	0.62/0.77	50/1.2	14.2/1.8
IQ imbalance $\Delta mag(dB)/\Delta phase(^{\circ})$	0.2/1	NA	NA	NA
Chip Area/mm ²	0.29	0.62	0.13 ^a	0.48
Technology	90-nm	0.18- μ m	65-nm	0.18- μ m
IIP ₃ /P _{DC}	4.46	0.56	0.21	0.17
FOM	17.8	13.2	15.7	3.9

^a Active core area exclude the Bias and LO generation and buffers.

It is observed that the mixer in this work, compared to the other state-of-the-art CMOS mixer, has achieved highest IIP₃/P_{DC}, and FOM, with smallest chip area.

IV. CONCLUSION

A low voltage low power high linearity quadrature mixer in a 90nm CMOS is present. It covers most recent used commercial frequency band from 300MHz to 6GHz with 7dB IIP₃ improvement. The proposed mixer has excellent performance in comparison with other CMOS mixers.

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