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Design of a CMOS Broadband Transimpedance Amplifier With Active Feedback

Zhenghao Lu, Kiat Seng Yeo, Wei Meng Lim, Manh Anh Do, *Senior Member, IEEE*, and Chirn Chye Boon

***Abstract*—In this paper, a novel current-mode transimpedance amplifier (TIA) exploiting the common gate input stage with common source active feedback has been realized in CHRT 0.18 μm–1.8 V RFCMOS technology. The proposed active feedback TIA input stage is able to achieve a low input impedance similar to that of the well-known regulated cascode (RGC) topology. The proposed TIA also employs series inductive peaking and capacitive degeneration techniques to enhance the bandwidth and the gain. The measured transimpedance gain is 54.6 dBΩ with a -3 dB bandwidth of about 7 GHz for a total input parasitic capacitance of 0.3 pF. The measured average input referred noise current spectral density is about 17.5 pA/$\sqrt{\text{Hz}}$ up to 7 GHz. The measured group delay is within 65 $\pm$ 10 ps over the bandwidth of interest. The chip consumes 18.6 mW DC power from a single 1.8 V supply. The mathematical analysis of the proposed TIA is presented together with a detailed noise analysis based on the van der Ziel MOSFET noise model. The effect of the induced gate noise in a broadband TIA is included.**

***Index Terms*—Active feedback, bandwidth extension, broadband, induced gate noise, regulated cascode (RGC), transimpedance amplifier (TIA).**

I. Introduction

TRADITIONAL optical receiver front-end circuits and devices are usually dominated by HEMT, HBT or Si Bipolar technologies due to their speed and noise advantages. However, due to the following reasons CMOS technology is becoming popular in short range optical communications, such as the 10G Ethernet very-short-reach (VSR) application. First, short-reach 10 Gb/s data communication standards (OC-192c, 10 Gb/s Ethernet VSR) have been specified with relaxed optical sensitivity requirements comparing to those long-haul optical communication standards, which subsequently alleviate the design challenges using CMOS technology. Second, the requirement of high volume, wide deployment of optical components in short-reach communication applications inevitably brings the cost factor to the top of all design considerations. Third, low-cost 850 nm vertical cavity surface emitting lasers (VCSEL) are widely used for optical transmitters in short-reach applications and 10 Gb/s CMOS compatible silicon photodetectors demonstrating reasonable responsivity in the 850 nm wavelength range have been reported [1], [2], making fully integrated CMOS optical receiver a good low-cost match for the 850 nm VCSEL transmitter [3]–[5]. Finally, deep-submicrometer RFCMOS transistors are well capable of high-frequency operations. With the help of carefully studied circuit design techniques, CMOS optical preamplifiers are also able to achieve comparable performances to those HBT, HEMT or Si Bipolar counterparts and maintain the merits of low-power, low-cost, high-integration and high-manufacturability [6]–[8].

CMOS transimpedance amplifiers usually employ current-mode topology realized in the form of common gate [8], [9] or current-mirror [8], [10] input stage to provide low input impedance. Regulated cascode (RGC) input stage [11], [12] is essentially a common gate configuration with active feedback to provide even lower input impedance than simple common gate input stage does. Therefore, better isolation of the relatively large input parasitic capacitance from bandwidth determination can be achieved. This paper examines another type of current-mode TIA topology based on the common gate input stage with common source active feedback, which provides as low input impedance as the RGC configuration does. Hence, the influence on the TIA bandwidth by the relatively large input parasitic capacitance including the photodetector capacitance can be greatly reduced. The idea of active feedback in TIA design has been introduced in [8] without any detailed realization. The proposed TIA in this paper also employs series inductive peaking method to extend the bandwidth. A two-stage capacitive degeneration is used to further enhance the bandwidth and the gain.

The mechanism of the current-mode TIA input topology with active feedback is introduced in Section II. The mathematical analysis of the proposed TIA design is presented in Sections III. The detailed noise analysis of the proposed TIA is provided in Section IV and the Appendix, which includes the induced gate noise. Section V presents the simulation and measurement results.

II. Common Gate Input Stage With Common Source Active Feedback

Fig. 1(a) shows the proposed common gate TIA input stage with common source active feedback. Similar to the RGC topology, Fig. 1(a) is both useful for current mirrors/amplifiers design [13] and high-speed low-noise preamplifier design. Before our analysis on this topology, a brief review of the RGC input configuration is necessary for the purpose of comparison. It is well known that the regulated cascode input stage [11] illustrated in Fig. 1(b) is able to provide very low input

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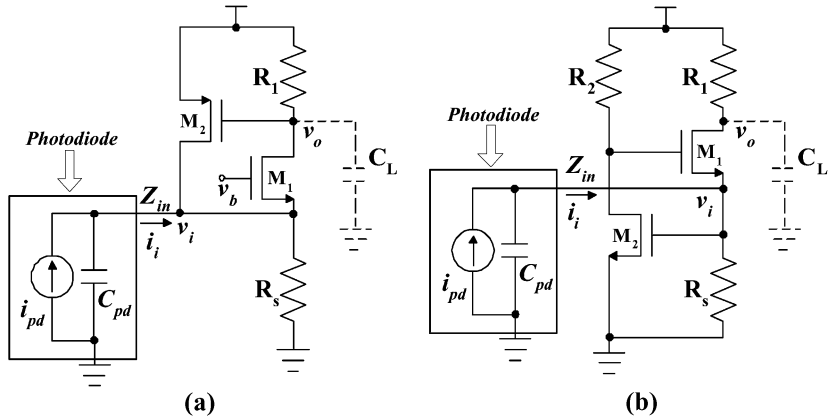

Fig. 1. (a) The proposed common gate TIA input stage with common source active feedback. (b) RGC (regulated cascode) input stage.

impedance. The low frequency input resistance of the RGC topology is about

$$Z_{in,\mathrm{RGC}}(0) \approx \frac{1}{g_{m1}(1+g_{m2}R_2)}. \tag{1}$$

The low frequency transimpedance gain of the RGC input stage is given by

$$Z_{T,\mathrm{RGC}}(0) \approx R_1. \tag{2}$$

The transfer function of the RGC input stage is given by [11]

$$Z_{T,\mathrm{RGC}}(s) = \frac{v_o}{i_{pd}} \approx \frac{R_1}{\left[1+s\frac{C_{pd}+C_i}{g_{m1}(1+g_{m2}R_2)}\right][1+sR_1(C_L+C_o)]} \tag{3}$$

where C_{pd} is the photodiode capacitance, $C_i \approx C_{sb1} + C_{gs2}$, $C_o \approx C_{gd1} + C_{db1}$ and C_L is the load capacitance due to the subsequent stage. According to (3), there are mainly two poles affecting the -3 dB bandwidth, namely $\omega_{i,\mathrm{RGC}} = g_{m1}(1 + g_{m2}R_2)/(C_{pd} + C_i)$ and $\omega_{1,\mathrm{RGC}} = 1/R_1(C_L + C_o)$. $\omega_{i,\mathrm{RGC}}$ is determined at the input node and $\omega_{1,\mathrm{RGC}}$ is determined at the drain of M_1. Due to the very small input resistance, $\omega_{i,\mathrm{RGC}} > \omega_{1,\mathrm{RGC}}$ and the dominant pole is $\omega_{1,\mathrm{RGC}}$. Nevertheless, $\omega_{i,\mathrm{RGC}}$ also contributes to the total roll-off effect and the actual -3 dB bandwidth is

$$f_{-3\ \mathrm{dB,RGC}} < \frac{\omega_1}{2\pi}. \tag{4}$$

There is one alternative to the RGC input configuration in the form of common gate input stage with common source active feedback, which is shown in Fig. 1(a). The NMOS transistor M_1 is the common gate input transistor and the PMOS transistor M_2 provides the active feedback. Fig. 2 shows the small-signal circuit model of the proposed TIA input stage in Fig. 1(a) with a simple photodetector model included. Intuitively, The low-frequency input resistance is given by

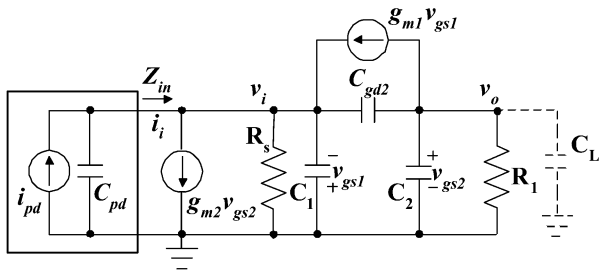

Fig. 2. Small-signal circuit model of the proposed common gate TIA input stage with common source active feedback.

$$Z_{in,\mathrm{CGA}}(0) \approx \frac{1}{g_{m1}(1+g_{m2}R_1)}. \tag{5}$$

Based on the small-signal circuit analysis, the transfer function of the proposed TIA input stage including the photodetector parasitic capacitance is given by (6), shown at the bottom of the page, where $C_1 \approx C_{gs1} + C_{sb1} + C_{db2}$, $C_2 \approx C_{gs2} + C_{gd1} + C_{db1}$. The low-frequency transimpedance gain can be derived from (6) as

$$R_{T,\mathrm{CGA}} = Z_{T,\mathrm{CGA}}(0) \approx \frac{R_1}{1+g_{m2}R_1} = R_1 /\!\!/ \frac{1}{g_{m2}}. \tag{7}$$

Comparing (1) with (5), we can find that the input impedance of RGC topology and the proposed active feedback topology is

$$Z_{T,\mathrm{CGA}}(s) = \frac{v_o}{i_{pd}} \approx \frac{(g_{m1}+sC_{gd2})}{\left\{\left[\frac{1}{R_s}+g_{m1}+s(C_{pd}+C_1+C_{gd2})\right]\left[\frac{1}{R_1}+s(C_L+C_2+C_{gd2})\right]+(g_{m1}+sC_{gd2})(g_{m2}-sC_{gd2})\right\}} \tag{6}$$

quite similar. In RGC topology, a large g_{m2} is required and the resistance of R_2 needs to be small to maintain stability [11]. In the proposed active feedback configuration, according to (5) and (7), it is desirable to choose a large R_1 resistance and a small g_{m2} to achieve low input resistance and maintain a relatively high gain. Moreover, the channel thermal noise $4KT\Gamma g_{d0,2}$ of M_2 adds directly to the total input-referred noise current, where Γ is the noise factor of the MOSFET, $g_{d0,2}$ is the zero-bias drain conductance of M_2 and T is the absolute temperature. Therefore, keeping the size of M_2 small is both desirable for gain and noise performances. By selecting an M_2 with small size (C_{gd2} very small) and assuming the resistance of R_s is relatively large, (7) can be simplified to (8), shown at the bottom of the page, where $R_{T,CGA}$ is given by (8), $\omega_n = \sqrt{\omega_i \omega_1}$ and $Q = (((1+g_{m2}R_1)\sqrt{\omega_i\omega_1})/(\omega_i + (1+g_{m2}R_1)\omega_1))$ with

$$\omega_i = \frac{g_{m1}(1+g_{m2}R_1)}{C_{pd}+C_1} \tag{9}$$

$$\omega_1 = \frac{1}{R_1(C_L+C_2)} \tag{10}$$

where ω_i is determined at the input node and ω_1 is determined at the drain of M_1. Because of the small input resistance, the dominant pole is ω_1 and $\omega_i > \omega_1$. (8) is a typical second-order system with the -3 dB bandwidth higher than the dominant pole ω_1. For Butterworth response, the cutoff frequency is $f_{-3\text{ dB}} = \omega_n/2\pi$ and

$$Q = \frac{(1+g_{m2}R_1)\sqrt{\omega_i\omega_1}}{\omega_i + (1+g_{m2}R_1)\omega_1} = \frac{\sqrt{2}}{2}. \tag{11}$$

The bandwidth extension ratio is

$$BWE = \frac{\omega_n}{\omega_1} = \sqrt{\frac{\omega_i}{\omega_1}}. \tag{12}$$

If we design $\omega_i = 2\omega_1$. The -3 dB cutoff frequency is

$$f_{-3\text{ dB},Butterworth} = \frac{\omega_n}{2\pi} = \sqrt{2}\frac{\omega_1}{2\pi}. \tag{13}$$

According to (11), we need to design $g_{m2}R_1 = 1$ if $\omega_i = 2\omega_1$. The -3 dB cutoff frequency is about 41% higher than the dominant pole ω_1 in the above case. Comparing (4) with (13) and (2) with (7), we can find that the proposed active feedback topology in Fig. 1(a) is advantageous over the RGC input configuration in terms of speed at the cost of lower gain. Suppose all other conditions to be the same, i.e., the noise contributions by R_1, M_1 and R_s are roughly the same for both topologies. The input noise contributed by M_2 of the proposed active feedback topology is about $4KT\Gamma g_{d0,2}$. The input noise due to M_2/R_2 of the RGC stage is roughly $(4KT(\Gamma g_{d0,2} + (1/R_2))/(g_{m2} + (1/R_2))^2)[(1/R_s^2) + \omega^2(C_{pd}+C_i)^2]$[11]. The proposed TIA input stage presents less noise than the RGC input stage does as frequency increases. However, because the gain of the proposed topology is less, the noise due to the subsequent stages will be higher. Therefore, the noise performance of the proposed topology and the RGC stage should be similar.

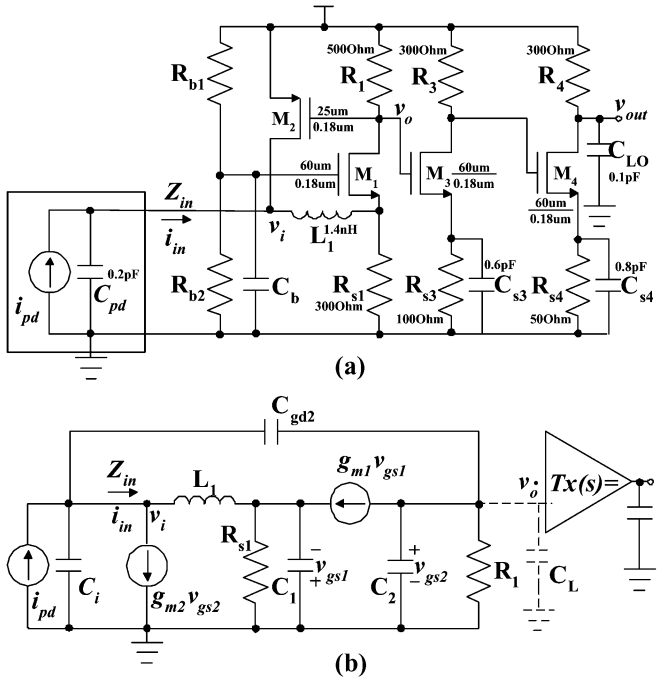

Fig. 3. (a) Circuit schematic of the proposed TIA design. (b) Its small-signal circuit model.

III. Circuit Design and Analysis

In this section, a transimpedance amplifier incorporating the proposed active feedback input topology is presented and analyzed. Fig. 3(a) shows the proposed TIA schematic including a simple photodetector model. The series input inductor L_1 is used for bandwidth extension. The gate of M_1 is biased using $[R_{b1}, R_{b2}, C_b]$. According to our discussion in Section II, the proposed TIA input topology provides good bandwidth performance at the expense of gain. Therefore, a two-stage capacitive degeneration $[M_3, R_3, R_{s3}, C_{s3}]$ and $[M_4, R_4, R_{s4}, C_{s4}]$ is employed to provide extra gain and boost the bandwidth at the same time.

The output impedance of a discrete TIA typically needs to be matched to 50 Ω to drive the transmission line. However, the trend is to integrate the TIA with the main amplifier on one chip [14], thereby avoiding the interstage 50 Ω matching. Our design goal is to integrate the proposed TIA with the main amplifier in the future. Therefore, the output load is not matched to 50 Ω

$$Z_{T,\text{CGA}}(s) \approx \frac{R_1}{1+g_{m2}R_1} \cdot \frac{1}{1+s\left[\frac{R_1(C_L+C_2)}{1+g_{m2}R_1} + \frac{C_{pd}+C_1}{g_{m1}(1+g_{m2}R_1)}\right] + s^2\frac{R_1(C_L+C_2)(C_{pd}+C_1)}{g_{m1}(1+g_{m2}R_1)}} = R_{T,\text{CGA}}\frac{1}{1+\frac{s}{\omega_n Q}+\frac{s^2}{\omega_n^2}} \tag{8}$$

to relax the gain and power dissipation tradeoffs. The low-frequency transimpedance gain is given by

$$Z_{T,\mathrm{TIA}}(0) = R_T \approx \frac{R_1}{1+g_{m2}R_1}\frac{g_{m3}R_3}{1+g_{m3}R_{s3}}\frac{g_{m4}R_4}{1+g_{m4}R_{s4}}. \tag{14}$$

Fig. 3(b) shows the small-signal circuit model of the proposed TIA. The two-stage capacitive degeneration part is simplified to a voltage amplifier model with transfer function $Tx(s)$. The output load capacitor C_{LO} is mainly due to the parasitic capacitance of the output pad, which is around 100 fF in this design. According to Fig. 3(b), the complete transfer function of the proposed TIA is

$$Z_{T,\mathrm{TIA}}(s) = \frac{v_{out}}{i_{pd}} \approx Z_{T,\mathrm{CGA}}(s)\cdot Tx(s) \tag{15}$$

where $Z_{T,\mathrm{CGA}}(s)$ is the transfer function of the proposed TIA input stage with series inductive peaking, which is given by (16), shown at the bottom of the page, where $C_i \approx C_{pd}+C_{db2}$, $C_1 \approx C_{gs1}+C_{sb1}$, $C_2 \approx C_{gs2}+C_{gd1}+C_{db1}$ and C_L is the load capacitance due to the second stage, which is approximately the sum of the Miller capacitances of C_{gd3} and C_{gs3}. As mentioned in Section II, M_2 is designed with small size. Comparing to other parts, C_{gd2} is negligible. Assuming the resistance of R_s is relatively large, (16) can be simplified to (17), shown at the bottom of the page.

In Fig. 3, $Tx(s) = v_{out}/v_o$ is the transfer function of the two-stage capacitive degeneration part, where v_{out} is the small-signal output voltage and v_o is the small-signal voltage at the drain node of M_1. The first capacitive degeneration stage $[M_3, R_3, R_{s3}, C_{s3}]$ contributes a zero $\omega_2 = (R_{s3}C_{s3})^{-1}$ that can be used to compensate part of the roll-off effect due to the input stage. Besides this zero, the capacitive degeneration also generates an additional pole $\omega_3 = (1+g_{m3}R_{s3})/R_{s3}C_{s3}$ at a considerably higher frequency. Because we also need this stage to provide extra gain, the resistance of R_3 is designed to be relatively large.

The second capacitive degeneration stage $[M_4, R_4, R_{s4}, C_{s4}]$ generates a zero at $\omega_4 = (R_{s4}C_{s4})^{-1}$, which is used to cancel the pole determined at the drain node of M_3. This stage also creates a pole $\omega_5 = (1+g_{m4}R_{s4})/R_{s4}C_{s4}$ at a considerably higher frequency. After the bandwidth extension by the two-stage capacitive degeneration, the -3 dB bandwidth of the TIA is mainly determined by the pole located at the output node $\omega_0 = (R_4C_{LO})^{-1}$, which is at about $1/(2\pi\cdot 300\,\Omega\cdot 100\,\mathrm{fF}) \approx 5.3$ GHz in this design. Nevertheless, the other poles at considerably higher frequencies such as ω_3 and ω_5 also contribute to the total roll-off effect. For the purpose of analysis simplicity, we neglect all these poles at higher frequencies. Based on the above discussion, the transfer function $Tx(s)$ in Fig. 3(b) is give by

$$Tx(s) = \frac{v_{out}}{v_o} \approx \frac{g_{m3}R_3}{1+g_{m3}R_{s3}}\frac{g_{m4}R_4}{1+g_{m4}R_{s4}}\frac{1+\frac{s}{\omega_2}}{1+\frac{s}{\omega_0}}. \tag{18}$$

The zero $\omega_2 = (R_{s3}C_{s3})^{-1}$ is used to compensate part of the roll-off effect due to the input stage. The pole $\omega_0 = (R_4C_{LO})^{-1}$ is determined at the output node. The complete transfer function of the proposed TIA is therefore given by (19), shown at the bottom of the page, where C_i, C_1, C_2 and C_L are defined in (16), $R_{TX} = R_1(g_{m3}R_3/(1+g_{m3}R_{s3}))(g_{m4}R_4/(1+g_{m4}R_{s4}))$, $\omega_1 \approx [R_1(C_L+C_2)]^{-1}$, ω_0 and ω_2 are defined in (18). Equation (19) is a fourth order system. As mentioned previously, the zero ω_2 is used to compensate part of the roll-off effect due to the input stage. Because of this zero in the numerator of (19), the transfer function cannot be resolved to a standard Butterworth response. To investigate the frequency response of the proposed TIA regarding the bandwidth extension effect by the capacitive

$$Z_{T,\mathrm{CGA}}(s) = \frac{v_o}{i_{pd}} \approx \frac{R_1}{(g_{m2}-sC_{gd2})R_1 + \left\{s(C_i+C_{gd2}) + \left(\frac{1}{R_s}+g_{m1}+sC_1\right)\left[1+s^2L_1(C_i+C_{gd2})\right]\right\}\frac{1+sR_1(C_L+C_2+C_{gd2})}{g_{m1}+sC_{gd1}}} \tag{16}$$

$$Z_{T,\mathrm{CGA}}(s) = \frac{v_o}{i_{pd}} \approx \frac{R_1}{\left\{g_{m2}R_1 + \left(1+s\frac{C_1}{g_{m1}}\right)\left[1+sR_1(C_L+C_2)\right] + \left(1+sg_{m1}L_1+s^2L_1C_1\right)\left[1+sR_1(C_L+C_2)\right]s\frac{C_i}{g_{m1}}\right\}} \tag{17}$$

$$\begin{aligned} Z_{T,\mathrm{TIA}}(s) &= \frac{v_{out}}{i_{pd}} \approx Z_{T,\mathrm{CGA}}(s)\cdot Tx(s) \\ &\approx \frac{1+\frac{s}{\omega_2}}{1+\frac{s}{\omega_0}}\cdot\frac{R_{TX}}{\left\{g_{m2}R_1 + \left(1+s\frac{C_1}{g_{m1}}\right)\left(1+\frac{s}{\omega_1}\right) + \left(1+sg_{m1}L_1+s^2L_1C_1\right)\left(1+\frac{s}{\omega_1}\right)s\frac{C_i}{g_{m1}}\right\}} \end{aligned} \tag{19}$$

degeneration and the series inductive peaking, we reorganize (19) to

$$Z_{T,\mathrm{TIA}}(s) \approx R_T \frac{1+c_1 x}{(1+a_1 x+a_2 x^2+a_3 x^3+a_4 x^4)(1+b_1 x)} \tag{20}$$

where R_T is given by (14) and

$$x = s/\omega_n = j\omega/\omega_n \tag{21}$$

$$a_1 = \omega_n \left(\frac{1}{\omega_1}+\frac{C_1+C_i}{g_{m1}}\right)/(1+g_{m2}R_1) \tag{22}$$

$$a_2 = \omega_n^2 \left(\frac{C_1+C_i}{\omega_1 g_{m1}}+L_1 C_i\right)/(1+g_{m2}R_1) \tag{23}$$

$$a_3 = \omega_n^3 L_1 C_i \left(\frac{1}{\omega_1}+\frac{C_1}{g_{m1}}\right)/(1+g_{m2}R_1) \tag{24}$$

$$a_4 = \omega_n^4 \frac{L_1 C_i C_1}{\omega_1 g_{m1}}/(1+g_{m2}R_1) \tag{25}$$

$$b_1 = \frac{\omega_n}{\omega_0} \tag{26}$$

$$c_1 = \frac{\omega_n}{\omega_2}. \tag{27}$$

When $|x| = 1$, which means $\omega = \omega_n$, (20) becomes

$$Z_{T,\mathrm{TIA}}(\omega_n) \approx R_T \frac{1+jc_1}{[(1+a_4-a_2)+j(a_1-a_3)](1+jb_1)}. \tag{28}$$

If we want $\omega_n/2\pi$ to be the -3 dB cutoff frequency $\omega_c/2\pi$, we can write

$$a_1 = a_3 \tag{29}$$

$$\sqrt{\frac{1+c_1^2}{1+b_1^2}}\frac{1}{|1+a_4-a_2|} = \frac{\sqrt{2}}{2}. \tag{30}$$

From (29) we obtain

$$\omega_n^2 = \frac{\left(\frac{1}{\omega_1}+\frac{C_1+C_i}{g_{m1}}\right)}{L_1 C_i \left(\frac{1}{\omega_1}+\frac{C_1}{g_{m1}}\right)}. \tag{31}$$

In this design, because of the gain and noise requirements, we set $g_{m2}R_1 = 1$ with $g_{m2} = 2$ mS and $R_1 = 500\ \Omega$. The dominant pole ω_1 at the drain of M_1 is at about 1.8 GHz when $R_1 = 500\ \Omega$. As mentioned previously, after the bandwidth extension by the two-stage capacitive degeneration, the -3 dB bandwidth is determined by ω_0. According to (20) and (26), it is desirable to design ω_0 as high as possible. However, due to the gain-bandwidth tradeoff, we can only make ω_0 as high as $2\pi\cdot 5.3$ GHz with about 55 dBΩ transimpedance gain according to the calculation. The bandwidth of the core TIA is not enough for 10 Gb/s applications and additional bandwidth extension is to be achieved by inductive peaking with the inductor L_1. The bandwidth extension using series inductors has been extensively studied in numerous publications such as [8], [15]–[17].

Now we start to solve equations from (22)–(31) on conditions that $g_{m2} = 2$ mS, $R_1 = 500\ \Omega$, $\omega_1 \approx 2\pi \cdot 1.8$ GHz, $\omega_0 \approx 2\pi\cdot 5.3$ GHz and $g_{m1}/C_1 \approx 2\pi f_T \approx 2\pi\cdot 60$ GHz. By numerical calculation and assuming the input parasitic capacitance C_i, which includes the photodiode capacitance, is about 300 fF, we obtain $L_1 \approx 1.4$ nH, $\omega_n \approx 2\pi \cdot 8.6$ GHz, $g_{m1} \approx 15$ mS, $a_1 = a_3 \approx 3.01$, $a_2 \approx 3.601$, $a_4 \approx 0.521$, $b_1 \approx 1.62$ and $c_1 \approx 2.61$. As mentioned previously, (20) cannot be resolved to standard Butterworth response due to the zero ω_2. (32) is the normalized transfer function of the proposed TIA circuit.

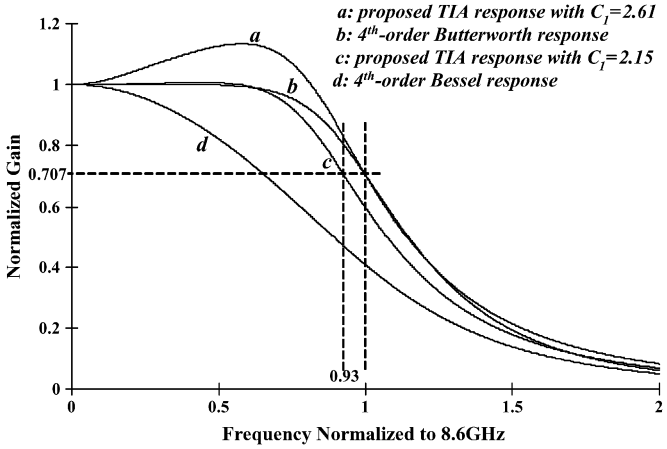

Fig. 4. MATLAB calculated normalized frequency response based on (32).

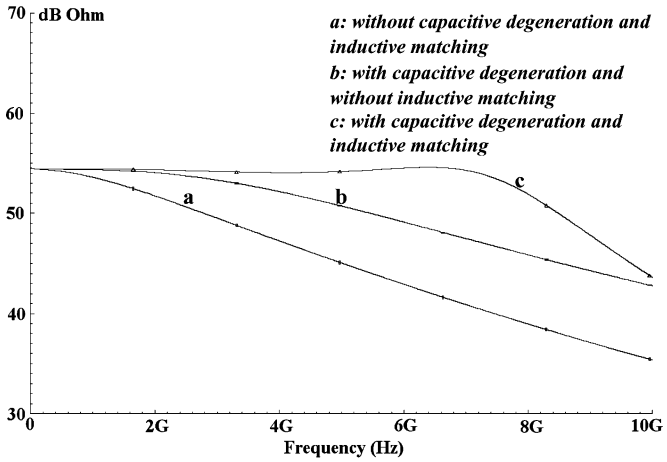

Fig. 5. Post-layout simulated transimpedance frequency response of the proposed TIA under different conditions.

$$Z_{T,\mathrm{TIA},normalized}(s) \approx \frac{1+c_1 x}{(1+a_1 x+a_2 x^2+a_3 x^3+a_4 x^4)(1+b_1 x)}. \tag{32}$$

Fig. 4 shows the MATLAB calculated frequency response based on (32). The normalized standard fourth-order Butterworth and Bessel frequency response are also plotted in Fig. 4 for comparison. In Fig. 4, the \$y\$-axis is the normalized gain and the \$x\$-axis is the normalized frequency. The frequency is normalized to $\omega_n/2\pi$ at about 8.6 GHz. With $c_1 \approx 2.61$, although a -3 dB bandwidth of $\omega_c/2\pi = \omega_n/2\pi \approx 8.6$ GHz is achieved, the frequency response exhibits nearly 20% overshoot. By numerical analysis, we are able to obtain a very close to maximally-flat gain response when $c_1 \approx 2.15$ with other polynomial coefficients unchanged. The -3 dB cutoff frequency in this case is about $\omega_c/2\pi \approx 0.93\omega_n/2\pi \approx 8$ GHz, which is calculated with MATLAB. Therefore, the finalized

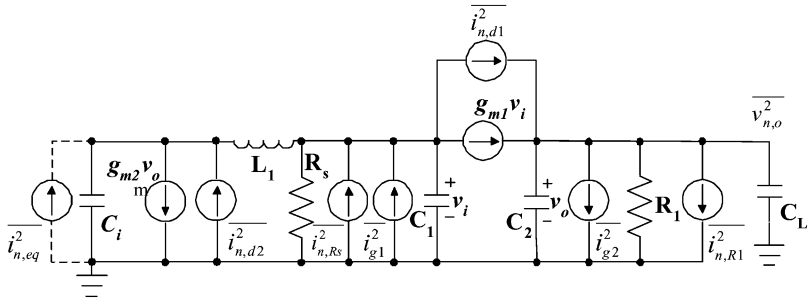

Fig. 6. Small-signal circuit model of the proposed TIA input stage with series input inductor for noise analysis.

frequency response of our proposed TIA circuit is shown by curve "c" in Fig. 4 with a -3 dB bandwidth of 8 GHz. As shown in Fig. 4, the proposed frequency response is between the Butterworth response with maximally-flat gain and the Bessel response with maximally-flat group delay. The finalized transfer function is

$$Z_{T,\mathrm{TIA}}(s) \approx R_T \frac{1+2.15x}{(1+3.01x+3.601x^2+3.01x^3+0.521x^4)(1+1.62x)} \tag{33}$$

where R_T is given by (14) and $x = s/\omega_n = j\omega/\omega_n$. Based on the above analysis, all design parameters can be calculated.

The transimpedance frequency response is also simulated using the Cadence SpectreRF with CHRT 0.18 μm RFCMOS PDK with all parasitics included (post-layout simulation). The simulation result is shown in Fig. 5 for comparison. The devices (MOSFETs, Resistors, Inductors and Capacitors) used in our calculation in Section III are ideal. However, they are non-ideal in reality. Therefore, some small adjustments on the device sizes with the help of circuit simulator are necessary to meet the design objectives. The finalized device sizes are illustrated in Fig. 3. The simulated transimpedance gain is about 54.5 dBΩ. In Fig. 5, curve "a" is the simulated transimpedance frequency response without series inductive peaking and capacitive degeneration, which has a -3 dB bandwidth of about 2.2 GHz. Curve "b" of Fig. 5 is the simulated result with capacitive degeneration but without inductive peaking, which has a -3 dB bandwidth of about 4.6 GHz. After the bandwidth extension by capacitive degeneration and series inductive peaking, the simulated -3 dB bandwidth is about 8 GHz, which is shown by curve "c" in Fig. 5. The simulation results agree with the mathematical calculation very well, which confirms our circuit analysis and design procedure.

IV. Noise Analysis of the Proposed TIA

The noise characteristics of the transimpedance preamplifier in terms of the input referred noise current spectral density or the equivalent input noise current spectral density is of primary importance in the determination of the sensitivity of the whole optical receiver front-end [8], [14].

In this section, we will investigate the equivalent input noise current characteristics of the proposed TIA with noise reduction effect provided by the series input inductor L_1 shown in Fig. 3(a). The noise analysis is based on the van der Ziel MOSFET noise model [18] including the channel thermal noise, induced gate noise and their cross-correlation. The detail of the van der Ziel MOSFET noise model and its application in noise analysis could be found in [7], [18], [19].

It is well-known that besides bandwidth extension, the input series inductor can also help to reduce the equivalent input noise [10], [20], [21]. The small-signal circuit model based on the van der Ziel noise model for noise analysis of the proposed TIA input stage including the input series inductor L_1 is shown in Fig. 6, where C_{gd2} is neglected for analysis simplicity according to the discussions in Sections II and III. In the following derivations from (34)to (38) and in the Appendix, $C_i \approx C_{pd} + C_{db2}$, $C_1 \approx C_{sb1} + C_{gs1}$, $C_2 \approx C_{gd1} + C_{db1} + C_{gs2}$, $C_{in} \approx C_i + C_1$, $C_o \approx C_L + C_2$, $Z_o \approx R_1//(1/sC_o)$, Z_T is given by (17), K is Boltzmann constant, T is the absolute temperature, Γ is the noise factor of the MOSFET, g_{d0} is the zero-bias drain conductance and $\alpha = g_m/g_{d0}$.

To derive the total equivalent input noise current spectral density, one need to derive the equivalent input noise contributed by each noise sources in Fig. 6 such as M_1, M_2, R_1 and R_s, respectively, then add up all these noise contributions together. The detailed derivation can be found in the Appendix. The total equivalent input noise current spectral density of the propose TIA input stage with series inductive peaking can be obtained by summing up the respective noise components from (A.7)–(A.14), which is given by

$$\overline{i_{n,eq}^2} \approx \overline{i_{n,eq,R}^2} + \overline{i_{n,eq,M1}^2} + \overline{i_{n,eq,M2}^2} \tag{34}$$

where

$$\overline{i_{n,eq,R}^2} \approx (1-\omega^2 L_1 C_i)^2 \frac{1}{R_s} + \frac{1}{R_1} \times \left[(1-\omega^2 L_1 C_i)^2 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} \times \left(1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i} \right)^2 \right] \tag{35}$$

$$\overline{i_{n,eq,M1}^2} \approx (1-\omega^2 L_1 C_i)^2 \delta \frac{\omega^2 C_{gs1}^2}{5 g_{d0,1}} \left(1 - |c|^2\right) + \frac{\omega^2 C_{in}^2}{g_{m1}^2} \Gamma g_{d0,1} \times \left[\left(1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i} \right) - (1-\omega^2 L_1 C_i) \frac{C_{gs1}}{C_{in}} |c| \sqrt{\frac{\delta \alpha^2}{5\Gamma}} \right]^2 \tag{36}$$

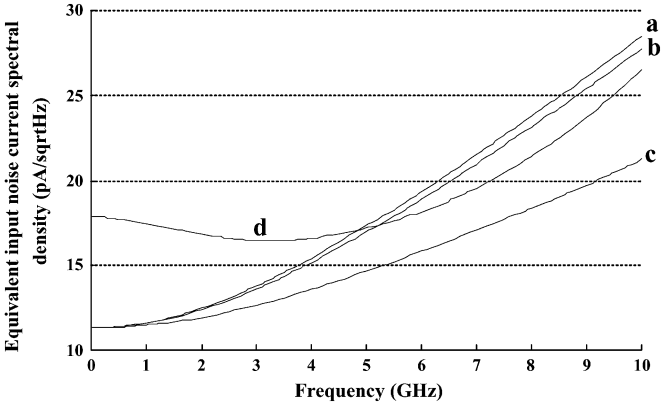

Fig. 7. MATLAB calculated equivalent input noise current spectral density based on (47). Curve a: without induced gate noise and L_1. Curve b: with induced gate noise but without L_1. Curve c: with induced gate and with L_1. Curve d: the noise sum of the input stage and second stage.

$$\overline{i_{n,eq,M2}^2} \approx (1-\omega^2 L_1 C_i)^2 \delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} + \Gamma g_{d0,2}\left[1-\left(1-\omega^2 L_1 \frac{C_1 C_i}{C_1+C_i}\right) \times \frac{\omega C_{gs2} C_{in}}{g_{m1}}|c|\sqrt{\frac{\delta\alpha^2}{5\Gamma}}\right]^2 + \left(1-\omega^2 L_1 \frac{C_1 C_i}{C_1+C_i}\right)^2 \times \delta \frac{\omega^2 C_{gs2}^2}{5g_{d0,2}} \frac{\omega^2 C_{in}^2}{g_{m1}^2}\left(1-|c|^2\right). \quad (37)$$

Fig. 7 shows the MATLAB calculated input referred noise current spectral density of the proposed TIA input stage without/with the series inductive peaking based on (34), where we use $\Gamma = 1.2$, $\alpha = 1$ and $\delta = 4/3$. For curve "a", the induced gate noise and the correlated noise are absent. For curve "b", we use $c = -0.7j$ in the calculation. Both curve "a" and "b" are without the inductive peaking.

According to curve "a" and "b" of Fig. 7, the correlated noise helps to reduce the total input referred noise but this noise reduction effect is not significant. Such kind of noise reduction at optimum transistor size is considerable in short channel MOSFETs [22]. However, the optimum transistor size for best noise performance may not be achievable if there is not enough design headroom left for noise optimization after meeting the gain-bandwidth requirement. According to (34), the size of M_1 needs to be very large to achieve a significant noise reduction, which will also reduce the bandwidth by a considerable amount. Due to the technology limitation and the tradeoff between the noise and the gain-bandwidth product, we cannot achieve the best noise performance without degrading the gain-bandwidth product for this design. Therefore, neglecting the effect of the induced gate noise in a broadband TIA usually does not cause too much noise prediction error. Curve "c" of Fig. 7 is the calculated noise based on (34) with the series input inductor $L_1 = 1.4$ nH. The induced gate noise and the correlated noise are included. Comparing curve "b" with curve "c", the series input inductor can help to reduce the input referred noise significantly.

According to the discussion in Section II, the gain of the proposed common gate TIA input stage with common source active feedback is not high enough to suppress the noise of the second stage to a negligible level. Therefore, it is more accurate to include the noise contribution by the second stage to evaluate the noise performance of the whole TIA circuit. Nevertheless, the effect of the noise due to the second stage is not as important as the input stage. We therefore neglect the induced gate noise of the second stage for mathematical simplicity. Based on the schematic shown in Fig. 3, the input referred noise current spectral density contributed by the capacitive degeneration second stage (M_3, R_3, R_{S3}) is given by

$$\overline{i_{n,eq,3}^2} \approx \left|\frac{1}{Z_T}\right|^2 \frac{4KT}{1+\omega^2 R_{s3}^2 C_{s3}^2} \times \left[\left(\Gamma g_{d0,3}+\frac{1}{R_3}\right)\left(\frac{1+g_{m3}R_{s3}}{g_{m3}}\right)^2 + R_{s3}\right] \quad (38)$$

where Z_T is given by (17). As we can see from the denominator of (38), the capacitive degeneration topology has a counter-effect to noise increment as frequency increases. The total equivalent input noise current spectral density of the proposed TIA can be evaluated by

$$\overline{i_{n,eq}^2} \approx \overline{i_{n,eq,R}^2} + \overline{i_{n,eq,M1}^2} + \overline{i_{n,eq,M2}^2} + \overline{i_{n,eq,3}^2}. \quad (39)$$

Curve "d" of Fig. 7 shows the MATLAB calculated input referred noise current spectral density based on (39), which includes the noise contribution of the input stage and the second stage of our propose TIA circuit in Fig. 3(a). This result is also used in Fig. 11 to estimate the noise performance of the whole TIA circuit.

V. Simulation and Measurement Results

The circuit simulation is carried out using the Cadence SpectreRF with CHRT 0.18 μm RFCMOS PDK with parasitics included (post-layout simulation). The transimpedance response simulation result is shown in Fig. 5. The simulated transimpedance gain of the proposed TIA is about 54.5 dBΩ with a -3 dB bandwidth of about 8 GHz, which is shown by curve "c" in Fig. 5. Fig. 8 shows the post-layout simulated output eye-diagram with $2^{31}-1$ PRBS (Pseudo-Random-Binary-Sequence) NRZ input data.

To test the feasibility of the proposed common gate TIA input stage with active feedback and to verify the proposed TIA design in Fig. 3, the propose TIA is implemented with CHRT 0.18 μm 2-poly 6-metal RFCMOS process. L_1 is implemented using on-chip spiral inductor for the purpose of monolithic implementation and improving area efficiency. Fig. 9 shows the chip microphotograph of the proposed TIA. An on-chip MIM capacitor C_{pd} of 0.2 pF is used to mimic the effect of the photodiode parasitic capacitance. Together with the parasitic capacitance of the input pad that is around 0.1 pF, the total input parasitic capacitance is about 0.3 pF. The chip is measured on wafer with Cascade Microtech Coplanar Ground-Signal-Ground (GSG) probes. The frequency response is measured using HP8510C network analyzer. Fig. 10 shows

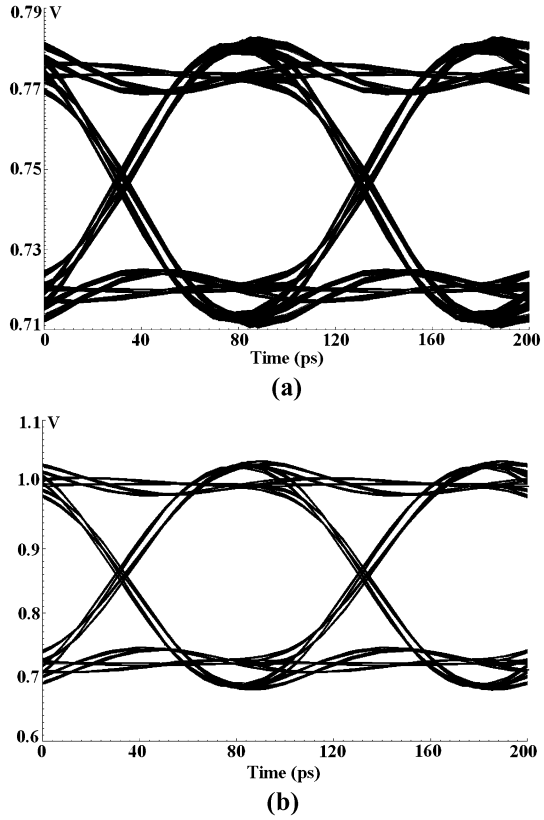

Fig. 8. Post-layout simulated output eye-diagram of the proposed TIA with (a) 0.1 mA peak-peak input current, (b) 0.5 mA peak-peak input current, both with 10-Gb/s $2^{31} - 1$ PRBS NRZ input data.

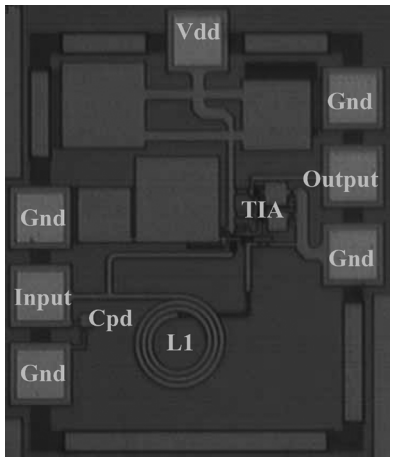

Fig. 9. Chip microphotograph of the proposed TIA.

the measured transimpedance/S_{11} frequency response, which is represented by the solid curve in Fig. 10. For a typical 10 Gb/s TIA, the bandwidth is usually around 0.6 B to 0.7 B for NRZ data if the receiver bandwidth is set by the TIA, where B stands for the bit rate [8]. As shown in Fig. 10, the transimpedance frequency response is tested from 500 MHz to 10 GHz and the data is captured using Agilent IC-CAP. The measured low-frequency transimpedance gain is around 54.6 dBΩ and the -3 dB bandwidth is about 7 GHz (0.7 B).

Comparing to the simulated results also plotted in Fig. 10, the measured gain matches the predicted gain very well at low frequencies. However, the measured gain drops faster as frequency increases. The measured -3 dB bandwidth is 1 GHz lower than the predicted. This is most possibly due to the non-ideality or inaccurate model of the spiral inductor. The spiral inductor model provided by this process is optimized at 2.45 GHz while it is not accurate for frequencies beyond that. To investigate this issue, extra resistive and capacitive parasitics are added to the inductor used in the simulation. The adjusted simulation result with extra parasitics added to the inductor is also shown in Fig. 10 by the dashed curve, where we can see that the corrected simulation can be well fitted to the measured curve. Although such kind of adjustment by simply adding extra parasitics is not rigid, we still can infer that the difference between the measured and predicted transimpedance gain is most probably due to the spiral inductor. The EM radiation loss, the silicon substrate loss and process variations may also contribute to such bandwidth degradation. However, such kind of degradation effect is not significant in this case. The measured S_{11} is below -10 dB up to 9 GHz. As mentioned in Section III, the output load is not matched to 50-Ω for future integration with the main amplifier. Therefore, the measured S_{22} is around -5 dB.

Fig. 11 shows the measured input referred noise current spectral density from 800 MHz to 10 GHz. The predicted input referred noise current spectral density based on curve "d" of Fig. 7 is also shown in Fig. 11 for comparison. The measured input referred noise current spectral density is about 17.5 pA/$\sqrt{\text{Hz}}$ in average up to 7 GHz. According to Fig. 11, the calculated input referred noise current spectral density matches the measured noise very well. This confirms the validity of our noise analysis in Section IV. The measured total input referred RMS noise current is about 1.8 μA integrated up to 10 GHz. This translates to an optical sensitivity of -13.8 dBm at 10^{-12} bit-error-rate if a CMOS compatible 10 Gb/s photodetector with 0.3 A/W responsivity is assumed [8], [14], [25]. According to [26] and [25], the optical sensitivity requirements for 10G Ethernet VSR (2–300 m) and OC-192c short-haul (17–20 km) applications are -9.9 dBm and -12 dBm, respectively.

The optimum bandwidth alone does not guarantee the performance of the TIA. Even if the transimpedance frequency response $|Z_T(s)|$ is flat up to sufficient high frequency, distortions in the form of data dependent jitter may occur if the phase linearity of $Z_T(s)$ is not sufficient. The group delay is used to measure the phase linearity. Typically, a group delay variation of less than $\pm 10\%$ of the bit rate over the specified bandwidth is require to limit the generation of data dependent jitter [8]. The group delay is calculated from the measured phase response. The measured group delay frequency response of the proposed TIA is shown in Fig. 12. According to Fig. 12, the group delay is about 65 ± 10 ps, which is within the requirement of $\pm 10\%$ of the bit rate over the specified bandwidth for 10 Gb/s applications.

The chip consumes 18.6 mW DC power from a single 1.8 V supply. The whole chip size is 0.55×0.6 mm^2 including pads and the circuit occupies 0.4×0.25 mm^2. Table I summarizes the performance of the proposed TIA and presents a comparison to some other TIAs in 0.18-μm CMOS. All the results listed in Table I are based on measurements. The figure-of-merit of

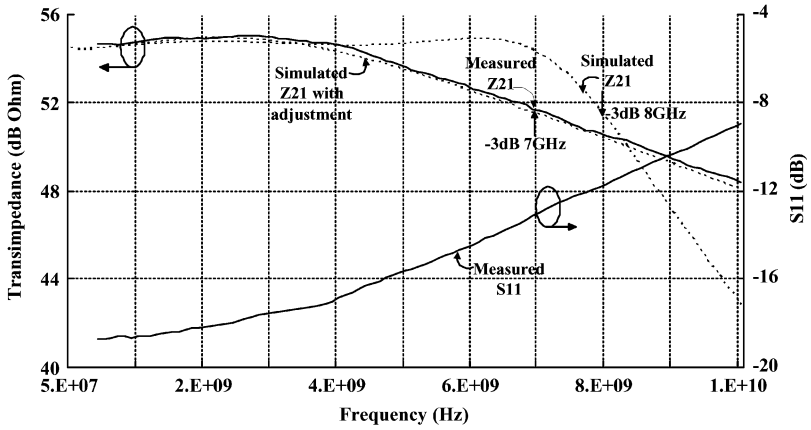

Fig. 10. Measured transimpedance/S_{11} frequency response of the proposed TIA.

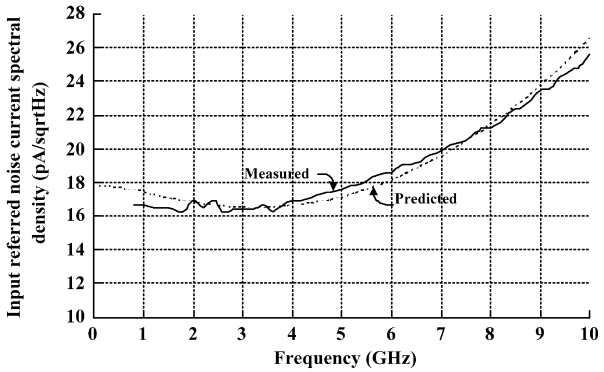

Fig. 11. Measured/Preicted input referred noise current spectral density of the proposed TIA.

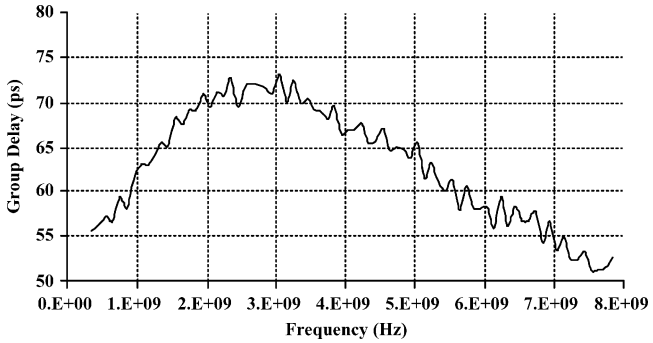

Fig. 12. Measured group delay frequency response of the proposed TIA.

wide-band amplifiers in terms of gain-bandwidth-product per DC power $(\mathrm{GHz}\Omega/\mathrm{mW})$ is also shown in Table I. According to the comparison, the proposed TIA achieves similar performance to the RGC TIA of [17]. The gain-bandwidth product of the proposed TIA is less than the RGC TIA mostly because the RGC TIA in [17] employs a 5th-order input matching and that of the proposed TIA is a 3rd-order one. However, the proposed TIA shows improved phase-linearity.

VI. Conclusion

A novel 10 Gb/s CMOS transimpedance amplifier based on the proposed current-mode input topology with active feedback is designed and silicon-verified. The proposed TIA is designed to exhibit a transimpedance frequency response between the Butterworth response and the Bessel response. A noise analysis based on the van der Ziel MOSFET noise model is presented. The effect of the induced gate noise in a broadband TIA is included. The noise analysis indicates that in broadband TIA designs, it is usually not possible to achieve optimum noise and wide bandwidth simultaneously. Therefore, the noise reduction effect by the induced gate noise in a broadband TIA is not significant. The measurement data confirms our circuit design procedure and noise analysis method. The measured noise performance meets the sensitivity requirements for 10G Ethernet VSR and OC-192c short-haul applications.

Appendix
Noise Analysis

Before we start to derive the input referred noise current spectral density contributed by each of the noise sources of the proposed TIA, we will first derive the equivalent input noise current spectral density contributed by R_1 as an example. According to Fig. 6, the equivalent input noise current due to R_1 is given by

$$i_{n,eq,R1} = \frac{v_{n,o}}{Z_T} \tag{A.1}$$

where $v_{n,o}$ is the output noise due to the thermal noise of R_1 and Z_T is the input stage transimpedance gain given by (17) Based on Fig. 6 and regarding the noise sources as linear voltage/current signals, we obtain

$$v_{n,o} = Z_o(i_{n,R1} - i_1) \tag{A.2}$$

$$i_1 \approx i_2 \frac{g_{m1}}{\frac{1}{R_s} + g_{m1} + sC_i + \left(\frac{1}{R_s} + g_{m1}\right) s^2 L_1 C_i} \tag{A.3}$$

$$i_2 = g_{m2} v_{n,o} \tag{A.4}$$

where $i_{n,R1}$ is the thermal noise current of R_1. Based on (A.1)–(A.4) and assuming the resistance of R_s is relatively large to simplify the analysis, we obtain

$$i_{n,eq,R1} \approx A \cdot \frac{Z_o}{Z_T} \cdot i_{n,R1} \tag{A.5}$$

TABLE I
PERFORMANCE COMPARISON OF TIAS IN 0.18-μm CMOS

References	Bandwidth (GHz)	Gain (dBΩ)	Power Consumption (mW)	Input-Referred Noise ($pA/\sqrt{Hz}$)	Chip Area (mm^2)	Group Delay (ps)	Design Techniques Employed	GBP/P_{dc} (GHzΩ/mW)
[23]	15 without Photodiode Capacitance	58	200@ 1.8V	12	NA	NA	Three-stage Cascode Distributed Amplifiers	60
[24]	30.5@ 0.05pF	51	60.1@ 1.8V	34.3	1.17×0.46	NA	Multi-stage π-Type Inductor Peaking	180.1
[17]	8@ 0.25pF	53	13.5@ 1.8V	18	0.45×0.25	±20	Input-stage 5th-Order Passive Matching	266.7
[15]	9.2@ 0.5pF	54	130@ 2.5V	17	0.8×0.8	±25	Multiple Interstage Passive Matching	33.5
This Design	7@ 0.2pF	55	18.6@ 1.8V	17.5	0.4×0.25	±10	Input-stage 3rd-Order Passive Matching	206.9

where

$$A \approx \left(1 + s\frac{C_i}{g_{m1}} + s^2 L_1 C_i\right) \times \left(1 + s\frac{C_i}{g_{m1}} + s^2 L_1 C_i + \frac{g_{m2} R_1}{1 + sR_1 C_o}\right). \quad \text{(A.6)}$$

In the above analysis, we regard the noise sources as linear voltage/current signals. However, for noise calculation, each noise contribution must be expressed in mean square value. Therefore, the input referred noise current spectral density contributed by R_1 is given by

$$N_{n,R1} \approx \overline{i_{n,R1}^2}\left|A\frac{Z_o}{Z_T}\right|^2 \approx \frac{4KT}{R_1}\left[(1-\omega^2 L_1 C_i)^2 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} \times \left(1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}\right)^2\right]. \quad \text{(A.7)}$$

The equivalent input noise current spectral density contributed by each noise sources could be obtained based on Fig. 6 following the similar noise analysis procedure. Starting from left side of Fig. 6, the equivalent input noise current spectral density attributed to the channel thermal noise of M_2 is given by

$$N_{n,d2} = \overline{i_{n,d2}^2} = 4KT\Gamma g_{d0,2} \quad \text{(A.8)}$$

where $\Gamma = 2/3$ for long channel devices and can be more than one in short channel devices [7], [18], [19]. The equivalent input noise current spectral density due to R_s is given by

$$N_{n,Rs} \approx \frac{4KT}{R_s}(1-\omega^2 L_1 C_i)^2. \quad \text{(A.9)}$$

The equivalent input noise current spectral density contributed by the induced gate noise of M_1 is given by

$$N_{n,g1} \approx 4KT\delta\frac{\omega^2 C_{gs1}^2}{5g_{d0,1}}(1-\omega^2 L_1 C_i)^2 \quad \text{(A.10)}$$

where $\delta = 4/3$ for long channel devices and increases in short channel devices [7], [18], [19]. The equivalent input noise current spectral density contributed by the channel thermal noise of M_1 is given by

$$N_{n,d1} \approx \overline{i_{n,d1}^2}\left[\left|A\frac{Z_o}{Z_T}\right|^2 - (1-\omega^2 L_1 C_i)^2\right] \approx 4KT\Gamma g_{d0,1}\frac{\omega^2 C_{in}^2}{g_{m1}^2}\left(1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}\right)^2. \quad \text{(A.11)}$$

The equivalent input noise current spectral density contributed by the induced gate noise of M_2 is given by

$$N_{n,g2} \approx \overline{i_{g2}^2}\left|-A\frac{Z_o}{Z_T}\right|^2 \approx 4KT\delta\frac{\omega^2 C_{gs2}^2}{5g_{d0,2}}\left[(1-\omega^2 L_1 C_i)^2 + \frac{\omega^2 C_{in}^2}{g_{m1}^2} \times \left(1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}\right)^2\right]. \quad \text{(A.12)}$$

The channel thermal noise and the induced gate noise are cross-correlated. Based on (A.10), (A.11), the correlated noise of i_{g1} and $i_{n,d1}$ is

$$N_{n,c1} \approx -2|c|\frac{\omega C_{in}}{g_{m1}}(1-\omega^2 L_1 C_i) \times \left(1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}\right)\sqrt{\overline{i_{g1}^2 i_{n,d1}^2}}. \quad \text{(A.13)}$$

Based on (A.8) and (A.12), the correlated noise of i_{g2} and $i_{n,d2}$ is

$$N_{n,c2} \approx -2|c|\frac{\omega C_{in}}{g_{m1}}\left(1 - \omega^2 L_1 \frac{C_1 C_i}{C_1 + C_i}\right)\sqrt{\overline{i_{g2}^2 i_{n,d2}^2}} \quad \text{(A.14)}$$

where c is the correlation coefficient. The value of the correlation coefficient is theoretically $c = -0.395j$ for long channel MOSFETs for noise polarities that the channel thermal noise flows from the drain to the source and the gate noise flows from the source to the gate [18], [19]. For short channel MOSFETs, the magnitude of the correlation coefficient can take an abstract value of more than 0.75 [22].

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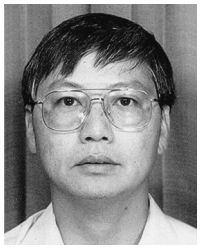

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