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Design of an electronic synapse with spike time dependent plasticity based on resistive memory device

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This paper presents a design of electronic synapse with Spike Time Dependent Plasticity (STDP) based on resistive memory device. With the resistive memory device whose resistance can be purposely changed, the weight of the synaptic connection between two neurons can be modified. The synapse can work according to the STDP rule, ensuring that the timing between pre and post-spikes leads to either the long term potentiation or long term depression. By using the synapse, a neural network with three neurons has been constructed to realize the STDP learning. © 2013 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4795280>]

I. INTRODUCTION

In the past three decades, neural network^{1,2} has received much attention, due to its remarkable ability in fuzzy pattern recognition, associative memory, and self-learning, etc., while those are difficult or time-consuming for realization by solid state devices and software. Neural network, generally, consists of neurons and synapses between neurons. Synapses are crucial elements for computation and information storage in both human brain and artificial neural systems. Each synapse represents a particular strength (i.e., the synaptic weight) of the connection between adjacent neurons, and thus, the information is stored in synapses by different synaptic strength. On the other hand, the spiking activity of neurons can modify the strength of the synapses connecting the neurons,^{3,4} by which a neural network possesses self-learning ability. Pre-synaptic and post-synaptic actions and their timing are critical to synaptic weight modification. The sequence mechanisms are known as Long Term Potentiation (LTP) and Long Term Depression (LTD), respectively. If the pre-synaptic spike precedes the post-synaptic spike, the synapse undergoes a LTP, while if the post-synaptic spike precedes the pre-synaptic spike, LTD signal is generated. The time interval between the pre-synaptic spike and post-synaptic spike determines the variation of synaptic strength. The combination of the sequence and timing mechanisms is called Spike Time Dependent Plasticity (STDP).⁵

Several techniques have been used to implement synapse, including resistors, dynamic capacitive storage,⁶ EEPROM (electrically erasable/programmable read-only memory)/floating gate memory,^{7,8} etc.; such techniques are either not reprogrammable or very complicated. Resistive memory device is emerging as a promising candidate.^{9–14} A resistive memory is reprogrammable, i.e., the resistance of the device can be modified by applying a voltage or current with different amplitudes, different polarities, or different durations between its two terminals, and the resistance state can be maintained for a certain

period. It has attracted a lot of interests due to its simple structure, high density, high speed, low power consumption, and great compatibility with the standard CMOS process.

In this paper, we propose a design of synapse based on resistive memory device. The proposed synapse includes a resistive switching device, a LTP block, a LTD block, and a peripheral circuit. The synapse can modify its weight (i.e., resistance of the resistive memory device) according to a STDP learning rule. The artificial neural network constructed with the designed synapses can learn like a neural system.

II. DESIGN CONSIDERATION

The synapse was designed and simulated with HSPICE by using a standard 0.13 μm CMOS process. The resistive memory device model was built with Verilog-AMS, and its device parameters are extracted from Ref. 13. The resistance modification of the resistive memory device is assumed proportional to both pulse amplitude and width. And the device is a bipolar resistive memory, i.e., a positive pulse leads to an increase in its conductance while a negative pulse causes a decrease in the conductance. It is worthy to mention that the design presented in this work can also be implemented with a unipolar resistive memory device by modifying some block parameters.

According to the STDP learning rule,⁵ the weight modification of a synapse relies on the timing relationship between pre- and post-synaptic spikes. If the pre-synaptic spike precedes the post-synaptic spike, the strength of the synapse undergoes a LTP. The conductance of the synapse increases, leading to strengthening of the connection between the adjacent neurons. However, if the post-synaptic spike precedes the pre-synaptic spike, a LTD occurs. The conductance of the synapse decreases, leading to reduction of the connection between the adjacent neurons. Furthermore, a shorter time interval between pre-synaptic spike and post-synaptic spike leads to a larger change of the conductance. If the time interval between pre- and post-synaptic spikes is larger than a certain value (i.e., the STDP time window^{3,15}), there will be no modifications in synaptic strength.

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The proposed synapse consists of a LTP block, a LTD block, a resistive memory device, and a peripheral circuit. The LTP block and LTD block are shown in Figs. 1(a) and 1(b), respectively. The topology of the two blocks is actually the same, except that the signals are complementary. Firing of the pre- and post-neurons induces a LTP signal and LTD signal, respectively, following the STDP rule.

In Fig. 1(a), nodes PRE and POST are connected to the pre-neuron and post-neuron, respectively. At the initial state, nodes SP and SD are both set to low and I4 acts as an inverter. Once the pre-neuron fires, the transistor MP1 is switched on. The capacitor C1 is charged to VDD (supply voltage), and thus the LTP state node SP rises to high, which inhibits NAND I8 in Fig. 1(b) and thus the LTD block from working. As a result, the LTD block is forbidden while the LTP block is working. Afterwards, the capacitor is discharged through transistors MN1 and MN2, and the discharge current is controlled by V_{bp} . There is a maximum time for the capacitor discharging called LTP time window. If the post-neuron fires within this window, the charges rearranged to capacitor C2 will turn on the inverter I1, forcing LTP output high. The earlier the post-neuron fires, the longer duration the LTP output keeps at high. If the interval between pre- and post-neuron fires larger than the LTP time window, there is no LTP output. The duration that LTP output keeps at high is approximately inversely proportional to the interval between pre- and post-neuron firings. To avoid a sudden voltage reduction on C1 after charge rearrangement, C2 should be at least 10 times smaller than C1. In the case that post-neuron fires first, a similar process occurs in the LTD block, but the LTP block is forbidden while the LTD block is working. A pre-neuron firing within the LTD time window produces a LTD output. The synaptic strength modification block composed of the LTP and LTD blocks is used in the proposed electronic synapse, as illustrated in Fig. 2. The LTP and LTD signals produced by the above two blocks are applied to the resistive memory device, R_m , as shown in Fig. 2. The resistance of the resistive

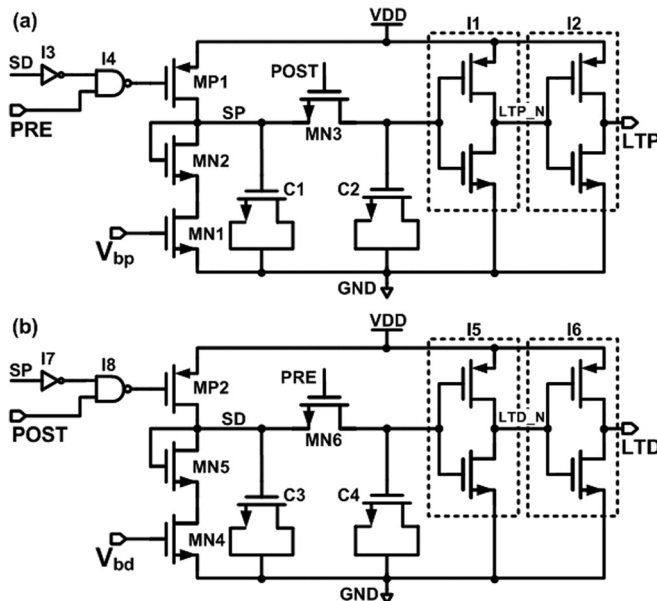


FIG. 1. (a) LTP block and (b) LTD block.

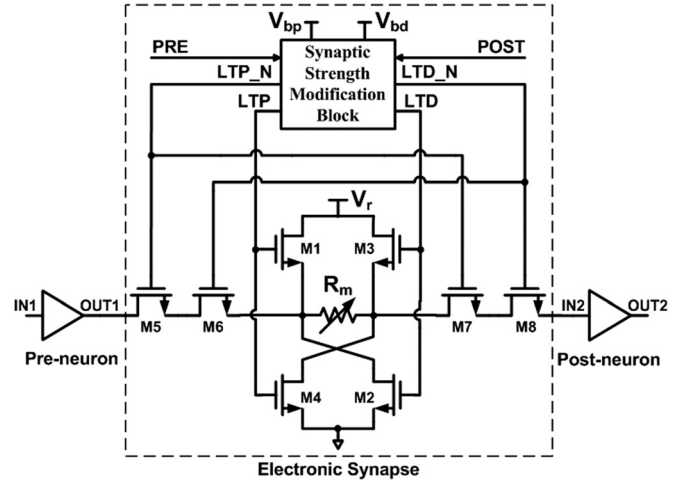


FIG. 2. Schematic illustration of the designed electronic synapse.

memory device changes with the applied signals and the change depends on the amplitude, width, and polarity of the signals.¹³

During the quiescent state, the LTP and LTD signals are low, while their inverted signals LTP_N and LTD_N are high. All the transistors in the path between pre-neuron and post-neuron (M5–M8) remain on, and the spikes produced by pre-neuron can transmit to post-neuron via R_m . Once the LTP occurs, transistors M1 and M4 are turned on by the LTP signal, and the strength modification voltage V_r is applied to R_m . The R_m resistance is then decreased. When the LTD signal occurs, transistors M3 and M2 are turned on by the LTD signal, a negative V_r is then applied to R_m . The R_m resistance is increased. Whenever LTP or LTD occurs, two transistors among M5–M8 would turn off; therefore, the path between pre-neuron and post-neuron is blocked. It should be noted that the above implementation is applicable to a bipolar resistive memory device. To realize a synapse with unipolar resistive memory device, V_r should be replaced by two different voltages V_{set} and V_{reset} on the drains of M1 and M3, respectively.

III. SIMULATION RESULTS

Fig. 3 shows a typical transient response for different spike timing of the pre- and post-neurons. At 5 ms from the beginning, a pre-synaptic spike precedes a post-synaptic spike for 1 ms as shown in Fig. 3(a). A LTP pulse with a width of 21 ms is generated while the LTD channel is prohibited. The resistance of R_m is reduced from 10 k Ω to 9.3 k Ω as shown in Fig. 3(g). At 65 ms, another pre-synaptic spike precedes a post-synaptic spike for 15 ms, while the width of the generated LTP pulse is 14 ms. The resistance of R_m is reduced from 9.3 k Ω to 9.1 k Ω . It should be noted that a shorter LTP pulse will be generated with a longer interval between pre-neuron and post-neuron spikes according to STDP. At 125 ms, a post-neuron spike precedes a pre-neuron spike for 1 ms, and a LTD pulse with the width of 21 ms is generated. The resistance of R_m is increased due to the negative V_r . At 185 ms, a post-neuron spike precedes a pre-neuron spike for 15 ms. A LTD pulse of 14 ms is applied on R_m , leading to increase of R_m resistance. A longer interval

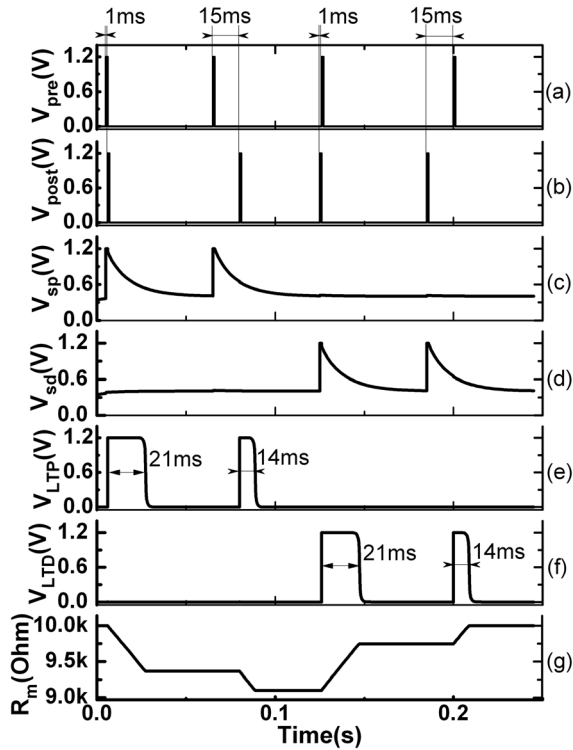


FIG. 3. (a) V_{pre} , (b) V_{post} , (c) V_{sp} , (d) V_{sd} , (e) V_{LTP} , (f) V_{LTD} , and (g) R_m in time domain. LTP and LTD are realized with the designed synapse.

between the post- and pre-spikes results in a shorter LTD pulse according to STDP. In Fig. 3(g), the change of the R_m resistance is proportional to the pulse width of LTP or LTD.

The widths of the LTP and LTD time windows can be adjusted by varying V_{bp} and V_{bd} , respectively. Fig. 4 shows the width of LTP pulse (t_w) as a function of the time interval between pre-neuron spike and post-neuron spike (t_d) at various V_{bp} . The width of the LTP time window is the sum of t_w and t_d , and it is determined by V_{bp} . For a fixed V_{bp} , with the time interval increasing, the LTP pulse width is reduced. When the time interval exceeds the LTP time window, there will be no LTP pulse generated. Similarly, the width of LTD can also be adjusted by the interval between post-neuron and pre-neuron spikes.

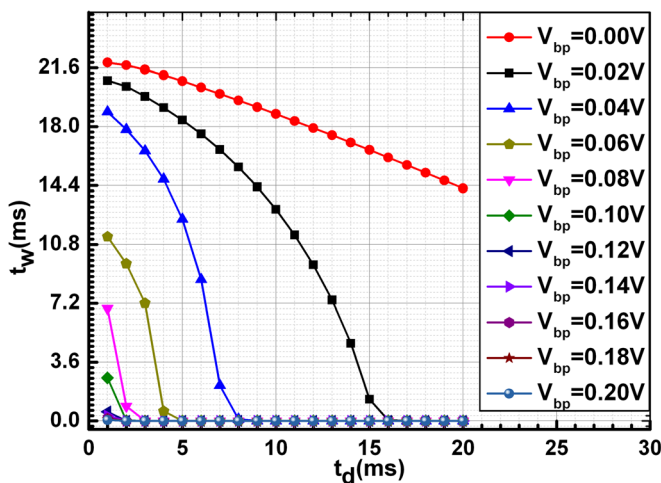


FIG. 4. Width of LTP pulse (t_w) as a function of the interval between pre- and post-spikes (t_d) at various V_{bp} .

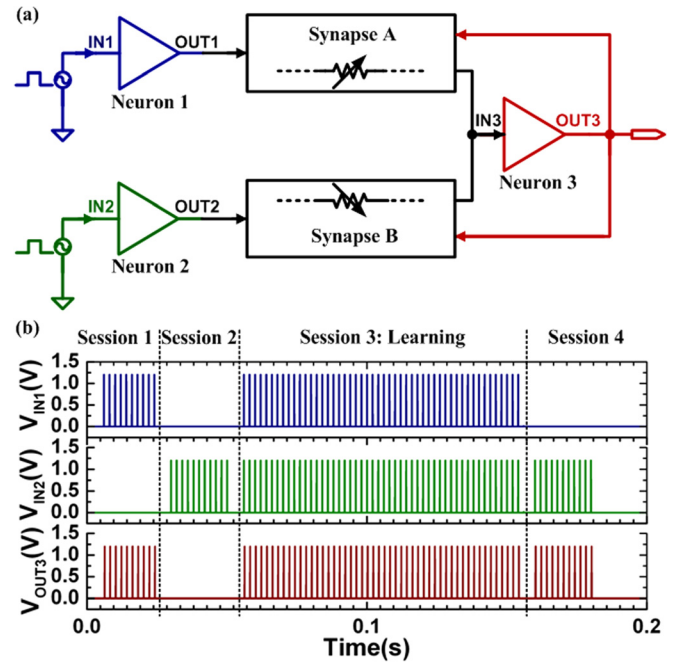


FIG. 5. (a) A three-neuron network constructed with the designed synapse; and (b) associative learning realized with the three-neuron network.

In Fig. 5(a), a three-neuron network was constructed to demonstrate the associative learning in a classical conditioning experiment.^{16,17} Excitations on IN1 and IN2 represent the unconditioned stimulus (sight of food) and the conditioned stimulus (ringing of bell), respectively. OUT3 represents the response (salivation). Initially, we assume that the connection between neuron 1 and neuron 3 is strong. That means the weight of synapse A is high (i.e., the resistance of R_{mA} is low). As can be seen in session 1 in Fig. 5(b), the input of unconditioned stimulus (sight of food) leads to the response (salivation). In session 2, there is no response for the input of the conditioned stimulus (ringing of bell) as the weight of the synapse B is low (i.e., the resistance of R_{mB} is high). In session 3, OUT3 has an output due to the input of neuron 1. At the same time, there is also input of the conditioned stimulus (ringing of bell) from IN2. Now the conditioned stimulus (ringing of bell) precedes the response (salivation) of synapse B. According to the STDP learning rule, the weight of synapse B increases. As a result, in session 4 the input of the conditioned stimulus (ringing of bell) alone can cause the response (salivation) due to the increase of the weight of synapse B. It is clear from above discussion that the neuron network constructed with the designed synapses can realize the STDP learning. The transistor area of the electronic synapse in the present design is $4142 F^2$ (not including the capacitors) where F is the feature size of the transistors, which is only about 7.6% of that of the design based on the conventional CMOS circuits.¹⁸ If the present design is realized with 90 nm technology, the transistor area is $\sim 3.4 \times 10^{-7} \text{ cm}^2$, which is acceptable to large-scale integration.

IV. CONCLUSIONS

A design of electronic synapse based on resistive memory device has been presented in this work. The proposed

synapse well imitates the LTP, LTD, and STDP operations. The learning procedure is realized with a three-neuron network based on the designed synapse. The simplicity of the electronic synapse makes it suitable for applications in large scale neural networks.

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