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Design of a hysteresis lock detector for dual-loops clock and data recovery circuit

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Abstract — In dual-loops clock and data recovery (CDR) circuit design, lock detector is crucial in controlling the switching within CDR loop. The setting of the frequency accuracy of lock detector is a tough task as large ppm will leads to a longer lock time for phase tracking loop and small ppm will leads to more switching time between the loops. A novel lock detector with hysteresis property is proposed in this paper. It provides two different ppms in both different conditions; a smaller ppm for in-lock condition and a larger ppm for out-of-lock condition. This paper also provides a detailed analysis of the proposed lock detector at different conditions. The proposed lock detector is simulated in 0.18- μ m technology and it consumes 1.1-mW at a 1.8V supply voltage.

Index Terms — dual-loops clock and data recovery circuit, frequency lock detector, hysteresis property.

I. INTRODUCTION

As the demand for data communication has increased exponentially in the past decade, optical fiber has become one of the critical mediums in communication system. Due to the importance of clock and data recovery (CDR) circuit in optical communication system [1], researchers have introduced different types of CDR architecture [2]. In order to achieve a faster locking time, dual-loops CDR architectures were explored [3, 4].

Fig. 1 shows the block diagram of a dual-loops CDR architecture [5]. The architecture is formed by two main loops: a frequency tracking loop and a phase tracking loop. The lock detector (LD) [6] in this architecture acts as a vital role to control the switching between the loops. At the starting, as the frequency of voltage control oscillator (VCO) is further away from the operating frequency, the LD will enable the frequency tracking loop. The frequency tracking loop will track the VCO frequency so that its frequency is within a certain ppm of the required operating frequency. The LD will then switch the loop to phase tracking loop when VCO frequency meets the required ppm. The loop will then continue to track the frequency and phase of the VCO and provides a recovered clock. The LD will only switch the loop back to frequency

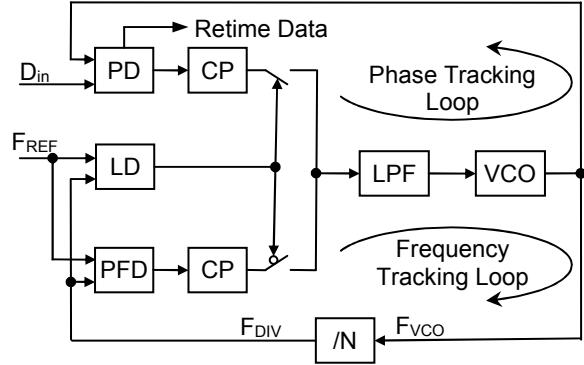


Fig. 1. Block diagram of a dual-loops CDR architecture.

tracking loop when the VCO frequency is being interrupted and is out of the required ppm. Through this architecture, the CDR is able to track its frequency with a shorter time. The locking range of the CDR is also expanded through the additional frequency tracking loop.

One of the problems in the conventional LD architecture is that there is only one required ppm to switch between frequency tracking loop and phase tracking loop [7]. The setting of the required ppm has been a challenging task for the designer. When the required ppm is set to be small, the frequency tracking loop will track the VCO frequency to a closer operating frequency which helps to shorten the lock time of the CDR. However, during the phase tracking loop, the VCO frequency may be out of the required ppm if it is set to be too small. Instead of having a shorter lock time, the CDR will then take a longer time to lock as more switching activity occurs between both frequency tracking loop and phase tracking loop. However, if the required ppm is set to be large, the phase tracking loop will have a longer lock time as the VCO frequency is further away from the operating frequency.

In order to circumvent this difficulty, a novel lock detector with hysteresis property is proposed in this paper. Section II describes the architecture of the proposed LD and section III shows the calculation and analysis of the proposed LD. Section IV provides simulation results and discussion while section V summarizes the paper.

II. ARCHITECTURE OF THE PROPOSED LOCK DETECTOR

In order to circumvent the problem of having only one required ppm, the hysteresis property of the proposed LD provides two different required ppms for two different conditions. During the frequency tracking loop, the required ppm is preferred to be small so that the lock time of the CDR can be decreased. Vice versa, the required ppm is preferred to be larger when the CDR is in the phase tracking loop which prevents the loop from switching back to frequency tracking loop while the CDR is recovering the clock. Through these conditions, the hysteresis property of LD will have smaller required ppm to switch the loop from frequency tracking loop to phase tracking loop (in-lock condition) and vice versa for a larger required ppm to switch the loop from phase tracking loop to frequency tracking loop (out-of-lock condition).

Fig. 2 shows the block diagram of the proposed LD architecture. It is basically composed of 2 N-bits counters, three D-flip-flops (DFF), and a few decision logic circuits. The main purpose of the counter is to count the cycle number of the reference clock (F_{REF}) and the VCO clock after the divider (F_{DIV}) respectively. The pass-transistor logic after the counter is to control the hysteresis property of the LD circuit. The decision logic circuit at the bottom of Fig. 2 helps to decide whether the frequency is lock or not.

The main concept of the proposed LD architecture is that during the in-lock condition, both N-bit counters of F_{REF} and F_{DIV} will begin to start counting the number of cycles of each clock. The logic circuit will then compare the value of both cycles. If either one of the counter reaches the number of $2^{N-1} + 1$ while the other number is still smaller than 2^{N-1} , then the logic value of C will become one which means that the frequency of VCO is still greater than the required ppm. A small pulse of reset signal, R , will then occur and trigger a *low* to the output signal, $LOCK$. The counters will then be reset and recount the number of cycle again. The whole process will continue until the other counter number is greater or equal to 2^{N-1} . The timing diagrams of the in-lock condition are shown in Fig. 3(a).

As for the out-of-lock condition, the pass transistor logic will then increase the number of cycle count. Instead of comparing the cycle number of $2^{N-1} + 1$, the logic circuit is now compared to the cycle number of $2^{N-1} + 2^k$, where k is an integer. Due to this increase in number, the required ppm has increased for out-of-lock condition. Fig. 3(b)

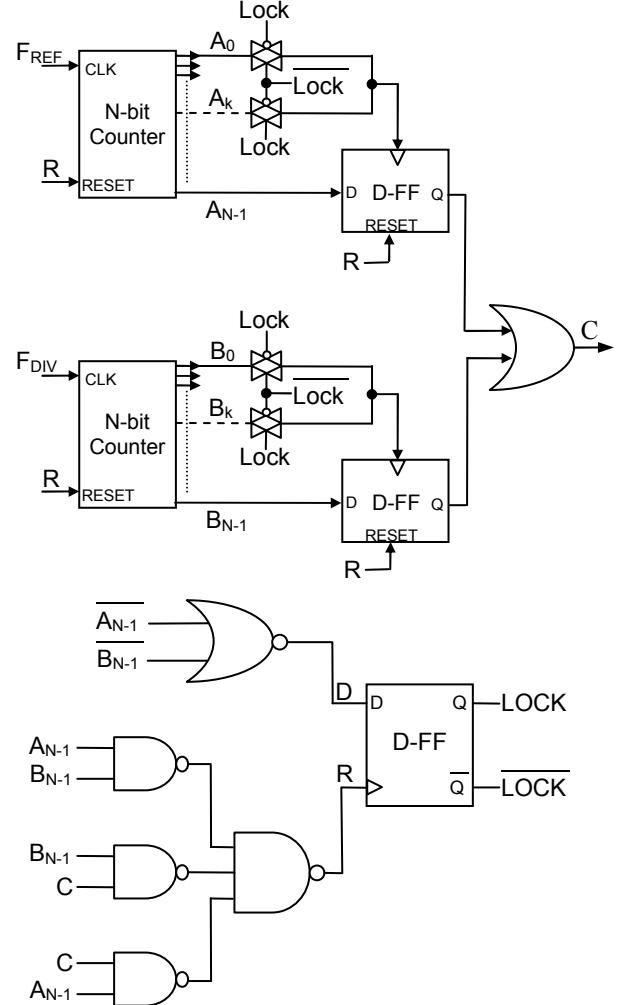


Fig. 2. Block diagram of the proposed LD architecture.

shows the timing diagrams of out-of-lock condition. The following section will show the calculation and analysis of the proposed LD circuit.

III. CALCULATION AND ANALYSIS

For the in-lock condition, the logic circuit compares both cycle number of 2^{N-1} and $2^{N-1} + 1$. In order to obtain a logic *high* for the $LOCK$ signal, the period of VCO has to satisfy the following conditions,

$$(2^{N-1} + 1) \cdot T_{REF} \geq 2^{N-1} T_{DIV} \quad (1a)$$

$$\text{and } (2^{N-1} + 1) \cdot T_{DIV} \geq 2^{N-1} T_{REF} \quad (1b)$$

where T_{REF} and T_{DIV} are the period of F_{REF} and F_{DIV} respectively. By combining these two conditions, the

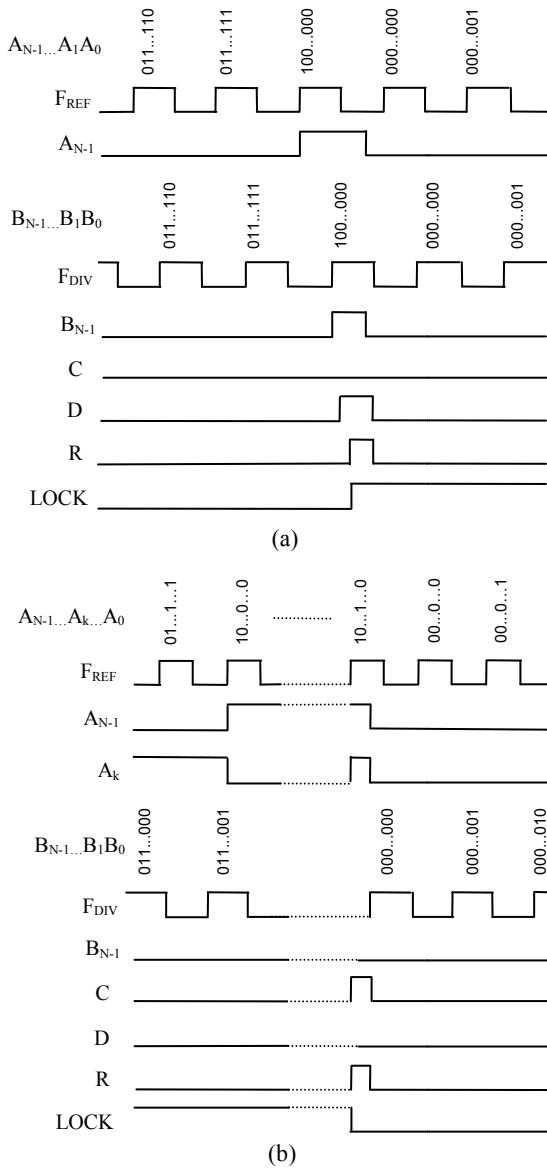


Fig. 3. Timing diagrams of the proposed LD architecture.

frequency range of DIV and VCO for the in-lock is given as follows,

$$\frac{2^{N-1}}{(2^{N-1}+1)}f_{REF} \leq f_{DIV} \leq \frac{(2^{N-1}+1)}{2^{N-1}}f_{REF} \quad (2a)$$

$$\frac{2^{N-1}}{(2^{N-1}+1)}f_{lock} \leq f_{VCO} \leq \frac{(2^{N-1}+1)}{2^{N-1}}f_{lock} \quad (2b)$$

where f_{lock} is the required VCO frequency. When N is equal to 12, the required ppm for in-lock condition will be

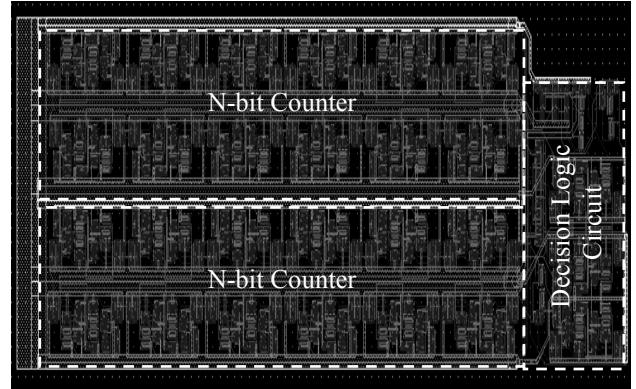


Fig. 4. Layout of the proposed LD architecture.

around $\pm 488\text{ppm}$ and the equation can be written as

$$0.999512f_{lock} \leq f_{VCO} \leq 1.000488f_{lock} \quad (3)$$

In order for the lock detector to change from in-lock to out-of-lock, it will then use $2^{N-1} + 2^k$, where k is an integer, as a reference instead of $2^{N-1} + 1$. Hence, the frequency range will be larger and is given by

$$\frac{2^{N-1}}{(2^{N-1}+2^k)}f_{lock} \leq f_{VCO} \leq \frac{(2^{N-1}+2^k)}{2^{N-1}}f_{lock} \quad (4)$$

As the value of N has been set by the previous required ppm, the ppm for out-of-lock is then being set by the value of k . If the value of k is chosen to be 2, the required ppm is around $\pm 1950\text{ppm}$ and can be written as

$$0.99805f_{lock} \leq f_{VCO} \leq 1.00195f_{lock} \quad (5).$$

IV. SIMULATION RESULTS AND DISCUSSION

The proposed LD circuit is implemented by using Global-foundries' 0.18- μm CMOS process. It is simulated in Cadence SpectreRF environment. The N-bit counter is implemented with the transmission gate architecture and the logic gates are implemented with static complementary CMOS technology. Fig. 4 shows the layout diagram of the proposed LD design. It consumes a total area of $120 \times 425 \mu\text{m}^2$.

In order to ensure the functionality of the proposed LD, it is simulated in a dual-loops CDR design shown in Fig. 1. The CDR operates under a data rate of 10-Gb/s with a frequency divider of 16. The simulation results are shown in Fig. 5. At the starting, as VCO frequency is very far away for the operating frequency, the LOCK signal is *low* to enable the frequency tracking loop to track the frequency. As the frequency of VCO is being locked, the LOCK signal changes to *high*. The phase tracking loop

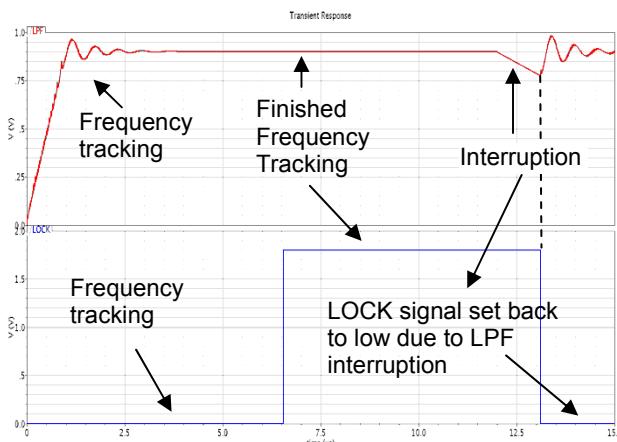


Fig. 5. Simulation results of the proposed LD architecture.

will start to track the phase and recover the clock. However, when there are some interruptions to the control voltage, the LD will then signal a *low* to the LOCK signal so that the frequency tracking loop will track the frequency again. At a power supply voltage of 1.8V, the proposed LD consumes only 1.1-mW.

V. CONCLUSION

A novel lock detector with hysteresis property is proposed in this paper. It has the ability to give a smaller required ppm for in-lock condition and a larger required

ppm for out-of-lock condition. It offers a compact design and consumes only 1.1-mW at 1.8V supply voltage.

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