Design and realization of low dropout voltage regulator and voltage reference in deep-submicron CMOS for emerging Internet-of-Things and satellites

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**Design and Realization of
Low DropOut Voltage Regulator and
Voltage Reference
in Deep-Submicron CMOS for
Emerging Internet-of-Things and
Satellites**

Jiang Jize

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2018

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The contributions of the co-authors are as follows:

- I am the main designer of the proposed circuit. I did the simulation and hardware characterization. I prepared the manuscript drafts.
- Dr Shu Wei co-designed the circuit and revised the manuscript.
- Prof Chang provided the initial project direction and revised the manuscript.

Chapter 4 is published as J. Jiang, W. Shu, and J. S. Chang "A 5.6 ppm/°C Temperature Coefficient, 87-dB PSRR, Sub-1-V Voltage Reference in 65-nm CMOS Exploiting the Zero-Temperature-Coefficient Point," IEEE Journal of Solid-State Circuits, vol. 52, no. 3, pp. 623-633, March 2017.

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Summary

This Ph.D. program pertains to the design and realization of two fundamental analog circuits in deep-submicron CMOS – a Low DropOut voltage regulator (LDO) and a voltage reference. The target applications for the LDO and the voltage reference are respectively the emerging Internet-of-Things (IoTs) and both the said IoTs and satellites. Some of the most imperative considerations for the design of contemporary Integrated Circuits (ICs) and Systems-on-Chip (SoCs) for IoTs include a small form factor, complex functionality, yet low power and low cost. These attributes are often realized by employing deep-submicron CMOS processes, e.g., 65nm, resulting in a somewhat challenging operating environment, including a low supply voltage, large thermal gradient, severe noise (coupling), etc. For satellites operating in an extra-terrestrial environment, the operating environment for ICs/SoCs is even more challenging due to the extended temperature range and the need for immunity to radiation effects, i.e., ‘radiation-hardened’.

For the LDO design for the said IoTs, the most critical and challenging attribute is arguably the high Power Supply Rejection Ratio (PSRR), not only over a wide frequency range but also over a large load current range. In this Ph.D. program, we propose an LDO, realized in 65nm CMOS, featuring the highest PSRR reported in literature to date – $>60\text{dB}$ over 10MHz frequency range, and over 100mA load current range. We achieve the high PSRR by our proposed Feed Forward Ripple Cancellation (FFRC) technique embodying an adaptive load current tracking scheme. In addition, by means of embodying an NMOS-based power stage, our proposed LDO achieves very

low dropout voltage of 80mV and features very small overshoot and undershoot of 2mV and 4mV, respectively.

For the design of the voltage reference for the said IoTs and satellites, a sub-1V voltage reference featuring a low Temperature Coefficient (TC) over a wide temperature range is increasingly imperative. In this Ph.D. program, we propose a sub-1V MOSFET-only voltage reference realized in 65nm CMOS featuring a low TC of 5.6ppm/°C over a wide temperature range from -40°C to 125°C and a high PSRR over a wide frequency range (87dB from DC to 800kHz, and 75dB at 1MHz). We achieve the said low TC attribute by a novel curvature-compensation technique based on our comprehensive investigation into the mechanism of the Zero Temperature Coefficient (ZTC) point of an NMOS transistor – our discovery of a new phenomenon of the effect of the drain-to-source voltage of an NMOS on TC. Our proposed MOSFET-only voltage reference is, to our knowledge, hitherto the only MOSFET-only voltage reference embodying curvature compensation. We achieve the said high PSRR by means of an active attenuator and an impedance adapting frequency compensation. Further, by exploiting the inherent immunity of the ZTC point against radiation effects, our proposed MOSFET-only voltage reference features ‘radiation hardened’ – a paradigm of the Radiation Hardened By Design (RHBD) approach for analog circuits. A prototype design realized in 130nm CMOS tested under irradiation conditions features very high radiation hardness. Specifically, under 1Mrad Total Ionizing Dosage, it features <1.5% output variation and is error-free under Linear Energy Transfer of 77MeVcm²/mg. This feature is particularly imperative for MOSFET-only radiation-hardened ICs/SoCs for satellites and IoTs for extra-terrestrial applications.

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CHAPTER 1

Introduction

1.1 Motivation

This Ph.D. program pertains to the design of two rudimentary circuit blocks under the broad Power Management Integrated Circuit (PMIC) [1] field, and their realization in deep-submicron Complementary Metal Oxide Semiconductor (CMOS) – a Low DropOut voltage regulator (LDO) [2] and a voltage reference [3]. The target application for the LDO is the emerging Internet-of-Things (IoTs) [4] where the attributes of interest are low dropout voltage and high Power Supply Rejection Ratio (PSRR). The target applications for the voltage reference, on the other hand, are both IoTs and satellites [5]. For IoTs, the attributes of interest are low Temperature Coefficient (TC), high PSRR, and low supply voltage. For satellites, the attributes of concern are the same as that for IoTs but with the added imperative need for immunity against radiation effects [6], qualified by Total Ionizing Dosage (TID) [7] and Single Event Effects (SEEs) [8]. These motivations for the design of the LDO and the voltage reference will now be delineated in turn.

Figure 1.1 depicts a simplified block diagram of the electronic system of a typical IoT, where the PMIC [1] is an indispensable functional block. It serves to provide high-quality power supplies for analog, mixed-signal, Radio Frequency (RF), and digital circuits therein, e.g., data converter [9, 10], Phase Locked Loop (PLL) [11], microprocessor (μ P) [12, 13], memory [14, 15], etc. Of particular interest, the PMIC

relies on the co-design of switching regulator [16] and LDO where the switching regulator should feature inherently high power-efficiency (e.g., >85%) in view of the energy storage elements (i.e., the capacitor and the inductor). However, there is substantial switching noise (at its switching frequency) due to the nature of the switching operation. The LDO, by means of its linear operation, suppresses the switching noise to provide a well-regulated power supply. However, its power-efficiency is often compromised due to its dropout voltage.

Figure 1.1. A simplified block diagram of electronics in IoTs.

In general, the design of the PMIC for IoTs emphasizes three desirable salient attributes, including low power dissipation, small form-factor, and low output noise. The low power dissipation facilitates a long battery life and in cases where the IoT embodies a non-replaceable primary battery [17], the lifespan of the IoT is extended. To achieve a low power dissipation, a low quiescent current and a high power-efficiency are imperative. The small form-factor expands the application space of the

IoT devices under diverse environmental conditions, particularly in view of wearable IoTs [18]. In general, the small form-factor requires the electronics in IoTs to be highly integrated. In view of this high integration, it is critical that the output noise is low because a high supply noise would otherwise degrade the performance of sensitive subcircuits [19], e.g., data converters, Phase Locked Loops (PLLs), and memory.

The said three attributes and their inter-relationships pose somewhat formidable challenges for the design of the PMIC for IoTs, including that relating the LDOs therein. Specifically, to realize ever-decreasing form-factor IoTs, including the reduction of the size of the inductor and capacitor of the switching regulator, undesirably leads to compromised noise performance and reduced power-efficiency [20, 21]. This is because the switching noise is larger (e.g., 50mV peak-to-peak) at the output of the switching regulator, V_{out_SR} , for a higher switching frequency (e.g., 10MHz [21]). Consequently, to accommodate these compromises arising from the switching regulator, the LDO would need to feature a very high PSRR over a wide frequency range (e.g., >60dB over 10MHz, see later) to provide for low output noise. Moreover, the said high PSRR needs to be achieved with a low dropout-voltage (e.g., <100mV) to avoid further power-efficiency degradation.

In the perspective of ever-decreasing feature size of advanced CMOS fabrication process, the design challenges for high PSRR and low dropout-voltage LDO are further exacerbated. In many IoTs embodying low-voltage Systems-on-Chip (SoCs) with integrated LDOs, the supply noise due to the noisy on-chip environment is particularly challenging. This is because if the noise is high, the effective operating supply voltage is reduced. Put differently, to cope with the low supply voltage, the supply noise should be commensurably low to guarantee desirable performance metrics of noise sensitive

circuits (e.g., the Spurious Free Dynamic Range (SFDR) of a data converter [22, 23], the clock jitter of a Phase Locked Loop (PLL) [24, 25], etc.). For example, a 1V 14bit Analog-to-Digital Converter (ADC) featuring 90dB SFDR can only tolerate $\sim 100\mu\text{V}$ ripple voltage at its power supply [26]. In this example, an LDO featuring at least 54dB PSRR over a 10MHz frequency range is required to be placed after a switching regulator with 50mV switching noise at 10MHz [21]. For completeness, the said noise performance includes the dynamic current, i.e., the PSRR would need to be qualified and quantified over the full dynamic current range of the said ADC. For example, if the ADC draws a maximum current of 100mA, the PSRR of the LDO should be at least 54dB over the current range of the minimum current to the maximum current of the ADC. In the perspective of the IoT where the operation space [27] is wide, i.e., the current load range is wide (e.g., 0 to 100mA), the PSRR would need to be qualified over the full operation space.

The design-art of LDOs is very mature [2, 28-51]. Figure 1.2 depicts a simplified block diagram of an LDO comprising a controller, a feedback network, a power transistor, and a voltage reference. The first three components constitute a regulation loop to regulate the output of the LDO, V_{out} , to an amplified version of the output of the voltage reference, V_{REF} . Power supply (V_{in}) noise can be coupled to V_{out} via the power transistor leading to a finite PSRR. Reported approaches to obtain high PSRR in LDOs include the pre-regulated supply means [29, 32, 34] and the FeedForward Ripple Cancellation (FFRC) method [39, 40, 43-46, 50]. The former is realized by circuits such as the cascode transistor topology [32, 34], passive low-pass filter [29], etc. However, as these circuits are additional, i.e., in series with the LDO power transistor, the dropout voltage can become intolerably high (e.g., $>0.5\text{V}$), thereby

compromising the power efficiency and in some cases seriously reducing the available output voltage.

Figure 1.2. A simplified block diagram of an LDO.

FFRC, on the other hand, is advantageous as the dropout voltage is not compromised. This is because FFRC involves the augmentation of a parallel feedforward signal path from the power supply to the LDO output to neutralize the existing supply noise transmission via the power transistor. The effectiveness of the FFRC technique is ascertained by the gain of the said augmented feedforward signal path, where the optimal feedforward gain is a dynamic parameter that varies with the load current [39, 43].

A reported FFRC LDO [40] featuring a constant feedforward gain improves PSRR but only within a limited space variation, i.e., a limited load current range of 1-25mA. Several reported approaches have attempted to address this limitation. For example, a reported design [44] adopted a built-in 1-bit quantizer to alter the

feedforward gain based on the load current condition. However, this approach is effective only to a limited extent due to the coarse quantization. Another reported approach [43] adopted the gain calibration methodology, but the hardware overhead penalty is somewhat high. An improved design [39] suggested a variable-gain feedforward path and demonstrated good PSRR over a wider load current range (from 10mA to 140mA). However, the efficacy of this approach is limited under light-load conditions, e.g., <10mA.

In short, although the design art of FFRC LDO is somewhat mature, state-of-the-art LDOs remain inadequate to provide sufficiently high PSRR over a wide frequency range (e.g., >60dB over 10MHz) and over a large load current range (e.g., 100 μ A to 100mA). In the perspective of highly integrated IoTs, this inadequacy is a somewhat serious limitation of state-of-the-art IoTs.

Consider now the voltage reference. A voltage reference generating a Process, Voltage (i.e., supply voltage), and Temperature (PVT) insensitive output voltage is another essential building block of PMIC for IoTs, particularly as a sub-circuit for the LDO. Note that the output of an LDO is an amplified version of the output (including its variations/noise) of the voltage reference [2]. Put simply, congruous with the demand for high-performance LDOs as aforementioned, there is also a real need for high precision voltage reference for IoTs [52-70].

In general, the voltage reference for IoTs needs to feature three salient attributes. First, to be compatible with the deep-submicron CMOS low-voltage SoCs for IoTs, the voltage reference needs to accommodate a low supply voltage (e.g., the supply rail, $V_{DD}<1V$) and should be realized in deep-submicron CMOS. Second, it is imperative for the voltage reference to feature a low TC (e.g., $TC<10\text{ppm}/^\circ\text{C}$) over a wide temperature

range (e.g., from -40°C to 125°C) because SoCs often suffer undesirably high on-chip thermal gradient [71] due to its complexity and IoT devices are sometimes placed in harsh ambient environments [72]. Third, as discussed earlier, a wideband high PSRR (e.g., $\text{PSRR} > 60\text{dB}$ over a 10MHz frequency range) is highly desirable to accommodate the switching noise of switching regulator and the strong supply noise that is coupled from the noisy digital modules in SoCs. In the perspective of deep-submicron CMOS fabrication processes, where the minimum feature-size continues to shrink, these attributes are increasingly challenging due to the inferior transistor characteristics, including severe short channel effects [73], increasing leakage current [74], reduced transistor intrinsic gain [75], etc.

Bandgap references are presently the most ubiquitous voltage references and are typically realized by the parasitic vertical PNP Bipolar Junction Transistors (BJTs) in CMOS technology [76]. The design art of bandgap references is mature and well established, particularly in dated technology nodes (e.g., $0.18\mu\text{m}$ CMOS). Bandgap references offer two attractive attributes but suffer from several shortcomings. The first attractive attribute is their output insensitivity to process variations because their output is determined by the silicon bandgap phenomenon [77]. Second, they can feature very low TC (e.g., $< 10\text{ppm}/^{\circ}\text{C}$ over -40°C to 125°C) with appropriate curvature compensation [53, 54, 66].

However, because of the said phenomenon leading the said first attractive attribute, i.e., the silicon bandgap ($\sim 1.2\text{V}$), and because of the non-scalable turn-on voltage of BJT ($\sim 0.7\text{V}$), bandgap references typically require a relatively high supply voltage ($V_{DD} > 1\text{V}$) [54, 56, 64, 66]. Further, the said advantages of bandgap references diminish when realized in deep-submicron CMOS (e.g., 65nm CMOS and below).

Specifically, the degraded characteristics of the BJTs in these CMOS technology nodes deteriorate the performance of the bandgap references. For an example, the TC of bandgap references deteriorates due to the reduced BJT current gain [61, 78]. To accommodate this deterioration, the analytical expression to predict the output of bandgap references would need to augment a process-sensitive term involving the process/temperature spread of the BJT current gain [78]. Put simply, state-of-the-art bandgap references are in part inappropriate for IoT applications when they are realized in deep-submicron CMOS and whose $V_{DD} < 1V$.

To accommodate the requirement of sub-1V V_{DD} , several Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET)-only voltage references have been reported in the literature [58, 59, 63, 65, 67, 70]. Of these, the subthreshold MOSFET voltage references [58, 59, 63] are most prevalent; subthreshold MOSFETs exhibit similar temperature behavior to BJT, and their mechanisms for voltage references are similar. Subthreshold MOSFET voltage references, however, suffer from insufficient temperature operating range. Specifically, their temperature range is typically limited to $-20^{\circ}C$ to $80^{\circ}C$ [58, 59]. This is largely because the characteristics of the subthreshold MOSFET are severely affected by leakage current, which is exacerbated at high temperature, and smaller minimum transistor feature size. Put simply, subthreshold MOSFET voltage references are often inappropriate for many IoT applications.

The Zero-Temperature-Coefficient (ZTC) voltage reference [79] is potentially advantageous over its bandgap and subthreshold counterparts for IoTs for two promising attributes. First, unlike the bandgap reference, the ZTC voltage reference can operate at sub-1V in view of the scalable ZTC voltage. Second, compared to and unlike the subthreshold voltage reference, the ZTC voltage reference operates in the strong

inversion region. It is hence potentially more accurate and is unaffected by leakage current. Nevertheless, the design art of the ZTC approach is somewhat immature in the sense that reported ZTC voltage references to date have not outperformed the well-established bandgap and subthreshold approaches. In this thesis, we argue that because of the potential of the ZTC voltage reference, there is a strong motivation to further explore novel and effective design techniques to improve the design of the ZTC voltage reference for emerging IoTs, including sub-1V applications and that realized in deep-submicron CMOS processes.

Consider now the satellite applications, where a high precision CMOS voltage reference featuring immunity against radiation effects is typically mandated [80]. As mentioned earlier, the radiation effects include an accumulation of the dosage of radiation (TID) and that due to the heavy-ion particle strikes (SEEs). In general, there are two approaches to realize radiation-hardened (rad-hard) electronics – Radiation-Hardened-By-Process (RHBP) [81, 82] and Radiation-Hardened-By-Design (RHBD) [83-85].

At this juncture, the only rad-hard voltage references are that based on the RHBP approach. In general, the RHBP approach is disadvantageous because the process is particularly esoteric and extremely prohibitive in terms of cost. Further, from an applications perspective, RHBP voltage references are difficult to procure as they are export-controlled items.

Given the limitations of the RHBP approach, it is apparent that the RHBD approach would be the appropriate approach. However, the design of the RHBD CMOS voltage reference is challenging in the sense that the prevalent CMOS voltage references at this juncture (including the bandgap reference and the subthreshold

voltage reference) are sensitive to TID effect [86]. This is because the TID effect deteriorates the characteristic of the BJT and MOSFET biased at subthreshold region [87, 88]. For the bandgap reference, the TID effect is serious – it is severe even when the irradiation dose rate is low – the phenomenon is known as the Enhanced Low Dose Rate Sensitivity (ELDRS) effect [89]. For example, [90] reported a bandgap reference with undesirable significant output variations of ~2% under a low ~200krad TID level.

Interestingly, despite the unsatisfactory performance of RHBD voltage references based on CMOS, deep-submicron CMOS is potentially advantages. Particularly, it is well established, at this juncture, that MOSFETs in <130nm commercial CMOS fabrication technology are largely and increasingly less sensitive to TID as the minimum feature-size scales smaller [91]. That is because the gate oxide thickness of deep-submicron MOSFET transistors is sufficiently thin, thereby leading to negligible TID effects when MOSFET transistors are biased at strong inversion; for completeness, MOSFET biased at weak inversion is still sensitive to TID due to the leakage current introduced by the thick isolation oxide [7, 87].

From an RHBD voltage reference design, the ZTC voltage reference realized in deep submicron CMOS is a potential solution to obtain a rad-hard voltage reference because all the MOSFETs therein can be biased at the TID-free strong inversion region. Nevertheless, no such design has been reported to date. We attribute this in part due to the immaturity of the design art of the ZTC-based voltage references. Put simply, for IoTs and satellites, a rad-hard voltage reference based on CMOS remains unreported.

In summary, the motivations of this Ph.D. research program stem from the ever-increasing demand for and the formidable design challenges of LDO for IoTs and voltage reference for both IoTs and satellites. Specifically, this Ph.D. research program

pertains to the design and monolithic realization in deep-submicron CMOS of a high PSRR, low dropout voltage LDO for IoTs, and of a high precision, rad-hard ZTC voltage reference for IoTs and satellites.

1.2 Objectives

In view of the aforesaid motivations, the overall objectives of this Ph.D. research program pertain to the design and monolithically realization of two rudimentary circuit blocks for PMIC – an LDO and a voltage reference. For the LDO for IoTs, the primary attribute of interest is an unprecedented high PSRR over a wide frequency range and over a wide load current range, yet with low dropout voltage. For the voltage reference for IoTs, the primary attributes of interest are a low TC over a wide temperature range, a high PSRR over a wide frequency range, and low voltage operation. For the voltage reference for satellites, the primary attributes of interest include the same said attributes for IoTs, but with an added immunity against radiation effects.

The specific objectives pertaining to the LDO are:

- (i) To review the fundamentals of LDO and state-of-the-art LDOs, particularly to analytically ascertain the mechanisms leading to the limitations of PSRR.
- (ii) For IoT applications, to design and monolithic realize in deep-submicron CMOS an LDO featuring high PSRR over a wide frequency range and over a large load current range, yet with a low dropout voltage for IoTs. The specifications for this LDO are tabulated in Table 1.1.

Table 1.1. Design specifications for the LDO.

Parameter	Specifications
Output voltage	1.0V
Dropout voltage	<100mV
Load current range	0-100mA
PSRR	>60dB (up to 10MHz)
Overshoot/undershoot	<10mV
Power dissipation	<50 μ W

The specific objectives pertaining to the voltage reference are:

- (a) To review the fundamentals of voltage reference and state-of-the-art voltage references, particularly to analytically ascertain the mechanisms leading to the limitations of TC, PSRR, low-voltage operation, and radiation hardness.
- (b) For IoT applications, to design and monolithically realize in deep-submicron CMOS a voltage reference featuring low-voltage, low TC (over a wide temperature range), and high PSRR (over a wide frequency range).

The specifications for this voltage reference are tabulated in Table 1.2.

Table 1.2. Design specifications for the voltage reference for IoTs.

Parameter	Specifications
Temperature range	-40°C to 125°C
Temperature Coefficient	<20ppm/°C
PSRR	>60dB (up to 10MHz)
Supply voltage	<1V
Power dissipation	<20 μ W

- (c) For satellite applications, to design and monolithically realize in deep-submicron CMOS a voltage reference as that specified in (b) above but with

immunity to radiation effects – a rad-hard voltage reference. The radiation immunity specifications are tabulated in Table 1.3 below.

Table 1.3. Radiation immunity specifications for the voltage reference for satellites.

Parameter	Specifications
TID immunity	up to 1Mrad
SEE immunity	up to 60MeV•cm ² /mg

1.3 Contributions

The contributions made in this Ph.D. research program and reported herein are congruous to the objectives outlined above. The overall contributions pertain to the design, monolithic realization and hardware characterization of two rudimentary circuit blocks for PMIC – a high PSRR LDO with low dropout voltage for IoTs, and a low TC high PSRR sub-1V voltage reference for IoTs and the same but with added immunity against radiation effects for satellites.

The specific contributions pertaining to the LDO are:

- (i) A comprehensive review of the fundamentals of LDOs and of state-of-the-art LDOs, and on the basis of this review, and investigation into the mechanisms leading to the limitations of PSRR.
- (ii) An investigation into the mechanisms of FFRC. Following this investigation, the proposal of a novel FFRC technique that adaptively optimizes the PSRR of the LDO over a wide frequency range and over a large load current variation.

- (iii) On the basis of said (ii), the design, monolithic realization, and physical characterization of a LDO based on 65nm CMOS and featuring the highest PSRR to date, yet with low dropout voltage for IoT applications. The key performance parameters of our LDO is tabulated in Table 1.4.

Table 1.4. Key performance parameters for the proposed LDO.

Parameter	Specifications
Output voltage	1.0V
Dropout voltage	80mV
Load current range	0.1mA-100mA
PSRR	87dB at DC
	62dB at 10MHz
Overshoot/undershoot	4mV
Power dissipation	40 μ W

The specific contributions pertaining to the voltage reference are:

- (a) A comprehensive review of the fundamentals of voltage references and state-of-the-art voltage references, and on the basis of this review, an investigation into the mechanisms leading to the limitations of TC, PSRR, and radiation hardness.
- (b) An investigation into the mechanism of the ZTC point of an NMOSFET, and the discovery of a previously unreported second-order mechanism/phenomenon of the ZTC point. This discovery lead to the proposal of a curvature compensation technique for MOSFET-only voltage references.
- (c) On the basis of the said (b), the design, monolithically realization, and physical characterization of a voltage reference based on 65nm CMOS and featuring low-voltage, low TC (over a wide temperature range), and high

PSRR (over a wide frequency range) for IoTs. The key performance parameters of our voltage reference is tabulated in Table 1.5.

Table 1.5. Key performance parameters for the proposed voltage reference for IoTs.

Parameter	Specifications
Temperature range	-40°C to 125°C
Temperature Coefficient	5.6ppm/°C
PSRR	87dB at DC
	65dB at 10MHz
Supply voltage	0.8V
Output variation	<1%
Power dissipation	13μW

- (d) The proposal of an RHBD voltage reference, in part, based on our discovered ZTC phenomenon in (b).
- (e) On the basis of the said (d), the design, monolithic realization, and physical characterization under irradiation of a voltage reference based on 130nm CMOS for satellites. The realized voltage reference featured immunity against radiation effects – the only rad-hard voltage reference to date realized with full MOSFET. The radiation immunity of this voltage reference against TID and SEEs are tabulated in Table 1.6 below.

Table 1.6. Radiation immunity specifications for the voltage reference for satellites.

Parameter	Specifications
TID immunity	up to 1Mrad
SEE immunity	up to 77MeV•cm ² /mg

1.4 Organization

The remainder of this thesis is organized as follows.

In Chapter 2, a comprehensive and critical literature review on LDO and voltage reference is provided in turn to serve as the preamble for the following Chapters 3 and 4, respectively; including a review of radiation effects on ICs. Specifically, for the review of the LDO, an overview of LDO terminology and key design parameters are first described. Subsequently, prior art design techniques pertaining to PSRR improvement are presented, and several state-of-the-art LDOs featuring high PSRR are reviewed with a succinct but critical analysis of their respective merits and limitations. For the review of the voltage reference, an overview of the terminology and key design parameters of the voltage reference is first described. Subsequently, well established and accepted voltage reference topologies are presented with several representatives; followed by a succinct but critical review of the merits and limitations of state-of-the-art voltage reference. For the review of radiation effects, the mechanism of the TID effect and various SEEs are described.

In Chapter 3, the design of our proposed LDO realized in 65nm CMOS featuring >60dB PSRR over a 10MHz frequency range and over a 100mA load current range is described, including its monolithic realization, and characterization by means of hardware measurements. This design embodies a novel adaptive FFRC technique leading to the said high PSRR. In addition to PSRR, comprehensive analyses on the stability and the dropout voltage of the proposed LDO are also presented. Lastly, the proposed LDO is benchmarked against state-of-the-art designs.

In Chapter 4, the design of our proposed high precision rad-hard ZTC voltage reference is presented, including its monolithic realization, and characterization by means of hardware measurements. This design embodies our proposed of a new phenomenon for the ZTC point. On the basis of our discovery of this phenomenon, the proposed voltage reference featuring a low TC over a wide temperature range is delineated. The design considerations towards PSRR and process variations are subsequently presented. The radiation hardness of the proposed voltage reference is also investigated and verified by irradiation tests, and the ensuing radiation hardness are demonstrated. Lastly, the proposed voltage reference is benchmarked against state-of-the-art designs.

In Chapter 5, conclusions of the thesis are drawn and recommendations for future work are presented.

Chapter 2

Literature Review

In this chapter, the LDO and the voltage reference will be reviewed in turn, including a delineation of several representative state-of-the-art LDO and voltage reference designs. The radiation effects on ICs will also be reviewed. These reviews, in part, serve as a preamble to our LDO and voltage reference designs in Chapters 3 and 4, respectively.

2.1 Review of the design of the LDO

In this section, we will first review the fundamentals of the LDO, including its operating mechanisms and the associated critical design parameters. Subsequently, several LDO topologies will be reviewed, followed by considerations for the design of LDOs for various applications. This review emphasizes PSRR, as described in Chapter 1, due to its imperative need in the PMIC for IoTs. This review will further include various reported PSRR enhancing techniques with several representative designs, and our critical appraisal of their merits and limitations.

2.1.1 Review of the design parameters of an LDO

The design-art of LDOs is very mature and some of the earliest designs go back to the early 1970s [92]. The primary function of the LDO is to provide its load circuit with a robust and low-noise output voltage, V_{out} , that is insensitive to supply voltage and load current variations. A simplified LDO block diagram was depicted earlier in

Figure 1.2, where the V_{out} regulation is achieved by means of a regulation loop. We will now discuss several critical design parameters of the LDO – dropout voltage, line regulation, load regulation, PSRR, and noise – in turn.

Dropout voltage

The dropout voltage (V_{do}) is the voltage difference between the minimum input voltage of an LDO, V_{in_min} , and V_{out} , i.e., $V_{do}=V_{in_min}-V_{out}$. Figure 2.1 depicts V_{out} versus V_{in} of an ideal LDO with dropout, where the LDO requires a minimum $V_{in}=V_{in_min}$ to achieve the desired V_{out} regulation. For the case when $V_{in}<V_{in_min}$, V_{out} is unregulated due to the insufficient loop gain of the regulation loop. Note that in practice the V_{out} - V_{in} characteristic depicted in Figure 2.1 varies with I_{load} . In general, V_{in_min} (and hence V_{do}) increases as I_{load} increases [2].

In view of this, V_{do} of an LDO should be specified under the worst-case condition where $I_{load}=I_{load_max}$, the maximum I_{load} specified. In general, a low V_{do} reduces the power loss by the power transistor, hence high power-efficiency and a better thermal performance. In view of this, there is a continuous effort to reduce the dropout voltage of an LDO. At this juncture of LDO technology-art, state-of-the-art LDOs [48] can achieve a V_{do} of $\sim 100\text{mV}$ with $\sim 300\text{mA}$ maximum I_{load} .

Figure 2.1. V_{out} versus V_{in} of an ideal LDO with dropout voltage.

Line Regulation

The Line Regulation (L_R) is a static design parameter that specifies the sensitivity of the V_{out} of an LDO against V_{in} variations. Figure 2.2 depicts the V_{out} versus V_{in} of a practical LDO. Unlike the plot in Figure 2.1 where V_{out} is insensitive to V_{in} when $V_{in} > V_{in_min}$, V_{out} is practically sensitive to V_{in} . This is because the loop gain is finite. L_R is expressed as:

$$L_R = \frac{\Delta V_{out}}{\Delta V_{in}} \quad (\text{for } V_{in} > V_{in_min}) \quad (2.1)$$

L_R is ascertained by the loop gain of the regulation loop of the LDO, where a large loop gain leads to a desirable small L_R [2].

Figure 2.2. V_{out} versus V_{in} of a practical LDO.

Load Regulation

The Load Regulation (LD_R) is a static design parameter that measures the sensitivity of the V_{out} of an LDO to load current, I_{load} , variations. Figure 2.3 depicts the V_{out} versus I_{load} of both an ideal LDO and a practical LDO. V_{out} is practically sensitive to I_{load} due to the finite loop gain. LD_R is expressed as:

$$LD_R = \frac{\Delta V_{out}}{\Delta I_{load}} \quad (2.2)$$

LD_R is largely ascertained by the loop gain of the regulation loop, where a large loop gain leads to a desirable small LD_R [2].

Figure 2.3. V_{out} versus I_{out} of an ideal and a real LDO.

Load Transient Response

The load transient response is a measure of how V_{out} responds to the dynamic variations of I_{load} and is characterized with a load current (I_{load}) step. The rising (falling) times of the I_{load} step are usually in the range of several tens of ns to several μ s [30, 35]; a short rising (falling) time causes a large output transient. Figure 2.4 depicts the load transient response of an LDO, from where the overshoot, undershoot, and the settling time are indicated. The load transient response of an LDO is ascertained by its output impedance. At low frequencies within the regulation loop bandwidth, the output impedance is effectively attenuated by the regulation loop [2, 76]. For frequency beyond the regulation loop bandwidth, the output impedance is largely ascertained by the inherent characteristics of the load circuit of the LDO [28, 48].

Figure 2.4. Load transient response of an LDO.

Power Supply Rejection Ratio (PSRR)

PSRR measures the small signal gain of v_{out}/v_{in} (v_{in} refers to noise on the power supply of the LDO, typically 10s of mV) over a specified frequency range (e.g., from 10Hz to 10MHz). The PSRR at a given frequency point is obtained as

$$PSRR = 20\log(v_{out}/v_{in}) \quad (2.3)$$

It is worthy to note that the PSRR of an LDO is related to many other design parameters, including load current, dropout voltage, etc. [2] In view of this, the test condition would need to be adequately defined for the PSRR measurement. PSRR is one of the most critical design parameters of LDOs for IoTs because its input is connected to the output of a switching regulator containing substantial switching noise [16, 21]. A succinct but critical analysis of PSRR for various LDO topologies will be delineated in the next subsection.

Noise

Noise in an LDO is a physical phenomenon that occurs with transistors and resistors [42]. It can be characterized based on spectral noise density or integrated noise, where their units are $\mu\text{V}/\sqrt{\text{Hz}}$ and μV_{rms} , respectively. It is well established that the voltage reference is the primary noise contributor of the LDO because V_{out} of an LDO is an amplified version of the voltage reference output [51]. In view of this, a passive filter is often placed after the output of the voltage reference to obtain low noise. The noise performance of an LDO also depends on the closed loop gain and the stability of the regulation loop. Insufficient phase margin may cause undesired closed loop gain peaking near the unity-gain frequency point [31]. Consequently, noise at these frequencies is amplified and may become unacceptably significant.

We have reviewed several critical design parameters of the LDO. For IoTs, the critical design parameters include dropout voltage, PSRR, and light-load current efficiency due to the limited power budget and the noisy power supply. In view of this review, the primary targets of our design in Chapter 3 for the LDO for IoTs are low dropout voltage and high PSRR beyond that provided by state-of-the-art LDOs.

2.1.2 Review of the LDO topologies

In view of the maturity of the design-art of the LDO, it is not surprising that there are numerous reported LDO topologies, each having its specific merits and limitations. Choosing the appropriate LDO topology is a somewhat critical design consideration for the specific application. We will now critically review several representative LDO topologies.

There are several ways to categorize the different LDO topologies and two types of categories are most prevalent. First, on the basis of the power transistor type, LDOs can be categorized into either a PMOS LDO [35, 40, 43] and an NMOS LDO [47-49]. Second, on the basis of the presence of output capacitor, LDOs can be categorized into cap-LDO and capless-LDO.

Consider now the first category where LDOs are categorized based on the power transistor type. Figures 2.5(a) and (b) depict the block diagram of a PMOS LDO and an NMOS LDO, respectively. There are two primary differences between the PMOS LDO and the NMOS LDO. First, the V_{REF} is applied to the positive input terminal of the opamp in PMOS LDO, whereas V_{REF} is applied to the negative input terminal of the opamp in NMOS LDO. This is because the power stage of the PMOS LDO is in a common-source configuration with negative gain, while the power stage of the NMOS LDO is in common-drain configuration with positive gain. The second difference is

manifested in the power supply of the opamp. Specifically, in the PMOS LDO, the opamp and the PMOS power transistor can share the same V_{in} . In contrast, in the NMOS LDO, the opamp requires a higher supply voltage, V_H ($V_H > V_{in}$) to achieve a low dropout voltage [48]. This is because V_{gs} of the NMOS power transistor usually exceeds the dropout voltage. The requirement of the additional power supply, V_H , somewhat increases the design complexity of the NMOS LDO, and its application.

Figure 2.5. The block diagram of an (a) PMOS LDO, and a (b) NMOS LDO.

Due to the increased design complexity of the NMOS LDO over its PMOS counterpart, its application used to be less prevalent. Nevertheless, in the contemporary battery-powered IoTs, the V_{in} of the LDOs is usually the output of a buck (step-down) DC-DC converter, and the relatively higher V_H voltage can be readily provided by the battery – the battery voltage is higher than that of the buck DC-DC converter. In view of this, it is not surprising that NMOS LDOs are increasingly applied in battery-powered IoTs [48].

The NMOS LDO outperforms its PMOS counterparts in many aspects including dropout voltage, load transient response, silicon area, etc. A low dropout voltage LDO requires the power transistor to operate in the triode region, and therefore degrades the

power stage gain of both the NMOS and PMOS LDO. Nevertheless, in the NMOS LDO, as the power stage is in common-drain configuration, it suffers from lesser gain degradation compared to the common-source power stage of the PMOS LDO. Consequently, the NMOS LDO can advantageously tolerate a smaller dropout voltage without deteriorating its performance [47].

The superior transient response of NMOS LDO stems from its relatively low output resistance [28]. Note that the inherent Z_{out} of an NMOS LDO is $\sim 1/g_m$ (g_m is the transconductance of the power transistor), whereas the Z_{out} of a PMOS LDO is $\sim r_{out}$ (r_{out} is the output resistance of the power transistor). Finally, the NMOS LDO requires less silicon area than the PMOS LDO for the same channel resistance because electrons feature higher mobility compared to holes [93]. In contemporary applications where cost is a critical design parameter, the NMOS LDO is hence advantageous.

Consider now the second category where LDOs are categorized based on the presence of the output capacitor [2]. The LDO requiring and not requiring an output capacitor (several μF) are named as the cap-LDO and the capless-LDO, respectively. The capless-LDO evidently offers a smaller form factor compared to the cap-LDO [45]. However, the performance of the capless-LDO is compromised particularly in terms of load transient response [28] and PSRR at high frequencies. The cap-LDO features superior load transient response that can accommodate the rapid load current changes without affecting V_{out} of the LDO. This is because the large capacitor serves as a charge reserve and can provide instantaneous current according to the load demands.

Consider now the PSRR at high frequencies. The PSRR at high frequencies is largely ascertained by the impedance divider comprising the impedance of the power transistor and the output impedance (see later in section 2.1.3). A large output capacitor

advantageously contributes to a small output impedance, thereby facilitating a high PSRR at high frequency [29].

The selection of the LDO topology is highly application-dependent. Table 2.1 tabulates the power supply requirement for several analog, mixed-signal and RF circuits based on a reported survey [94]. Not unexpectedly, the cap-LDO is the common and unique solution for all the (tabulated) noise-sensitive circuits because of its superior load transients and higher PSRR. It is interesting to note that the dropout voltage of the LDO for RF circuits is higher than most other applications because RF circuits have more stringent requirements on power supply quality [33]. The higher dropout voltage, in general, facilitates higher PSRR by allowing the insertion of augmented circuits (e.g., passive low pass filter [29] and cascode transistor [34]) in series with the power transistor.

Table 2.1. Power supply requirement for several analog, mixed-signal, and RF circuits.

	Amplifiers	Mixers/RF	ADC/DAC	RF PA	PLL/VCO	Transceivers
% of analog	99%	99%	50%	100%	50%	80%
Analog section	amplifier	amplifier	S/H, amplifier, clock	bias gain control, amplifier	VCO, charge pump	ADC/DAC/ VCO/PA
Digital section	gain control	gain control	digital core, interface	Nil.	driver	digital core interface
Target DC accuracy	5%	5%	5%	5%	5%	2%
Noise sensitivity (frequency)	high (>100kHz)	high (DC to GHz)	high (>100kHz)	very high (DC to GHz)	very high (DC to GHz)	very high (DC to GHz)
Ripple requirement	<100 μ V	<100 μ V	1mV	<10 μ V	<100 μ V	<100 μ V
Typical Power solution	switching regulator + cap-LDO	switching regulator + cap-LDO	switching regulator + cap-LDO	cap-LDO (higher dropout)	cap-LDO (higher dropout)	cap-LDO (higher dropout)

Capless-LDOs, on the other hand, are often utilized for digital circuits despite their PSRR being inferior to cap-LDOs. This is because digital circuits, in general, can

tolerate larger supply noise due to their large noise margin [30]. In this case, the small form factor of the capless-LDO is advantageous.

We have critically reviewed various LDO topologies. This review ascertains the appropriate LDO topology for IoTs and leading to the parameters of our design in Chapter 3 – an NMOS cap-LDO. Specifically, the NMOS power transistor and the output capacitor facilitate low dropout voltage and high PSRR, respectively.

2.1.3 Review of the PSRR mechanisms of the LDO

As delineated earlier, the PSRR is arguably the most important design parameter for LDOs for noise-sensitive circuit (e.g., data converters, RF power amplifiers, Phase Lock Loops (PLL), and etc.), particularly in view of the noisy switching regulator that precedes the LDO. We will now review the mechanisms of the PSRR of an LDO to ascertain the mechanisms leading to the limitation of the PSRR.

The PSRR of an LDO can be analyzed and expressed based on Mason's gain formula [95] where

$$PSRR = \frac{v_{out}}{v_{in}} = \frac{\sum FF_p}{1 - \sum L} \quad (2.4)$$

where FF_p is the gain of the feedforward signal path from V_{in} to V_{out} , and

L is the loop gain.

Figure 2.6 depicts the conceptual schematic of a PMOS cap-LDO, and there are three feedforward signal paths from V_{in} to V_{out} , where FF_{p1} , FF_{p2} , and FF_{p3} are signal paths via the power transistor, the opamp, and the voltage reference, respectively. The

effect of FF_{p3} can be minimized by means of a high PSRR voltage reference and will now be discussed.

We can easily express the sum of the gain of FF_{p1} and FF_{p2} as:

$$\begin{aligned}
 FF_{p1} + FF_{p2} &= \left. \frac{v_{out}}{v_{in}} \right|_{p1} + \left. \frac{v_{out}}{v_{in}} \right|_{p2} \\
 &= (g_m + g_{ds})Z_{out} - A_{dd_opamp}g_mZ_{out} \\
 &= ((1 - A_{dd_opamp})g_m + g_{ds})Z_{out}
 \end{aligned} \tag{2.5}$$

where g_m and g_{ds} are the transconductance and the output conductance of the power transistor, respectively,

A_{dd_opamp} is the noise coupling via the opamp, and

Z_{out} is the output impedance of the LDO.

Figure 2.6. Conceptual schematic of a PMOS cap-LDO for PSRR analysis.

Figure 2.7 depicts the conceptual schematic of an NMOS cap-LDO, where there are also three signal paths from the power supplies (V_{in} and V_H) to V_{out} . In this case, we can easily express the sum of the gain of FF_{p1} and FF_{p2} as

$$\begin{aligned}
FF_{p1} + FF_{p2} &= \left. \frac{v_{out}}{v_{in}} \right|_{p1} + \left. \frac{v_{out}}{v_{bat}} \right|_{p2} \\
&= g_{ds} Z_{out} + A_{dd_opamp} g_m Z_{out}
\end{aligned} \tag{2.6}$$

Figure 2.7. Conceptual schematic of an NMOS cap-LDO for PSRR analysis.

From eqns. (2.5) and (2.6), it can be noted that the A_{dd_opamp} of the opamp has a significant impact on the PSRR of the LDO. Specifically, A_{dd_opamp} should be close to 1 (i.e., unity) to achieve a high PSRR for the PMOS LDO, and A_{dd_opamp} should be close to 0 to achieve a high PSRR for the NMOS LDO.

The opamp in LDO is usually realized with a differential-input and single-end-output structure embodying a diode-connected MOSFET for differential-to-single-end conversion [93]. A_{dd_opamp} is ascertained from the topology of the opamp, particularly the implementation of the said differential-to-single-end conversion. Figures 2.8(a) and (b) depict two opamp topologies where the differential-to-single-end conversion are implemented with a diode-connected PMOS and NMOS, respectively. We name the respective opamp as type-P and type-N opamp, respectively. As delineated above, it is well established that the type-P opamp is the appropriate opamp topology for PMOS LDO requiring $A_{dd_opamp}=1$, and the type-N opamp is the appropriate opamp topology for NMOS LDO requiring $A_{dd_opamp}=0$ [96].

Figure 2.8. Schematic of the (a) type-P opamp, and (b) type-N opamp.

Consider now the A_{dd_opamp} of the type-P opamp and the type-N opamp in turn. In the type-P opamp, there are two signal paths (i.e., path P1 via M_{p1} , and path P2 via M_{p2} , M_{p3} , and M_{p4}) from V_{in} to V_{out_op} . The current flowing through path P1 (i_{p1}) and path P2 (i_{p2}) are respectively:

$$i_{p1} = v_{in} (g_{m_p1} + g_{ds_p1}) \quad (2.7)$$

$$i_{p2} = v_{in} (-g_{m_p2} + g_{ds_p3}) \quad (2.8)$$

On the basis of eqns. (2.7) and (2.8), we can derive A_{dd_opamp} of type-P opamp as:

$$\begin{aligned} A_{dd_opamp} &= \frac{v_{out_op}}{v_{in}} \\ &= \frac{(i_{p1} + i_{p2})Z_{out_op}}{v_{in}} \\ &= \frac{g_{m_p1} - g_{m_p2} + g_{ds_p1} + g_{ds_p3}}{g_{ds_p1} + g_{ds_p4}} \end{aligned} \quad (2.9)$$

In practice, as (M_{p1}, M_{p2}) , and (M_{p3}, M_{p4}) are designed to be matched transistor-pairs, $g_{m_p1} \approx g_{m_p2}$, and $g_{ds_p3} \approx g_{ds_p4}$. In view of this, A_{dd_opamp} of type-P opamp is ~ 1 .

In contrast, A_{dd_opamp} of the type-N opamp is ~ 0 . In the type-N opamp, the ripple on V_{in} leads to a ripple on V_x . Hence, V_{out} is affected by two signal paths (i.e., path N1 via M_{N1} , and path P2 via M_{N2} , M_{N3} , and M_{N4}) from V_x to V_{out_op} . The currents flowing through path P1 (i_{n1}) and path P2 (i_{n2}) are, respectively:

$$i_{n1} = v_x g_{m_n1} \quad (2.10)$$

$$i_{n2} = -g_{m_n4} v_y = -g_{m_n4} (g_{m_n2} / g_{m_n3}) v_x \quad (2.11)$$

In practice, as both (M_{N1}, M_{N2}) and (M_{N3}, M_{N4}) are designed to be matched transistor-pairs, $g_{m_n1} = g_{m_n2}$, and $g_{m_n3} = g_{m_n4}$. In view of this, $i_{n1} + i_{n2} \approx 0$, and A_{dd_opamp} of the type-N opamp is ~ 0 .

Consider now the frequency response of the PSRR of an LDO by analyzing eqn. (2.4). In view of the pole at the V_{out} node ($\omega = \omega_{po}$) and the dominant pole of the regulation loop ($\omega = \omega_{p1}$), we rewrite eqn. (2.4) as:

$$\begin{aligned} PSRR &= \frac{\frac{A_F}{1 + s / \omega_{po}}}{1 + \frac{A_L}{1 + s / \omega_{p1}}} \\ &= \frac{A_F}{A_L} \frac{(1 + s / \omega_{p1})}{(1 + s / \omega_{po})(1 + s / \omega_{pu})} \end{aligned} \quad (2.12)$$

where A_F and A_L are the DC feedforward gain from V_{in} to V_{out} and the DC loop gain, respectively, and

$\omega_{pu} = A_L \omega_{p1}$ is the unity gain frequency of the regulation loop.

From eqn. (2.12), the frequency of ω_{po} , ω_{p1} , and ω_{pu} ascertains the PSRR in the frequency domain. Consider now two scenarios, $\omega_{po} > \omega_{p1}$ and $\omega_{po} = \omega_{p1}$.

Figures 2.9(a) and (b) depict the PSRR versus frequency for $\omega_{po} > \omega_{p1}$ and $\omega_{po} = \omega_{p1}$, respectively; note the specific definition of PSRR in eqn. (2.3). In Figure 2.9(a), for the case where $\omega_{po} > \omega_{p1}$, the PSRR of the LDO deteriorates in the mid-range frequencies (from ω_{p1} to ω_{po}). On the other hand, for the case where $\omega_{po} = \omega_{p1}$ in Figure 2.9(b), the PSRR is superior in the sense that the PSRR does not degrade in the mid-range frequencies. This is because the effects of ω_{po} and ω_{p1} cancel one another, to a first order.

Figure 2.9. PSRR of an LDO for (a) $\omega_{po} > \omega_{p1}$, and (b) $\omega_{po} = \omega_{p1}$.

Note that $\omega_{po} > \omega_{p1}$ is often the case for the capless-LDO where ω_{po} is located at high frequency and is a potential stability issue [45]. As a result, a frequency compensation scheme (e.g., Miller compensation [93], cascode frequency compensation [97], or damping factor control compensation [98]) is applied to ascertain a lower ω_{p1} to ensure the stability of the regulation loop. On the other hand, $\omega_{po} = \omega_{p1}$ is often the case for the cap-LDO where ω_{po} is located at low frequency due to the large output capacitor ($\sim \mu\text{F}$). In view of this, the cap-LDO, in general and expectedly, outperforms the capless-LDO in terms of PSRR, particularly in the mid and high frequencies.

We have reviewed the impact of the error amplifier on the PSRR of an LDO. This review leads to the adopted topology of the opamp utilized in our proposed LDO in Chapter 3 – the type-N opamp for an NMOS LDO. We have also reviewed the impact of the output capacitor on the PSRR of an LDO where we have derived that cap-LDO features higher PSRR than capless-LDO.

2.1.4 Review of prior-art PSRR enhancing techniques

In view of the increasingly stringent PSRR requirement of LDOs for IoTs, the desired high PSRR cannot be achieved solely by appropriately choosing the topologies of the LDO and the opamp. Hence it is increasingly imperative to adopt PSRR enhancement techniques. We will now review several prevalent PSRR enhancement techniques [29, 33, 34, 39, 40, 45], including the pre-regulation [29, 34] and the FeedForward Ripple Cancellation (FFRC) [40, 45] techniques.

Pre-regulation technique

The pre-regulation technique is generally realized by a circuit augmented after the LDO input to shield the power transistor. Figure 2.10 depicts an example [34]. To obtain high PSRR, a cascode NMOS transistor is placed between V_{in} and the supply of the main LDO to increase the resistance between V_{in} and V_{out} [34]. However, the cascode NMOS transistor imposes two issues. First, a high gate voltage (higher than V_{in}) is required for the NMOS transistor. To obtain this, a charge pump is utilized to generate the said high gate voltage. Second, the cascode NMOS augments a new signal path from V_{in} to V_{out} via the gate of the NMOS. To mitigate the effect of this new signal path, a voltage reference with an output RC filter is often utilized to provide a clean gate voltage for the NMOS. Consequently, the hardware overhead is undesirably increased.

Figure 2.10. A high PSRR LDO with a cascode NMOS.

A reported [34] LDO design embodying the cascode NMOS achieved a ~ 30 dB PSRR improvement (over a 10MHz frequency range) over its counterpart without the cascode NMOS. However, the cascode NMOS adversely compromises the dropout voltage and load transient response. Specifically, the dropout voltage of the prototype design is a high 0.6V, and the undershoot voltage increases by 171mV compared to the case without the cascode NMOS. Moreover, as the reported design [34] is a capless-LDO, the high-frequency PSRR is inherently low (27dB at ~ 6 MHz) despite having the cascode NMOS.

FeedForward Ripple Cancellation (FFRC) technique

The FFRC technique is often realized by augmenting a compensation signal path from the input to the LDO output. Specifically, the gain of the augmented signal path is designed to be opposite of the gain of the inherent signal path from V_{in} to the LDO output. Figures 2.11(a) and (b) depict the schematic and the signal flow diagram of an FFRC LDO [40], respectively. In Figure 2.11(a), a feedforward amplifier is utilized to amplify V_{in} , and the feedforward gain is defined by the ratio of two resistors, R_{ff1} and R_{ff2} . The output of the feedforward amplifier is thereafter combined with the output of

the error amplifier of the main regulation loop by a summing amplifier. Figure 2.11(b) depicts the signal flow diagram of the FFRC LDO. From this, the PSRR of the FFRC LDO can be derived as:

$$PSRR = \frac{v_{out}}{v_{in}} = \frac{g_{ds_MP} + (1 - A_{ff} A_{sum}) g_{m_MP}}{1 - \sum L} \quad (2.13)$$

where g_{m_MP} and g_{ds_MP} are the transconductance and the output conductance of M_P , respectively,

A_{ff} and A_{sum} are the gain of the feedforward amplifier and the summing amplifier, respectively, and

L is the regulation loop gain.

From (2.13), the PSRR of the FFRC LDO can be optimized (i.e., $v_{out}/v_{in}=0$) by designing

$$A_{ff} A_{sum} = 1 + g_{ds_MP} / g_{m_MP}. \quad (2.14)$$

For completeness, the capacitor C_{ff} is utilized to compensate for the pole of the summing amplifier so that eqn. (2.14) is valid over a wide frequency range.

A reported design based on the said FFRC technique achieved a PSRR improvement of ~20dB (when the load current is 25mA) over its counterpart without FFRC. Of particular interest, the FFRC technique does not compromise the dropout voltage because the feedforward signal path is implemented in parallel with the power transistor. In view of this, the reported design [40] achieved a low dropout voltage of ~150mV. However, the effectiveness of the reported FFRC LDO may not be robust over wide load current variations, i.e., its PSRR may deteriorate depending on the load conditions. This is because the gain of the feedforward signal path is a *fixed* value that

is determined by the feedback resistors while the optimum feedforward gain is a *dynamic* parameter that pertains to the intrinsic gain of the power transistor (see eqn. (2.14)) and is subjected to the load current, temperature, and process variations.

Figure 2.11. FFRC LDO: (a) Block diagram, and (b) Signal flow diagram.

We have reviewed the pre-regulation and the FFRC techniques for PSRR enhancement with a critical review of their merits and shortcomings. Reported designs embodying these two techniques have demonstrated their effectiveness in various applications. Nevertheless, in view of our target IoTs, these state-of-the-art techniques remain insufficient. Specifically, the pre-regulation technique incurs an undesirably

high dropout voltage, and the reported FFRC LDO may not be able to accommodate the wide-space variations (e.g., load current variation) of IoTs.

2.2 Review of the design of the voltage reference

In this section, we will first review the fundamentals of the voltage reference including the operating mechanisms and the associated critical design parameters. Subsequently, several voltage reference topologies, including the prevalent bandgap and the subthreshold topologies, will be reviewed. This review includes our critical appraisal of the merits and limitations of state-of-the-art voltage references for IoT applications.

2.2.1 Review of design parameters of the voltage reference

The primary function of a voltage reference is to generate a robust reference voltage, V_{REF} , against Process, Voltage, and Temperature (PVT) variations [93]. Several critical parameters that qualify its performance will now be described in turn, including Temperature Coefficient (TC), initial accuracy, line sensitivity, PSRR, and noise.

Temperature Coefficient (TC)

TC is the parameter that qualifies the temperature-insensitivity of V_{REF} and whose dimension unit is part-per-million per degree Celsius (ppm/°C). It is expressed [3] as:

$$TC = \frac{V_{REF_MAX} - V_{REF_MIN}}{V_{REF_NOM} (T_{MAX} - T_{MIN})} \times 10^6 \quad (2.15)$$

where V_{REF_MAX} and V_{REF_MIN} are the maximum V_{REF} and the minimum V_{REF} in the temperature range of T_{MIN} to T_{MAX} , respectively, and

V_{REF_NOM} is the nominal V_{REF} .

TC is characterized by different temperature ranges for various application standards. Specifically, the commercial, industrial, extended industrial, and military temperature ranges are 0°C to 85°C, -40°C to 100°C, -40°C to 125°C, and -55°C to 125°C, respectively [76].

Initial accuracy

The initial accuracy reflects how tight the distribution of V_{REF} of a number of voltage reference samples is, and it can be qualified by the coefficient of variation, σ/μ , where σ and μ are the standard deviation and the mean value of V_{REF} , respectively [99]. The initial accuracy of V_{REF} is critical for systems where calibration is not applicable. However, for systems where calibration is allowed – the more common case – the initial accuracy is less important. This is because post-fabrication calibration (e.g., trimming) can adjust V_{REF} to the desired value [100].

Line Sensitivity (LS) and PSRR

LS qualifies how sensitive V_{REF} is against supply voltage variations, and is expressed [3] as:

$$LS = \frac{V_{REF_MAX} - V_{REF_MIN}}{V_{DD_MAX} - V_{DD_MIN}} \quad (2.16)$$

where V_{REF_MAX} and V_{REF_MIN} are the maximum V_{REF} and the minimum V_{REF} in the supply voltage range of V_{DD_MIN} to V_{DD_MAX} , respectively.

PSRR, on the other hand, measures the small-signal gain of v_{ref}/v_{dd} (where v_{dd} is the supply noise), and is typically quantified over the frequency range of interest. Low LS and high PSRR are typically critical for the voltage reference, particularly for the applications where the supply of the voltage reference is noisy or when noise is not tolerated.

Noise

The output noise of V_{REF} is typically a critical parameter for low-noise and high-precision applications. However, in view of the usual practice of the augmentation of a bypass capacitor that filters high-frequency noise in practical applications, the frequency range of noise of interest is, in general, narrow, e.g., from 0.1Hz to 10kHz [100].

In view of the maturity of the design-art of voltage references, it is not surprising that there are numerous reported voltage reference topologies. Amongst these topologies, the bandgap references and the subthreshold voltage references are the most prevalent. A critical review on these two topologies will be reviewed in turn in the subsequent sections.

2.2.2 Review of the design of bandgap references

Bandgap references are arguably the most prevalent voltage references. We will now review the design concept/techniques of bandgap references. This review includes a critical appraisal of the merits and limitations of bandgap references.

The concept of the bandgap reference

The bandgap reference achieves the temperature-insensitive V_{REF} by exploiting the I - V characteristic of the BJT. The I_C - V_{BE} characteristic of a BJT [76] can be expressed as

$$I_C = AI_S \exp(V_{BE} / V_T) \quad (2.17)$$

where I_C is the collector current of the BJT,

A is the base-emitter junction area of the BJT,

I_S is the saturation current,

V_{BE} is the base-emitter voltage of the BJT,

$V_T = kT/q$ is the thermal voltage,

k is the Boltzmann constant, and

T is the absolute temperature.

From eqn. (2.17), V_{BE} as a function of T can be expressed as,

$$V_{BE}(T) = V_{BE}(T_r) \frac{T}{T_r} + V_T \ln\left(\frac{I_C(T)}{I_C(T_r)} \times \frac{I_S(T_r)}{I_S(T)}\right) \quad (2.18)$$

where T_r is an arbitrary temperature.

As I_S is temperature dependent [93], where $I_S \propto \mu k T n_i^2$, $\mu \propto T^m$ is the carrier mobility, $n_i^2 \propto T^3 \exp[-E_g/(kT)]$ is the intrinsic minority carrier concentration of silicon, m is the temperature exponent of μ , and E_g is the bandgap energy of silicon, $V_{BE}(T)$ can be rewritten as

$$\begin{aligned}
V_{BE}(T) &= V_{BG} - \frac{V_{BG} - V_{BE}(T_r)}{T_r} T - (\eta - \gamma) V_T \ln \frac{T}{T_r} \\
&= V_{BG} - \left(\frac{V_{BG} - V_{BE}(T_r)}{T_r} + (\eta - \gamma) \frac{k}{q} \ln T_r \right) T - (\eta - \gamma) V_T \ln T
\end{aligned} \tag{2.19}$$

where $V_{BG}=E_g/q$ is the bandgap voltage of silicon,

$\eta=4+m$ [64], and

β is the temperature exponent of IC, assuming $I_C \propto T^\beta$.

In view of eqn. (2.19), V_{BE} of the BJT is a Complementary To Absolute Temperature (CTAT) voltage, and combining it with a Proportional To Absolute Temperature (PTAT) voltage, a temperature insensitive V_{REF} can be obtained. In the bandgap reference, the said PTAT voltage is generated by the V_{BE} difference, ΔV_{BE} , of two BJTs (e.g., BJT1 and BJT2) with different current densities. ΔV_{BE} can hence be expressed as:

$$\Delta V_{BE} = V_T \ln \left(\frac{I_1 / A_1}{I_2 / A_2} \right) \tag{2.20}$$

By appropriately scaling of ΔV_{BE} and combining it with V_{BE} , V_{REF} is, to the first order, temperature-insensitive, and $V_{REF}=V_{BG}$. However, V_{REF} of the bandgap reference, in general, suffers from higher-order temperature dependency due to the $V_T \ln T$ in eqn. (2.19) [64]. Note that V_{BE} is not linearly related to temperature unless $\eta-\gamma=0$, which is difficult to achieve. As a result, V_{REF} of a generic bandgap reference suffers from $>10\text{ppm}/^\circ\text{C}$ temperature coefficient within $\sim 100^\circ\text{C}$ temperature range [60].

Note that $V_{REF}=V_{BG}$ is the bandgap voltage of silicon which pertains to material property and is not subjected to process variations. Leveraging on this, V_{REF} of bandgap reference can feature excellent robustness against process variations [3].

Bandgap reference in bipolar (Widlar bandgap [92] and Brokaw bandgap [101])

Figure 2.12 depicts the first bandgap reference circuit proposed by Widlar in 1971 [92]. V_{REF} herein is obtained by combining the V_{BE} of Q_3 , V_{BE_3} , with a scaled $\Delta V_{BE1,2}$; the V_{BE} difference between Q_1 and Q_2 . V_{REF} is expressed as

$$V_{REF} = V_{BE_3} + \frac{R_2}{R_3} \Delta V_{BE1,2} \quad (2.21)$$

Figure 2.12. Widlar bandgap reference [92].

The reported Widlar bandgap reference was fabricated in bipolar technology, and it featured very low V_{REF} temperature drift (0.02%/°C over -55°C to 125°C; equivalent to ~20ppm/°C TC) by adopting the bandgap concept and by exploiting the V_{BE} of the npn transistor. However, the Widlar bandgap reference suffered from several drawbacks including the non-adjustable output (V_{REF} is fixed at V_{BG}) and the output error caused by the base current flowing in R_1 and R_2 ; the base current introduces error into the current density ratio of Q_1 and Q_2 .

Figure 2.13 depicts the Brokaw bandgap reference [101] that reported resolved the said two drawbacks in the Widlar bandgap reference. Specifically, V_{REF} of the

Brokaw bandgap reference is adjustable by means of augmenting follower Q_7 and resistors R_4 and R_5 , and the base current issue is resolved by R_3 , where R_3 is designed to

$$R_3 = \frac{R_2}{R_1} \times \frac{R_4 R_5}{R_4 + R_5} \quad (2.22)$$

In view of this, V_{REF} of Brokaw bandgap reference is expressed [101] as:

$$V_{REF} = \left(1 + \frac{R_4}{R_5}\right)(V_{BE1} + \frac{2R_1}{R_2} \Delta V_{BE1,2}) \quad (2.23)$$

Figure 2.13. Brokaw bandgap reference [101].

The reported Brokaw bandgap reference was also fabricated in bipolar technology, and it achieved an impressive lowest TC of 5ppm/°C. However, Brokaw bandgap reference can only generate V_{REF} that is larger than V_{BG} , although the V_{REF} is adjustable. As a result, a high supply voltage is required. For example, the reported Brokaw bandgap reference requires a minimum supply voltage of 4V to achieve

$V_{REF}=2.5V$. in the context of present-day applications, this high minimum voltage is somewhat unacceptable.

Bandgap reference in CMOS technology

The aforementioned two classic bandgap references were both realized in the dated bipolar technology; wherein the BJT characteristic is largely ideal and predictable. However, as CMOS has now become the dominant technology in IC design for its low-power and small feature size, there is a real need to migrate the implementation of the bandgap reference from bipolar technology to CMOS technology.

In CMOS technology, the ideal BJT is unavailable. In view of this, the CMOS bandgap reference has to utilize the parasitic BJT in CMOS [93]. [Figure 2.14](#) depicts the cross-section view of the parasitic pnp transistor in CMOS. The emitter, base, and collector of the BJT are formed by p+ diffusion, n-well, and p-substrate, respectively. Note that only pnp transistor is available in a p-substrate CMOS process, and the collector of the pnp (i.e., the p-substrate) must be connected to the ground (i.e., the lowest potential of the circuit). Compared to the BJT in bipolar technology, the characteristics of the parasitic BJT in CMOS are inferior. Specifically, the base resistance is larger and the current gain is smaller. Consequently, the output accuracy of the CMOS bandgap reference is degraded [78].

Figure 2.14. Parasitic BJT in CMOS.

Figure 2.15 depicts the schematic of a CMOS voltage reference with non-ideal parasitic BJTs. The current mirror (M_1 and M_2) and the OTA equalize the emitter current flow through Q_1 and Q_2 . The emitter-base junction area of Q_1 is designed to be N times larger than that of Q_2 to create a ΔV_{BE} term. In view of the small current gain of Q_1 and Q_2 and their non-negligible base resistance, V_{REF} of the CMOS voltage reference can be expressed as:

$$V_{REF} = V_{BE2} + V_{B2} + \frac{R_2}{R_1} (\Delta V_{BE} + \Delta V_B) \quad (2.24)$$

where $V_{B2} = I_B R_B$ is the voltage across R_B ,

R_B is the base resistance of Q_2 ; the base resistance of Q_1 is R_B/N due to its large emitter-base junction area, and

I_B is the base current of Q_2 .

Figure 2.15. CMOS bandgap reference with non-ideal parasitic BJTs.

As aforementioned, the inferior characteristic of the parasitic BJT affects the performance of CMOS bandgap reference. Specifically, the large base resistance and

the small current gain [78] introduce error terms, V_{B2} and ΔV_B , to V_{REF} . V_{B2} and ΔV_B can be respectively expressed as

$$V_{B2} = \frac{(\Delta V_{BE} + \Delta V_B)R_B}{(1 + \beta)R_1} = \frac{NR_B}{(1 + \beta)R_1} \Delta V_{BE} \quad (2.25)$$

$$\Delta V_B = (1 - \frac{1}{N})V_{B2} = \frac{(N-1)R_B}{(1 + \beta)R_1} \Delta V_{BE} \quad (2.26)$$

where β is the current gain of the parasitic BJT.

V_{REF} can then be more precisely rewritten as:

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1} \Delta V_{BE} + \frac{\lambda R_B}{(1 + \beta)R_1} \Delta V_{BE} \quad (2.27)$$

where $\lambda = ((R_1 + R_2)N - R_2)/R_1$.

The error term in eqn. (2.27) is ascertained by R_B and β . Since these two parameters are sensitive to temperature and process variations, their resultant error term deteriorates both the TC and initial accuracy of V_{REF} . This effect is more severe in advanced CMOS technology because the current gain of the parasitic BJT reduces significantly as technology scales down [78].

Further, the OTA affects the accuracy and the TC of V_{REF} due to the undesired offset voltage. The OTA offset voltage can be classified into two categories, the random offset voltage and the systematic offset voltage [60]. The former is largely caused by the transistor mismatch, and therefore it can be reduced by utilizing long channel devices. The latter is due to the unbalanced transistor biasing condition, and it can be

minimized by adopting a simple OTA structure (e.g., one-stage OTA) that eases the optimization of the biasing of the OTA [60].

Another design challenge of CMOS bandgap reference stems from the decreasing supply voltage due to CMOS technology scaling. Note that the CMOS bandgap reference depicted in Figure 2.15 requires a minimum supply voltage of $\sim 1.4\text{V}$, which may exceed the maximum allowable supply voltage of deep-submicron CMOS technologies.

A current-mode bandgap reference, e.g., [52] depicted in Figure 2.16, can accommodate a lower supply voltage of $\sim 1\text{V}$. The operation of the current-mode bandgap reference relies on the generation of a temperature-insensitive current, I_{REF} , and the conversion of I_{REF} to V_{REF} by a resistor. I_{REF} and V_{REF} are respectively expressed [52] as:

$$I_{REF} = \frac{V_{BE2}}{R_2} + \frac{\Delta V_{BE1,2}}{R_1} \quad (2.28)$$

$$V_{REF} = \frac{R_3}{R_2} \left(V_{BE2} + \frac{R_2}{R_1} \Delta V_{BE1,2} \right) \quad (2.29)$$

On the basis of eqn. (2.29), the V_{REF} of current-mode bandgap reference is a fraction of the silicon bandgap voltage, thereby enabling low-voltage operation. However, it is still difficult for current-mode bandgap reference to operate with a sub-1V supply due to the non-scalable turn-on voltage of the BJT which is $\sim 0.7\text{V}$ and is even higher at low temperature.

To further reduce the supply voltage to sub-1V in view of the CMOS technology scaling, Figure 2.17 depicts a reported bandgap reference [69] incorporated a switched capacitor circuit. In Figure 2.17, a charge pump circuit that locally boosts the supply voltage is utilized to generate the required V_{BE} , and the ΔV_{BE} is stored in capacitor C_{Δ} . Note that in each clock period, charges are dissipated via the BJT, $Q_D = I_{Q2}T$, and charges are supplied by V_{DD} , $Q_S = C_f V_{DD}$. At steady-state, $Q_D = Q_S$. In view of this, $I_{Q1} = I_{Q2}$, and ΔV_{BE} is generated due to the different junction areas of Q_1 and Q_2 . Further, a switched capacitor network is utilized to generate the V_{REF} by appropriately scaling and combining the V_{BE} and ΔV_{BE} .

The reported switched capacitor bandgap reference achieves a minimum supply voltage of 0.5V and an ultra-low power of 32nW. However, the TC of V_{REF} is undesirably high, 75ppm/°C (from 0°C to 80°C). Moreover, the drawbacks of the switched capacitor voltage reference include undesired output ripple ($\sim 50\mu\text{V}$) and long settling time ($>5\text{ms}$).

The aforementioned bandgap references all generate V_{REF} simply by combining V_{BE} and ΔV_{BE} . Due to the non-linear thermal characteristic of V_{BE} (see eqn. (2.19)), V_{REF} of these voltage references typically suffers from high-order temperature dependency. Consequently, the TC of these voltage references is undesirably relatively high. In view of this, it is imperative to adopt curvature-compensation techniques to reduce the high-order temperature dependency of V_{REF} to achieve a low TC.

Figure 2.18 depicts the schematic of a curvature-compensated current-mode bandgap reference [53]. A non-linear current, I_{NL} that is proportional to $V_T \ln T$ is generated to compensate for the nonlinear term of V_{BE} . Note from eqn. (2.19) that the nonlinear term of V_{BE} pertains to the temperature exponent of I_C , γ . Consequently, V_{BE2} and V_{BE3} exhibit different temperature characteristics because I_{C2} is a PTAT current with $\gamma=1$, and I_{C3} is largely a temperature-insensitive current with $\gamma=0$. As a result, I_{NL} can be expressed [64] as:

$$I_{NL} = \frac{V_{BE,Q1} - V_{BE,3}}{R_4} = \frac{V_T \ln \frac{T}{T_r}}{R_4} \quad (2.30)$$

and V_{REF} is

(2.31)

On the basis of eqn. (2.31), the TC of V_{REF} may be optimized by designing

(2.32)

Figure 2.18. Curvature-compensated bandgap reference.

The reported curvature-compensated bandgap reference [53] achieves a low TC of 7.5ppm/°C over a 80°C temperature range. Although the curvature compensation approach can potentially improve the temperature independence of V_{REF} , a complicated trimming process is typically required to ensure the efficacy of the curvature compensation.

Trimming of the bandgap reference

Process variations of and non-idealities in the CMOS fabrication introduce errors into the bandgap reference and therefore deteriorate the accuracy of V_{REF} and its TC. Although the said errors stem from various sources, they can be classified into two

categories based on their thermal characteristics, i.e., PTAT error and non-PTAT error [62]. For example, in Figure 2.16, the PTAT error may be caused by the resistor mismatch between R_1 and R_2 , mismatch of the current mirror, and mismatch between Q_1 and Q_2 . The non-PTAT error, on the other hand, may be caused by the non-linear thermal characteristics of V_{BE} , the offset voltage of the OTA, the error introduced by the small β and large R_B (see eqn. (2.27)), etc.

To correct for these errors, trimming of the critical elements (e.g., R_1 and R_2 in Figure 2.16) in the bandgap reference is typically required. In view of low cost and simple implementation, the room-temperature trimming [62] is arguably the most commonly adopted trimming technique for the bandgap reference. This trimming exploits the nature of the bandgap reference, i.e., the temperature independent V_{REF} equals to V_{BG} , which is a process-independent and a known parameter ($V_{BG} \approx 1.205\text{V}$). In view of this, by adjusting V_{REF} to $\sim 1.205\text{V}$ at room temperature, the TC of V_{REF} can be simultaneously optimized. Room-temperature trimming can effectively correct for the PTAT error. However, when the non-PTAT error is pronounced, the basic assumption that $V_{REF} = V_{BG}$ becomes invalid, hence requiring a more complicated trimming process. Most curvature compensated bandgap references aim at resolving the non-linear thermal characteristics of V_{BE} (a non-PTAT error) by adopting multi-temperature trimming and/or multi-element trimming [64, 66]. Note that as CMOS fabrication process scales down, the non-PTAT error caused by the reduced parasitic BJT current gain may be more significant. As a result, more complicated trimmings may be required for the bandgap reference realized in deep-submicron CMOS technology.

In short, the ubiquitous bandgap references are typically realized by the parasitic vertical PNP BJTs in CMOS. The bandgap references in general require a relatively high supply voltage (e.g., $V_{DD} > 1\text{V}$), and their design-art is mature, particularly in mature technology nodes. However, in view of deteriorated BJT characteristics (e.g., reduced current gain and increased current gain spread) in deep-submicron CMOS, the said advantages of bandgap voltage references diminish with CMOS technology scaling.

2.2.3 Review of the subthreshold voltage reference

Subthreshold voltage references [58, 59, 63, 65, 70, 79] are alternative voltage references, and they are suitable for sub-1V applications, congruous with many present-day applications. The operation mechanisms of the subthreshold voltage reference is somewhat akin to bandgap references in the sense that the I - V characteristics and the thermal characteristics of the subthreshold MOSFET are akin to the BJT [102]. The I_D - V_G characteristic of a subthreshold MOSFET can be expressed [102] as:

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \times (1 - \exp(-\frac{V_{DS}}{V_T})) \quad (2.33)$$

where K is the aspect ratio of the transistor,

$I_0 = \mu C_{OX}(n-1)V_T^2$ is the saturation current,

C_{OX} is the gate oxide capacitance,

n is the subthreshold slope factor,

V_{GS} is the gate-to-source voltage of the transistor, and

V_{TH} is the threshold voltage of the transistor.

From eqn. (2.33), the V_{GS} of the subthreshold MOSFET is

$$V_{GS} = V_{TH} + nV_T \ln\left(\frac{I_D}{KI_0}\right) \quad (2.34)$$

From eqn. (2.34), ΔV_{GS} of two subthreshold MOSFETs ($M1$ and $M2$) with different current density (I_{D1}/K_1 and I_{D2}/K_2) is a PTAT voltage, and it is expressed as:

$$\Delta V_{GS} = nV_T \ln\left(\frac{I_{D1}/K_1}{I_{D2}/K_2}\right) \quad (2.35)$$

Note that V_{TH} of a MOSFET is a CTAT voltage, and can be expressed as:

$$V_{TH} = V_{TH0} - \eta T \quad (2.36)$$

where V_{TH0} is V_{TH} at 0K, and

η is the temperature coefficient of V_{TH} .

From eqn. (2.35) and eqn. (2.36), the subthreshold voltage reference generates the temperature-insensitive V_{REF} by combining the PTAT ΔV_{GS} and the CTAT V_{TH} , and the output voltage of V_{REF} equals to V_{TH0} .

Figure 2.19 depicts a reported schematic of a subthreshold voltage reference [59].

V_{REF} in this design can be expressed as:

$$\begin{aligned} V_{REF} &= V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} \\ &= V_{TH0,4} - \eta T + nV_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right) + nV_T \ln\left(\frac{I_{D4}}{K_4I_{0,4}}\right) \end{aligned} \quad (2.37)$$

where $V_{TH0,4}$ is the V_{TH} of M_4 at 0K,

K_{3-7} are the aspect ratio of M_{3-7} ,

I_{D4} is the drain current of M_4 , and

$I_{0,4}$ is the saturation current of M_4 .

The TC of V_{REF} is minimized by appropriately sizing M_3 - M_7 so that ηT and $nV_T \ln(2K_3K_5/K_6K_7)$ in eqn. (2.37) are compensated. The remaining temperature dependency of V_{REF} is largely due to the temperature-dependent I_{D4} and $I_{0,4}$.

Figure 2.19. Subthreshold voltage reference proposed by Ueno [59].

The reported subthreshold voltage reference fabricated in 0.35 μ m CMOS process achieved a V_{REF} of 745mV with a supply voltage of 1.4V, and the TC was 15ppm/ $^{\circ}$ C (-20 $^{\circ}$ C to 80 $^{\circ}$ C). Note that a lower supply voltage can be used if the reported design were fabricated in deep-submicron CMOS, where V_{TH} of MOSFET is lower. As all MOSFETs in this design were biased in the subthreshold region, the power dissipation is low, $\sim$ 300nW. Nevertheless, the main drawback of the subthreshold voltage reference is the limited temperature range for two reasons. First, the subthreshold slope factor, n , is temperature dependent, where an increase in temperature leads to a reduction of n . Second, the junction leakage current drastically increases with temperature, and therefore, the thermal characteristics of subthreshold MOSFET are affected and cannot be adequately modeled by eqn. (2.33). These two reasons [102] may be inferred from Figure 2.20 which depicts the I_D - V_{GS} curve of a subthreshold MOSFET under various temperatures.

Figure 2.20. I_D - V_{GS} curve of a subthreshold MOSFET under various temperatures.

The subthreshold voltage reference can also be implemented by two different types MOSFET with different V_{TH} . Figure 2.21(a) depicts the schematic of a 2-Transistor (2-T) voltage reference [65], where two NMOS transistors are stacked vertically and have different threshold voltages ($N1$ is a native nFET, and $N2$ is an IO nFET).

Figure 2.21. Schematics of voltage reference [65] of the (a) ideal stacked '2-Transistor' structure, and (b) stacked '2-Transistor' structure with leakage current.

The temperature independence of the 2-T voltage reference is based on the assumption of the current balance at node V_{REF} , where

$$I_{DS1} = I_{DS2} \quad (2.38)$$

and V_{REF} may be expressed [65] as:

$$\begin{aligned} V_{REF} &= (V_{TH2} - V_{TH1}) + V_T \ln\left(\frac{C_{OX1}K_1}{C_{OX2}K_2}\right) \\ &= (V_{TH0,2} - V_{TH0,1}) + (\eta_1 - \eta_2)T + V_T \ln\left(\frac{C_{OX1}K_1}{C_{OX2}K_2}\right) \end{aligned} \quad (2.39)$$

From eqn. (2.39), it can be seen that by appropriately sizing N_1 and N_2 , V_{REF} is temperature independent where the last two terms are mutually compensated. Consequently, V_{REF} equals to the V_{TH} difference of N_1 and N_2 at 0K. The reported 2-T voltage reference [65] achieved a V_{REF} of 176mV with a minimum supply voltage of 0.5V and an ultra-low power of only 2.2pW (at room temperature). The ultra-low power is largely attributed to the subthreshold operation and the simple realization. The TC of V_{REF} is ~60ppm/°C in the temperature range of -20°C to 80°C. Nevertheless, the primary drawback of the 2-T voltage reference is its limited temperature range that is largely a consequence of the undesired junction leakage current of N_1 and N_2 . This is because, in practice, the assumption that $I_{DS1}=I_{DS2}$ is invalid due to the parasitic diodes depicted in Figure 2.21(b). When the non-ideal leakage current due to these parasitic diodes is considered, the current at node V_{REF} can be re-expressed as:

$$I_{DS1} = I_{DS2} + I_{SB1} + I_{DB2} \quad (2.40)$$

where I_{SB1} is the source-to-bulk leakage current of N_1 , and I_{DB2} is the drain-to-bulk leakage current of N_2 .

As I_{SB1} and I_{DB2} are highly temperature dependent where they increase exponentially as temperature increases, I_{SB1} and I_{DB2} become significant, particularly at

high temperature. Consequently, the 2-T voltage reference becomes highly temperature-sensitive at high temperatures [67].

At this juncture of voltage reference design-art, subthreshold voltage references are arguably the most prevalent MOSFET-only voltage references, and they are advantageous over the BJT-based bandgap references in deep-submicron CMOS for low-voltage and low-power operation. However, most subthreshold voltage references can operate reliably only over a limited temperature range due to the junction leakage current. This drawback somewhat limits the application space of subthreshold voltage references in our target IoTs because the IoT devices are often placed in an environment with large temperature variations.

2.3 Review of radiation effects on ICs

We will now critically review the radiation effects on ICs, particularly the radiation effects on MOSFETs and parasitic BJTs in CMOS technology. This review ascertains the mechanisms leading to the limitations of state-of-the-art voltage references for satellite applications, leading to our design of a rad-hard MOSFET-only voltage reference for our target satellite applications in Chapter 4 later.

Radiation effects can be largely classified into the accumulative TID effect caused by irradiative ionizing dosage and transient SEEs caused by heavy ions. These two effects will now be reviewed in turn.

2.3.1 Total Ionizing Dose (TID) Effect

The Total Ionizing Dose (TID) effect is an accumulative effect that causes the transistor characteristics to drift which may ultimately lead to a permanent functional

failure of the IC [87, 91]. The TID effect is induced by the ionization energy deposited by the high-energy particles passing through the insulation layer of a transistor. The unit of TID is rad, which denotes the energy absorbed per unit mass of the material; one rad equal to 100ergs absorbed by one gram of the material [5].

Figure 2.22 [7] depicts the mechanisms of the TID effect that involves three stages. In stage one, electron-hole pairs are generated inside the SiO₂ due to the strike of the high-energy particles. In stage two, a portion of electron-hole pairs are recombined. The rest electron-hole pairs are separated apart by the vertical electric field across SiO₂. Specifically, the electrons with higher mobility are quickly swept out of the SiO₂. On the other hand, the holes are slowly transported to the SiO₂-Si interface. In stage three, the said slowly transported holes are captured and trapped inside the SiO₂ layer, and this lead to a negative shift of transistor threshold voltage (V_{th}).

Figure 2.22. Mechanisms of the TID damage on MOSFETs.

The amount of threshold voltage shift, ΔV_{th} , is largely ascertained by the SiO₂ thickness, t_{ox} , where $\Delta V_{th} \propto t_{ox}^2$ [5, 7, 91]. Note that in deep-submicron CMOS, t_{ox} is in general less than 3nm, and the TID induced ΔV_{th} is negligible for two reasons. First, the thin gate SiO₂ results in a strong electron tunnelling effect, and the trapped holes are compensated by the tunnelling electrons. Second, the relatively large gate

capacitance due to the thin SiO₂ further resists the shift of the threshold, noting that $V=Q/C$.

Figure 2.23 depicts the I_d - V_g characteristics of an NMOS in GlobalFoundries 65nm CMOS under TID=0rad and 500krad [88]. From Figure 2.23, it is interesting to note that although the deep submicron CMOS is largely free from the TID induced threshold voltage shift, the off-state current of the NMOS is undesirably increased due to the TID effect. This is largely due to the presence of the thick Shallow Trench Isolation (STI) SiO₂ (~300nm) [7].

Figure 2.23. I_d - V_g characteristics of an NMOS under TID=0rad and 500krad.

Figure 2.24 [88] depicts the cross-section view of an NMOS. Due to the presence of the thick STI SiO₂ at the edge of the NMOS, the NMOS can be modeled as a combination of the main NMOS and a TID-susceptible parasitic NMOS [88]. The total drain current, I_{d_tot} equals to the summation of the main NMOS current, I_{d_main} , and the parasitic NMOS current, I_{d_par} . As the parasitic NMOS is susceptible to the TID effect, I_{d_par} is largely constant for $V_g > 0V$ (see Figure 2.23). In view of the relatively small size of the parasitic NMOS, $I_{d_par} \ll I_{d_main}$ in the strong inversion region. However, I_{d_par} affects the off-state current drastically in the deep subthreshold region where

$I_{d_par} > I_{d_main}$. Consequently, subthreshold voltage reference is sensitive to TID effect. Note that since TID causes negative shift of transistor threshold voltage, only the NMOS is subjected to I_{d_par} .

Figure 2.24. Cross-section view of a MOSFET.

The said thick STI SiO_2 and the ensuing TID issue also exist in the parasitic BJT in CMOS technology [86]. Figure 2.25 depicts the cross-section view of the emitter-base region of the parasitic BJT, where thick SiO_2 surrounds the emitter p-diffusion. Due to the thick STI SiO_2 , an unwanted side pn junction is augmented into the parasitic BJT, which consequently affects the characteristics of the parasitic BJT. In view of this, CMOS bandgap references may not be appropriate for space-grade applications because of the TID-susceptible parasitic BJT.

Figure 2.25. TID effect in parasitic BJT in CMOS technology.

TID further affects the noise performance of a MOSFET because the radiation-induced interface traps can significantly increase the $1/f$ noise in a MOSFET [7]. Figure 2.26 depicts the noise characteristics of an NMOS before and after irradiation. It can be seen that the $1/f$ noise increases significantly after irradiation. Nevertheless, this phenomenon is pronounced only when the irradiation level is high (e.g., 10Mrad).

Figure 2.26. Noise spectra before and after irradiation of an NMOS with $W/L=1000/0.35$ at $I_D=100\mu A$.

Our review of the TID effects on CMOS technology depicts the challenge of designing a rad-hard voltage reference in CMOS. Put simply, the TID leads to three undesirable effects, including threshold voltage drift, leakage current increment of MOSFET, and current-gain degradation of parasitic BJT. Although the first effect is negligible in deep-submicron CMOS because of the thin gate SiO_2 , it is not the case for the other two effects. Put simply, the prevalent BJT-based bandgap references and subthreshold voltage references are sensitive to TID – there is no reported MOSFET-only voltage reference that is insusceptible to TID.

2.3.2 Single Event Effects (SEEs)

SEEs refer to radiation effects that originate from a single high-energy particle that penetrates into the semiconductor device. The degree of SEEs is ascertained by the energy of the particle, which is quantified by its Linear Energy Transfer (LET). The unit of LET is MeVcm^2/mg , and it denotes the energy loss per unit length of the particle [5].

Figure 2.27 depicts the mechanisms of SEEs. The high-energy particle creates electron-hole pairs along its track and results in a transient current. The effect of SEEs can be modeled as an augmented current pulse on the affected circuit node [103]. SEEs can induce both soft errors and hard errors. Specifically, soft errors, such as the Single Event Upset (SEU) [104] and the Single Event Transient (SET) [83] may cause the affected circuit to suffer from transient errors. Soft errors are not destructive and they can be corrected. However, hard errors (e.g., Single Event Latchup (SEL)) [8], may result in permanent damage to the device.

Figure 2.27. Mechanism of SEEs.

An SEU occurs when the single-event-induced current pulse occurs in digital circuits, particularly the storage elements (e.g., SRAM and latch), and results in bit-flip in the storage elements [83]. Note that due to the considerably high density of transistors stemming from technology scaling, the SEU effect is increasingly

pronounced in deep submicron CMOS, in the sense that a single event can even cause multiple bit-flips [104]. An SET, on the other hand, causes a voltage spike at a circuit node. Both digital and analog circuits are susceptible to SETs [103]. In digital circuits, particularly combinational logic, the said voltage spike may lead to a functional error when it is captured by the flip-flop. In analog circuits, the said voltage spike is manifested as high-frequency noise. Although the SET effect can be reduced by filtering, this is generally avoided as the bandwidth of the analog circuit would otherwise be compromised. Like the SEU, deep submicron CMOS is increasingly susceptible to SET because of the frequent switching activities and the relatively weak signal power arising from the reduced supply voltage.

The SEL is a particularly important effect to avoid as it is a destructive effect, and is caused by the single-event-induced current pulse that triggers the parasitic Silicon Controlled Rectifier (SRC) in CMOS [8]. Figure 2.28 depicts the schematic of the said SRC. The two cross-coupled parasitic BJTs form a positive feedback loop. During normal operation, the two BJTs are both in the off-state, and the positive feedback loop is not activated because the loop gain is less than one. However, once the single-event-induced current pulse turns on one of the BJTs, a positive feedback loop is activated in turn. Consequently, the two power rails are shorted, leading to a huge current that usually leads to thermal damage. The most common practice of mitigating SEL is to utilize guard rings in the design because the guard rings reduce the resistance of R_1 and R_2 (see Figure 2.28), which prevents the BJTs from being turned on by the single-event-induced current pulse [105].

Figure 2.28. Parasitic SRC in CMOS technology.

2.4 Conclusions

We have reviewed the fundamentals and the design of LDOs. On the basis of our review, we have delineated the mechanisms leading to the limitations of the PSRR of the LDO. We have also reviewed the fundamentals and the design of voltage references. On the basis of our review, we have also delineated the mechanisms leading to the limitations of TC, PSRR and low-voltage operation of the voltage reference. In our review of both the LDO and the voltage reference, we have also presented the representative state-of-the-art designs, and our ensuing critical comments of their merits and shortcomings. Of particular note, we have delineated the insufficiency of PSRR of state-of-the-art LDOs – the basis of our work described in Chapter 3. We have also reviewed the radiation effects on ICs where we have discussed the susceptibility of BJTs and MOSFETs in the subthreshold region to radiation effects. On this basis, we have ascertained the limitations of state-of-the-art bandgap references and subthreshold voltage references in satellite applications. Of particular note, we have delineated the need for a voltage reference that is insusceptible to radiation – a rad-hard voltage reference which remains unreported in literature. This absence of a rad-hard MOSFET-only voltage reference is, in part, the basis of our work in Chapter 4.

CHAPTER 3

A 65nm NMOS LDO for IoTs featuring >60dB PSRR over 10MHz frequency range and 100mA load current range

A large portion of this chapter has been accepted for publication in IEEE Journal of Solid-State Circuits [106].

In this chapter, we propose an NMOS LDO featuring the highest PSRR (>60dB up to 10MHz) reported to-date and over a large load current range (100 μ A-100mA). As delineated in Chapters 1 and 2, these attributes are often imperative in IoTs where a low noise power supply is extremely critical and a high power-efficiency is essential. The high PSRR in our proposed LDO is achieved by means of a novel adaptive FeedForward Ripple Cancellation (FFRC) technique embodying a proposed adaptive auxiliary amplifier with a gain-tracking feature to adaptively adjust its gain to the optimal value, independent of the load current variations. An NMOS power transistor is employed to obtain a low dropout voltage and a small overshoot and undershoot for load transient.

This chapter is organized as follows. Section 3.1 presents the design of our proposed LDO and the design considerations/mechanism for high PSRR, stability, and low dropout voltage. Section 3.2 presents the measured static performance, dynamic performance, PSRR, and noise of our proposed LDO. Section 3.3 summaries the

performance of our proposed LDO and benchmarks our design against state-of-the-art counterparts. Section 3.4 draws the conclusions.

3.1. Design of the proposed LDO

This section delineates the design of the proposed LDO and the pertinent design techniques and considerations. Simulations are also provided to verify the analysis and derivations thereto.

Figure 3.1 depicts the schematic of the proposed LDO comprising an NMOS power transistor (N_P), the proposed adaptive auxiliary amplifier (AUX), an error amplifier, summing stage, buffer stage, and frequency compensation capacitor (C_C). The load of the proposed LDO is modeled as a resistor (R_L) with an output capacitor (C_{out}). The proposed LDO requires two power supplies, V_{bat} and V_{in} , respectively the filtered battery voltage and the input of the proposed LDO. V_{bat} provides power for all the sub-blocks, save for N_P . V_{in} , on the other hand, is the output of the switching regulator and provides power for N_P , and is also the input of AUX .

In this schematic, the NMOS power transistor enables a low dropout voltage of $\sim 80\text{mV}$ when the load current is 100mA . Further, it enables a small output impedance attribute leading to small overshoot/undershoot during load transients. The proposed AUX embodies a novel gain-tracking scheme and hence can enhance the PSRR of the LDO by $\sim 20\text{dB}$ over a large load current range ($0.1\text{-}100\text{mA}$) and a wide frequency range (DC to 10MHz). The buffer stage serves to drive N_P and features a wide bandwidth of $\sim 60\text{MHz}$ by employing a shunt feedback transistor, N_8 . The wideband feature of the buffer stage facilitates the stability of the proposed LDO and assures the effectiveness of the adaptive auxiliary amplifier over a wide frequency range.

3.1.1. Design considerations for a high PSRR

Figure 3.2 depicts the conceptual block diagram of the proposed LDO, where the error amplifier, summing stage, buffer stage, and the proposed adaptive auxiliary amplifier are denoted as *EA*, *SUM*, *BUF*, and *AUX*, respectively.

Figure 3.2. The conceptual block diagram of the proposed LDO.

There are two noise sources in Figure 3.2 including the battery output ripple, and the switching regulator output ripple at V_{in} . In an NMOS LDO, the noise at V_{in} is usually of primary interest [48]. This is because, in an NMOS LDO, the current supplied by the battery is only to the control circuit and is low (e.g., collectively the *EA*, *SUM*, *BUF*, and *AUX* consume $<1\text{mA}$). In view of this, the battery output ripple can be easily and significantly suppressed without compromising the dropout voltage of the LDO by placing a relatively large series resistor (e.g., $\sim 100\Omega$) between the battery output and V_{bat} and an input capacitor (e.g., several μF) between V_{bat} and ground. This input capacitor is routinely used in many applications [42].

The PSRR of the LDO is enhanced by the mutual compensation of two signal paths from V_{in} to V_{out} , i.e., Path 1 (the inherent signal path due to the power transistor, N_P), and Path 2 (the augmented signal path by the adaptive AUX). Consider now this mutual compensation mechanism.

On the basis of Mason's gain formula [95], the PSRR of the proposed LDO is:

$$PSRR = \frac{V_{out}}{V_{in}} = \frac{A_F(s)}{1-L(s)} \quad (3.1)$$

where $A_F(s)$ is the feedforward gain from V_{in} to V_{out} , and

$L(s)$ is the sum of the loop gain of the signal loops in the proposed LDO.

From Figure 3.2, $A_F(s)$ comprises two components, respectively Path 1 and Path 2 from V_{in} to V_{out} :

$$\begin{aligned} A_F(s) &= g_{dsp}Z_{out} + A_x A_{sum} g_{mp} Z_{out} \\ &= g_{dsp} Z_{out} (1 - A_x A_{int_p}) \end{aligned} \quad (3.2)$$

where g_{dsp} is the output conductance of N_P ,

Z_{out} is the output impedance at node V_{out} ,

A_x is the gain of the proposed adaptive AUX ,

A_{sum} is the gain of the summing stage and is designed to ~ -1 by appropriately sizing N_4 and N_6 (see Figure 3.1),

g_{mp} is the transconductance of N_P , and

$A_{int_p} = g_{mp}/g_{dsp}$ is the intrinsic gain of N_P .

From eqns. (3.1) and (3.2), the PSRR of the proposed LDO can be optimized by ascertaining that $A_F(s) = 0$, specifically that $A_x = 1/A_{int_p}$.

Figure 3.3 depicts the conceptual block diagram of the proposed adaptive *AUX* whose gain is $A_x = V_x/V_{in} = 1/A_{int_p}$. The proposed adaptive *AUX* comprises an OTA, feedback network (formed by R_{X1} and R_{X2}), NMOS (N_X), dependent current source (I_x , that provides dynamic biasing current to N_X), and an independent current sink (I_R , that sinks the current flowing through R_{X1} and R_{X2}). The output of the proposed adaptive *AUX*, V_x , is the output of the OTA. A_x is designed to be equal to $1/A_{int_p}$ and can track its variations due to loading current variations by two steps. First, A_x is designed to be equal to $1/A_{int_x}$, where A_{int_x} is the intrinsic gain of N_X . Second, A_{int_x} is designed to be equal to A_{int_p} by means of realizing N_X as a scaled replica of N_P with a ratio of 1/500. We will now delineate these two steps in turn.

Figure 3.3. Conceptual diagram of the proposed adaptive *AUX*.

In Figure 3.3, the OTA and NMOS (N_X) constitute a two-stage opamp, where V_y is the output of the said two-stage opamp. R_{X1} and R_{X2} form the feedback network, and they are designed to be identical so that $V_y/V_{in} = -1$. The gain from V_x (the output of the

proposed adaptive *AUX*) to V_y largely equals to $-A_{int_x}$ because the output resistance of the current sources, I_x and I_R , and the resistance of R_{X2} are designed to be substantially larger than the output resistance of N_X . On this basis, A_x can be derived as

$$A_x = V_x / V_{in} = (V_y / V_{in}) / (V_y / V_x) = 1 / A_{int_x} \quad (3.3)$$

Figure 3.4 depicts the schematic of the proposed adaptive *AUX*, where A_{int_x} is designed to be equal to A_{int_p} by three means. First, as N_X is designed with the same channel length as the power transistor, N_P , they experience the same degree of short channel effects. Second, N_X and N_P are designed to carry the same current density by a current sensing scheme and by the current sink I_R that minimizes the loading effect of R_{X1} and R_{X2} . Third, V_{ds} of N_X and V_{ds} of N_P are designed to be equal by a reference voltage, $V_{REFX} = V_{in} - V_{out}/2$, i.e., N_X is a scaled replica of N_P both in terms of geometry and biasing conditions. In this fashion, the adaptive $A_x (= 1/A_{int_p})$ can innately track $1/A_{int_p}$ even when A_{int_p} varies due to load current variations.

The gain tracking capability of the auxiliary *AUX* degrades as ripple magnitude at V_{in} increases. This is because the gain of V_y/V_{in} is negative, and hence when V_{ds} of N_P increases as V_{in} increases, V_{ds} of N_x decreases, and vice versa. Nevertheless, as V_{in} is the output of switching regulator whose voltage ripple, in general, is of several tens of mV, the gain tracking capability of the auxiliary *AUX* is largely unaffected – e.g., our simulation (see Figure 3.10 later) shows that the effectiveness of the proposed auxiliary *AUX* slightly drops by 2dB when V_{in} noise (peak-to-peak) increases from 50mV to 100mV, and our measurement (see Figure 3.21 later) shows that the adaptive *AUX* can achieve ~20 PSRR improvement despite 60mV ripple on V_{in} .

Figure 3.4. Schematic of the proposed adaptive AUX.

The bandwidth of A_x ascertains the efficacy of the proposed adaptive AUX over frequency, and the OTA in the proposed AUX is dynamically biased (see Figure 3.4) to improve the PSRR over a wide frequency range under heavy-load conditions. On the other hand, under light-load conditions, the PSRR is intrinsically high in high frequencies (see eqn. (3.6) and Figure 3.7 later). In view of this, the ensuing primary design consideration is to improve the PSRR in the low frequencies whilst minimizing the power dissipation due to the proposed adaptive AUX . The dynamic-biasing feature leads to a low current consumption of the adaptive AUX at light-load condition; 20% of the total quiescent current of the LDO. Table 3.1 tabulates the size of the transistors, resistors and capacitors depicted in Figure 3.1 and Figure 3.4 and the current consumption of each block of the LDO; the biasing circuit consumes $8\mu\text{A}$.

Figure 3.5 depicts the optimal $A_x (=1/A_{int_p})$ derived from eqn. (3.2) and the simulated A_x of the proposed adaptive AUX versus I_{load} ranging from $100\mu\text{A}$ to 100mA . The PSRR improvement due to the proposed AUX is also illustrated and is compared with the case when A_x is otherwise a fixed value. It can be observed from Figure 3.5 that A_x closely tracks $1/A_{int_p}$ with the discrepancy of $<1\text{dB}$ (i.e., $\sim\times 1.1$) when $1/A_{int_p}$ experiences substantial variation of 3.7dB (i.e., $\sim\times 1.5$) over large load current variations ($100\mu\text{A}$ - 100mA). Because of the adaptive A_x , the proposed adaptive AUX substantially improves the PSRR by between $18\text{-}24\text{dB}$ over the $100\mu\text{A}$ to 100mA load current range; worst-case is 18dB at $I_{load}=100\mu\text{A}$. By comparison, when A_x is a fixed value and optimized for 100mA load current, the degree of PSRR improvement decreases substantially – to 4dB at $I_{load}=100\mu\text{A}$.

Table 3.1 Transistors size and power breakdown of the LDO.

Block (current)	Device	Parameter	Block (current)	Device	Parameter
Error amplifier in Figure 3.1 (10μA)	N_0	2.4μm/0.6μm	Adaptive AUX in Figure 3.4 (8μA)	N_{P2}	6μm/0.06μm
	P_{1a}, P_{1b}	6μm/1μm		P_{W1}, P_{W2}	128μm/0.2μm
	P_{2a}^*, P_{2b}^*	16μm/0.3μm		N_{W1}, N_{W2}	64μm/2μm
	N_{1a}^*, N_{1b}^*	8μm/1μm		N_{W3}	32μm/2μm
	N_{2a}^*, N_{2b}^*	2μm/1μm		P_{W3}, P_{W5}	16μm/0.4μm
	N_{3a}, N_{3b}	20μm/0.6μm		P_{W4}, P_{W6}	128μm/0.4μm
Summing stage and buffer stage in Figure 3.1 (14μA)	P_3	16μm/1μm		P_{X1c}, P_{X1d}	8μm/0.4μm
	P_4^*	0.5μm/0.3μm		N_X	24μm/0.06μm
	N_4^*	0.5μm/0.3μm		N_{X1a}	16μm/2μm
	N_5^*	2μm/1μm		N_R^*	0.6μm/0.6μm
	N_6^*	0.5μm/0.3μm		P_{X1a}^*, P_{X1b}^*	5μm/1μm
	N_7	1.2μm/0.6μm		P_{X2a}^*, P_{X2b}^*	8μm/0.4μm
	N_8	0.4μm/0.1μm		N_{X1b}^*	4.8μm/0.6μm
Power transistor	N_P	3000μm/0.06μm		N_{X2a}^*, N_{X2b}^*	24μm/0.3μm
Compensation capacitors	C_C	2.5pF		N_{X3a}^*, N_{X3b}^*	8μm/0.4μm
	C_{CX}	0.1pF	Resistors	R_{X1}, R_{X2}	100kΩ

* thick gate oxide I/O transistor.

Figure 3.5. Simulated A_x and the optimal A_x , and PSRR improvement for fixed A_x and for the proposed adaptive AUX .

Consider now the analytical model of our proposed LDO depicted in Figure 3.6 for modeling PSRR. As aforementioned, arising from the proposed adaptive AUX , there are two feedforward paths, Path 1 and Path 2. Due to C_C , there are two signal loops, Loop 1 and Loop 2. On the basis of eqns. (3.1) and (3.2), the PSRR of the proposed LDO can be derived as:

$$PSRR = \frac{A_F(s)}{1-L(s)} = \frac{g_{dsp} Z_{out} (1 - A_x A_{int_p})}{g_{mp} Z_{out} A_{oe} (1 + s \frac{C_C}{g_{m1}})} \quad (3.4)$$

$$1 + \frac{g_{m1}}{(1 + s \frac{C_{oe}}{g_{oe}})(1 + s \frac{C_C}{g_{m2}})}$$

where $A_{oe} = g_{m1}/g_{oe}$ is the DC gain of the error amplifier,

g_{m1} is the transconductance of the differential input pair (i.e., N_{1a} and N_{1b} in Figure 3.1),

g_{oe} is the equivalent output conductance at the output of the error amplifier, V_{oe} ,
 C_{oe} is the capacitance associated with node V_{oe} , and
 g_{m2} is the transconductance of P_{2a} in Figure 3.1.

Figure 3.6. Small signal model of the proposed LDO for PSRR analysis.

It is worthy to note that as $L(s)$ decreases as frequency increases, (3.4) can be decomposed into two parts with respect to frequency by comparing $L(s)$ with 1 (unity). The PSRR of the proposed LDO for the case of $L(s) > 1$ and $L(s) < 1$ can be respectively expressed as

$$PSRR|_{L(s)>1} = \frac{1}{A_{oe}A_{int_p}} (1 - A_x A_{int_p}) (1 + s \frac{C_{oe}}{g_{oe}}) \quad (3.5)$$

$$PSRR|_{L(s)<1} = g_{dsp} Z_{out} (1 - A_x A_{int_p}) \quad (3.6)$$

Note that eqn. (3.5) is a simplified expression without considering the terms of $(1 + sC_C/g_{m1})$ and $(1 + sC_C/g_{m2})$ in eqn. (3.4). This is because at low frequency where $L(s) > 1$, $(1 + sC_C/g_{m1}) \approx 1$ and $(1 + sC_C/g_{m2}) \approx 1$ in the proposed LDO.

From eqns. (3.5) and (3.6), the PSRR characteristics of the proposed LDO can be summarised by the following three salient points. First, the proposed *AUX* enhances the PSRR by introducing the term $(1-A_xA_{int_p})$ into eqns. (3.5) and (3.6). Second, the PSRR degrades from frequencies beyond $f=g_{oe}/2\pi C_{oe}$ due to the pole at the output of the error amplifier. Third, the PSRR conversely improves at high frequencies when $L(s)<1$ because the PSRR is largely unaffected by $L(s)$ when $L(s)<1$, and because of the capacitive characteristic of Z_{out} which decreases with frequency.

Figure 3.7 depicts the simulated PSRR of the proposed LDO with and without the proposed adaptive *AUX*, and under heavy-load ($I_{load}=100\text{mA}$) and light-load ($I_{load}=100\mu\text{A}$) conditions. Note that in the case without the adaptive *AUX*, $V_{in}=1.2\text{V}$ with ac noise is applied only to the power transistor, while $V_{in}=1.2\text{V}$ without ac noise is applied to the adaptive *AUX*. In this fashion, the biasing conditions of the LDO are the same for both cases, thereby a fair comparison. The same setup is also applied for our hardware measurement. These simulations validate our aforementioned analysis and derivations from the following perspectives.

(a)

(b)

Figure 3.7. Simulated PSRR of the proposed LDO with and without the proposed adaptive *AUX* for (a) $I_{load}=100\text{mA}$, and (b) $I_{load}=100\mu\text{A}$.

- (i) In Figure 3.7(a), when $I_{load}=100\text{mA}$, the proposed adaptive *AUX* significantly improves the PSRR throughout the 10Hz to 10MHz frequency range – by more than 20dB from 10Hz to 4MHz, and subsequently to 13dB at 10MHz.
- (ii) In Figure 3.7(b), when $I_{load}=100\mu\text{A}$, the proposed adaptive *AUX* similarly significantly improves the PSRR but in a narrower frequency range – by ~18dB from 10Hz to 4MHz, and decreases to 0dB for frequencies beyond 7MHz. This is not unexpected because as delineated earlier, the proposed adaptive *AUX* is dynamically-biased where its bandwidth is limited when I_{load} is low.
- (iii) In the high-frequency range, the PSRR is intrinsically higher when $I_{load}=100\mu\text{A}$ than $I_{load}=100\text{mA}$. This is because, at high frequencies, the PSRR is ascertained by g_{dsp} (see eqn. (3.6)), which decreases as the loading current decreases. In other

words, the 0dB improvement beyond 7MHz in item (ii) is not disadvantageous because the PSRR is already very high.

- (iv) The PSRR for both $I_{load}=100\text{mA}$ and $I_{load}=100\mu\text{A}$ expectedly degrades at the pole frequency of the error amplifier output ($\sim 60\text{kHz}$). This observation is congruous to our derivation in eqn. (3.5).
- (v) The PSRR improves when $L(s)<1$, whose corresponding frequency is $\sim 100\text{kHz}$ and $\sim 1\text{MHz}$ for $I_{load}=100\mu\text{A}$ and $I_{load}=100\text{mA}$, respectively. This frequency increases with loading current because it is ascertained by g_{mp} (see eqn. (3.4)).
- (vi) Finally, in the PSRR plots, a trough is observed for both loading conditions. This phenomenon is because Z_{out} reaches its minimum value at $\sim 3\text{MHz}$ due to the ESR ($10\text{m}\Omega$) and ESL (0.5nH) associated with the $4.7\mu\text{F}$ C_{out} .

In addition to the load current variations, the LDO is similarly expected to feature high PSRR over PVT variations. This is likewise obtained by means of the gain-tracking feature of the adaptive AUX . The PSRR of the LDO is simulated under 20 PVT corners (five process corners $\times$ two temperature corners (0°C and 80°C) $\times$ two V_{bat} corners (2.4V and 3.2V)). Figures 3.8(a) and (b) depict the simulated PSRR when $I_{load}=100\text{mA}$ and $I_{load}=100\mu\text{A}$, respectively, and for the cases with and without the adaptive AUX . As expected, the effectiveness of the adaptive AUX is robust against PVT variations, where the adaptive AUX offers a PSRR improvement of 23~24dB and 15~26dB when $I_{load}=100\text{mA}$ and $I_{load}=100\mu\text{A}$ (to 2MHz), respectively.

(a)

(b)

Figure 3.8. PVT corner simulation results of the LDO for

(a) $I_{load}=100\text{mA}$, and (b) $I_{load}=100\mu\text{A}$.

In practice, it is also important to ascertain the effect of transistor mismatch on the performance of the LDO. This is because transistor mismatch causes the mismatch between the current density of N_x and N_P (see Figure 3.3), thereby degrading the

effectiveness of the adaptive *AUX*. To ascertain this, a 200-run Monte-Carlo simulation on PSRR is carried out under the worst-case PVT corner and at the worst-case frequency for both $I_{load}=100\text{mA}$ and $I_{load}=100\mu\text{A}$; on the basis of our corner simulations in Figure 3.8, the worst-case PVT corner for both $I_{load}=100\text{mA}$ and $I_{load}=100\mu\text{A}$ is when process corner=SS, $V_{bat}=2.4\text{V}$ and temperature= 80°C , and the worst-case frequency is 1MHz and 100kHz, respectively.

Figures 3.9(a) and (b) depict the statistics of the 200-run Monte Carlo for $I_{load}=100\text{mA}$ and $I_{load}=100\mu\text{A}$, respectively. When $I_{load}=100\text{mA}$, the PSRR at 1MHz is a high mean value of 71dB with 7dB standard deviation. When $I_{load}=100\mu\text{A}$, the PSRR at 100kHz is a high mean value of 80dB with a smaller standard deviation of 3dB. Put simply, the effectiveness of the adaptive *AUX* to improve the PSRR remains high despite transistor mismatches. Of particular interest, under the same PVT corner, the PSRR without the adaptive *AUX* is a low $\sim 46\text{dB}$ at 1MHz when $I_{load}=100\text{mA}$ and a relatively low $\sim 64\text{dB}$ at 100kHz when $I_{load}=100\mu\text{A}$. Also, the PSRR spread for $I_{load}=100\text{mA}$ is larger than that for $I_{load}=100\mu\text{A}$, because the gain of N_x (and N_P) is more sensitive to current density variations (arising from transistor mismatches) when I_{load} is relatively large (see Figure 3.5).

(a)

(b)

Figure 3.9. Monte-Carlo simulations of PSRR for 200 samples of the LDO

(a) when $I_{load}=100\text{mA}$ and frequency=1MHz, and

(b) when $I_{load}=100\mu\text{A}$ and frequency=100kHz.

The PSRR depicted so far (Figure 3.7, 3.8, and 3.9) are obtained from small signal AC analysis in the frequency domain. However, in real applications, V_{in} contains several tens of mV ripple, to investigate how the ripple amplitude affects the effectiveness of the proposed *AUX*, transient simulation in the time domain is performed. Figure 3.10 depicts the simulated V_{out} of the proposed LDO when the ripple of V_{in} is 50mV (solid lines) and 100mV (dashed lines). The simulations are performed under the condition where $I_{load}=100\text{mA}$ and the noise frequency is 1MHz — the worst-case PSRR according to the earlier simulations. On the basis of simulation results in Figure. 3.10(b), when V_{in} includes a 50mV ripple, the proposed LDO features a high 68dB PSRR (calculated from $18\mu\text{V}/50\text{mV}$). Not unexpectedly, the PSRR of the proposed LDO degrades slightly by 2dB from the previous 68dB to 66dB (calculated from $48\mu\text{V}/100\text{mV}$) when V_{in} includes a higher ripple of 100mV. In view of the simulation results, the PSRR of the proposed LDO is largely insensitive to changes in V_{in} when the ripple is less than 100mV peak-to-peak. Note that the 100mV ripple is sufficiently high as the noise of the preceding switching regulator is typically several tens of mV.

(a)

(b)

Figure 3.10. (a) V_{in} including a 50mV and 100mV noise at 1MHz, and

(b) ac coupled V_{out} when the auxiliary AUX is enabled.

3.1.2. Design considerations for stability

Figure 3.11 depicts the small-signal model of the proposed LDO for stability analysis, where the intention is to derive the loop gain transfer function, $T(s)$, of the regulation loop. From Figure 3.11, it can be seen that without C_C , the regulation loop comprises three dominant poles at V_{oe} , V_g , and V_{out} . We adopt two means to address the

stability issue. First, a wideband buffer [35, 41] is adopted to move the pole at V_g to a higher frequency. Second, subsequent to the first means, a compensation capacitor C_C is augmented to compensate for the other two dominant poles. Consider now these two means in turn.

Figure 3.11. Small signal model for stability analysis.

Figure 3.12 depicts the schematic of the wideband buffer [35, 41]. P_3 , P_4 , and N_7 form a conventional common-drain buffer. N_8 serves as a shunt feedback network that extends the bandwidth, and C_{par} is the parasitic capacitance at the gate of N_8 . We derive the transfer function of the buffer stage as:

$$\frac{v_g}{v_{sum}} = \frac{g_{m4}(g_{m8} + sC_{par})}{g_{m4}g_{m8} + s(g_o C_g + g_{m4}C_{par}) + s^2 C_g C_{par}} \quad (3.7)$$

where g_{m4} and g_{m8} are transconductances of P_4 and N_8 , respectively, and

g_o is the equivalent output conductance at node V_{g8} .

From eqn. (3.7) and by designing $g_o C_g \gg g_{m4} C_{par}$, the bandwidth of the wideband buffer is $\sim g_{m4} g_{m8} / 2\pi g_o C_g$. Compared to the conventional common drain buffer [76], the shunt feedback herein extends the bandwidth by $\times g_{m8} / g_o$.

Figure 3.12. Schematic of the wideband buffer.

Figure 3.13 depicts the simulated gain and phase frequency responses of the wideband buffer with $C_g \approx 6\text{pF}$ emulating the power transistor gate capacitance. The bandwidth of the wideband buffer is $\sim 60\text{MHz}$, which is $\sim \times 60$ higher than the unity gain bandwidth of the regulation loop (see Figure 3.14 later). On this basis, the pole at V_g is moved to a higher frequency, hence non-dominant.

Figure 3.13. The frequency response of the wideband buffer.

Consider now the mechanism of the frequency compensation capacitor, C_C , which serves to split the poles at V_{oe} and V_{out} , particularly under heavy-load conditions.

Note that the pole at V_{oe} is $\sim 60\text{kHz}$, and it is largely unaffected by the loading current. The pole at V_{out} , on the other hand, shifts substantially from $\sim 100\text{Hz}$ to $\sim 40\text{kHz}$ when I_{load} increases from $100\mu\text{A}$ to 100mA . Under light-load conditions, the LDO is inherently stable because the poles at V_{oe} and V_{out} are far away. However, under heavy-load conditions, the LDO is otherwise unstable without C_C , as the poles at V_{oe} and V_{out} are closely located.

The transfer function of the loop gain, $T(s)$, can be expressed as:

$$T(s) = \frac{g_{m1}r_{oe}(1 + s\frac{C_C}{2g_{m2}} - s^2\frac{C_C C_{oe}}{g_{m2}g_{mp}})}{1 + s(r_{oe}C_C + \frac{C_{out}}{g_{mp}}) + s^2\frac{r_{oe}C_{oe}C_{out}}{g_{mp}} + s^3\frac{r_{oe}C_{oe}C_C C_{out}}{g_{m2}g_{mp}}} \quad (3.8)$$

$T(s)$, under heavy-load conditions with a large g_{mp} ($g_{mp} > C_{out}/r_{oe}C_C$), can be simplified to:

$$T(s)|_{heavy} = \frac{g_{m1}r_{oe}(1 + s\frac{C_C}{2g_{m2}})(1 - s\frac{2C_{oe}}{g_{mp}})}{(1 + sr_{oe}C_C)(1 + s\frac{C_{oe}C_{out}}{C_C g_{mp}} + s^2\frac{C_{oe}C_{out}}{g_{m2}g_{mp}})} \quad (3.9)$$

From (3.9), it can be seen that an oversized C_C leads to complex poles in $T(s)$ which deteriorates the stability. To circumvent this, C_C is optimized to:

$$C_C = \frac{1}{2} \sqrt{\frac{g_{m2}C_{oe}C_{out}}{g_{mp_max}}} \quad (3.10)$$

where g_{mp_max} is g_{mp} under the maximum loading current condition. In the proposed LDO, C_C is set to $\sim 2.5\text{pF}$ to accommodate the 100mA maximum loading current.

The pole-splitting effect of C_C diminishes as the loading current decreases. This is due to the reduced g_{mp} leading to $r_{oe}C_C < C_{out}/g_{mp}$. In view of this, $T(s)$ expressed in eqn. (3.8) under the light-load conditions with reduced g_{mp} ($g_{mp} < C_{out}/r_{oe}C_C$) can be simplified to:

$$T(s)|_{light} = \frac{g_{m1}r_{oe}(1+s\frac{C_C}{2g_{m2}})(1-s\frac{2C_{oe}}{g_{mp}})}{(1+s\frac{C_{out}}{g_{mp}})(1+sr_{oe}C_{oe})(1+s\frac{C_C}{g_{m2}})} \quad (3.11)$$

As aforementioned, the proposed LDO is stable under the light-load conditions because the separation between poles at V_{oe} and V_{out} becomes wider as the loading current decreases. On this basis, the worst-case stability is expected to occur under medium-load conditions. Specifically, the separation between poles at V_{oe} and V_{out} is narrower compared to the light-load conditions, and the pole-splitting effect of C_C is weaker compared to heavy-load conditions.

From eqns. (3.9) and (3.11), $T(s)$ contains two zeros under both heavy-load and light-load conditions. The two zeros are the left-hand-plane zero at $2g_{m2}/2\pi C_C$ and the right-hand-plane zero at $g_{mp}/2\pi(2C_{oe})$. As these two zeros are located at high frequencies beyond the unity gain bandwidth, they do not affect the stability of the proposed LDO.

To verify $T(s)$, we simulate $T(s)$, depicted in Figure 3.14, under different I_{load} ranging from 100 μ A to 100mA. From the plots, it can be seen that the simulations validate our preceding discussions. Particularly, with the optimized 2.5pF C_C , the complex poles are not observed at maximum loading current ($I_{load}=100$ mA), and the Phase Margin (PM) for the cases when $I_{load}=100$ mA, $I_{load}=1$ mA, and $I_{load}=100\mu$ A are 60°, 30°, and 50°, respectively. These simulations are congruous with our analysis and

derivation, and the worst-case PM of 30° is sufficient to ensure the stability of the proposed LDO.

Figure 3.14. The loop gain of the proposed LDO for $I_{load}=100\mu\text{A}$, $I_{load}=1\text{mA}$, and $I_{load}=100\text{mA}$.

The proposed adaptive *AUX* also needs to be stable to ensure the stability of the proposed LDO. From Figure 3.4, the proposed adaptive *AUX* comprises a two-stage amplifier and a resistive feedback network. In view of this, the Ahuja frequency compensation [97] is adopted here to stabilize the signal loop with a frequency compensation capacitor, C_{CX} . Figure 3.15 depicts the simulated loop gain of the adaptive *AUX* for $I_{load}=100\mu\text{A}$ and $I_{load}=100\text{mA}$, where it can be seen that the adaptive *AUX* is stable for both cases. The unity gain bandwidth increases with the load current because the adaptive *AUX* is dynamically biased. Specifically, when $I_{load}=100\mu\text{A}$, the unity gain bandwidth, and the phase margin are 6MHz and 86° , respectively. When $I_{load}=100\text{mA}$, the unity gain bandwidth is $\sim\times 5$ higher (30MHz), and the phase margin is 77° .

Figure 3.15. The loop gain of the adaptive AUX for $I_{load}=100\mu\text{A}$, and $I_{load}=100\text{mA}$.

3.1.3. Design considerations for a low dropout voltage

The reduced dropout voltage deteriorates the static output accuracy of the LDO because the low dropout voltage may push the power transistor into the triode region. This, in turn, degrades the power stage gain and hence the DC loop gain. Subjected to this constraint, the minimum dropout voltage of state-of-the-art LDOs, particularly for those adopting PMOS power transistor, is often large $\sim 200\text{mV}$.

The proposed LDO accommodates a lower dropout voltage by adopting the NMOS power transistor [47]. With the NMOS power transistor, the power stage (see Figure 3.1) is realized as a common-drain configuration. The DC gain of the power stage, A_{POW} , can be expressed as:

$$A_{POW} = \frac{g_{mp}}{g_{mp} + g_{dsp}} = \frac{1}{1 + 1/A_{int_p}} \quad (3.12)$$

From eqn. (3.12), it can be seen that as long as $A_{int_p} \gg 1$, A_{POW} is largely insensitive to A_{int_p} . Consequently, A_{POW} and the DC loop gain of the proposed LDO experience less degradation. This remains true even though A_{int_p} suffers substantial reduction when the power transistor enters into the triode region due to low dropout voltage. Put simply, the proposed LDO can achieve a low dropout voltage without compromising its static output accuracy.

To verify this, we plot in Figure 3.16 the simulated $T(s)$ at DC (i.e., the DC loop gain), A_{POW} , and A_{int_p} versus dropout voltage, V_{do} , of the proposed LDO at $I_{load}=100\text{mA}$ and $I_{load}=50\text{mA}$. It can be seen that A_{POW} and the $T(s)$ at DC decrease by only 5dB and 7dB, respectively, despite A_{int_p} suffering a substantial reduction of 18dB under the condition of $V_{do}=50\text{mV}$ and $I_{load}=50\text{mA}$. For completeness, to achieve $\leq \pm 0.1\%$ static output error, $T(s)$ at DC would need to be greater than 54dB, which is the case here. On this basis, the minimum dropout voltage of the proposed LDO is $\sim 50\text{mV}$ and $\sim 80\text{mV}$ when the $I_{load}=50\text{mA}$ and $I_{load}=100\text{mA}$, respectively.

Figure 3.16. Simulated $T(s)$ at DC, A_{int_p} , and A_{POW} versus dropout voltage at $I_{load}=50\text{mA}$ and $I_{load}=100\text{mA}$.

3.2. Hardware measurements of the proposed LDO

Figure 3.17 depicts the microphotograph of the proposed LDO fabricated in 65nm bulk CMOS process. The active area of the proposed LDO is $\sim 0.05\text{mm}^2$, and the proposed LDO requires an off-chip C_{out} of $4.7\mu\text{F}$. To mitigate potential issues arising from the parasitic resistance and inductance of the bonding wires, the Kelvin connection [40] is adopted. The nominal voltage of V_{bat} , V_{in} , V_{out} , and V_{REFX} (see Figure 3.3) of the proposed LDO are 2.5V, 1.2V, 1.0V, and 0.7V, respectively. The quiescent current of the proposed LDO is $\sim 40\mu\text{A}$.

Figure 3.17. Microphotograph of the proposed LDO.

3.2.1. Static performance measurements

The static characteristics, line regulation, minimum dropout voltage, and load regulation of the proposed LDO are depicted in Figure 3.18. Figure 3.18(a) depicts the measured static output error ($V_{o_e} = V_{out} - V_{REF}$) versus dropout voltage ($V_{do} = V_{in} - V_{out}$) for different loading current conditions ($I_{load} = 0.1\text{mA}$, 1mA , 25mA , 50mA and 100mA). The line regulation of the proposed LDO is 8.75mV/V when loading current is 100mA . We

attribute the excellent line regulation to the high PSRR ($\sim 90\text{dB}$ of the proposed LDO) at DC, arising from the proposed adaptive *AUX*. The minimum dropout voltage with $<2\text{mV}$ output error is a low 80mV when $I_{load}=100\text{mA}$. As expected, the minimum dropout voltage reduces with lower I_{load} and is a low 60mV and 40mV when $I_{load}=50\text{mA}$ and 25mA , respectively. This low dropout voltage is attributed to the adoption of the NMOS power transistor embodied in the proposed LDO.

Figure 3.18(b) depicts the output error versus loading current under the nominal condition where $V_{in}=1.2\text{V}$. The load regulation of the proposed LDO is $10\mu\text{V}/\text{mA}$. The excellent load regulation is a consequence of a small closed-loop output resistance [2], arising from the low output resistance of NMOS power transistor and from sufficient loop gain.

(a)

(b)

Figure 3.18. (a) Measured static output error versus dropout voltage under different I_{load} , and
(b) Measured V_{out} versus I_{load} when $V_{in}=1.2V$.

3.2.2. Load transient measurements

Figure 3.19(a) depicts the load transient response of the LDO for $100\mu A$ to $100mA$ I_{load} variations with $1\mu s$ rising and falling time. Figure 3.19(b) depicts the detailed waveform (scaled in time) near the rising-edge of I_{load} in the bottom trace in Figure 3.19(a). When I_{load} falls from $100mA$ to $100\mu A$, the overshoot voltage and the settling time is $2mV$ and $20\mu s$, respectively. On the other hand, when I_{load} rises from $100\mu A$ to $100mA$, the undershoot voltage and the settling time is $4mV$ and $3\mu s$, respectively. The small overshoot and undershoot voltages ($<0.4\%$ the output voltage) are largely attributed to the NMOS power transistor that offers a small output resistance of $\sim 1/g_{mp}$, and to the $4.7\mu F$ C_{out} . The $20\mu s$ overshoot settling time is longer than the $3\mu s$ undershoot

settling time because the bandwidth of the regulation loop is narrower under light-load conditions than under heavy-load conditions (see Figure 3.14). Figure 3.19 (c) depicts the load transient response of the LDO for $100\mu\text{A}$ to 100mA I_{load} variations with 50ns rising and falling times. Figure 3.19 (d) depicts the detailed waveform (scaled in time) near the rising-edge of I_{load} in the bottom trace in Figure 3.19 (c). The transient response depicted in (c) and (d) are largely the same as those in (a) and (b) in terms of overshoot, undershoot, and settling time. However, a 20mV and 14mV spike are observed at the rising edge and the falling edge, respectively. The duration of the spikes is $\sim 30\text{ns}$, which is largely the same as the 50ns rising and falling time. This voltage spike is expected in view of the presence of the ESL of C_{out} [28].

(a)

(b)

(c)

(d)

Figure 3.19. (a) Measured V_{out} under 100mA load transient with 1μs rising and falling time,

(b) 1μ rising edge of the load transient;

(c) Measured V_{out} under 100mA load transient with 50ns rising and falling time, and

(d) 50ns rising edge of the load transient.

3.2.3 PSRR measurements

Figure 3.20 depicts the measured PSRR of the proposed LDO under various loading current conditions, $I_{load}=100\mu\text{A}$, 1mA, 25mA, 25mA, and 100mA. The PSRR of the proposed LDO is measured with the Agilent E5061B network analyzer and the Picotest J2120A line injector. A noise with -20dBm noise power (equivalent to 60mV peak-to-peak voltage ripple) is applied to V_{in} , while V_{bat} is powered by a constant 2.5V. The PSRR exceeds 80dB in the relatively low-frequency range from 10kHz to 100kHz and under all loading current conditions. On the other hand, in the higher frequency range from 100kHz to 10MHz, >60dB PSRR is achieved for all loading current conditions. In the high-frequency range, the PSRR expectedly worsens when the

frequency exceeds the resonant frequency of C_{out} , $\sim 3\text{MHz}$, because the ESL of the capacitor dominates at frequencies beyond 3MHz . C_{out} utilized in the proposed LDO is the TDK CLL series capacitor.

Figure 3.20. Measured PSRR for I_{load} ranging from $100\mu\text{A}$ to 100mA .

Figures 3.21(a) and (b) compare the measured PSRR with and without the adaptive AUX for $I_{load}=100\text{mA}$ and $I_{load}=100\mu\text{A}$, respectively. In the low-to-mid frequency range (10kHz to 1MHz), the adaptive AUX improves (over the case without the adaptive AUX) the PSRR by 25dB and 16dB when $I_{load}=100\text{mA}$ and $I_{load}=100\mu\text{A}$, respectively. We attribute the substantial PSRR improvement observed over the wide I_{load} range to the adaptive AUX adaptively optimizing its gain despite the load current variations. In the mid-to-high frequency range (1MHz to 10MHz), the PSRR improvement, when $I_{load}=100\text{mA}$, is 23dB at 1MHz , and it is 7dB at 10MHz . For the case of $I_{load}=100\mu\text{A}$, there is no PSRR improvement beyond 4MHz , because the bandwidth of the adaptive AUX is narrower when I_{load} is relatively small. This is of little consequence because the PSRR, in this case, is already high. In short, the PSRR improvement due to the adaptive AUX is very worthwhile.

(a)

(b)

Figure 3.21. Measured PSRR with and without the adaptive *AUX* when

(a) $I_{load}=100\text{mA}$, and (b) $I_{load}=100\mu\text{A}$.

PSRR of the proposed LDO against V_{bat} noise ($PSRR_{bat}$) is also characterized.

Figure 3.22(a) depicts the measurement setup, where an RC filter ($R=100\Omega$ and

$C=4.7\mu\text{F}$) is placed between the power source and the V_{bat} node of the proposed LDO. Figure 3.22(b) depicts the measurement result of $PSRR_{bat}$ when $I_{load}=100\text{mA}$. A $>60\text{dB}$ $PSRR_{bat}$ is obtained over the 10MHz frequency range. Specifically, the worst-case $PSRR_{bat}$ is 68dB at 10MHz . Although in the proposed LDO, $PSRR_{bat}$ is relatively smaller compared to the PSRR against V_{in} (i.e., switching regulator output), it is acceptable. This is because the battery output ripple is, in general, less than switching regulator output ripple in many systems/applications due to the small internal impedance of the battery, and the extensive utilization of decoupling capacitor in the system.

Figure 3.22. (a) Block diagram of our LDO with RC filter placed at V_{bat} node, and
(b) Measured $PSRR_{bat}$.

3.2.4. Noise measurements

Figure 3.23 depicts the measured output noise of the proposed LDO when $I_{load}=100\text{mA}$, measured with the R&S FSUP signal source analyzer. The output noise density at 10Hz and 1kHz are $2\mu\text{V}/\text{Hz}^{1/2}$ and $65\text{nV}/\text{Hz}^{1/2}$, respectively. The thermal noise dominates at frequencies beyond 1kHz where the noise density is $40\text{nV}/\text{Hz}^{1/2}$. The primary noise contributor in LDOs is the voltage reference noise [24], and a lower LDO output noise can be obtained with a lower noise voltage reference [51, 107]. In the proposed LDO, the reference voltage is externally generated.

Figure 3.23. Measured output noise of the proposed LDO.

3.3. Design summary and Benchmarking

Table 3.2. Benchmarking the proposed LDO against reported high PSRR LDOs.

		This work	[40]	[46]	[48]	[108]	[45]	[50]
Technology (CMOS)		65nm	0.13μm	65nm	0.13μm	0.25μm	0.18μm	0.18μm
Power transistor		NMOS	PMOS	PMOS	NMOS	NMOS	PMOS	PMOS
Maximum I_{load}		100mA	25mA	25mA	300mA	150mA	50mA	100mA
V_{out}		1.0V	1.0V	1.0V	1.0V	1.8V	1.6V	1.6V
Minimum dropout		80mV	150mV	150mV	50mV	240mV	200mV	200mV
C_{out}		4.7μF	4μF	4.7μF	1μF	1μF	capless	capless
Load regulation		10μV/mA	48μV/mA	40μV/mA	6μV/mA	N.A.	140μV/mA	N.A.
Quiescent current		40μA	50μA	150μA	14μA	1.24μA	55μA	71μA
Overshoot/Undershoot		2mV/4mV	15mV/10mV	12mV/12mV	24mV/56mV	65mV/135mV	120mV/80mV	100mV/110mV
Rising and falling time		50ns	10ns	50ns	1μs	10ns	100ns	100ns
PSRR @ heavy -load	Heavy I_{load}	100mA	25mA	300mA	150mA	25mA	50mA	50mA
	100kHz	89dB	62dB	28dB	10dB	61dB	61dB	50dB
	1MHz	70dB	67dB	15dB	35dB	61dB	72dB	76dB
	10MHz	62dB	50dB	32dB	37dB	47dB	37dB	0dB
PSRR @ light- load	Light I_{load}	100μA	1mA	N.A.	N.A.	1mA	1mA	N.A.
	100kHz	81dB	67dB			61dB	50dB	
	1MHz	95dB	80dB			63dB	65dB	
	10MHz	75dB	59dB			55dB	42dB	
Area		0.048mm ²	0.049mm ²	0.14mm ²	0.1825mm ²	0.108mm ²	0.018mm ²	0.033mm ²
FoM		245ps	16ns	45ns	27ps	23ps	264fs	96fs

$$FoM = C_{out} \times \Delta V_{out} \times I_q / I_{load_max}^2$$

Table 3.2 benchmarks the proposed LDO against state-of-the-art high-PSRR LDOs; PSRR is benchmarked at 100kHz, 1MHz, and 10MHz in accordance with the switching frequency of switching regulator. The proposed LDO features the highest PSRR over all state-of-the-art LDOs in Table 3.2, save at 1MHz where the LDOs [45, 50] reported slightly higher PSRR (only at the 1MHz point) but at lower heavy I_{load} (50mA vs 100mA in the proposed LDO). Of particular interest, the proposed LDO is the only design that achieves >60dB PSRR throughout the 10MHz frequency range and for 100mA load current range. In contrast, the PSRR of state-of-the-art LDOs are high only over a limited loading current range (≤ 50 mA) and/or limited frequency range. The highest loading current (100mA) of the proposed LDO is more than $\times 2$ larger and the lowest loading current (100 μ A) is an order of magnitude lower than the reported designs [40, 45, 46, 50]. Put simply, the proposed LDO features the highest PSRR for 3-orders of magnitude change in the loading current (100 μ A to 100mA) whilst the reported competing LDOs suffer lower PSRR despite having a substantially lower loading current range of less than 2-orders of magnitude.

The proposed LDO employs an NMOS as the power transistor instead of PMOS; several other LDOs [18-21] employ the same. By this means, the proposed LDO features the lowest dropout voltage, the best load regulation, and the smallest overshoot and undershoot. The smallest overshoot and undershoot attribute also obtained in part from the 4.7 μ F output capacitor. As expected, the overshoot and undershoot of capless LDOs (i.e., LDOs do not utilize output capacitor) [45, 50] are $\sim \times 10$ larger than LDOs with output capacitor [40, 46], although they feature very small FoM. The active area of the proposed LDO is one of the largest; the power transistor occupies a significant area for the sake of providing 100mA maximum loading current, and the proposed adaptive AUX

incurs area as well. For completeness, the quiescent current of the proposed LDO is comparable with other designs.

3.4. Conclusions

In conclusion, we have presented the design of a 65nm CMOS LDO embodying an adaptive Feed Forward Ripple Cancellation technique with an adaptive load current tracking scheme. The LDO features very high PSRR over a wide frequency range and large load current range, low dropout voltage, and small overshoot and undershoot.

CHAPTER 4

A 5.6ppm/°C Temperature Coefficient, 87dB PSRR, sub-1V, rad-hard MOSFET-only voltage reference exploiting the ZTC point of an NMOS

A large portion of this chapter has been published in IEEE Journal of Solid-State Circuits [107], 2018 IEEE Nuclear and Space Radiation Effects Conference (NSREC) [109], and described in a patent application [110].

In this chapter, we propose a high-precision rad-hard MOSFET-only voltage reference based on a comprehensive investigation into the first-order and the second-order mechanism of the ZTC point of an NMOS. The proposed voltage reference features excellent performance in terms of low TC (average 5.6ppm/°C over -40°C to 125°C), high PSRR (>50dB up to 10MHz) and radiation hardness (<2% variation up to 1MRad ionizing dosage and free of SEL up to 77MeV·cm²/mg). Two prototype designs are realized in 65nm CMOS and 130nm CMOS.

This chapter is organized as follows. Section 4.1 presents our investigation into the ZTC point mechanism and our discovery of a ZTC mechanism/phenomenon. Section 4.2 presents the design of our proposed voltage reference and the design considerations for TC, PSRR, noise, and process variations. Section 4.3 presents the measurement results of a prototype design realized in 65nm CMOS. Section 4.4 summarizes the performance of our proposed voltage reference and benchmarks our

design against state-of-the-art counterparts. Section 4.5 presents another prototype design realized in 130nm CMOS, and physical measurements that demonstrate its radiation hardness. Section 4.6 draws the conclusions.

4.1 Investigation of the ZTC point mechanism

The primary mechanism of the ZTC point is the mutual compensation of temperature effects on the threshold voltage, V_{th} , and carrier mobility, μ . Figure 4.1(a) depicts the simulated drain-current (I_d) versus gate-to-source voltage (V_{gs}) of an NMOS for three temperatures ($T_L < T_N < T_H$, where T_L , T_N , and T_H are low, nominal and high temperature respectively). Ideally, all three curves intersect at the same point, the ZTC point. However, as observed from Figure 4.1(b), the three curves do not intersect at the same point in practice. For sake of unambiguous definition, we define the ZTC point of the NMOS as a group of points with the same I_d but with different V_{gs} at different temperatures; in Figure 4.1(b), V_{gsTL} , V_{gsTN} , and V_{gsTH} are the corresponding V_{gs} at T_L , T_N , and T_H respectively. Specifically, I_{d_ZTC} is the current at the intersection of the I_d - V_{gs} curves with T_L and T_H . Put simply, the ZTC point is temperature-sensitive, qualified by the temperature sensitivity of V_{gs} . We will now show that the temperature-sensitive ZTC point (V_{gs_ZTC}) is largely due to the secondary effect of mismatch between the mobility temperature exponent and the velocity saturation index.

Figure 4.1. (a) ZTC point of an NMOS, and (b) Temperature sensitive ZTC point.

On the basis of the α -power law, I_d is expressed as

$$I_d = k\mu(T)(V_{gs}(T) - V_{th}(T))^\alpha \quad (4.1)$$

where k is a constant,

α is the velocity saturation index; on the basis of the α power model,

$$I_d \propto (V_{gs} - V_{th})^\alpha.$$

As both $\mu(T)$ and $V_{th}(T)$ are temperature dependent, they can respectively be expressed as

$$\mu(T) = k_\mu T^{-\beta} \quad (4.2)$$

$$V_{th}(T) = V_{th0} - \eta T \quad (4.3)$$

where k_μ is a constant,

V_{th0} is V_{th} extrapolated at 0K and is temperature independent,

η ($\eta > 0$) is the temperature coefficient of V_{th} , and

β is the temperature exponent of μ ; $\mu \propto T^{-\beta}$.

Hence, by substituting eqns. (4.2) and (4.3) into eqn. (4.1), dI_d/dT is derived as

$$\begin{aligned}\frac{dI_d}{dT} &= k\left(\frac{d\mu(T)}{dT}\right)(V_{gs}(T) - V_{th}(T))^\alpha + \alpha k\mu(T)(V_{gs}(T) - V_{th}(T))^{\alpha-1}\left(\frac{dV_{gs}(T)}{dT} - \frac{dV_{th}(T)}{dT}\right) \\ &= kk_\mu T^{-\beta-1}(V_{gs}(T) - V_{th}(T))^{\alpha-1}(-\beta(V_{gs}(T) - V_{th}(T)) + \alpha T\left(\frac{dV_{gs}(T)}{dT} + \eta\right))\end{aligned}\quad (4.4)$$

At the ZTC point where $I_d = I_{d_ZTC}$ is a temperature-independent current (i.e., $dI_{d_ZTC}/dT=0$),

$$\beta(V_{gs_ZTC}(T) - V_{th}(T)) = \alpha T\left(\frac{dV_{gs_ZTC}(T)}{dT} + \eta\right) \quad (4.5)$$

As $V_{gsTL} = V_{gsTH}$, there exists a temperature where $dV_{gs_ZTC}(T)/dT=0$. With a denotation that this temperature is T_0 ($T_L < T_0 < T_H$), and T_0 is the temperature where $dV_{gs}/dT = 0$.

$$\left.\frac{dV_{gs_ZTC}(T)}{dT}\right|_{T=T_0} = 0 \quad (4.6)$$

By substituting eqn. (4.6) into eqn. (4.5), we obtain

$$V_{gs_ZTC}(T_0) - V_{th}(T_0) = \frac{\alpha\eta T_0}{\beta} \quad (4.7)$$

and substituting eqn. (4.7) into eqn. (4.1), I_{d_ZTC} is expressed as

$$I_{d_ZTC} = k\mu(T_0)\left(\frac{\alpha\eta T_0}{\beta}\right)^\alpha = kk_\mu T_0^{-\beta}\left(\frac{\alpha\eta T_0}{\beta}\right)^\alpha \quad (4.8)$$

On the basis of eqn. (4.8), $V_{gs_ZTC}(T)$ and dV_{gs_ZTC}/dT are expressed as

$$\begin{aligned}V_{gs_ZTC}(T) &= V_{th}(T) + \left(\frac{I_{d_ZTC}}{kk_\mu T^{-\beta}}\right)^{\frac{1}{\alpha}} \\ &= V_{th0} - \eta T + \frac{\alpha\eta T_0}{\beta}\left(\frac{T}{T_0}\right)^\beta\end{aligned}\quad (4.9)$$

$$\frac{dV_{gs_ZTC}}{dT} = -\eta + \eta \left(\frac{T}{T_0}\right)^{\left(\frac{\beta}{\alpha}-1\right)} \quad (4.10)$$

On the basis of eqns. (4.9) and (4.10), the ideal ZTC point ($dV_{gs_ZTC}/dT \equiv 0$) exists only if $\beta = \alpha$. However, $\beta \neq \alpha$ in practice because β is largely a constant equal to 1.5, whereas α is a variable whose value is between 1 and 2, depending on the operation region of the NMOS. Specifically, $\alpha \approx 1$ and $\alpha \approx 2$ when the NMOS is in the triode and saturation region respectively. To depict the effect of the unequal β and α , we derive the second-order derivative of V_{gs_ZTC} over T as:

$$\frac{d^2V_{gs}}{dT^2} = \left(\frac{\beta}{\alpha} - 1\right)\eta T_0^{\left(\frac{\beta}{\alpha}-1\right)} T^{\left(\frac{\beta}{\alpha}-2\right)} \quad (4.11)$$

Eqn. (4.11) depicts that when $\alpha < \beta$, $d^2V_{gs_ZTC}/dT^2 > 0$, and that there is a local minimum.

On the other hand, when $\alpha > \beta$, $d^2V_{gs_ZTC}/dT^2 < 0$, and there is a local maximum.

Figure 4.2 depicts the simulated V_{gs_ZTC} against T for a low V_{ds} of 100mV, a high V_{ds} of 700mV and a medium V_{ds} of 300mV. For the low $V_{ds} = 100\text{mV}$ where the NMOS is in the triode region, we obtain $\alpha < \beta$ and as expected, V_{gs_ZTC} is a convex curve with a local minimum, where the TC is 20ppm/°C. Conversely, for the high $V_{ds} = 700\text{mV}$ where the NMOS is in the saturation region, we obtain $\alpha > \beta$ and as expected, V_{gs_ZTC} is a concave curve with a local maximum, where the TC is 26ppm/°C. It is interesting to note that when V_{ds} is the medium voltage of 300mV, the V_{gs_ZTC} curve exhibits a concave-convex idiosyncrasy: concave at low T and convex at high T . This is not unexpected because at low T where V_{th} is high, $V_{ds} = 300\text{mV}$ is considered as a relatively high voltage ($V_{ds} > V_{gs} - V_{th}$) such that the NMOS is in the saturation region. Conversely, at high T where V_{th} is low, $V_{ds} = 300\text{mV}$ is considered as a relatively low voltage ($V_{ds} < V_{gs} - V_{th}$) such that the NMOS is in the triode region. The characteristics of V_{gs_ZTC} are

somewhat akin to V_{REF} in curvature compensation bandgap voltage references. On the basis of simulation results, when $V_{ds} = 300\text{mV}$, the TC of the curvature-compensated V_{gs_ZTC} can be very low, e.g., $\sim 5\text{ppm}/^\circ\text{C}$. This is ~ 5 times lower than when the NMOS is in the saturation region (e.g., $V_{ds} = 700\text{mV}$) such as that employed in a reported ZTC voltage reference.

Figure 4.2. Simulated V_{gs_ZTC} when $V_{ds}=100\text{mV}$, 300mV , and 700mV .

In summary, there exists an optimized V_{ds} , i.e., V_{ds_ZTC} where the ZTC point temperature sensitivity is minimized. At this optimized point, the NMOS is in the saturation region ($\alpha > \beta$) at low temperature and in the triode region ($\alpha < \beta$) at high temperature. In this fashion, the undesired mismatch between the mobility temperature exponent and the velocity saturation index is largely compensated over the entire temperature range, thereby minimizing the temperature sensitivity of the NMOS ZTC point. Put simply, by means of V_{ds_ZTC} , a curvature-compensated V_{gs_ZTC} can be obtained.

4.2 Realization and design considerations of the proposed ZTC voltage reference

4.2.1 ZTC voltage reference design

Figure 4.3 depicts the schematic of our proposed voltage reference, wherein an NMOS (N_X comprising the 4 stacked NMOS, N_{X1} to N_{X4}) is biased at its ZTC point (V_{gs_ZTC} , I_{d_ZTC} , and V_{ds_ZTC}). Table 4.1 tabulates the size of the transistors and the value of the resistors and capacitors.

Figure 4.3. Schematic of the proposed voltage reference.

Table 4.1. Size of the transistors and value of the resistors and capacitors.

Component	Parameter	Component	Parameter
$N_{X1} \sim N_{X4}$	$W=4\mu\text{m}, L=4\mu\text{m}$	R_1	112k Ω
N_5, N_6	$W=16\mu\text{m}, L=2\mu\text{m}$	R_{2a}	37k Ω
N_7	$W=16\mu\text{m}, L=4\mu\text{m}$	R_{2b}	20k Ω
N_8	$W=4\mu\text{m}, L=4\mu\text{m}$	R_b	110k Ω
N_9	$W=32\mu\text{m}, L=4\mu\text{m}$	R_{C+}	30k Ω
P_1, P_2	$W=16\mu\text{m}, L=2\mu\text{m}$	R_{C-}	10k Ω
P_3, P_4	$W=16\mu\text{m}, L=2\mu\text{m}$	C_{C+}	2.4pF
P_5, P_6	$W=2\mu\text{m}, L=1\mu\text{m}$	C_{C-}	7.2pF

The precise ZTC point is achieved by three means. First, N_X is biased at its ZTC point by appropriately designing R_1 . Figure 4.4 depicts the characteristic curves of N_X and R_1 , denoted as IV_{NX} and IV_{R1} respectively. The intersection of these two curves is the designated bias point of R_1 and N_X because R_1 and N_X are biased to the same operating point by the OTA (N_5 , N_6 , N_9 , P_3 , and P_4) and the current mirror (P_1 and P_2). Hence, the ZTC point of N_X can be obtained by

$$R_1 = V_{gs_ZTC} / I_{d_ZTC}. \quad (4.12)$$

V_{gs_ZTC} and I_{d_ZTC} are pre-characterized by simulations, and in practice, V_{gs_ZTC} and I_{d_ZTC} may deviate due to process variations. Nevertheless, the said deviation can be easily mitigated by trimming R_1 as part of a single element trimming for two (extreme) temperatures; see later.

Figure 4.4. Characteristic curves of R_1 and N_X .

Second, the ZTC point temperature sensitivity is further minimized by appropriately designing R_2 . From Figure 4.3, the ZTC point of N_X is optimized by

$$R_2 = (V_{gs_ZTC} - V_{ds_ZTC}) / I_{d_ZTC} \quad (4.13)$$

As in the case of V_{gs_ZTC} and I_{d_ZTC} , V_{ds_ZTC} is pre-characterized from simulations, and it is similarly somewhat sensitive to process variations. We will show later that the process variation of V_{ds_ZTC} can be easily mitigated by our proposed trimming circuit.

Third, the PSRR of V_{REF} is optimized by realizing R_2 by two serial resistors, R_{2a} and R_{2b} , and by designing $R_{2a} = 1/g_{m_NX}$ (see later). On this basis, V_{REF} is expressed as a weighted ZTC voltage:

$$V_{REF} = V_{gs_ZTC} (1 - R_{2a} / R_1) \quad (4.14)$$

In summary, our proposed voltage reference generates V_{REF} on the basis of exploiting the ZTC point of N_X , and the low TC attribute of V_{REF} is achieved by means of a previously ‘unused’ V_{ds_ZTC} which minimizes the temperature sensitivity of N_X ZTC point. In addition to the low TC, our proposed voltage reference also offers high PSRR at both low frequencies and high frequencies and low output noise. The design considerations leading to these two latter attributes will now be described.

4.2.2 PSRR and output noise

Figure 4.5 depicts the simplified schematic of our proposed voltage reference that embodies an active attenuator (enclosed within the dashed box), somewhat akin to the peaking current source [111].

Figure 4.5. Simplified schematic of the proposed voltage reference.

The PSRR of v_{ref} can be obtained from the following two equations:

$$v_o = A_{dd}(s)v_n + A_0(s)g_{mp}(Z^+ - Z^-)(v_n - v_o) \quad (4.15)$$

$$v_{ref} = A_x(s)g_{mp}Z^-(v_n - v_o) \quad (4.16)$$

Consequently, PSRR is expressed as

$$PSRR = \frac{v_{ref}}{v_n} = \frac{Z^-}{Z^+ - Z^-} \times \frac{(1 - A_{dd}(s))A_x(s)}{A_0(s)} \quad (4.17)$$

where v_n is the supply noise,

v_o is the small signal voltage at the output of the OTA,

$A_{dd}(s) = v_o/v_n$ is the gain from the power supply to the OTA output, and it is largely a constant over a wide frequency range [112],

$A_x(s) = v_{ref} / v_{gx}$ is the gain of the proposed active attenuator,

v_{gx} is the small signal voltage at the gate of N_X ,

Z^+ and Z^- are impedance at the positive and negative inputs of the OTA, respectively,

$A_0(s) = A_0 / (1+s/\omega_{p0})$ is the gain of the OTA,

A_0 is the DC gain of the OTA, and

ω_{p0} is the pole frequency of the OTA output.

In view of eqn. (4.17), the mechanisms affecting PSRR of the v_{ref} are $(1-A_{dd}(s))$, $A_x(s)$ and $1/A_0(s)$. Further, as $(1-A_{dd}(s))$ and $A_x(s)$ are largely a constant over a wide frequency range, the degradation of the PSRR at high frequencies is largely ascertained by ω_{p0} .

Figure 4.6 depicts the simulated PSRR, $(1-A_{dd}(s))$, $A_x(s)$ and $1/A_0(s)$. On the basis of the simulation results, our proposed active attenuator boosts the PSRR by ~30dB. Note that as $A_x(s)$ of the proposed active attenuator can be expressed as $(1-g_{m_NX}R_{2a})$, the PSRR can be improved by setting $R_{2a} \approx 1/g_{m_NX}$, where $A_x(s) \approx 0$. The PSRR degrades beyond ~1MHz, which is largely equivalent to the pole frequency of $A_0(s)$. Note that the pole frequency of $A_0(s)$ is ascertained by the frequency compensation employed to stabilize the circuit. We will now discuss the frequency compensation of our voltage reference.

Figure 4.6. Simulated PSRR and its components.

The stability of our proposed voltage reference is achieved in two ways. First, in terms of feedback, our proposed voltage reference comprises two feedback loops — the negative feedback loop formed by the OTA, P_1 , and R_1 ; and the positive feedback loop formed by the OTA, P_2 , and N_X . Stability is ascertained by designing the negative feedback loop to be ‘stronger’ than the positive feedback loop.

Second, there are two adjacent poles in each feedback loop. The poles at the output and input of the OTA (realized by N_4 - N_6 , P_3 , and P_4) are $\omega_{p0} = \sim 1\text{MHz}$ and $\omega_{p1} = \sim 8\text{MHz}$ respectively. To provide for stability, a frequency compensation circuit is required. Specifically, we adopt the impedance adapting compensation (see Figure 4.5) to introduce a left-hand-plane zero to neutralize the effect of ω_{p0} [113]. The adopted compensation approach is advantageous over the conventional Miller compensation because it does not shift ω_{p0} to an undesirably low frequency, thereby maintaining ω_{p0} at high ($\sim 1\text{MHz}$) frequency and achieving a high PSRR at high frequencies. Further, it is worthwhile to note that the proposed active attenuator isolates v_{ref} node from the

feedback loop. Consequently, the proposed voltage reference can accommodate a relatively large range of capacitive loading (up to 1nF) without affecting stability. Note that the proposed voltage reference is unable to drive a resistive load because the resistive load would affect the bias point of N_X .

In addition to boosting PSRR, the proposed active attenuator reduces the output noise. This is because noise transmitted from the gate of N_X (v_{gx}) to the output (v_{ref}) is significantly suppressed by the proposed active attenuator. Consequently, the output noise at v_{ref} is largely contributed by N_X and R_2 .

Figure 4.7 depicts the simulated noise at v_{gx} and v_{ref} , without a filtering capacitor. As expected, the output noise at v_{ref} is more than $>10\times$ smaller than the noise at v_{gx} . Specifically, the flicker noise corner is at $\sim 2\text{kHz}$ and the thermal noise density at v_{ref} is $27\text{nV/Hz}^{1/2}$; this noise density is comparable to reported low-noise voltage references. Nevertheless, the flicker noise corner frequency is higher than the reported low-noise bandgap reference ($\sim 20\text{Hz}$) [57]. This is expected because the flicker noise of a MOSFET is much larger than a BJT with the same size and bias current [57].

Figure 4.7. Simulated noise at v_{ref} and v_{gx} .

In summary, our proposed voltage reference achieves wideband high-PSRR despite the challenges posed by technology scaling, including reduced transistor intrinsic gain and limited supply voltage. The high PSRR at low and high frequencies is achieved by the active attenuator and the impedance adapting compensation respectively, largely without power dissipation penalty. Our proposed voltage reference also features relatively low thermal noise and is attributed to the proposed active attenuator.

4.2.3 Process variations

Like most MOSFET-only voltage references, the proposed voltage reference is sensitive to process variations because the ZTC voltage of a MOSFET is fundamentally process-sensitive. Further, the operating point of N_X may deviate from the desired ZTC point due to process variations. Consequently, process variations result in undesired V_{REF} spread, and a deteriorated TC and TC spread. To mitigate V_{th} spread (and other process variations), a large effective gate area of N_X was achieved by stacking four

identical NMOS (N_{X1} - N_{X4} in Figure 4.3) with the maximum L ($4\mu\text{m}$) allowed in the process used. In addition, trimming of R_1 and R_2 was adopted to optimize TC and TC spread.

We will now show that trimming R_1 (Figure 4.3 and 4.5) can adjust the bias point of N_X to the desired ZTC point (Figure 4.4) and trimming R_2 provides a means to optimize V_{ds} of N_X to the desired V_{ds_ZTC} (see eqn. (4.5)) to minimize the TC of the ZTC point. Figure 3.8 depicts the schematic of the trimming circuit, where R_1 and R_2 are realized by connecting the same number of unit resistors (R_{1_unit} and R_{2_unit} , respectively) in series; and R_{1_unit} and R_{2_unit} are ratiometric, where $R_{2_unit} \approx 0.5R_{1_unit}$ in the proposed design. Consequent to eqns. (4.13) and (4.14), $R_2/R_1 = 1 - V_{ds_ZTC} / V_{gs_ZTC}$, and is largely constant despite the process variations. This is because both V_{gs_ZTC} and V_{ds_ZTC} vary monotonically with respect to V_{th} variations, the dominant process variation. By exploiting the constant R_2/R_1 , we simplify the trimming process by concurrently trimming R_1 and R_2 with four trimming bits (b_1 - b_4); i.e., equivalent to one-element trimming.

Figure 4.8. Trimming circuit of the proposed voltage reference.

From a 200-run Monte-Carlo simulation, Figure 4.9 depicts the box plot of the statistics of untrimmed TC and trimmed TC (including 3-bit, 4-bit, and 5-bit trimmings). It can be seen that the proposed trimming can substantially reduce the TC and the TC

spread, and they are reduced by increasing the number of trimming bits. We choose to adopt the 4-bit trimming as it is a cogent tradeoff between trimming effectiveness and cost.

Figure 4.9. Statistics of untrimmed TC and trimmed TC from a 200-run Monte-Carlo simulation.

Figure 4.10 depicts the trimming process in the proposed voltage reference. In view of the process-sensitive ZTC voltage, the trimming needs to be performed at two temperatures (e.g. -40°C and 125°C) to ascertain the optimum trimming code. At each said temperature, we obtain the plot of V_{REF} versus code by sweeping the trimming code (typically, only two trimming codes are chosen for each temperature). The two plots intersect at a point, and the corresponding code at this intersection point is the desired trimming code ('0111' in Figure 4.10), where the TC is minimized. The proposed two-point trimming can ensure a robust low TC by concurrently trimming R_1 and R_2 . In the perspective of post-manufacturing calibration, trimming involving two temperatures (vis-à-vis one temperature or no trimming) is undesirable, as this is a cost penalty – a disadvantage of virtually all voltage references embodying curvature compensation; see Table 4.3 later.

Figure 4.10. Trimming process of the proposed voltage reference.

Figure 4.11 depicts the statistics of the untrimmed and our trimmed V_{REF} obtained from the said 200-run Monte-Carlo simulation. The variation coefficient of untrimmed V_{REF} (σ/μ) and trimmed V_{REF} (σ_t/μ_t) are 5.5% ($\mu = 428\text{mV}$ and $\sigma = 23\text{mV}$) and 4% ($\mu_t = 426\text{mV}$ and $\sigma_t = 17\text{mV}$) respectively. The trimmed V_{REF} features smaller spread because the proposed trimming scheme can optimize N_X closer to the ZTC point, independent of geometry mismatch, e.g. mirror mismatch and opamp offset, etc. On the basis of these simulations, we assert that the residual V_{REF} spread after trimming is mainly due to the spread of the ZTC voltage of N_X – this is congruous to literature depicting the spread of the ZTC voltage in most MOSFET-only voltage references. It is, nevertheless, worthwhile to note from eqn. (4.14) that the V_{REF} spread due to process variations can be further mitigated by an additional trimming of the ratio of R_1 and R_{2a} . This is because V_{REF} is a weighted ZTC voltage. This additional trimming is not adopted in this design because of the associated trimming cost.

Figure 4.11. Statistics of untrimmed and trimmed V_{REF} from a 200-run Monte-Carlo simulation.

4.3. Hardware measurements of the proposed voltage reference

Figure 4.12 depicts the microphotograph of the proposed voltage reference whose active area is $80\mu\text{m}\times 130\mu\text{m}$ realized in a commercial 65nm bulk CMOS process. 50 samples of our proposed voltage reference are measured.

Figure 4.12. Microphotograph of the proposed voltage reference.

Figure 4.13 depicts the measured V_{REF} versus temperature of one of the samples. The V_{REF} versus temperature curve depicts the desired curvature compensated characteristics – concave at low temperature (-40°C to 35°C) and convex at high temperature (35°C to 125°C). The average V_{REF} is 428.7mV, and V_{REF} features a low TC of 5.6ppm/ $^{\circ}\text{C}$ over a wide temperature range from -40°C to 125°C . As described in Section 4.1 (see Figure 4.2), the curvature compensation and the ensuing low TC are attributed to our exploitation of V_{ds_ZTC} , which minimizes the temperature sensitivity of the ZTC point. The wide temperature range, on the other hand, is attributed to the

characteristic of the ZTC point, which is unaffected by the junction leakage current effect.

Figure 4.13. Measured V_{REF} versus temperature of one sample (trimmed).

Figure 4.14 depicts V_{REF} versus temperature of the 50 measured samples (trimmed) and the measured TC ranges from 3.2ppm/°C to 9.8ppm/°C with an average TC of 5.6ppm/°C. Statistically, our voltage reference exhibits a relatively robust low TC (TC<10ppm/°C) after trimming, and all 50 samples depict the desired curvature-compensated attribute. This robustness is attributed to our proposed trimming circuit (see Figure 4.8). For completeness, note that the TC of 50 samples ranges from 4.3ppm/°C to 72.8ppm/°C before trimming.

Figure 4.14. V_{REF} versus temperature of 50 measured samples (trimmed).

Figure 4.15 depicts the statistics of trimming codes. In the proposed voltage reference, we employ 4-bit trimming (16 trimming codes) where 7 out of 16 trimming codes were needed to trim the 50 samples. This is expected because we designed the 4-bit trimming based on Monte-Carlo simulations, which may overestimate the process variation of samples fabricated on the same wafer. In the case of samples from different wafers, we expect to use all 16 trimming codes.

Figure 4.15. Statistics of trimming codes.

Figure 4.16 depicts the statistical measurements (trimmed) of V_{REF} of the 50 samples. The mean (μ) V_{REF} is 428.5mV, and its standard deviation (σ) is 1.67mV; i.e., a coefficient of variation σ/μ of 0.4%. The measured σ/μ is substantially lesser than that estimated by Monte-Carlo simulations. This is, as discussed earlier, largely because all the 50 measured samples were fabricated on the same wafer.

Figure 4.16. Statistical measurement results of V_{REF} (trimmed).

Figure 4.17 depicts the measured PSRR of V_{REF} . Our proposed voltage reference exhibits a high PSRR of 87dB at low frequency ($< 800\text{kHz}$), and the PSRR degrades beyond 800kHz. As described earlier, the high PSRR at low frequencies and at relatively high frequencies is achieved respectively by means of the active attenuator and the impedance adapting compensation; both techniques do not incur excessive power dissipation penalty. It is worthy to note that compared to state-of-the-art CMOS voltage references, our design achieves the highest PSRR (see Table 4.2 and Table 4.3 later) at both low frequencies and relatively high frequencies. This is despite the reduced

transistor intrinsic gain and the ensuing inadequate circuit loop gain of the 65nm CMOS process (compared to more dated CMOS processes).

Figure 4.17. Measured PSRR of the proposed voltage reference.

Figure 4.18 depicts the measured V_{REF} versus V_{DD} from 0.5V to 1.4V (1.4V is the maximum supply voltage in 65nm CMOS process) for three temperatures, -40°C , 27°C and 125°C . It can be observed that the minimum V_{DD} for our design is $\sim 0.8\text{V}$ for all three temperature conditions. This sub-1V operation can be explained by noting that $V_{DD} = V_{gs_ZTC} + V_{ds_P1}$ (see Figure 4.3), where $V_{gs_ZTC} \sim 600\text{mV}$ (insensitive to temperature variations) and $V_{ds_P1} > 200\text{mV}$ for normal operation. Similar to the design mechanism for the realization of high PSRR at low frequencies, the supply insensitive attribute is achieved by the active attenuator. From the low-frequency PSRR, we estimate that the Line Sensitivity (the parameter that quantifies V_{REF} sensitivity against supply variations), $LS \approx 0.1\%/V$; the limited resolution of our measurement equipment does not permit a direct LS measurement.

Figure 4.18. Measured V_{REF} versus V_{DD} .

4.4. Design summary and Benchmarking

Table 4.2. Performance benchmarking against bandgap voltage references.

		This work	[54]	[56]	[62]	[64]	[66]	[68]
Technology (CMOS)		65nm	0.6 μ m	0.35 μ m	0.16 μ m	0.35 μ m	0.5 μ m	90nm
V_{REF}[mV]		428	1142	858	1087	618	1285	720
Temperature Range [°C]		-40 to 125	0 to 100	-20 to 100	-40 to 125	-15 to 150	-40 to 100	0 to 100
Average TC [ppm/°C]		5.6	5.3 ^a	12.4	5-12	4.9	7.2	32.6
Curvature compensation		Yes	Yes	No	Yes	Yes	Yes	Yes
Coefficient of Variation		0.39%	N.A.	0.15%	0.05%	N.A.	0.01%	1.3%
Trimming		2-Temp	2-Temp	1-Temp	1-Temp ^b	Multi Temp	4-Temp	No
PSRR	10Hz	87	47	68	74	N.A.	70	51
	1MHz	75	10	N.A.	N.A.	N.A.	10	N.A.
Minimum V_{DD}		0.8V	2V	1.4V	1.6V	2.5V	1.6V	1.15V
Power		13 μ W	46 μ W	162 μ W	88 μ W	95 μ W	40 μ W	0.58 μ W

a. Not average TC; TC obtained from one sample only

b. A chopper requiring an external clock is involved in the design

Table 4.3. Performance benchmark against subthreshold MOSFET-only voltage references.

		This work	[58]	[59]	[63]	[65]		[70]
Technology		65nm	0.35 μ m	0.35 μ m	0.35 μ m	0.13 μ m	65nm	65nm
V_{REF}[mV]		428	670	858	263	176	328	474
Temperature Range [°C]		-40 to 125	0 to 80	-20 to 80	0 to 125	-20 to 80	-20 to 80	-40 to 90
Average TC [ppm/°C]		5.6	10	15	165	29	89 to 118	40
Curvature		Yes	No	No	No	No	No	No
Coefficient of Variation		0.39%	3.1%	0.94%	3.9%	0.18%	N.A.	3.4%
Trimming		2-Temp	N.A.	N.A.	N.A.	1-Temp	N.A.	2-Temp;
PSRR[dB]	10Hz	87	47	45	45	51	40	40
	1MHz	75	40	N.A.	12	62	N.A.	20
Minimum V_{DD}		0.8V	0.9V	1.4V	0.45V	0.5V	0.5V	0.75V
Power		13 μ W	36nW	0.3 μ W	3nW	30pW	240pW	0.3 μ W

Table 4.2 and Table 4.3 respectively benchmarks the performance of our proposed voltage reference against state-of-the-art bandgap references and subthreshold MOSFET-only voltage references. When benchmarked against reported bandgap voltage references (Table 4.2), our proposed voltage reference is advantageous in the following three aspects. First, as expected, our voltage reference features the lowest minimum V_{DD} . Second, despite our proposed voltage reference being realized in the smallest feature-size CMOS process, its average TC (from 50 samples) is the second lowest; the TC of ref [54] is not an average TC as it is based on one sample and the average TC of ref is obtained from only five samples. Third, our proposed design features the highest PSRR both at low and high frequencies. Of specific interest, the PSRR of our design at 10Hz and 1MHz is respectively a substantial 13dB and very substantial 60dB higher than designs that reported their PSRR. The shortcoming of our voltage reference is its relatively high coefficient of variation – the second highest amongst reported designs.

When benchmarked against subthreshold MOSFET-only voltage references (Table 4.3), our design is advantageous in three aspects. First, our proposed design features the lowest TC: $\sim 2\times$ lower than the next best design. Second, the stipulated temperature range of our design is the widest – yet featuring the lowest TC. Of specific interest, for the design with the next lowest TC, the stipulated temperature range of our design is a substantial $2\times$ wider, i.e., 165°C vis-à-vis 80°C . For completeness, it is pertinent to note that in general, the wider the temperature range, the larger is the expected TC – particularly at higher temperatures. As described earlier, this is largely because of the junction leakage current effect. It is worthwhile to note that the junction leakage current effect is not pertinent in our design for reasons already described. Third, our proposed design features the highest PSRR both at low and high frequencies. Of

specific interest, the PSRR of our design at 10Hz and 1MHz is respectively a substantial 36dB and 11dB higher than the design with the next best PSRR. The V_{REF} spread of our design is the second smallest among the reported subthreshold voltage references. The shortcoming of our design over subthreshold designs is, as expected, the higher power dissipation. This is due to the fact that the critical transistors in our design are operated in the strong inversion region.

In conclusion, the design of a 65nm MOSFET-only voltage reference exploiting a previously unreported second-order mechanism of the ZTC point is presented. The voltage reference features competitive attributes including a low TC over a wide temperature range, a high PSRR over a wide frequency range, and sub-1V operation.

4.5 Irradiation verification of the proposed voltage reference

In addition to the general circuit attributes of low temperature coefficient and high PSRR, a prototype design of the proposed voltage reference implemented in 130nm CMOS also exhibits hardening towards TID (up to 1MRad ionizing dosage) and Single-Event Effects (SEEs) by means of several RHBD techniques. Specifically,

- (a) The TID is, to the first order, mitigated by means of designing all the deep-submicron MOSFETs therein at strong inversion (i.e. $V_{gs} > V_{th}$). Of particular interest, N_X (in Figure 4.3) that is the key to the ZTC mechanism, always operates at strong inversion. That is because the gate-to-source voltage of N_X , V_{gs_ZTC} , is always equal to V_{th0} [5], and V_{th0} is always greater than V_{th} (see eqn. (4.14)). Single MOSFET of GF 130nm CMOS is characterized under TID, and as expected, it is

largely insensitive to TID when it is biased at strong inversion; see Figure 4.21 later.

- (b) The TID is, to the second order, mitigated by means of tuning R_{2a} (see Figure 4.3). When $R_{2a} < 1/g_{mx}$ (@certain krad TID), V_{REF} decreases as TID increases, and when $R_{2a} > 1/g_{mx}$ (@certain krad TID), V_{REF} increases as TID increases – a second order effect. Given the characteristic shift of N_X over an expected TID range (= estimated dose rate $\times$ expected lifespan in space), R_{2a} can be pre-tuned to minimize the variation of V_{REF} over the entire lifecycle. In this design, as the expected TID range is up to 1Mrad, the variation of V_{REF} is optimized by setting $R_{2a} = 1/g_{mx}$ (@~50kRad).
- (c) The Single-Event-Transient (SET) is mitigated by means of the employment of R_{2a} that substantially mitigate external disturbance to V_{REF} when $R_{2a} = 1/g_{mx}$. Our SET mitigation approach efficiently targets V_{REF} , the most critical node of the entire circuit.
- (d) The SET is further mitigated by featuring a high driving capability. Specifically, our CMOS-only voltage reference can drive a large loading capacitor (C_L), ~1nF, thereby leading to lower SET due to low-pass filtering therein [5].
- (e) The destructive Single-Event-Latchup (SEL) effect is mitigated by means of RHBD layout techniques including extensive utilization of guard rings [7]; the proposed voltage reference is immune to SEL up to 77.3MeV•cm²/mg based on the irradiation tests at the cyclotron at Texas A&M University.

Irradiation Test Results

Figure 4.19 depicts the microphotograph of the prototype design. It is realized in Global Foundries 0.13 μ m bulk CMOS.

The TID test was performed in Cobham RAD Solution, Colorado Spring, USA. Both the proposed MOSFET-only voltage reference realized in 130nm CMOS and a single NMOS transistor of the same technology is characterized at seven TID levels (0krad, 50krad, 100krad, 200krad, 300krad, 500krad, and 1000krad). The respective dose rate for the CMOS-only voltage reference and the single transistors are 77rad(Si)/s and 76rad(Si)/s. The TID test followed MIL-STD-883 TM 1019, Cond. A.

Figure 4.19. Microphotograph of the prototype design in 130nm CMOS.

Figure 4.20 depicts V_{REF} over 0-1Mrad TID under various supply voltage conditions (V_{DD} =1.2V to 1.6V with 0.1V increment). The nominal V_{REF} (i.e., V_{REF} at 0krad and 1.5V V_{DD}) is ~590mV. It can be observed that V_{REF} varies by only 9mV (i.e., 1.5% of its nominal value). The achieved low sensitivity to TID is largely attributed to the aforesaid two TID mitigation approaches.

Figure 4.20. V_{REF} v.s. TID under various supply voltages.

Specifically,

- (i) All transistors, particularly N_x , are biased at strong inversion. As depicted in Figure 4.21, the NMOS at strong inversion (i.e. $V_{gs} > V_{th}$) is largely insensitive to TID; the same for PMOS. The ZTC point of the NMOS (N_x) is biased at strong inversion with $V_{gs} \approx 770\text{mV}$. At the ZTC point vicinity, the NMOS is still somewhat sensitive to TID, wherein the ZTC voltage varies monotonically by 16mV (2.3% variation) over the 1000krad TID range. This is the primary reason that the proposed voltage reference varies 1.5% due to TID.

Figure 4.21. 130nm NMOS characteristic v.s. TID, and ZTC voltage v.s. TID.

For completeness, it can also be observed that the NMOS at weak inversion (i.e. $V_{gs} < V_{th}$) is highly sensitive to TID, and the consequence is a substantially increased leakage current of more than five orders of magnitude over the 1Mrad TID range. In view of this, subthreshold voltage reference [6] is inappropriate for space application.

- (ii) To further mitigate the TID effect, R_{2a} is tuned to be $1/g_{mx}$ (@~50krad). Consequently, it can be observed from Figure 4.20 that the V_{REF} variation is optimized by embodying a second-order curvature wherein the turning point is at TID=~50krad.

On the basis of the measurement results above, it can be concluded that the TID insensitivity of the proposed MOSFET-only voltage reference largely relies on the TID insensitivity of the adopted CMOS process. In view of this, the proposed MOSFET-

only voltage reference design would feature even better TID immunity when it is realized in CMOS process with smaller feature size.

For completeness, Figure 4.22 depicts the TID characteristics of a single NMOS transistor in GF 65nm CMOS [3] and its ZTC point v.s. TID level. Not unexpectedly, the NMOS transistor in 65nm CMOS features superior TID insensitivity over that in 130nm CMOS. Of particular interest, the pertinent ZTC voltage varies by <1% over the 500krad TID range. In view of this, our CMOS-only voltage reference, when being realized in 65nm CMOS, is expected to feature improved TID immunity.

Figure 4.22. 65nm NMOS characteristic v.s. TID, and ZTC voltage v.s. TID.

4.6 Conclusions

In conclusion, the design of a MOSFET-only voltage reference exploiting a previously unreported second-order mechanism of the ZTC point is presented. The voltage reference features competitive attributes including a low TC over a wide temperature range, a high PSRR over a wide frequency range, superior immunity against

radiation hardness, and sub-1V operation. Two prototype designs have been realized in 65nm CMOS and 130nm CMOS, respectively. The 65nm design demonstrates a 5.6ppm/°C TC over a -40°C to 125°C temperature range, and an 87dB PSRR. The 130nm design features 1.5% output variation over 1000krad TID and is immune to SEL up to 77.3MeV•cm²/mg.

CHAPTER 5

Conclusions and Recommendations

This chapter draws the conclusions of the work reported in this Ph.D. research program and delineates recommendations for future work.

5.1 Conclusions

The primary objectives of this Ph.D. program pertained to the design, monolithic realization in deep-submicron CMOS, and physical characterization of a proposed high-performance LDO for emerging IoTs, and a proposed high-precision reference for both IoTs and satellites. The conclusions of the research work are as follows.

In Chapter 1, the motivation, objectives, and contributions of this Ph.D. program have been presented in this thesis.

In Chapter 2, a comprehensive literature review on the LDO and the voltage reference, and the effects of radiation on ICs has been reviewed. Specifically, the review of the LDO has ascertained the mechanisms leading to the limitations of PSRR of an LDO. The review of the voltage reference has ascertained the mechanisms leading to the limitations of TC, PSRR, and low-voltage operation of a voltage reference. Finally, the review of radiation effects has ascertained the mechanisms leading to the limitations of radiation hardness of a voltage reference.

In Chapter 3, a high-performance NMOS LDO featuring $>60\text{dB}$ PSRR over a 10MHz frequency range and a 100mA load current range has been proposed. Our proposed adaptive FFRC technique leading to the high PSRR has been delineated. The design considerations in terms of PSRR, stability, and dropout voltage have been discussed. Physical characterization results have been demonstrated to validate the design concept of the proposed LDO. The proposed LDO has been benchmarked against several state-of-the-art counterparts, where it demonstrated the highest PSRR to-date.

In Chapter 4, a high-precision rad-hard MOSFET-only voltage reference has been proposed. The investigation of the mechanism of the ZTC point of a MOSFET leading to our discovery of a new ZTC phenomenon – the basis of our proposed voltage reference – has been delineated. The design considerations for PSRR and to accommodate process variations have been described. Physical characterization results have been delineated, verifying the design concept of our proposed MOSFET-only voltage reference. The said physical characterization included irradiation tests that demonstrated the radiation immunity of our proposed MOSFET-only voltage reference. The proposed voltage reference has been benchmarked against several state-of-the-art counterparts. On the basis of the benchmarking, our proposed voltage reference is the only MOSFET-only voltage reference embodies curvature-compensation, and it is the only rad-hard MOSFET-only voltage reference to-date.

As a general conclusion, we have made significant contributions towards the design and realization of a high-performance LDO for IoTs and a voltage reference for IoTs and satellites.

5.2 Recommendations for future work

On the basis of the literature review and the research work in this research program, we recommend the following for future work.

- (i) An investigation into the design of a capless-LDO for IoTs featuring high PSRR and low dropout voltage by exploiting our proposed adaptive FFRC technique

As delineated in Chapter 1, a small form factor is one of the most imperative attributes for the emerging IoTs, and the capless-LDO is evidently advantageous over the cap-LDO in terms of form factor. However, as reviewed in Chapter 2, capless-LDOs are often inferior to cap-LDO in terms of PSRR, particularly at high frequencies. Our proposed adaptive FFRC technique delineated in Chapter 3 is a potential solution that would enable a high PSRR capless-LDO due to its effectiveness over a wide frequency range. Put simply, we recommend an investigation into the design of a capless-LDO for IoTs featuring high PSRR and low dropout voltage by exploiting our proposed adaptive FFRC technique.

- (ii) The investigation into the design of an RHBD LDO embodying our proposed rad-hard voltage reference for satellites

The LDO is one of the most critical blocks for satellites because the failure of the power supply under irradiation is one of the major failure mechanisms of satellites. To improve the mission success of satellites, a rad-hard LDO is essential. To this end, it is worthwhile to note that our proposed rad-hard voltage reference in Chapter 4 can be utilized as a sub-block for the design of the rad-hard LDO. Consequently, the subsequent design for the rad-hard LDO should focus on

applying RHBD approach in the remaining sub-circuits described in Chapter 1, including the controller, the power transistor, and the feedback network. Put simply, we recommend an investigation into the design of an RHBD LDO embodying our proposed rad-hard voltage reference for satellites.

- (iii) The investigation into the design of a high-precision ZTC voltage reference featuring sub- μ W power dissipation and a simple room-temperature trimming for IoTs

Despite our proposed ZTC voltage reference featuring high precision, it nevertheless suffers from relatively high power dissipation of 13μ W. In addition, similar to many state-of-the-art curvature-compensated voltage references, our proposed voltage reference requires a somewhat costly two-temperature trimming. To expand the application space of our proposed voltage reference in IoTs, it would be advantageous to mitigate these two limitations. Specifically, in view of the tight power budget and low-cost constraint in many IoTs, a sub- μ W ZTC voltage reference with simple room-temperature trimming would be desirable. Put simply, we recommend an investigation into the design of a high-precision ZTC voltage reference featuring sub- μ W power dissipation and requiring a simple room-temperature trimming for IoTs.

AUTHOR'S PUBLICATIONS

Patents

- [1] J. S. Chang, W. Shu, and J. Jiang
"Method for Providing a Voltage Reference at a Present Operating Temperature in a Circuit,"
PCT/SG2015/050230, applied to industry.

- [2] J. S. Chang, W. Shu, and J. Jiang
"Electronic Circuits for Single-Event Latch-Up Detection and Protection,"
PCT/SG2015/050452, applied to industry.

Journal Publications

- [1] J. Jiang, W. Shu, and J. S. Chang
"A 5.6 ppm/°C Temperature Coefficient, 87-dB PSRR, Sub-1-V Voltage Reference in 65-nm CMOS Exploiting the Zero-Temperature-Coefficient Point,"
IEEE Journal of Solid-State Circuits, vol. 52, no. 3, pp. 623-633, March 2017.

- [2] J. Jiang, W. Shu and J. S. Chang
"A 65nm CMOS Low DropOut Regulator featuring >60dB PSRR over 10MHz Frequency Range and 100mA Load Current Range,"
IEEE Journal of Solid-State Circuits, vol. 53, no. 8, pp. 2331-2342, August 2018.

Conference Publications

- [1] J. Jiang, W. Shu, and J. Chang, and J. Liu
"A novel subthreshold voltage reference featuring 17ppm/°C TC within -40°C to 125°C and 75dB PSRR,"
IEEE ISCAS, Lisbon, 2015.

- [2] J. Jiang, W. Shu, K. S. Chong, T. Lin, N. K. Z. Lwin, J. S. Chang, and J. Liu
"Total Ionizing Dose (TID) effects on finger transistors in a 65nm CMOS process,"
IEEE ISCAS, Montreal, QC, 2016.

- [3] J. Jiang, W. Shu, Y. Qu, K. S. Chong, and J. S. Chang
"Design and Test of a RHBD CMOS-Only Voltage Reference,"
IEEE Nuclear and Space Radiation Effects Conference (NSREC), Kona, Hawaii, 2018.

- [4] J. S. Chang, K. S. Chong, W. Shu, T. Lin, J. Jiang, N. K. Z. Lwin, and Y. Kang
"Radiation-hardened library cell template and its total ionizing dose (TID) delay characterization in 65nm CMOS process,"
IEEE MWSCAS, College Station, TX, 2014.

- [5] T. Lin, K. S. Chong, W. Shu, N. K. Z. Lwin, J. Jiang, and J. S. Chang
"Experimental investigation into radiation-hardening-by-design (RHBD) flip-flop designs in a 65nm CMOS process,"
IEEE ISCAS, Montreal, QC, 2016.

BIBLIOGRAPHY

- [1] C. Shi, B. C. Walker, E. Zeisel, B. Hu, and G. H. McAllister, "A Highly Integrated Power Management IC for Advanced Mobile Applications," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 1723-1731, 2007.
- [2] G. A. Rincón-Mora, *Analog IC Design with Low-Dropout Regulators, Second Edition*: McGraw-Hill Education, 2014.
- [3] W.-S. T. Chi-Wah Kok, *CMOS Voltage References: An Analytical and Practical Perspective*: Wiley-IEEE Press, 2013.
- [4] J. A. Stankovic, "Research Directions for the Internet of Things," *IEEE Internet of Things Journal*, vol. 1, pp. 3-9, 2014.
- [5] J. D. Cressler and H. A. Mantooth, *Extreme Environment Electronics*: CRC Press, 2012.
- [6] T. R. Oldham, "Analysis of Damage in MOS Devices for Several Radiation Environments," *IEEE Transactions on Nuclear Science*, vol. 31, pp. 1236-1241, 1984.
- [7] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Transactions on Nuclear Science*, vol. 50, pp. 483-499, 2003.
- [8] G. Bruguier and J. M. Palau, "Single particle-induced latchup," *IEEE Transactions on Nuclear Science*, vol. 43, pp. 522-532, 1996.

- [9] Q. Liu, W. Shu, and J. S. Chang, "A 400-MS/s 10-b 2-b/Step SAR ADC With 52-dB SNDR and 5.61-mW Power Dissipation in 65-nm CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, pp. 3444-3454, 2017.
- [10] F. N. U. Juanda, W. Shu, and J. S. Chang, "A 10-GS/s 4-Bit Single-Core Digital-to-Analog Converter for Cognitive Ultrawidebands," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, pp. 16-20, 2017.
- [11] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1723-1732, 1996.
- [12] K. S. Chong, B. H. Gwee, and J. S. Chang, "Energy-Efficient Synchronous-Logic and Asynchronous-Logic FFT/IFFT Processors," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 2034-2045, 2007.
- [13] K. S. Chong, K. L. Chang, B. H. Gwee, and J. S. Chang, "Synchronous-Logic and Globally-Asynchronous-Locally-Synchronous (GALS) Acoustic Digital Signal Processors," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 769-780, 2012.
- [14] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 748-754, 1987.
- [15] S. Rixner, W. J. Dally, U. J. Kapasi, P. Mattson, and J. D. Owens, "Memory access scheduling," in *Proceedings of 27th International Symposium on Computer Architecture (IEEE Cat. No.RS00201)*, 2000, pp. 128-138.

- [16] K. Cui, V. Adrian, B. H. Gwee, and J. S. Chang, "A Noise-Shaped Randomized Modulation for Switched-Mode DC-DC Converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, pp. 394-405, 2018.
- [17] A. A. Aziz, Y. A. Sekercioglu, P. Fitzpatrick, and M. Ivanovich, "A Survey on Distributed Topology Control Techniques for Extending the Lifetime of Battery Powered Wireless Sensor Networks," *IEEE Communications Surveys & Tutorials*, vol. 15, pp. 121-144, 2013.
- [18] C. F. Pasluosta, H. Gassner, J. Winkler, J. Klucken, and B. M. Eskofier, "An Emerging Era in the Management of Parkinson Disease: Wearable Technologies and the Internet of Things," *IEEE Journal of Biomedical and Health Informatics*, vol. 19, pp. 1873-1881, 2015.
- [19] S. Shekhar, S. Sankar, and A. K. Jain, "Electrical modeling for sub-millivolt noise in compact IoT system designs," in *2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*, 2017, pp. 231-236.
- [20] M. D. Mulligan, B. Broach, and T. H. Lee, "A 3MHz Low-Voltage Buck Converter with Improved Light Load Efficiency," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 2007, pp. 528-620.
- [21] C. Zheng and D. Ma, "A 10MHz 92.1%-efficiency green-mode automatic reconfigurable switching converter with adaptively compensated single-bound hysteresis control," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 204-205.

- [22] W. Yang, D. Kelly, L. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1931-1936, 2001.
- [23] Y. S. Shu, L. T. Kuo, and T. Y. Lo, "An Oversampling SAR ADC With DAC Mismatch Error Shaping Achieving 105 dB SFDR and 101 dB SNDR Over 1 kHz BW in 55 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, pp. 2928-2940, 2016.
- [24] R. Farjad-Rad, W. Dally, N. Hiok-Tiaq, R. Senthinathan, M. J. E. Lee, R. Rathi, *et al.*, "A low-power multiplying DLL for low-jitter multigigahertz clock generation in highly integrated digital chips," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1804-1812, 2002.
- [25] N. D. Dalt, "A design-oriented study of the nonlinear dynamics of digital bang-bang PLLs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, pp. 21-31, 2005.
- [26] T. Instruments. (2017). *ADC344x Quad-Channel, 14-Bit, 25-MSPS to 125-MSPS, Analog-to-Digital Converters* [online]. Available: <http://www.ti.com/lit/ds/symlink/adc3444.pdf>
- [27] T. Lin, K. S. Chong, J. S. Chang, and B. H. Gwee, "An Ultra-Low Power Asynchronous-Logic In-Situ Self-Adaptive VDD System for Wireless Sensor Networks," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 573-586, 2013.
- [28] B. M. King. (2000). *Understanding the load transient response of LDOs* [online]. Available: http://www.ti.com/sc/docs/apps/msp/journal/nov2000/nov_04.pdf

- [29] I. Maxim Integrated Products, Sunnyvale, CA. (2002). *Application Note 883: Improved Power Supply Rejection for IC Linear Regulators* [online]. Available: http://www.maximic.com/appnotes.cfm/appnote_number/883
- [30] I. Maxim Integrated Products, Sunnyvale, CA. (2002). *Application Note 898: Selecting LDO Linear Regulators for Cellphone Designs* [online]. Available: http://www.maximic.com/appnotes.cfm/appnote_number/898
- [31] J. C. Teel. (2005). *Understanding noise in linear regulators* [online]. Available: <http://www.ti.com/lit/an/slyt201/slyt201.pdf>
- [32] K. Wong and D. Evans, "A 150mA Low Noise, High PSRR Low-Dropout Linear Regulator in 0.13 μ m Technology for RF SoC Applications," in *2006 Proceedings of the 32nd European Solid-State Circuits Conference*, 2006, pp. 532-535.
- [33] E. Alon, J. Kim, S. Pamarti, K. Chang, and M. Horowitz, "Replica Compensated Linear Regulators for Supply-Regulated Phase-Locked Loops," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 413-424, 2006.
- [34] V. Gupta and G. A. Rincón-Mora, "A 5mA 0.6 μ m CMOS Miller-Compensated LDO Regulator with -27dB Worst-Case Power-Supply Rejection Using 60pF of On-Chip Capacitance," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 2007, pp. 520-521.
- [35] M. Al-Shyoukh, H. Lee, and R. Perez, "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 1732-1742, 2007.

- [36] V. Ivanov, "Design Methodology and Circuit Techniques for Any-Load Stable LDOs with Instant Load Regulation and Low Noise," in *Analog Circuit Design: High-speed Clock and Data Recovery, High-performance Amplifiers, Power Management*, M. Steyaert, A. H. M. v. Roermund, and H. Casier, Eds., ed Dordrecht: Springer Netherlands, 2009, pp. 339-358.
- [37] W. Kruiskamp and R. Beumer, "Low drop-out voltage regulator with full on-chip capacitance for slot-based operation," in *ESSCIRC 2008 - 34th European Solid-State Circuits Conference*, 2008, pp. 346-349.
- [38] A. P. Patel and G. A. Rincon-Mora, "High Power-Supply-Rejection (PSR) Current-Mode Low-Dropout (LDO) Regulator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, pp. 868-873, 2010.
- [39] A. Amer and E. Sánchez-Sinencio, "A 140mA 90nm CMOS low drop-out regulator with -56dB power supply rejection at 10MHz," in *IEEE Custom Integrated Circuits Conference 2010*, 2010, pp. 1-4.
- [40] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, "High PSR Low Drop-Out Regulator With Feed-Forward Ripple Cancellation Technique," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 565-577, 2010.
- [41] C. Y. Tseng, L. W. Wang, and P. C. Huang, "An Integrated Linear Regulator With Fast Output Voltage Transition for Dual-Supply SRAMs in DVFS Systems," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2239-2249, 2010.
- [42] G. Morita. (2011). *Noise Sources in Low Dropout (LDO) Regulators* [online]. Available: <http://www.analog.com/media/en/technical-documentation/application-notes/AN-1120.pdf>

- [43] B. Yang, B. Drost, S. Rao, and P. K. Hanumolu, "A high-PSR LDO using a feedforward supply-noise cancellation technique," in *2011 IEEE Custom Integrated Circuits Conference (CICC)*, 2011, pp. 1-4.
- [44] E. N. Y. Ho and P. K. T. Mok, "Wide-Loading-Range Fully Integrated LDR With a Power-Supply Ripple Injection Filter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, pp. 356-360, 2012.
- [45] C. J. Park, M. Onabajo, and J. Silva-Martinez, "External Capacitor-Less Low Drop-Out Regulator With 25 dB Superior Power Supply Rejection in the 0.4-4 MHz Range," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 486-501, 2014.
- [46] Y. S. Yuk, S. Jung, C. Kim, H. D. Gwon, S. Choi, and G. H. Cho, "PSR Enhancement Through Super Gain Boosting and Differential Feed-Forward Noise Cancellation in a 65-nm CMOS LDO Regulator," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, pp. 2181-2191, 2014.
- [47] Y. Lu, W. H. Ki, and C. P. Yue, "An NMOS-LDO Regulated Switched-Capacitor DC-DC Converter With Fast-Response Adaptive-Phase Digital Control," *IEEE Transactions on Power Electronics*, vol. 31, pp. 1294-1303, 2016.
- [48] Q. H. Duong, H. H. Nguyen, J. W. Kong, H. S. Shin, Y. S. Ko, H. Y. Yu, *et al.*, "Multiple-Loop Design Technique for High-Performance Low-Dropout Regulator," *IEEE Journal of Solid-State Circuits*, vol. 52, pp. 2533-2549, 2017.
- [49] S. Y. Peng, L. H. Liu, P. K. Chang, T. Y. Wang, and H. Y. Li, "A Power-Efficient Reconfigurable Output-Capacitor-Less Low-Drop-Out Regulator for Low-Power Analog Sensing Front-End," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, pp. 1318-1327, 2017.

- [50] S. J. Yun, J. S. Kim, and Y. S. Kim, "Capless LDO Regulator Achieving -76 dB PSR and 96.3 fs FOM," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, pp. 1147-1151, 2017.
- [51] R. Magod, N. Suda, V. Ivanov, R. Balasingam, and B. Bakkaloglu, "A Low-Noise Output Capacitorless Low-Dropout Regulator With a Switched-RC Bandgap Reference," *IEEE Transactions on Power Electronics*, vol. 32, pp. 2856-2864, 2017.
- [52] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, *et al.*, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 670-674, 1999.
- [53] P. Malcovati, F. Maloberti, C. Fiacchi, and M. Pruzzi, "Curvature-compensated BiCMOS bandgap with 1-V supply voltage," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1076-1081, 2001.
- [54] L. Ka Nang, P. K. T. Mok, and L. Chi Yat, "A 2-V 23 μ A 5.3-ppm/ $^{\circ}$ C curvature-compensated CMOS bandgap voltage reference," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 561-564, 2003.
- [55] D. Spady and V. Ivanov, "A CMOS bandgap voltage reference with absolute value and temperature drift trims," in *2005 IEEE International Symposium on Circuits and Systems*, 2005, pp. 3853-3856 Vol. 4.
- [56] R. T. Perry, S. H. Lewis, A. P. Brokaw, and T. R. Viswanathan, "A 1.4 V Supply CMOS Fractional Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 2180-2186, 2007.

- [57] K. Sanborn, D. Ma, and V. Ivanov, "A Sub-1-V Low-Noise Bandgap Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 2466-2481, 2007.
- [58] G. D. Vita and G. Iannaccone, "A Sub-1-V, 10 ppm/°C, Nanopower Voltage Reference Generator," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 1536-1542, 2007.
- [59] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 2047-2054, 2009.
- [60] Y. H. Lam and W. H. Ki, "CMOS Bandgap References With Self-Biased Symmetrically Matched Current-Voltage Mirror and Extension of Sub-1-V Design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, pp. 857-865, 2010.
- [61] F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts, and B. Nauta, "A 1.2-V 10- μ W NPN-Based Temperature Sensor in 65-nm CMOS With an Inaccuracy of 0.2°C (3 σ) from -70°C to 125°C," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2591-2601, 2010.
- [62] G. Ge, C. Zhang, G. Hoogzaad, and K. A. A. Makinwa, "A Single-Trim CMOS Bandgap Reference With a 3 σ inaccuracy of $\pm 0.15\%$ from -40°C to 125°C," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 2693-2701, 2011.
- [63] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 465-474, 2011.

- [64] C. M. Andreou, S. Koudounas, and J. Georgiou, "A Novel Wide-Temperature-Range, 3.9 ppm/°C CMOS Bandgap Reference Circuit," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 574-581, 2012.
- [65] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 2534-2545, 2012.
- [66] Z. K. Zhou, Y. Shi, Z. Huang, P. S. Zhu, Y. Q. Ma, Y. C. Wang, *et al.*, "A 1.6-V 25- μ A 5-ppm/°C Curvature-Compensated Bandgap Reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, pp. 677-684, 2012.
- [67] J. Jiang, W. Shu, J. Chang, and J. Liu, "A novel subthreshold voltage reference featuring 17ppm/°C TC within -40°C to 125°C and 75dB PSRR," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 501-504.
- [68] K. K. Lee, T. S. Lande, and P. D. Häfliger, "A Sub- μ W Bandgap Reference Circuit With an Inherent Curvature-Compensation Property," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, pp. 1-9, 2015.
- [69] A. Shrivastava, K. Craig, N. E. Roberts, D. D. Wentzloff, and B. H. Calhoun, "5.4 A 32nW bandgap reference voltage operational from 0.5V supply for ultra-low power systems," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1-3.
- [70] X. L. Tan, P. K. Chan, and U. Dasgupta, "A Sub-1-V 65-nm MOS Threshold Monitoring-Based Voltage Reference," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, pp. 2317-2321, 2015.

- [71] Y. C. Su, K. Y. Huang, T. W. Chen, Y. M. Tsai, S. Y. Chien, and L. G. Chen, "A 52 mW Full HD 160-Degree Object Viewpoint Recognition SoC With Visual Vocabulary Processor for Wearable Vision Applications," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 797-809, 2012.
- [72] L. D. Xu, W. He, and S. Li, "Internet of Things in Industries: A Survey," *IEEE Transactions on Industrial Informatics*, vol. 10, pp. 2233-2243, 2014.
- [73] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and W. Hon-Sum Philip, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, pp. 259-288, 2001.
- [74] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, pp. 305-327, 2003.
- [75] B. Razavi, "CMOS technology characterization for analog and RF design," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 268-276, 1999.
- [76] P. R. Gray, *Analysis and Design of Analog Integrated Circuits*: Wiley Publishing, 2009.
- [77] B. Razavi, "The Bandgap Reference [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 8, pp. 9-12, 2016.
- [78] P. K. T. Mok and L. Ka Nang, "Design considerations of recent advanced low-voltage low-temperature-coefficient CMOS bandgap voltage reference," in *Proceedings of the IEEE 2004 Custom Integrated Circuits Conference (IEEE Cat. No.04CH37571)*, 2004, pp. 635-642.

- [79] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, pp. 876-884, 2001.
- [80] P. C. Adell and L. Z. Scheick, "Radiation Effects in Power Systems: A Review," *IEEE Transactions on Nuclear Science*, vol. 60, pp. 1929-1952, 2013.
- [81] N. W. v. Vonno, B. Williams, S. D. Turner, E. J. Thomson, S. K. Bernard, and D. N. Goodhew, "Total Dose and Single Event Effects Testing of the Intersil ISL71090SEH and ISL71091SEH Precision Voltage References," in *2014 IEEE Radiation Effects Data Workshop (REDW)*, 2014, pp. 1-6.
- [82] Y. Gonzalez-Velo, A. Mahmud, W. Chen, J. L. Taggart, H. J. Barnaby, M. N. Kozicki, *et al.*, "Radiation Hardening by Process of CBRAM Resistance Switching Cells," *IEEE Transactions on Nuclear Science*, vol. 63, pp. 2145-2151, 2016.
- [83] D. G. Mavis and P. H. Eaton, "SEU and SET Modeling and Mitigation in Deep Submicron Technologies," in *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*, 2007, pp. 293-305.
- [84] N. A. Dodds, N. C. Hooten, R. A. Reed, R. D. Schrimpf, J. H. Warner, N. J. H. Roche, *et al.*, "Effectiveness of SEL Hardening Strategies and the Latchup Domino Effect," *IEEE Transactions on Nuclear Science*, vol. 59, pp. 2642-2650, 2012.
- [85] J. Guo, L. Zhu, W. Liu, H. Huang, S. Liu, T. Wang, *et al.*, "Novel Radiation-Hardened-by-Design (RHBD) 12T Memory Cell for Aerospace Applications in

- Nanoscale CMOS Technology," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. PP, pp. 1-8, 2017.
- [86] V. Gromov, A. J. Annema, R. Kluit, J. L. Visschers, and P. Timmer, "A Radiation Hard Bandgap Reference Circuit in a Standard 0.13 μ m CMOS Technology," *IEEE Transactions on Nuclear Science*, vol. 54, pp. 2727-2733, 2007.
- [87] R. C. Lacoe, J. V. Osborn, D. C. Mayer, S. Brown, and J. Gambles, "Total-dose tolerance of the commercial Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μ m CMOS process," in *2001 IEEE Radiation Effects Data Workshop. NSREC 2001. Workshop Record. Held in conjunction with IEEE Nuclear and Space Radiation Effects Conference (Cat. No.01TH8588)*, 2001, pp. 72-76.
- [88] J. Jiang, W. Shu, K. S. Chong, T. Lin, N. K. Z. Lwin, J. S. Chang, *et al.*, "Total Ionizing Dose (TID) effects on finger transistors in a 65nm CMOS process," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016, pp. 5-8.
- [89] R. L. Pease, R. D. Schrimpf, and D. M. Fleetwood, "ELDRS in Bipolar Linear Circuits: A Review," *IEEE Transactions on Nuclear Science*, vol. 56, pp. 1894-1908, 2009.
- [90] K. Kruckmeyer and T. Trinh, "ELDRS Characterization of Texas Instruments LM185, 1.2V Precision Reference: Retrograde Behavior Demonstrates Why Taking Interim Test Points Is Important," in *2014 IEEE Radiation Effects Data Workshop (REDW)*, 2014, pp. 1-4.

- [91] H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," *IEEE Transactions on Nuclear Science*, vol. 53, pp. 3103-3121, 2006.
- [92] R. J. Widlar, "New developments in IC voltage regulators," *IEEE Journal of Solid-State Circuits*, vol. 6, pp. 2-7, 1971.
- [93] B. Razavi, *Design of Analog CMOS Integrated Circuits*: McGraw-Hill, 2001.
- [94] I. Analog Devices. (2014). *Powering Noise Sensitive Systems* [online]. Available: <https://www.youtube.com/watch?v=p5qqU8Jpky0&t=648s>
- [95] S. J. Mason, "Feedback Theory-Some Properties of Signal Flow Graphs," *Proceedings of the IRE*, vol. 41, pp. 1144-1156, 1953.
- [96] V. Gupta, G. A. Rincon-Mora, and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in *IEEE International SOC Conference, 2004. Proceedings.*, 2004, pp. 311-315.
- [97] B. K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational-Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 18, pp. 629-633, 1983.
- [98] L. Ka Nang and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1691-1702, 2003.
- [99] T. Instruments. (2011). *Voltage Reference Selection Basics* [online]. Available: <http://www.ti.com/lit/an/snva602/snva602.pdf>

- [100] M. Lee. (1999). *Understanding and Applying Voltage References* [online]. Available:
<https://www.edn.com/contenteetimes/documents/schweber/c0955/c0955-ch35a.pdf>
- [101] A. P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 9, pp. 388-393, 1974.
- [102] Y. Tsividis, *Operation and Modeling of the MOS Transistor*: Oxford University Press, 1999.
- [103] J. Benedetto, P. Eaton, K. Avery, D. Mavis, M. Gadlage, T. Turflinger, *et al.*, "Heavy ion-induced digital single-event transients in deep submicron Processes," *IEEE Transactions on Nuclear Science*, vol. 51, pp. 3480-3485, 2004.
- [104] M. Turowski and K. Lilja, "Single-event effects in advanced CMOS technologies: Analysis and mitigation," in *2015 22nd International Conference Mixed Design of Integrated Circuits & Systems (MIXDES)*, 2015, pp. 33-33.
- [105] R. R. Troutman, "Epitaxial layer enhancement of n-well guard rings for CMOS circuits," *IEEE Electron Device Letters*, vol. 4, pp. 438-440, 1983.
- [106] J. Jiang, W. Shu, and J. S. Chang, "A 65nm CMOS Low DropOut Regulator featuring >60dB PSRR over 10MHz Frequency Range and 100mA Load Current Range," *IEEE Journal of Solid-State Circuits*, vol. 2018, accepted.
- [107] J. Jiang, W. Shu, and J. S. Chang, "A 5.6 ppm/°C Temperature Coefficient, 87-dB PSRR, Sub-1-V Voltage Reference in 65-nm CMOS Exploiting the Zero-

- Temperature-Coefficient Point," *IEEE Journal of Solid-State Circuits*, vol. 52, pp. 623-633, 2017.
- [108] B. B. Ravesh Magod, Sanjeev Manandhar, "A 1.24uA Quiescent Current NMOS Low Dropout Regulator With Integrated Low-Power Oscillator-Driven Charge-Pump and Switched-Capacitor Pole Tracking Compensation," *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 2356-2367, 2018.
- [109] J.Jiang, W.Shu, K-S.Chong, Y.Qu, and J.S.Chang, "Design and Test of a RHBD CMOS-Only Voltage Reference," in *2018 IEEE Nuclear and Space Radiation Effects Conference*, 2018.
- [110] J.S.Chang, W.Shu, and J.Jiang, "Method for Providing a Voltage Reference at a Present Operating Temperature in a Circuit," 2016.
- [111] D. V. Kerns, "Optimization of the peaking current source," *IEEE Journal of Solid-State Circuits*, vol. 21, pp. 587-590, 1986.
- [112] M. S. J. Steyaert and W. M. C. Sansen, "Power supply rejection ratio in operational transconductance amplifiers," *IEEE Transactions on Circuits and Systems*, vol. 37, pp. 1077-1084, 1990.
- [113] X. Peng, W. Sansen, L. Hou, J. Wang, and W. Wu, "Impedance Adapting Compensation for Low-Power Multistage Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 445-451, 2011.