Digitally-assisted power converter system for solar energy harvesting applications

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**DIGITALLY-ASSISTED POWER
CONVERTER SYSTEM FOR SOLAR
ENERGY HARVESTING APPLICATIONS**

BUI ANH KHOA

**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

A thesis submitted to the Nanyang Technological University in partial
fulfilment of the requirement for the degree of Doctor of Philosophy

Jul 2019

STATEMENT OF ORIGINALITY

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

A handwritten signature in black ink, consisting of a stylized 'B' followed by 'A' and 'K' with a long horizontal stroke extending to the right.

Name: Bui Anh Khoa

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Date: 15 July 2019

AUTHORSHIP ATTRIBUTION STATEMENT

This thesis contains material from 3 paper(s) published in the following peer-reviewed journal(s) / from papers accepted at conferences in which I am listed as an author.

Chapter 3 and 4 are published as:

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The contribution of the co-authors are as follows:

- Associate Prof Siek Liter provided the initial project direction, revised the design and reviewed manuscript drafts
- I prepared the manuscript drafts
- I co-designed the study with Mr. Z. Xiao and performed all the laboratory work consists of circuit simulation, experiment and data collection at School of Electrical and Electronic Engineering and Virtus, IC Design Centre of Excellence

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ABSTRACT

Nowadays, the power management unit (PMU) plays an essential role in electronic and communication devices and their reliability. More challenges for the power management industries are proposed from the increasing of low-voltage low-power electronic devices and growing demands of complex functionalities. Limited capacity of the finite power source is one of the limitations on the overall performance and the lifetime of these battery-powered devices. “Energy harvesting” is the process of collecting and converting minute amount of unharnessed energy from surrounding environment into usable electrical energy. There are plenty of ambient energy sources ranging from the most common sources such as thermal energy, solar energy, and mechanical vibrations to new-developed sources like RF microwave, bioenergy, etc. As energy harvesting increases the possibility of autonomous devices, efficient energy harvesting circuit design has become increasingly important and has gained immense popularity.

Scavenging energy from solar is a good solution to address the increase of power consumption in electronic devices. Modern circuits and systems require multiple voltage supplies to provide different functionalities. For example, 2.2-3V supplies power RF and antenna circuit, while analog circuit and digital circuit operate using different voltage supplies ranging from 0.6V to 1.8V. Using multiple voltage supplies can improve the overall performance while reducing the power consumption of the devices.

In this research, an energy scavenging system is proposed to extract photovoltaic (PV) energy and supply to application smart nodes of Internet-of-Things (IOT). The main part of the system consists of a single-inductor H-bridge configuration DC-DC converter connecting with dual inputs and dual outputs. It aims to regulate a constant 1V output voltage to supply for several applications such as signal transmitters and sensor. The surplus energy is stored in a super capacitor. The backup capacitor also serves as a secondary source of energy. The most critical issue in energy harvesting applications is maximum power extracting. In order to maximize power extraction under all conditions, a digital-controlled feed-forward maximum power point tracking (MPPT) system is implemented. An input approximation method is proposed to quickly predict the change in input power and shift the PV system to operate the maximum power point (MPP). Both pulse-frequency modulation (PFM) and pulse-width modulation (PWM) are then used to regulate the 1V output voltage at the MPP.

The PV system is designed using 0.18 μ m CMOS technologies. The controller part is mostly designed using digital circuit to enhance stability, reliability, and controllability. The system is able to extract energy from a single solar cell and deliver to multiple outputs loads. The proposed system achieves above 60% of conversion efficiency with a peak efficiency of 84.1% while driving 1 μ A to 1mW load current.

The next part of this research evaluates the possibility of using switched-capacitor (S) DC-DC converter in battery-powered electronic devices. Different designs of SC converter are proposed. The first design presents a single boundary

hysteretic controller for a SC converter. It can achieve optimal output voltage ripple by matching the converter switching frequency and the output sampling frequency. This $\frac{1}{2}$ step-down SC converter is fabricated in 0.18 μm CMOS technologies, using on-chip flying capacitors. The proposed design can achieve peak conversion efficiency of 86% while maintains power conversion efficiency higher than 65% while deliver output loads from 0.1mA to 7mA. In addition, a SC converter with integrated NMOS-LDOs is proposed to further improve the transient response and eliminate the output ripple. The power switches of the SC converter are functioned as the pass transistor of the low-dropout regulators. Adaptive gate slop technique and gate pre-charge technique are used to reduce output glitches as well as optimize the dead time during phase transitions. The second SC converter is also implemented in 0.18 μm CMOS technologies. It achieves peak efficiency of 83% while maintains the efficiency higher than 72% throughout the entire load range.

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CHAPTER 1: INTRODUCTION

1.1 BACKGROUND

In recent years, the rapid growth of information and communications technologies (ICT) has connected people around the world. Nowadays, Internet of Things (IOT) [1.1] has been increasingly developed and connected more than 10 billion devices. It is predicted to have 30 billion to 50 billion connected endpoints by 2020 [1.2]. The connected devices must be able to collect, transmit and process data with a minimum required level of intelligence. The growth of IOT has led to the large expansion of applications and devices in human life, ranging from military, home, vehicles to health-care applications, etc.

The limited availability of energy sources in these battery-powered devices increase the popularity of energy efficient power-management circuitry systems become. Therefore, the power management industries have developed to be one of the fastest growing sectors in the modern world today [1.3]. As the energy demands are increasing, the cost of conventional energy sources such as coal, oil and gas rises rapidly. Consequently, overdependence on these conventional energy sources results significant damages to the natural environment. Environmental issues and fast depleting of energy sources have led to the expansion of research on renewable energy. Renewable energy is a source that minimizes the negative effect of natural resource while meeting the increasing energy demands [1.4]. Despite the high installation cost of renewable sources, the long-time energy price costs less.

One of the most important renewable energy source is solar power. Solar energy is free, clean, and abundant. It can be easily captured and directly converted to electrical power using photovoltaic (PV) module. However, directly capturing power from solar energy and delivering to application load results sub-optimal efficiency. Due to the nonlinearity of the current-voltage relationship of the PV module and the dependence on the surrounding environment such as temperature and light intensity, it is important to develop efficient power circuit techniques that can extract the maximum power from the PV module.

1.2 OBJECTIVES & SCOPE

In this research, the PV system is considered a very low power system, generating less than 10mW and the voltages are capped to 5V. With the increasing demand for self-powered electronic devices for the IOT development, we extend the application of the power management system to these applications. The objective of this research is to develop an energy harvesting system that is able to extract the power from the PV source and supply to these IOT nodes. Specifically, a DC-DC converter system is designed for micro-power indoor PV energy harvesting.

The scope of this research consists of:

Design a single-inductor multiple-input multiple-output DC-DC converter to harvest PV energy in an efficient way. The power converter need to supply power to a low power application and recharge a backup storage. The system must be able to switch mode according to the change of loading conditions. Multiple-input multiple output buck-boost topology is preferred as it provides the

regulations to the output that is higher and lower than the input voltage. Maximum power point tracker will also be implemented to ensure that the connected PV cell always operates at its maximum power point. Several techniques to enhance overall cost efficiency are studied and applied such as pulse-width modulation (PWM), pulse-frequency modulation (PFM), zero-current detector (ZCD), dead-time controller (DTC), etc. The control circuit is design mainly in digital to make use of its high computational power. As the scale of low power application, the controller is required to consume low power.

1.3 ORGANIZATION

This report consists of five chapters. Chapter One provides the overall background of the research project. Chapter Two reviews the past literature with regards to the following topic:

- The PV cell model used in the research simulations and experiments,
- The maximum power point tracker topologies used to track the PV cell and achieve its maximum power point,
- Several power management devices such as linear regulators and second-order switching DC-DC converters,
- Several multiple-input multiple-output DC-DC converter topologies,
- Several controlling methods of DC-DC converter such as PWM, DTC and ZCD.

Chapter Three presents the proposed H-Bridge DC-DC converter for energy harvesting applications. Chapter Four presents circuit design of several blocks of

the controller, followed by the results and discussion of the proposed H-Bridge converter.

Chapter Five presents two designs of SC converter, together with results and discussions. Finally, Chapter Six summarizes the report and discusses some future works.

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CHAPTER 2: LITERATURE REVIEW

2.1 MODELS FOR PV MODULE

2.1.1 SINGLE DIODE EQUIVALENT MODEL FOR PV CELL

It is necessary to derive circuit model that is equivalent to the PV module to simulate the performance of the PV energy harvesting and find its maximum power point. This equivalent circuit model must be able to define the entire I-V relationship of the PV cell with high accuracy. One simplest and common use is the single diode model. From the physical principles of the PV module, we can derive the equivalent circuit [2.1-3]:

Figure 1 Single Diode Equivalent Circuit Model

Using Kirchhoff's current law, the I-V characteristic of the equivalent circuit in the figure 1 can be derived:

$$I_{PV} = I_L - I_D - \frac{V_{PV}}{R_{SH}}$$

Equation 1

In which, I_L represents the current generated by light absorption, I_D represents the current lost due to recombination and R_{SH} represents shunt resistances that cause losses.

The shunt resistance is large, so it usually can be neglected [2.4].

The light-generated current

$$I_L = \frac{\phi}{\phi_{REF}} [I_{SC_REF} + \mu_{ISC}(T_C - T_{C_REF})]$$

Equation 2

Using Shockley equation for ideal diode:

$$I_D = I_O \left[\exp \left(\frac{V_{PV} + I_{PV} R_S}{\alpha} \right) - 1 \right]$$

Equation 3

The diode reverse saturation current:

$$I_O = \frac{I_{L_REF}}{\exp \left(\frac{V_{OC_REF}}{\alpha_{REF}} \right) - 1} \left(\frac{T_C}{T_{C_REF}} \right)^3 \exp \left[\left(\frac{N_S \epsilon_{Si}}{\alpha} \right) \left(1 - \frac{T_{C_REF}}{T_C} \right) \right]$$

Equation 4

where,

$$\alpha = \frac{N_S n k T_C}{q} = \alpha_{REF} \frac{T_C}{T_{C_REF}}$$

Equation 5

$$\alpha_{REF} = \frac{\mu_{VOC} T_{C_REF} - V_{OC_REF} + N_S \varepsilon_{Si}}{\frac{T_{C_REF} \varepsilon_{Si}}{I_{L_REF}} - 3}$$

Equation 6

In these equations, V_{OC_REF} , V_{MP_REF} , I_{L_REF} , I_{SC_REF} , ϕ_{REF} , μ_{VOC} and μ_{ISC} are reference parameter at reference conditions. These parameters are usually provided by manufacturers and included in the PV module packages [2.5].

The nomenclature of symbols in these above equations is tabulated in table 1:

Table 1 Nomenclature of the PV Model

NOMENCLATURE	
V_{PV}	PV output voltage (V)
I_{PV}	PV output current (A)
I_L	Light-generated current (A)
I_{L_REF}	Light-generated current at reference condition (A)
I_D	Diode current (A)
I_O	Diode reverse saturation current (A)
R_S	Series Resistance (Ω)
R_{SH}	Shunt Resistance (Ω)
ε_{Si}	Band gap of Silicon (1.12 eV)

α	Function of temperature
α_{REF}	Function of temperature at reference condition
T_C	Ambient temperature (K)
T_{C_REF}	Reference ambient temperature (K)
ϕ	Irradiance (W/m ²)
ϕ_{REF}	Reference irradiance (W/m ²)
I_{SC_REF}	Short-circuit current at reference condition (A)
V_{OC_REF}	Open-circuit voltage at reference condition (V)
V_{MP_REF}	Maximum power point voltage at reference condition (V)
μ_{VOC}	Temperature coefficient of the open-circuit voltage (V/K)
μ_{ISC}	Temperature coefficient of the short-circuit current (A/K)
N_S	Number of PV cell in series of a PV module
n	Diode ideality factor
k	Boltzmann constant (1.381 x 10 ⁻²³ J/K)

q	Electron charge constant (1.602×10^{-19} C)
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2.1.2 PV MODEL CHARACTERISTIC

A test bench (in figure 2) was set up in order to investigate the electrical behaviors of the IXYS KXOB22-12X1 PV cell.

Figure 2 Test Bench to Study PV Cell

The I-V characteristic and P-V characteristic can be obtained by exposing the PV cell under a constant light power and constant temperature, while varying the output load. The characteristics of the PV cell are shown in the figures 3 and 4.

The red line represents the maximum power point (MPP) of the PV cell.

Figure 3 Voltage vs. Current of IXYS KXOB22-12X1 PV Cell

Figure 4 Power vs. Voltage of IXYS KXOB22-12X1 PV Cell

2.2 MAXIMUM POWER POINT TRACKER (MPPT) TOPOLOGIES

To maximize the energy harvested by a PV system, a MPPT must be implemented. The purpose of implementing MPPT is to ensure that maximum power is extracted from PV module for any environment condition. Theoretically, MPPT is a simple method of operating point matching between PV module and the power converter. However, due to the nonlinearity of the I-V characteristics and the consequence of environmental condition variation, the MPPT system is much more complex. They are classified in to different groups based on their complexity, algorithms and requirements.

This research involves the development of low power application. Power-hungry MPPT methods [2.6] such as fuzzy logic control (FLC), artificial neural network (ANN), particle swarm optimization (PSO), differential evolution (DE), etc.,

which require highly complex algorithms, and intensive hardware, are not suitable.

2.2.1 CURVE-FITTING METHOD

The nonlinear I-V characteristic of PV cell can be construct from the conventional single-diode model. However, it required difficult control that is not suitable for obtaining MPP. Thus, simpler model approaches are created to approximate the MPP. The nonlinear P-V characteristic of PV generator according to [2.7] can be approximated by:

$$P_{PV} = aV_{PV}^3 + bV_{PV}^2 + cV_{PV} + d$$

Equation 7

where a, b, c and d are coefficients determined by examine the large number of values of P_{PV} , V_{PV} , I_{PV} in different time intervals. The accuracy of the approximation depends on the number of samples. Hence, the maximum power can be calculated by manipulating the cubic function:

$$V_{MPP} = \frac{-b\sqrt{b^2 - 3ac}}{3a}$$

Equation 8

The main disadvantage of the curve-fitting method is the requirement of relatively accurate physical parameters of the PV cell and static environmental condition.

2.2.2 OPEN-CIRCUIT VOLTAGE PV GENERATOR

This method approximates the voltage at the maximum power point linearly proportional to its open-circuit voltage. The proportional ratio depends on the characteristics of the PV cell and the climatological condition.

$$k = \frac{V_{MPP}}{V_{OC}} \text{ (constant)}$$

Equation 9

The open-circuit voltage is measured by disconnecting the PV from the system. The maximum power point is then adjusted with the ratio k to the open-circuit voltage. Literately, k ranges from 0.7 to 0.8 for polycrystalline PV cell [2.8].

This method is simple and low-cost implemented. However, its disadvantage is the interruption of PV operation, which causes power loss. Besides, the incorrect measured value of open-circuit voltage, which is sensitive to environmental condition, will lead to the inaccurate maximum power extracted.

To avoid the problem of the interruption of PV operation, open-circuit voltage can be examined from a single test PV cell with similar characteristics and electrically isolated from the PV module. The results will be applied to the main PV module. However, due to mismatching between each cell of the PV module and the test PV cell, the maximum power will not be extracted accurately.

2.2.3 SHORT-CIRCUIT CURRENT PV GENERATOR

Similar to the open-circuit voltage method, this method uses the linear relation between the current at maximum power point and short-circuit current. The proportional ratio also depends on the characteristics of the PV cell.

$$k = \frac{I_{MPP}}{I_{SC}} \text{ (constant)}$$

Equation 10

Approximately, the ratio is around 0.8 for polycrystalline PV. The procedure of measuring short-circuit current and adjusting the maximum power point is similar to the open-circuit voltage method.

2.2.4 PERTURB-AND-OBSERVE (P&O) METHOD

This is one the most common method used in PV energy harvesting due to its easy implementation and accuracy. It obtains MPP by an iterative algorithm. Conceptually, perturbing the PV output voltage V_{PV} and observing the PV output power P_{PV} can locate the maximum power point. The change in direction of the PV output power will then determine the action for the next perturbation.

Doing this, the operating voltage of the PV module is perturbed a small increment ΔV_{PV} perturbs and the resulting change in power ΔP_{PV} is examined. If the change is positive, meaning PV output power increases, the next perturbation of the PV operating voltage should be the same direction of the previous increment. On the other hand, if the change ΔP_{PV} is negative, meaning PV output power goes far

from the maximum power point, the next perturbation should be in the opposite direction of the previous increment. The algorithm is summarized in table:

Table 2 Operation of P&O Method

V_{PV} perturbation	P_{PV} observation	Next V_{PV} perturbation
Increase (+)	Decrease (-)	Decrease (-)
Increase (+)	Increase (+)	Increase (+)
Decrease (-)	Decrease (-)	Increase (+)
Decrease (-)	Increase (+)	Decrease (-)

The maximum power is achieved when $dP_{PV}/dV_{PV} = 0$. It means the PV output power neither increase or decrease with the perturbation of output voltage V_{PV} . The operating point then oscillates around the maximum power point to maintain the steady state.

The main advantage of this method is that it does not require the PV characteristic. The feedback loop automatically adjusts to and oscillates around the maximum power point. Nevertheless, the drawback of the P&O method, according to [2.9], occurs when there is a sudden change in environmental condition. The quick change in irradiance will lead the maximum point moving far away from the operating point. The P&O method is generally slow. It takes a long time to react and requires multiple steps to move from a maximum power point to another maximum power point. Thus, this method is unsuitable for application operating under rapidly changing environmental conditions.

Although larger incremental step size can provide faster tracking, it causes worse oscillation. Consequently, it results unnecessary power loss and inaccurate maximum power point. To provide faster tracking speed and small oscillation, variable step size algorithm can be a solution [2.10].

2.3 POWER MANAGEMENT DEVICES

2.3.1 OVERVIEW OF POWER MANAGEMENT DEVICES

The increasing demand for more compact and power efficient portable devices has driven the development of system-on-chips (SOCs). Benefiting from the technology scaling, SOC (e.g. ARM-based Apple A SOC and Samsung Exynos SOC) integrate the central processing units (CPUs), graphic processing units (GPUs), memory, wireless communications modules (such as NFC, WIFI, 4G, Bluetooth, GPS) and most of the other key components that make the device function [2.11]. Reducing the power consumption in such complex system is a challenging and on-going research topic. One of the most well-established and popular used power reduction techniques today is the dynamic voltage scaling and dynamic frequency scaling (DVFS) for digital circuits. The power consumed by the embedded system can be reduced by lowering the frequency and/or voltage of the CPUs and attached modules. Specifically, The DVFS technique reduces the dynamic power consumption, which is given by [2.12]:

$$P_d = \sigma CV^2 f_{sw}$$

Equation 11

, where σ is the activity factor, C is the collective switching capacitance, V is the supply voltage and f_{sw} is the switching frequency.

In a same SOC, there are different modules performing different functionalities and requiring different power supply levels. To optimize the overall power consumption of the whole system, DVFS techniques can be apply independently to each individual module. The more functional of the system, the more and more bulky and complex power management unit is required with hard-to-integrate passive components (e.g. capacitors and inductors). Hence, as more functionalities continue to be integrated, generating an increasing number of independent power supply levels becomes costlier and more challenging and it requires more power supply pins and more off-chip passive components.

Figure 5 Typical Power Management Unit for SOC.

Figure 1 shows a typical SOC integrated circuit with power management unit (PMU) in battery-powered portable devices. In order to supply different modules, multiple independent supply voltages are generated by PMU from a single main battery. These voltage level can be either lower or higher than the battery supply voltage. They can be monitored and adjusted dynamically depending on the real-time performance and requirements, plus the main supply condition. A good solution to achieve high power conversion efficiency is using switching mode power converter.

2.3.2 LINEAR REGULATOR

Linear regulators have been popularly used in power management circuit system. They are suitable for noise sensitive applications such as analog and RF circuits. The most popular linear regulator is low drop-out regulator (LDO) [2.13,14]. It usually includes an output capacitor, a pass transistor, a resistive feedback voltage divider and an error amplifier. The pass transistor acts like a variable resistor. The difference between the feedback output voltage and voltage reference is sensed by the error amplifier. The output of the amplifier then adjusts the on resistance of the pass transistor to regulate the output voltage accordingly. The output value is calculated as:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) V_{REF}$$

Equation 12

Figure 6 A Typical LDO

As current is continuously drawn from the input via the linear regulator, the output noise is relatively low. It is much lower as compared to switching power converter. On the other hand, fast transient response can be achieved by using high loop gain bandwidth linear regulator. However, the back drawn of the linear regulator is the voltage drop between input and output. The pass transistor acts like variable resistor, which draws current continuously from the input supply. Thus, the output voltage generated by linear regulator can only be lower than the input voltage. Therefore, linear regulator is not suitable for the applications that require wide range of output voltage. The maximum achievable efficiency is:

$$\eta_{MAX} = \frac{V_{OUT}}{V_{IN}}$$

Equation 13

Linear regulator also has the advantage of low area cost as compared to other power converters. It usually requires a few simple passive components for energy transfer. However, in order to maintain system stability and reduce undershoot as well as overshoot during load transients, a large capacitor is needed. Therefore,

some new recent researches have proposed capacitorless LDO [2.15-17], which do not require these large output capacitors. With the elimination of output capacitors, capacitorless LDO have the potential of on-chip fully integrating. It is however a challenging topic and attracts a lot of researchers nowadays.

2.3.3 SWITCHING INDUCTOR DC-DC CONVERTER

Inductor-based DC-DC converter has dominated the designs of switching power converter in recent years [2.28-20]. In this research, second-order switching DC-DC converter is considered due to its low component count. Theoretically, the switching-inductor DC-DC converter can achieve 100% conversion efficiency. According to the input and output relationship, there are various topologies of switching DC-DC converter such as buck converter, boost converter and buck-boost converter.

2.3.3.1 BUCK DC-DC CONVERTER

A typical buck DC-DC converter is shown in Figure 6. It consists of two power switches and one inductor. The buck converter operates in two phases and regulates output voltage that is higher than input voltage. The output voltage can be adjusted by changing the duty cycle D of the power switches. The relationship between input and output voltage can be calculated as:

$$V_{OUT} = DV_{IN}$$

Equation 14

Figure 7 Schematic of Buck Converter

2.3.3.2 BOOST DC-DC CONVERTER

A typical boost DC-DC converter is shown in Figure 7. It consists of two power switches and one inductor. The boost converter also operates in two phases. However, its output voltage is lower than the input voltage. The output voltage is also controlled by the duty cycle D of the switches. The relationship between input and output voltage can be calculated as:

$$V_{OUT} = \frac{1}{1-D} V_{IN}$$

Equation 15

Figure 8 Schematic of Boost Converter

2.3.3.3 BUCK-BOOST DC-DC CONVERTER

A common buck-boost converter is four-transistor architecture. It consists of four power switches connecting to one inductor. It also operates in two phases. The relationship between input and output voltage can be calculated as:

$$V_{OUT} = \frac{D}{1-D} V_{IN}$$

Equation 16

Figure 9 Schematic of Four-Transistor Buck-Boost Converter

As compared to the two previous topologies, the four-transistor buck-boost topology is more favorable due to its flexibility. It can operate both bucking and boosting mode by adjusting the duty cycle D . The output voltage can be regulated to be higher or lower than the input voltage. However, the buck-boost converter also has some disadvantages.

Firstly, it requires two additional power transistors, resulting a higher component count. As more power transistors are needed, power switching loss are much higher. As a result, the overall conversion efficiency is lower than the two previous topologies. Besides, the four-transistor buck-boost converter has higher

average inductor current and current ripple. It further degrades the overall conversion efficiency.

To avoid the disadvantages of the four-transistor buck-boost converter, the two-transistor buck-boost converter [2.21] can be used. The relationship between input and output voltage of this buck-boost converter is like the four-transistor topology. By using only two power transistors, this converter can achieve lower switching power loss and higher transistor utilization rate. Consequently, the overall conversion efficiency is higher. In addition, it also has the same component count with the buck and boost converter.

However, the two-transistor buck-boost converter has the same high average inductor current and current ripple as the four-transistor converter. Thus, its conversion efficiency is also not as high as the buck and boost converter. On the other hand, the switching node V_L is greater than the other topologies. It leads to a higher switching loss. In addition, the input and output voltage have the different potential. As a result, the input voltage must operate on the output voltage, when output negative polarity is tightening to ground. Lastly, as input voltage stands on output voltage, the maximum voltage across the power transistors is higher. There is a voltage stress of $V_{IN} + V_{OUT}$ instead of V_{IN} or V_{OUT} as usual.

Figure 10 Schematic of Two-Transistor Buck-Boost Converter

2.3.4 SWITCHED CAPACITOR CONVERTER

Switched capacitor converter are another trending type of switching power converter. It makes use capacitors instead of inductors as a device for energy transferring [2.22-24]. Switched capacitor converter has been used widely for electronic applications. Recently, it is found that switched capacitor is a potential solution for self-powered portable devices for IOT application [2.25-27].

Figure 11 Schematic of 1/2 Switched Capacitor Converter

A sample switched capacitor is shown in the figure 11. It has the fixed conversion ratio of $\frac{1}{2}$. The converter consists of four power switches and a flying capacitor. This switched capacitor converter also operates in two phases. In the first phase,

two PMOS switches are on and two NMOS switches are off. The flying capacitor is charged to $V_{IN} - V_{OUT}$. In the second phase, two PMOS switches are off while two NMOS switches are on. The flying capacitor is discharge to V_{OUT} . Using charge redistribution method, V_{OUT} is equal to $\frac{1}{2} V_{IN}$. Theoretically, the maximum achievable conversion efficiency of switched capacitor converter is calculated by:

$$\eta_{MAX} = \frac{V_{OUT}}{M_{NL} V_{IN}}$$

Equation 17

where M_{NL} is the voltage conversion ratio under no-load condition. The conversion efficiency of the switched capacitor converter is equal to that of the linear regulator scaled down by the converter conversion ratio.

2.3.5 COMPARISON

A comparison of the linear regulator and switching converters is summarized in the table 3. Each topology has its own advantages and disadvantages.

Linear regulator has the advantage of smallest occupied area, lowest output noise and fast output transient. However, it output voltage swing is small due to the limitation of the pass transistor. Linear regulator can only regulate output voltage that is smaller than the input voltage. Its conversion efficiency is also limited by the voltage drop across the transistor, causing by significant conduction loss.

Switching power converter offer the capability to regulate output voltage which can be either lower or higher than the input voltage. Both types of switching

converter have high output noise and slow transient response. Due to high component count, they occupy large area and difficult to be fully integrated. Switching inductor power converter can achieve the highest power efficiency. In addition, switching inductor converter offer the flexibility to construct multiple-input multiple-output converter. Consequently, it is suitable for low power application and energy harvesting.

Table 3 Comparison of Typical Power Converter

Type	Linear Regulator	Inductor- Based	Capacitor- Based
Size	Small	Large	Large
Output Voltage	$V_{OUT} < V_{IN}$	$V_{OUT} < V_{IN}$ $V_{OUT} > V_{IN}$	$V_{OUT} < V_{IN}$ $V_{OUT} > V_{IN}$
Noise	Low	High	High
Transient Response	Fast	Slow	Slow
Conversion Efficiency	Low	High (100%)	Medium

2.4 MULTIPLE INPUT & MULTIPLE OUTPUT TOPOLOGIES

Different single-input single-output (SISO) DC-DC converter topologies have been briefly discussed in the previous section. Each SISO converter can

efficiently deliver power from a single input source to a single output. In order to deliver power from multiple inputs (MI) to multiple outputs (MO), multiple of these SISO converters can be used. However, it requires significant amount of hardware resource. Thus, single multiple-input multiple-output (MIMO) technique is implemented by reusing some of the common components of these SISO converters.

2.4.1 MULTIPLE INPUT

The most common input sources for low-power application is battery. It provides reliable and stable output power. Nevertheless, with the shortage of energy in the future, more and more research on renewable energy are developed. There are variety of clean and available renewable sources such as solar, wind, tidal, kinetic vibration and electromagnetic energy. Some of the renewable energy sources can be directly harvested and delivered to the output application. However, these renewable energy sources are unstable and greatly depend on environmental condition. To effectively harvest these energy sources, they multiple types of energy sources should be used concurrently with conventional power supplies. Using the combination of renewable energy sources and conventional power supplies such as battery can provide stable power supply while reduce the heavy reliance on any energy sources.

The easiest and most straightforward way to build an MI converter is to have multiple of conventional single-input converters and their outputs are connected in parallel [2.28]. The disadvantages of these MI converters are the additional

hardware components: inductor, diode, power switches, etc. In order to reduce the number of components, some common parts of a conventional converter have been reused. Single-inductor multiple-input (SIMI) converter, which has only one inductor, is used to deliver power from multiple input sources. Normally, multiple input sources are connected in parallel. Each of these sources is separated by input switches to prevent shorting inputs source to others. Time-multiplexing control scheme must be used to ensure only one of the input sources is used at any time [2.29].

Figure 12 Schematic of SIMI Converter

2.4.2 MULTIPLE OUTPUT

With the development of technologies and human requirements, the intention of creating electronic devices with multi-function has been increased. It leads to the requirement of multiple stable voltage supply. Even in a single-function electronic device, multiple power supply levels are required. The simplest method is to implement multiple power converters. Each of them regulates and

provides power to each voltage supply level. However, it increases the demand for area, cost and hardware requirement.

Single-inductor multiple-output (SIMO) converter has been proposed to minimize the hardware used, while provide multiple output levels. Similar to the SIMI converter, power switches with time-multiplexing algorithm are used to deliver power to each of the output levels. The first SIMO converter was proposed by Goder and Santo [2.30] in 1997.

Figure 13 Schematic of SIMO Converter

2.5 SWITCHING CONTROLLER

2.5.1 DEAD-TIME CONTROL AND ZERO-CURRENT DETECTOR

Figure 14 Boost DC-DC Converter Circuit for Observing the Characteristics Under DCM Operation

A boost converter operating in discontinuous conduction mode (DCM) is shown in Figure 14. Firstly, the NMOS power switch turns on to charge the inductor with the current I_L . After NMOS is switched off, the current I_L will continue flow through the body diode of the PMOS for a short period, which is called dead time period. Afterward, the PMOS transistor turns on and the inductor current I_L will be discharge to the load. During PMOS conducting, voltage at the switching node V_X can be expressed with respect to output voltage, inductor current and the on resistance of the PMOS power switch:

$$V_X = V_{OUT} + I_L r_{PMOS}$$

Equation 18

When the inductor current reaches zero, the PMOS power switch must be turned off to prevent negative current flowing through the inductor. Ideally, V_X is equal to output voltage when the inductor current reaches zero. By observing the

waveform of V_X , we can determine the performance of the converter. There are several cases categorized by observing V_X (figure 15):

Ideal switching: After NMOS turns off, the ideal case happens when PMOS is turned on exactly at the time when the voltage across it is zero and it is turned off exactly when the inductor current reaches zero. After both NMOS and PMOS are turned off, V_X will oscillate until the next switching cycle.

PMOS turns on early: In this case, there is a period that both PMOS and NMOS conduct. This is the worst case since the output voltage is shorted to ground. Shoot-through current between output voltage and ground will cause severe power loss and damage to the power switches and other control circuits. It is dangerous and control circuit must be designed to prevent the circuit from this situation.

PMOS turns on late: Dead time is necessary to eliminate shoot-through current. However, when the dead time exceeds the sufficient amount, high voltage across the PMOS may cause the body diode to start conducting. Hence, there will be a great conduction loss due to the conducting body diode. Practically, the gate driver delay also contributes to the dead time.

PMOS turns off early: Theoretically, the PMOS should be turned off when the inductor current reaches zero. However, if the PMOS is turned off too early, there will be remaining charge and current from the inductor. This remaining current will flow through the body diode of the PMOS and thus causes extra conduction loss. In this case, V_X is overshooting with a value higher than output voltage.

PMOS turns off late: Due to the delay introduced by the control blocks, the PMOS may be turned off too late. This causes the inductor current becomes negative. The reverse current flows through the body diode of the NMOS and thus causes conduction loss. The longer the amount of delay after inductor current reaches zero, the higher the reverse current peak. In this case, V_X is undershooting with a value below ground.

Figure 15 Waveform of Different Gate Switching Operations

(a) Ideal Switching. (b) PMOS is turned ON too late. (c) PMOS is turned OFF too late. (d) PMOS is turned OFF too early

2.5.2 PULSE-WIDTH MODULATION

A boost converter with a single loop control is shown in Figure 16. The duty cycle of the power switch is controlled by error voltage derived from output voltage and reference voltage.

Figure 16 Boost Converter with Voltage-mode Control PWM

The small signal model of this boost converter can be redrawn in Figure 16 with various stages. T_P is the transfer function of the power stage of the boost converter. T_{PWM} is the transfer function of the PWM generator. T_C is the transfer function of the error amplifier. T_F is the transfer function of the feedback attenuator. M_V is the input-to-output transfer function of the boost converter. Z_O is the output impedance. v_I , v_F , v_C , v_E , v_{REF} , i_O is the ac components of the input voltage, feedback voltage, output voltage of controller, error voltage, reference voltage and output current respectively. To simplify the model, we set $v_I=0$, $v_{REF}=0$ and $i_O=0$.

The general transfer function of the boost converter is:

$$T(s) = T_F(s)T_C(s)T_{PWM}(s)T_P(s)$$

$$= \frac{v_E(s)}{v_O(s)} \times \frac{v_C(s)}{v_E(s)} \times \frac{d(s)}{v_C(s)} \times \frac{v_O(s)}{d(s)}$$

Equation 19

Transfer function of power stages:

The small-signal model of the PWM boost converter is shown in Figure 17:

Figure 17 Small-signal Model of Boost DC-DC Converter

From the small-signal model, the transfer function of the power stage of the PWM boost converter can be derived:

$$T_P = \frac{v_O(s)}{d(s)} \approx \frac{V_O}{1-D} \times \frac{\left(1 + \frac{s}{\omega_{ZN}}\right) \left(1 - \frac{s}{\omega_{ZP}}\right)}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2}$$

Equation 20

in which,

$$\omega_{ZN} = \frac{1}{Cr_C}, \quad \omega_{ZP} = \frac{(1-D)^2 R_L - r_L}{L}$$

$$\omega_o = \sqrt{\frac{(1-D)^2 R_L + r_L}{LC(R_L + r_c)}}, \quad Q = \frac{\sqrt{LC(R_L + r_c)[(1-D)^2 R_L + r_L]}}{L + C[r(R_L + r_c) + (1-D)^2 R_L r_c]}$$

Equation 21

Transfer function of PWM:

The PWM generator is separately shown in Figure 18. Generally, it is an open-loop operational amplifier operating as a comparator. The control signal and ramp signal are applied to the non-inverting and inverting inputs of the comparator, respectively. As the control voltage V_C changes with the amount ϑ_C , the duty cycle D also changes with the amount d . According to the ramp function, the voltage-to-duty cycle transfer function of the PWM generator is:

$$T_{PWM} = \frac{d(s)}{v_c(s)} = \frac{D}{V_C} = \frac{1}{V_{SAW_M}} = \frac{1}{T_s \tan \gamma} = \frac{f_s}{\tan \gamma}$$

Equation 22

Figure 18 PWM Generator

(a) PWM Generator Circuit. (b) Waveform of the PWM Generator.

Transfer function of the feedback network:

The feedback network is simply a voltage divider. The transfer function of the feedback system is:

$$T_F = \frac{v_F(s)}{v_O(s)} = \frac{R_B}{R_A + R_B} = \alpha$$

Equation 23

Error amplifier:

The error amplifier is also called a compensator. It generates the control signal for the PWM by examining the error from the feedback output voltage and a reference voltage.

If the system is uncompensated, which means $T_C(s)=1$. The general transfer function of the PWM boost converter is:

$$T(s) = \frac{\alpha V_O}{V_{SAW_M}(1-D)} \times \frac{\left(1 + \frac{s}{\omega_{ZN}}\right) \left(1 - \frac{s}{\omega_{ZP}}\right)}{1 + \frac{s}{Q\omega_O} + \left(\frac{s}{\omega_O}\right)^2}$$

Equation 24

The system has two left-hand-plane (LHP) poles, one left-hand-plane zero and one right-hand-plane (RHP) zero. As the system has a RHP zero, it is unstable. The LHP zero is independent of the duty cycle, while the RHP zero depends on the duty cycle. When the duty cycle increases from 0, the RHP zero decreases and starts moving to the LHP as $D>1$. The system has the natural frequency ω_O and the quality factor Q .

Type I Compensator:

Type I controller introduces only one pole, which locates at origin to give pure integral action. Figure 19 show a typical type I controller.

The transfer function of a type I controller is:

$$T_{C_I}(s) = \frac{1}{sR_1C_1}$$

Equation 25

Type I controller has a gain that drops with frequency by a rate -20dB per decade and -90° phase shift.

Figure 19 Type I Compensator

Type II Compensator:

To further improve system's response, reduce dc error and sensitivity of the closed-loop gain, type II compensator is used. A type II compensator has an additional RC branch to flatten the gain and improve the phase response in the mid-frequency range. The type II controller is capable to provide extra 90° phase boost. A type II controller is shown in Figure 20:

Figure 20 Type II Compensator

The type II controller introduces a pole at origin and a single pole zero pair. The transfer function of the type II controller is:

$$T_{C_II}(s) = \frac{1}{R_1(C_1 + C_2)} \times \frac{1 + sC_1R_2}{s \left(s + \frac{R_2C_1C_2}{C_1 + C_2} \right)}$$

Equation 26

Type III Compensator:

In case of the type II compensator cannot provide enough phase margin, type II compensator is used to keep the system stable. Type III (shown in Figure 21) enhances the design by adding an additional zero-pole pair. The transfer function of type III compensator is:

$$T_{C_III}(s) = \frac{1}{R_1(C_1 + C_2)} \times \frac{1 + sC_1R_2}{s \left(s + \frac{R_2C_1C_2}{C_1 + C_2} \right)} \times \frac{1 + sC_3(R_1 + R_3)}{1 + sC_3R_3}$$

Equation 27

Figure 21 Type III Compensator

The type III compensator can theoretically provide up to 180° phase boost to the system and extend the bandwidth of the system.

2.6 ANALOG & DIGITAL CONTROLLER

Since the immersion of digital signal processor (DSP) and proportional integral derivative (PID), digitally assisted controlled DC-DC converter has increased the popularity with the wide range of application [2.31-33]. The digital controllers have the advantages of simplicity, high programmability with capability to implement complex control algorithms. Besides, digital controllers also have the high portability between semiconductor technologies.

The digital controller for DC-DC converter often requires analog-to-digital converter (ADC) to quantize the voltage and current values for processing in the digital domain [2.34]. The duty cycles of the switching signal are normally generated by a counter-based digital pulse-width modulation (DPWM). The DPWM requires tremendously high frequency clock to achieve sufficient resolution. Therefore, hybrid DPWM, which combines both counters and delay line are usually preferred to reduce the high frequency requirement [2.35,36].

On the other hand, analog controllers require fewer amounts of components. Therefore, analog controllers consume lower power and obtain higher resolution as compare to the digital controllers. However, the analog controllers are not programmable and lack of controllability. Hence, they need to be extremely well designed according to the specific applications. Moreover, analog control algorithms are not easily ported between different technologies.

The characteristics of both analog and digital controllers are summarized in Table 4. This research focuses on the high computation power, while trying to reduce the disadvantages of hardware requirement and power consumption of the digital controllers. The use of digitally assisted controller allows us to achieve high dynamic efficiency optimization over a wide range of operating mode of the PWM-PFM combination technique.

Table 4 Advantages and Disadvantages of Analog vs. Digital Controller

	Advantages	Disadvantages
Analog Controller	<ul style="list-style-type: none"> • Low component requirement • Low power consumption • Continuous duty ratio, no resolution issue 	<ul style="list-style-type: none"> • Not programmable • Low computation power • Low portability between technologies • Analog circuits need to be extremely well precise
Digital Controller	<ul style="list-style-type: none"> • High programmability • Simplicity in design • High computation power for complex functions • High portability between technologies 	<ul style="list-style-type: none"> • High component requirement • High power consumption • Discrete duty ratio, require high frequency clock to obtain good resolution

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CHAPTER 3: PROPOSED DIGITALLY- ASSISTED H-BRIDGE DC-DC CONVERTER FOR PV ENERGY HARVESTING SYSTEM

3.1 BACKGROUND

Energy harvesting allows the electronic application to capture and be powered for its entire lifecycle. With the development of IOT era, electronic applications and devices has been expanded in human life such as remote sensor or wearable medical devices. Modern remote sensors usually consist a lot of digital circuit. These digital circuit should be operating at low voltage supply, which is around $0.8 - 1$ V. Some remote sensors require very low power consumption. These devices usually have wake-up function, meaning that they only awake or work improved sensitivity when there is a demand. Otherwise, the devices are in battery-saving inactive mode. Indoor PV energy is a suitable solution to supply these very low power IOT application. However, as the output power of the PV cell is susceptible to the lighting intensity, energy storage devices, such as supercapacitor or battery is required to provide fast and sufficient energy.

3.2 OVERALL DESIGN

In order to harvest PV power for the IOT applications, a H-bridge single-inductor dual-input dual-output DC-DC converter (HBDIDO) is proposed. The converter uses the multiple-input and multiple-output power converter architecture. It has the efficient advantage that extracted power can be delivered to the core output load within only one conversion step.

The overall architecture of the proposed HBDIDO is presented in figure. As shown, the HBDIDO consists of only one single inductor L connected between PV source, backup storage and output load via six different power switches (P_1 , P_2 , P_3 , P_4 , N_1 , N_2). The input port of the inductor is connected to the PV source, via P_1 , for energy harvesting purpose. The output port of the inductor is to supply power to the 1.0 V core supply rail, via P_2 . There is an input-output pair connected to the backup storage, which is a super-capacitor, via P_3 and P_4 .

In normal operation mode, harvested power is delivered directly to the output load via a one-stage boost converter forming by P_1 , P_2 , N_1 , N_2 and L . When the harvesting energy exceeds the loading requirement, the surplus energy from the PV source is delivered and stored to the supercapacitor through a power converter forming by P_1 , P_4 , N_1 , N_2 and L . On the other hand, when the PV energy is depleted by the heavy output load, the power required by the output rail will be supplied from the backup capacitor.

Therefore, the operation can be divided into three modes (and its digital code M_1M_0):

- (i) PV to Load (11)
- (ii) PV to Backup (10)
- (iii) Backup to Load (01)

As the PV source power greatly varies by the surrounding environment, an automatic MPPT is necessary to track and lock the PV operation at its MPP. A digital-controlled feed-forward MPPT is implemented with a low-power power

estimator. Perturb-and-observe topology is used for its simplicity, precision and low power consumption.

The proposed system operates in discontinuous conduction mode (DCM) to minimize the power consumption of the controller. The converter regulates the output voltage and achieves maximum power extracted by a combination of pulse-width modulation (PWM) and pulse-frequency modulation (PFM).

The controller is mainly designed in digital to make use the advantage of high computation power. All the values of on time for power switches are store and manipulated in digital domain. Digital blocks are powered by low-voltage supply of 1V to further reduce the switching power losses. Current-starved and power-gating techniques are used for these digital blocks for reducing shoot-through current as well as shutting down these blocks when not in use.

Figure 22 Overall Block Diagram of the HBDIDO

3.3 CONTROL SCHEME

As shown in figure 22, the main control circuit of the HBDIDO consists of a Clock Generator, two Voltage Comparators for input and output, an MPPT, a Mode Selector, a Frequency Multiplexer, a Dead-Time Controller (DTC), a Zero-Current Detector (ZCD) and Gate Drivers.

In one switching cycle, although the HBDIDO has two inputs and two outputs, only one input and one output are activated. It is achieved by turn on and off six power switches accordingly. The selection of power switches is determined by the mode selector, which uses the output information of the output voltage comparison.

The respective gate drivers will then drive the selected power switches. The power converter is designed to operate with adaptive ON time controller. The ON time duration is stored and manipulated in digital domain before going to a digital pulse width modulation (DPWM). The DPWM will then generate a control signal for the drivers to drive these power switches on the first phase of the power conversion. The second phase of the power conversion will be control by the OFF time signal, which is generated by the dead-time controller (DTC) and zero-current detector (ZCD). The DTC and ZCD optimize the conduction loss from the second phase of the conversion. Specifically, DTC prevents shoot-through current from happening. While ZCD turns off the switches when the inductor current reduces to zero.

Perturb-and-observe method is used to lock the PV cell operating near the MPP regardless of illumination conditions. Step-by-step, it locates the MPP by perturbing the PV voltage V_{PV} and observing the PV power P_{PV} . In this proposed system, PV power P_{PV} is approximated by a novel power approximation circuit. Then, the power and voltage information are fetched in to a circuit to compare with the past value. The output of the power comparison determines the change

of the ON time of the power switches, which affect the change of V_{PV} . Consequently, the PV module will oscillate around its MPP.

For the power converter, every switching cycle is initiated and controlled by the internal clock, CLK. The internal clock is generated by the frequency modulation via the output comparison. Prior to the triggering of CLK, all analog and digital components, rather than the oscillator, are to be switched off to reduce quiescent power consumption. Although power consumptions from power switches are avoided in DCM mode by skipping the pulse, there are still power consumed by the controller circuit. Therefore, to further minimize the power consumption, part of the controller can be performed with slower speed, or only when necessary. For instance, during light load condition, voltage variation is low. The controller can perform less frequently as compared to the case of high load condition. Operating at lower frequency can significantly reduce the switching loss from these digital control circuits. A frequency modulator is designed to detect high/low conditions and adjust the main operating clock.

Although frequency modulation provides an efficient solution with the variation of load, changing frequency will affect the operating at MPP. It results a change of the output impedance of the PV cell. Thus, it drags the operating point relatively far from the MPP. Another circuit is proposed to rapidly estimate and bring the PV operating to its new MPP using square-root method.

3.4 PROPOSED DESIGN

3.4.1 OPERATING MODES AND SELECTION

Different kinds of sensors are widely used in smart devices of IOT. Some digital sensors with digital circuits usually require a voltage of 1 V or less to minimize the power consumption. This proposed converter system aims to regulate PV voltage of 0.4-0.7 V to supply these digital sensors. The four abovementioned operating modes is determined by the output comparisons and the mode selector.

There are two voltage reference levels for the output voltage: upper threshold V_{TH_U} and lower threshold V_{TH_L} . In normal condition, meaning V_L is between the upper threshold V_{TH_U} and lower threshold V_{TH_L} , a standard boost converter is used to regulate PV voltage to output load. In the condition of heavy load, if V_L drops below the lower threshold V_{TH_L} , backup supercapacitor will be served as the input source to provide immediate sufficient power to the load. The backup capacitor will be used to bring the output voltage V_L to the upper level V_{TH_U} . On the other hand, the light load mode is triggered when V_L surpasses V_{TH_U} . Excessive energy will be delivered and stored in the backup capacitor.

Figure 23 State Diagram of the Energy Harvesting System

Figure 24 Output Voltage Operating Waveform

The mode selector is designed by the circuit:

Figure 25 Output Voltage Comparison and Mode Selector

As we see, when V_L is higher than both the threshold voltages, the mode (M_1M_0) is 10, indicating the stage where harvested power is delivered and stored to the backup capacitor. Until V_L drops below V_{TH_U} but is still higher than (V_{TH_L} $V_{TH_U} > V_L > V_{TH_L}$), M_0 turns 1 but M_1 remains 1. The operating mode now is

PV to load (11). When V_L drops further to below V_{TH_L} , M_1 turns 0 and M_0 remains 1. The operating mode now is backup storage to load (01). The table summarizes the operating modes:

Table 5 Operating Modes

Mode	Digital Code
PV to Load	11
PV to Backup	10
Backup to Load	01

3.4.2 MAXIMUM POWER POINT TRACKER

3.4.2.1 MPPT ALGORITHM

As discussed in Chapter 2, maximum power point tracking is the most critical issue in energy harvesting system. As PV module is sensitive to its surrounding environment, it is necessary to locate and lock its operations so that maximum energy can be harvested. A P-V characteristic of a PV cell is shown:

Figure 26 P-V Characteristic of a PV Cell

In the figure 26, the MPP of the PV cell with different illumination level (Lux) is shown in the dotted line. The MPP is non-linear against the output voltage of the PV cell. In this proposed system, P&O method is used to obtain MPP. Conceptually, it locates the MPP by perturbing the PV output voltage V_{PV} and observing the PV output power P_{PV} .

In the boost mode, the V_{PV} can be adjusted by changing the output impedance of the PV cell. In addition, the output impedance of the PV cell is related to ON time of the power switches. The bellow figure shows the relationship between the PV voltage and power against the duty cycle of the boost converter.

Figure 27 Output Voltage and Power vs. Duty Cycle of PV Cell

From the plot, it can derive that the output voltage of the PV cell is non-proportional to the duty cycle. Specifically, increasing the duty cycle leads to the decrease of PV output voltage V_{PV} while decreasing the duty cycle increases the PV output voltage V_{PV} . Consequently, the algorithm shifts to perturbing the converter duty cycle and observing P_{PV} .

In stable condition, the P&O method can be classified into four cases, according to the changes (new and old values) of V_{PV} and P_{PV} . It is shown:

Figure 28 Four P&O MPPT Cases

The direction of changing in V_{PV} , P_{PV} and then duty cycle can be constructed in the following table:

Table 6 Summary of P&O Algorithm

Case	V_{PV}	P_{PV}	Duty Cycle	Remark
(a)	+	+	-	Need to increase V_{PV}
(b)	-	-	-	Need to increase V_{PV}
(c)	-	+	+	Need to decrease V_{PV}
(d)	+	-	+	Need to decrease V_{PV}

Figure 29 State Diagram of P&O MPPT

3.4.2.2 MPPT CIRCUITS

For the P&O to function, the instantaneous voltage and current of the PV are required for manipulation to determine the increase or decrease of the duty cycle in the subsequent state. However, as mention earlier, to minimize the power consumption, ADC and current sensor are not preferred. Therefore, a novel approach is proposed to approximate the power without using ADC and current sensor. After having the voltage and power profiles of the PV cell, a circuit is implemented to compare it with the previous values to determine the changing on duty cycle. The general block diagram of the MPPT is shown:

Figure 30 Block Diagram of Proposed MPPT

Using H-bridge configuration for the power stage, theoretically, the ON time can be approximate at:

$$t_{on} = \sqrt{\frac{2L}{R_{PV}f}}$$

Equation 28

From the above equation 28, it can be seen that the duty cycle is independent of V_{OUT} . In addition, the energy that is stored in the inductor during the first phase of the boost converter is largest when the converter operating at the MPP. This implies that the inductor current is directly proportional to the output power of the PV. The average inductor current can be approximate as:

$$i_L = \sqrt{\frac{V_{PV}t_{on}}{L}}$$

Equation 29

From the equation, it can be said that we can approximate the PV output power P_{PV} by observing $V_{PV}t_{ON}$ multiplication. Noted that the ON time t_{ON} is stored and

processed in digital domain in an up/down counter and DPWM, which will be discussed in later section.

3.4.2.3 DIGITALLY-ASSISTED POWER APPROXIMATION TECHNIQUE FOR MPPT

A novel power sensing method for MPPT is proposed in the figure 31:

Figure 31 Schematic of Power Approximation Circuit for MPPT

The power approximation circuit consists of a capacitive network with 4 capacitors with geometric progression values, a sampling capacitor and six sampling switches. It operates in three phases. As discussed, the value of ON time is stored in 4-bit digital value D3, D2, D1, D0. These four digital values control the four sampling switches.

In the first phase, all the four sampling capacitors and output capacitor are discharged to ensure that there is no initial charge stored.

In the second phase, the input switch ϕ_1 is closed and output switch ϕ_2 is opened. The PV voltage V_{PV} is sampled into the four sampling capacitors. The amount of charge stored in the sampling capacitor is control by the digital value of D3, D2,

D1, D0. Meaning that, when D is '1', the sampling switch is closed, and vice versa the sampling switch is opened when D is '0'. The total amount of charge that is transferred into four sampling capacitors is:

$$Q_1 = C(D_0 + 2D_1 + 4D_2 + 8D_3)V_{PV}$$

Equation 30

In the third phase, the input switch ϕ_1 is opened and output switch ϕ_2 is closed. All the four sampling switches are also closed, allowing charge sharing between four sampling capacitors and the output capacitor. The total charge in phase three is:

$$Q_2 = 16CV$$

Equation 31

Applying charge redistribution theory, $Q_1=Q_2$:

$$V_{OUT,SAMP} = \frac{D_0 + 2D_1 + 4D_2 + 8D_3}{16} V_{PV}$$

Equation 32

On the other hand:

$$t_{ON} = (D_0 + 2D_1 + 4D_2 + 8D_3)\delta$$

Equation 33

where δ is the fixed minimum step size of the DPWM.

Thus, it is derived that:

$$V_{OUT,SAMP} = \frac{V_{PV}t_{ON}}{16\delta}$$

Equation 34

Therefore, the voltage level stored at the C represents the value of $V_{PVT_{ON}}$, which is the PV power P_{PV} information. After having the current power value, it is compared with the previous value by a dynamic comparator. The output of the comparator will determine the increase or decrease of ON time by one step δ , via an input signal to the UP/DOWN counter.

3.4.3 PULSE SKIPPING AND FREQUENCY MODULATION

In this proposed design, voltage regulation is achieved by transferring energy from PV sources to output load that is low in energy. As the amount of energy stored in the capacitor is reflected by the voltage level, using output voltage comparisons with the reference threshold voltage can determine the operating mode. The converter is controlled using DCM, in which, power switches are activated during a short period within a switching cycle.

Although switching power consumption by the gate driver and power switches are avoided using DCM, the power is still continuously consumed by the controller's circuit. As the controller consists a lot of digital circuits, switching power consumption is high. To minimize the power consumption from the controller, parts of the control circuit should only be turned on when necessary. Meaning that, the voltage variation is slow when the load is in light condition, the converter can be performed with slower frequency as compare to the high-load condition.

In the above discussion, every switching cycle is initiated and controlled by the internal clock CLK. Using alone one fixed switching frequency is inefficient. The converter's controller consumes too much power than its requirements if it operates at the frequency that is faster than the optimum. On the other hand, if the converter operates at the lower frequency than its essential frequency, it is too slow to response to a heavy load condition. As consequence, pulse-frequency modulation is implemented to provide variation of operating frequency based on the input and output high/low condition. Conventionally, PFM (Roy 7.8 7.7) method requires error amplifier to compare output voltage with its voltage reference, then adjusts the operating frequency. This proposed power converter provides discrete frequency modulation. By comparing the output voltage with the reference threshold, the PFM can determine the frequency changes. If output voltage remains below the threshold voltage for three consecutive switching cycles, the frequency will be double to provide fast response to the heavy load. On the other hand, the frequency is halved when the output voltage is higher than the threshold voltage for four consecutive comparisons.

Overall, the operating frequency needs to be increase if the power converter experiences heavy load condition, where power is continuously drawn to the output load. It results the output load voltage fall below its threshold reference. The operating frequency is then doubled to increase the amount of energy drawing from the source and delivering to the output load.

On contrary, when the output load is low, the output voltage will be above their threshold reference for a long time. As such, the converter is in relaxed mode.

The power consumption of the controller can be reduced by halving the switching frequency.

However, changing the operating frequency of the converter results a change of the output impedance of the PV cell. Thus, its operating point is dragged relatively far from the maximum power point. In the boost mode of the HBDIDO, the ON time can be approximate at:

$$t_{on} = \sqrt{\frac{2L}{R_{PV}f}}$$

Equation 35

where R_{PV} is the output impedance of the PV cell.

From the equation 35, to keep the PV output impedance constant, ON time needs to be adjusted according to the change of frequency. It can be derived that doubling the switching frequency will lead to the on-time to decrease by $1/\sqrt{2}$ times while halving the switching frequency will lead to on-time to increase by $\sqrt{2}$ times. Therefore, the pulse-width modulation is modified with a novel pulse-width estimator that can quickly predict and bring the ON time near to the maximum power point.

As mention earlier, the ON time is stored in 4-bit digital domain D3, D2, D1, D0. It can be used to perform multiplication and division to $\sqrt{2}$ in digital domain. However, three extra bits (D-1, D-2, D-3) are added to form a 7-bit digital value. The three additional bits representing the decimal part, which make the generated pulse width more accurate.

In the form of 7-bit binary number, $\sqrt{2}$ and $1/\sqrt{2}$ can be represented by [0001.011] and [0000.110] respectively. A pulse-width estimation circuit is implemented by full adders and half adders. It performs the multiplications of $[D_3D_2D_1D_0 . D_{-1}D_{-2}D_{-3}]$ with [0001.011] and [0000.110].

The pulse-width estimator is shown in the bellow figure:

Figure 32 Proposed Pulse-Width Estimation Circuit

The pulse-width estimator is activated when the frequency changes. When enabled, it generates the new value of $[D_3D_2D_1D_0 . D_{-1}D_{-2}D_{-3}]$ based on the request half/double from the frequency modulation. The first four new bits D_3 ,

D2, D1, D0 is then flushed into the 4-bit up down counter of the DPWM. The up down counter, which is implemented by J-K flip flops, continues counting with the new value of D3, D2, D1, D0. Their up and down signal is determined by the P&O method as discussed earlier.

3.4.4 HYBRID PULSE GENERATOR

Finally, a hybrid pulse generator is used to generate ON time based on the digital value $[D_3D_2D_1D_0 \text{ . } D_{-1}D_{-2}D_{-3}]$. It is implemented by a series multiplexers and delay line. The delay line can be split into two different parts.

The first part is the offset delay, generated by $[D_{-1}D_{-2}D_{-3}]$ with the minimum step size of $\delta/8$. This amount of delay is not affected by the up down counter using for P&O method. Only when there is a need of changing in frequency, the offset delay is adjusted.

The second part is the delay that is generated by $[D_3D_2D_1D_0]$. It has the minimum step size of δ . This delay is controlled by the up down counter using to perturbing V_{PV} .

The overall circuit of hybrid pulse generator is shown:

Figure 33 Schematic of Hybrid Pulse Generator

3.4.5 DEAD-TIME CONTROL AND ZERO-CURRENT DETECTOR

According to the literature review section, by investigating the overshooting and undershooting characteristics of V_x , we can adjust the on-time of the power switches P_3 and N_1 to minimize the extra power losses. The voltage nodes V_{x1} and V_{x2} , which are the switching node of the buck and boost mode of the power converter, are monitored during the rising of the signal of the second phase of the conversion. If the condition of undershoot or overshoot is found, the OFF time (or on-time of the second phase) of the power switches will be increase or decrease accordingly and have effect in the next cycle. The process keeps repeated until no undershoot or overshoot are detected, which means the system had achieved the optimum pulse width and minimum conduction power loss.

The general block diagram of the DTC and ZCD for the case of boost mode (11/PV to Load) is described in the bellow figure. During phase two of the boost

converter, the DTC generates the starting signal, while ZCD circuit generates the stopping signal.

Figure 34 Block Diagram of the proposed DTC and ZCD

Figure 35 Boost Converter Circuit for Observing the Characteristics Under DCM Operation

The V_X sense consists of two parts: overshooting detector and undershooting detector. If the transistor PMOS during phase 2 is turned off late, due to the negative current, V_X is undershooting. In the situation of undershooting, the reverse diode current of the NMOS causes the voltage at V_X around -0.7 V. For that reason, as well as avoiding the propagation delay, the undershooting detector circuit is targeted to trigger as soon as V_X reaches negative 0.6 V.

On the other hand, overshooting involved in two situations: PMOS turns on late and PMOS turns off early. The overshooting detector circuit is aimed to trigger when V_X excess V_{OUT} .

Figure 36 Circuit Diagram of Undershooting Detector

The circuit to detect undershooting is shown in the figure 36. It consists of two transistors (one NMOS and one PMOS) connecting in series. PMOS is in diode-connected form, while the gate of NMOS is biased to a value of $(-0.6 \text{ V} + V_{THN})$, which is close to ground. In normal condition, V_{GS} of the NMOS is higher than V_{THN} , causing NMOS in weak region. PMOS is conducted and V_{US} is pulled to ground. However, when V_X drops below -0.6 V , V_{GS} of NMOS is now higher than its V_{THN} . NMOS starts triggering and pull the middle point to zero. Thus, V_{US} rises to logic high.

Figure 37 Circuit Diagram of Overshooting Detector

The circuit to detect overshooting is shown in the figure 37. It consists of two transistors and a resistor for biasing purpose. In normal condition, PMOS is in

weak region. V_{OS} is pulled to ground through the diode-connected NMOS. The bias current and resistor R_{THP} are used to keep the gate voltage of the PMOS below V_{OUT} an amount of V_{THP} . In the condition of overshooting, V_X is higher than V_{OUT} , the PMOS starts to turn on and pushes the V_{OS} to logic high.

Similar to the previous DPWM for ON-time, the DTC and ZCD also use counters to control the amount of delay from a delay line. The self-calibration algorithm of the DTC and ZCD is shown below. As the DTC has only one side control, when the dead time reaches the optimum amount, it will keep oscillating between that optimum dead time. Meaning that, if there is no need to count for providing longer delay, the ZCD will count down one step.

Figure 38 Flow Diagram of DTC

Figure 39 Flow Diagram of ZCD

The resolution of the ZCD and DTC are very critical in power losses. The proposed ZCD is controlled by an 8-bit counter and a delay generator with minimum step size 8ns; while the DTC is controlled by a 6-bit counter and a delay generator with minimum step size 125ps. The design and performance of these counters and delay generators is similar to the DPWM.

The ZCD and DTC signal are then fetched into an SR latch to generate the on-time for the second phase of the converter (OFF).

Figure 40 Waveform of OFF Time Generation

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CHAPTER 4: CIRCUIT DESIGN AND MEASUREMENT RESULTS

4.2 MAXIMUM POWER POINT TRACKING

The simulated result of the pulsed-width estimator is shown in the bellow figure. As we can see from the plot of duty cycle (ON time divided by switching period) with respect to time, when there is a need of double frequency by increase output load, the PWE will adjust the ON time according to the change of frequency.

For instance, when high-load condition is found, the PFM is activated to double the switching frequency, resulting a half switching period. The PWE will then multiply ON time by $1/\sqrt{2}$. The change on duty cycle:

$$D_{new} = t_{ON,new}f_{new} = \frac{1}{\sqrt{2}}t_{ON}2f = \sqrt{2}t_{ON}f$$

Equation 36

Therefore,

$$D_{new} = \sqrt{2}D$$

Equation 37

By applying the new value of ON time, simulated result shows that the duty cycle is brought close to its optimum value. That significantly reduces the transient respond of the MPPT by 90%. For the power rating of $1\mu\text{W}$ to $100\mu\text{W}$, the amount of switching cycles required to get back in to its MPP is less than 5 cycles.

Figure 41 Measured Waveform of the Output Voltage Controlled by the PFM

Figure 42 Simulated Result of Duty Cycle vs. Time

4.2 CONVERSION EFFICIENCY AND POWER LOSSES

The proposed HBDIDO converter was fabricate in 0.18 um CMOS process technology with an active area of 1.2 x 1.2 mm². The PV energy harvesting

system was tested with a commercial PV cell featuring a 2 cm^2 in size. Both output and input capacitor used 100nF off-chip capacitance. The test was conducted under indoor lighting condition with light intensity vary from 300 to 600 lux.

Figure 43 Measured Transient Waveform of Input Voltage and Output Voltage

The measured quiescent power of the converter is 300nW in no-load condition. Due to this low quiescent power, the converter can achieve above 60% efficiency for output power from 1 to $100\mu\text{W}$. When enabled, the power system can deliver $7\mu\text{W}$ of power from the PV cell to the output load with peak conversion efficiency of 84.1% at 10kHz switching frequency. The major power loss causes the decrease of conversion efficiency is the conduction loss from the power switches during the dead time and zero-current detection.

Figure 44 Measured Boost Conversion Efficiency under Different Output Current

Figure 45 Layout of the Proposed DC-DC Converter

The comparison with the state-of-art energy harvesters is shown in the bellow table. It can be seen that, this proposed converter system consumes the lowest power with 300nW. Low power consumption allows it to achieve the high conversion efficiency at sub microwatt power range. With the implemented of adaptive algorithm, the MPPT can extract the power from the PV cell with peak 90% efficiency. As discussed earlier, in energy harvesting system, the overall efficiency is divided into two parts: power extracted from the PV cell by the MPPT and power transferred by the power stage. Thus, it results the highest peak conversion efficiency as compared to other works.

Table 7 Comparison of the State-of-the-Art Systems

	[4.1]	[4.2]	[4.3]	This Work
Process	0.35 μ m	0.25 μ m	0.18 μ m	0.18 μ m
V _{IN}	0.6V	0.5-2V	0.2-1V	0.2-0.7V
V _{OUT}	3.3V	5V	1.2-1.8V	1V
Power	10 μ W-1mW	5 μ W-10mW	15-50mW	3-10 μ W
Architecture	Charge Pump	Inductive Boost	Inductive Boost	Inductive Buck-Boost
MPPT Method	Integrated Charge Pump	Sector Hill Climbing	Perturb & Observe	Perturb & Observe
Power Consumption	100 μ W	3.5 μ W	3.4mW	0.3 μ W
Efficiency (with MPPT)	70%	76%	80%	84.1%

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CHAPTER 5: SWITCH-CAPACITOR (SC) DC-DC CONVERTER FOR SELF-POWER AND BATTERY-POWERED APPLICATIONS

As compared to switched-inductor DC-DC converter, switched-capacitor DC-DC converter (SC) typically is easier to integrated. In addition, it achieves higher conversion efficiency than linear regulator. Thus, switched-capacitor converters are potential solutions to support the multiple supply rail while offer the ability to fully integrate to system-on-chip without the needs of external components.

Chapter 5 describes the researches on switched-capacitor DC-DC converters. Two different SC designs are proposed.

The first design will focus on investigating the output voltage ripple of SC. It aims to optimize the output voltage ripple through single boundary hysteretic controller together with frequency modulation.

The second design will propose another possible method to suppress the output voltage ripple by combining the low-dropout regulator with the power stage of the switched-capacitor DC-DC converter.

5.1 OPTIMAL-RIPPLE AND FAST-TRANSIENT HYSTERETIC SC DC-DC CONVERTER

5.1.1 INTRODUCTION

Current SCs regulate output voltage by adjusting operating frequency using single-boundary or multiple-boundary hysteretic control scheme. Hysteretic controllers are preferred over the traditional PFM method due to its fast-transient response and inherent stability. In traditional PFM method, an output error, which is derived from an output feedback network and a voltage reference, is amplified by an error amplifier. Then, the output of error amplifier is used to adjust the frequency by a voltage-controlled oscillator. A single-boundary and double-boundary control scheme is shown in figure 46:

Figure 46 Hysteretic Control of SC

As shown in figure 46, when the output voltage drops below a threshold V_L , the converter will be triggered to deliver charge to the output in a single phase. When the output voltage is higher than the threshold, the converter is in standby and output capacitor is then discharged by the load. With smaller output capacitance, the output voltage ripple is large enough for a single-phase transition. However, that leads to the issue about the voltage droop during step-up load transients.

Figure 46 shows a double-boundary control method with large output capacitor. When the output voltage drops below the lower threshold V_L , the converter is enabled. The converter delivers the power to load through multiple cycles and

causes the output voltage to increase. When the output voltage is above the upper threshold V_H , the converter is disabled, and output capacitor continues being discharged by the load.

5.1.2 PROPOSED HYSTERETIC CONTROL SCHEME

5.1.2.1 OVERALL SYSTEM ARCHITECTURE

To optimize output voltage ripple, a hysteretic control scheme is proposed. The proposed method locks the sampling frequency at different converter's switching frequency according to different load currents.

Figure 47 Proposed Hysteretic SC with Sampling Frequency Modulation

The overall architecture of the proposed SC system is shown in figure 47. It consists of two feedback loops. The first loop performs normal hysteretic voltage

regulation. The second feedback loop adjusts the sampling frequency to ensure a uniform converter switching frequency.

The frequency control loop keeps track the time between two consecutives phase changes. It stores the time data in digital domain by counting the number of skipped sampling pulses N_{skip} . When N_{skip} is constant over time, the sampling frequency will be constant, hence, the phase transitions and amount of charge transferred are uniform. However, when N_{skip} is smaller/larger than a reference value, the control system will increase/reduce the sampling frequency by adjusting the input voltage of the VCO.

5.1.2.2 POWER STAGE

The anti-phase 1-to-2 step-down SC is described in figure 48. In general, it consists of eight power switches (four NMOS, four PMOS), and two flying capacitor, forming two identical SCs which operate in opposites phase.

Figure 48 Power Stage of Proposed SC

The 180° -phase operation of the SC makes each switching phase essentially equivalent. During the switching event, one SC is switched from discharging

state to charging state and the other SC is switched from charging state to discharging state. Consequently, the amounts of charge transferred to the output are uniform over each switching phase.

To further reduce the gate conduction loss, the control voltage of the low-side transistors (S12, S13, S23, S22) ranges from V_{OUT} to 0, while the control voltage of the high-side transistor (S11, S14, S24, S21) ranges from V_{OUT} to V_{IN} . These high-side control voltages can be generated by adding the voltage across the low-side control voltages using level shifters. In addition, dead times are added between the transition event of the two switching phases to prevent shoot through current, which is caused when V_{OUT} is shorted to ground. Figure 49 shows the gate voltage control signals with different voltage swings.

The gate control signal generator consisted of start-up circuits, gate drivers, dead-time generators, level shifters is shown in figure 50.

Figure 49 Gate Signal Generator

The start-up circuit is designed to ensure safe operation when the SC powering up. The output voltage is clamped to twice diode voltage when the input voltage ramps up. The power stage is pushed to a state such that C_{fly1} is charged to V_{OUT} and C_{fly2} is charged to $V_{IN}-V_{OUT}$. The level-shifter capacitors are also charged to some level voltages. When V_{OUT} reach 0.8V, the converter operation transit from start-up to normal state in a smooth way. A transistor M_{DN} is used to pull v_p up and turn of the M_X and M_Y immediately when v_N is low. Figure {51} shows the transient of the circuit between start-up and normal phase.

Figure 50 Transient Response of Gate Signal Generator

5.1.2.3 HYSTERETIC REGULATION WITH FREQUENCY MODULATION

The proposed hysteretic regulation circuit consists of a dynamic comparator and a 3-bit up counter. Then, the output of the 3-bit counter is used to control the sampling frequency by a charge pump integrator and a VCO.

A conventional dynamic comparator is implemented to compare output and reference voltage. The dynamic comparator has two complementary output voltages. The operation of the dynamic comparator is summarized:

Table 8 Dynamic Comparator Operation

	CMP	CMPN
$V_{OUT} > V_{REF}$	Low	High
$V_{OUT} < V_{REF}$	High	Low

Figure 51 Output Comparator and Counter

As shown in figure 52, N_{SKIP} , which is the number of consecutive pulses of the CMPN is the time between two adjacent transitions. By regulating N_{SKIP} at a fixed value, we can ensure the charge transfer to output is uniform.

Figure 52 Output Voltage Comparison and Up Counter Operation

In this proposed design, N_{SKIP} is kept in digital domain by a 3-bit counter. The 3-bit counter take the input from CMPN. As the time different is longer, CMPN has more and more pulses, which triggers the counter to count from 000 to a maximum value of 111. After reach 111, the counter holds its maximum value without reset to 0. It only resets the value to 0 when CMP is raised, which indicating the start of the next transition phase. After that, N_{SKIP} is compared to a reference and determine the increasing or decreasing of the sampling frequency. When N_{SKIP} is less than its reference, an increment signal is sent to increase the sampling frequency. On the other hand, the sampling frequency is reduced when N_{SKIP} is greater than its reference. The circuits to control sampling frequency and VCO are shown in figure 53.

Figure 53 Sampling Frequency Control and VCO

5.1.2.3 ENHANCEMENT OF TRANSIENT RESPONSE

The sampling frequency, which is regulated by skipping a fixed period N_{SKIP} , is given by:

$$f_{sample} = (N_{SKIP} + 1)f_{ph_change}$$

Equation 38

The converter's switching frequency is able to increase up to N_{SKIP} times when load increases. Hence, if a load step is not greater than N_{SKIP} times, the converter can respond quickly without voltage droops.

As shown in figure 54, a high load transient causes a decrease of N_{SKIP} . Thus, the VCO input control signal is slowly increased until N_{SKIP} is regulated at a constant. Moreover, extremely high load transient causes N_{SKIP} to be zero. when N_{SKIP} is at zero, the VCO input control signal is set at the maximum value. Maximum sampling frequency is achieved quickly so that the converter can react with the voltage dropping.

(a)

Figure 54 Sampling Frequency Control During High Load Transient and Extremely High Load Transient

5.1.2 EXPERIMENT RESULTS

The proposed SC DC-DC converter was implemented in 0.18 μm CMOS technology by AMS. Figure 55 shows the chip micrograph. The effective area occupied is 0.75x0.66mm². The converter uses on-chip dual metal-insulator-metal capacitors as flying capacitors. It aims to deliver and regulate output voltage 0.8V from a 1.8V voltage supply.

Figure 55 Chip Micrograph

The performance of the proposed SC converter is summarized in the table 9:

Table 9 Summary of the Proposed Hysteretic SC DC-DC Converter

Conversion Ratio	01/2
Flying Capacitance	1.5nF (MIM)
Output Capacitance	2nF
V_{IN}	1.8V
V_{OUT}	0.8V
I_{OUT}	0.1-7mA
f	260kHz – 10MHz
Output Ripple	10mV – 48mV
Efficiency	86% (Peak)
Power Consumption	28 μ W

The transient response of the SC converter under different load condition varying from 0.2mA to 1mA is investigated. The steady state operations when load current is 1mA and 7mA are shown in figure 56:

(a)

(b)

Figure 56 Steady State Operation of Proposed SC Converter

(a) $I_{OUT}=1\text{mA}$; (b) $I_{OUT}=7\text{mA}$

Figure 57 shows the output voltage ripple and switching frequency w.r.t. load. The power losses, which consist of condition loss, switching loss and others, of the proposed SC converter are shown in figure 58. The power converter maintains power conversion efficiency higher than 65% while

deliver output loads from 0.1mA to 7mA. It achieves peak conversion efficiency of 86% at 2mA load.

Figure 57 Output Voltage Ripple vs Switching Frequency

Figure 58 Power Loss Investigation

Figure 59 Overall Power Conversion Efficiency

5.2 SC DC-DC CONVERTER WITH INTEGRATED NMOS-LDOS

5.2.1 INTRODUCTION

Normally, the output voltage of switching converter sustain high ripple noise. A solution to suppress these switching noise is connected an LDO to the output of the switching converter. The LDO should be designed so that it stays away from the drop-out region with sufficient headroom. When load current decreases, in order to increase the power efficiency, a dropout voltage tracking is presented to adjust the V_{DS} of the pass transistor.

A step-down SC converter with conversion ratio $2/3$ is proposed. To suppress the output voltage ripple, NMOS-LDOs is integrated with the SC converter, in both discharging and charging phases. By monitoring the V_{DS} across the pass

transistors, the drop-out voltage can be adjusted at minimum, to reduce the power loss. Besides, it optimizes the ripple rejection to the output of the converter. A proposed gate driving method is used to reduce the high-frequency switching noise and help the turning on of the regulated transistors.

5.2.2 PROPOSED SWITCHED-CAPACITOR CONVERTER WITH INTEGRATED LDO

5.2.2.1 OVERALL SYSTEM ARCHITECTURE

The overall system architecture of the proposed SC converter with integrated LDOs is shown in figure 60. A conventional SC converter is used with seven power switches: M1 to M7. In this proposed design, three transistor M3, M4, M7 are controlled by the error amplifier, which form and function as three NMOS-LDOs. M3 and M4 works as pass transistors during the charging phase, while M7 works as pass transistor during discharging phase. Theoretically, a fixed current, that is equivalent to the load current, is forced through the pass transistors, generating no output voltage ripple. By doing that, the control loop of the proposed switched-capacitor converter is not restricted by the converter switching frequency. The regulation achieves faster transient response, as similar to conventional LDOs.

Figure 60 Proposed SC Converter with integrated LDOs

5.2.2.2 POWER STAGE

Power stage of the proposed 2/3 SC converter consist of seven power transistor M1 to M7. It operates in five phases, including two main operating (charging/ discharging) phases, two intermediate phases and one dead-time phase. The transitions of these operating phase are shown in figure 61

Figure 61 Power Stage of the Proposed 2/3 SC Converter

The three middle phases are used to ensure sufficient dead time and eliminate shoot-through current. In addition, they reduce the switching noise during phase transition.

During the charging phase, both M3 and M4 function as LDOs' pass transistor while M2 operates as normal power switch. Charges are transferred to two flying

capacitor C1 and C2 through M3 and M4. As the voltage across C1 and C2 increases, the node voltage NB and NC decreases, which leads to the decrease of V_{DS} of two transistors M3 and M4. The charging phase ends when the drain-to-source voltage drops below a minimum value $V_{DS,min}$, a value around 80mV. The voltage across two flying capacity can be approximated:

$$V_{fly,max} = V_{IN} - V_{OUT} - V_{DS,min}$$

Equation 39

Hence, the range of the node voltage NB and NC is approximated from: $V_{IN} - V_{fly,max}$ to $V_{IN} - V_{fly,min}$. And the drain-to-source of the pass transistor M3, M4 is varied from $V_{IN} - V_{OUT} - V_{fly,max}$ to $V_{IN} - V_{OUT} - V_{fly,min}$. The charging phase is ended when M3, M4, and then M1, M2 are OFF.

On the other hand, M7 functions as LDOs' pass transistor while M5 and M6 operates as normal power switches in discharging phase. Two flying capacitor C1 and C2 are connect in series and they discharge to the output. As the charge transferred to output, node voltage NA reduces, thus voltage across M7 reduces. When V_{DS} of M7 drops below a minimum value $V_{DS,min}$, discharging phase will end. By sizing two capacitors identically, we have the voltage across the flying capacitor:

$$V_{fly} = \frac{1}{2} (V_{OUT} - V_{DS})$$

Equation 40

The node voltage NA varies from $2V_{fly,min}$ to $2V_{fly,max}$. The discharging phase is ended when M7, and then M5, M6 are OFF. During zero load condition, there is no discharging, voltage across both flying capacitor is constant:

$$V_{fly,min} = V_{fly,max}$$

Equation 41

Thus,

$$V_{OUT} = \frac{2}{3}V_{IN} - V_{DS,min}$$

Equation 42

The no-load ration is achieved at 2/3 when the power switches are ideal and there is no minimum V_{DS} . Figure 62 shows the node voltage and voltage ripple of the flying capacitors.

Figure 62 Node Voltages across Flying Capacitors

To implement these switching behaviours, gate signal generator is used with non-overlapping latch and delay line. It is designed to ensure four power switches M1, M2, M5, M6 are turned ON earlier and turned OFF later than three LDOs' pass transistors M3, M4, M7.

Figure 63 Gate Signal Generator

To detect phase transition when V_{DS} of the pass transistors drops below a value $V_{DS,min}$, a comparator is used compare the voltage values at both side of the transistor.

Figure 64 Comparator for Phase Transition

5.2.2.3 SWITCHING INTEGRATED LDOS

As discussed, M7 works as the pass transistor of LDO during discharging phase, while M3 and M4 work as the pass transistors of LDO during charging phase. The input of the LDOs are connected to the output of the SC converter, which is related to the node voltages NA, NB, NC. Thus, the input voltage of these LDOs varies during operation.

Figure 65 NMOS-LDO Circuit

Practically, V_{IN} is 1.8V while V_{OUT} is 1V. From the abovementioned formula, it is derived that $V_{fly,min}=0.54V$ and $V_{fly,max}=0.72V$. Hence, the LDOs are required to suppress the input ripple of 0.18V. From figure 65, in an NMOS-LDO, input rejection ratio is given by:

$$IRR_{NMOS} = \frac{1}{1 + g_m r_o [A(s) + 1]} \approx \frac{1}{A(s) g_m r_o}$$

Equation 43

The circuit of SC converter with integrated LDOs is shown in figure 66. M3 and M4 carries half of the output current in charging phase, while M3 carry full output current during in discharging phase. Thus, M3 and M4 can be designed with same size; and M7 can be designed with double the size of M3 or M4.

These pass transistors are driven by a two-stage error amplifier and a buffer. The first stage is designed using cascode current mirror to achieve higher gain. The buffer is used to attenuate the impedance node at the input of the pass transistor. Consequently, the pole can be pushed to high frequency. The size of M_{sf1} and M_{sf2} can be designed as small so that it generates a non-dominant pole at the output of the second stage. The output of the first stage is designed with dominant pole using Miller capacitor.

Figure 66 NMOS-LDO and SC Converter

Figure 67 Small Signal Model of NMOS-LDOs

Figure 67 shows the equivalent small signal model of the proposed NMOS-LDOs. The NMOS-LDOs is simulated under different output loads. The loop gain and phase margin are shown in figure 68. The proposed circuit achieves 75dB loop gain and 90° phase margin when delivering output 100mA. The phase margin drop as the current drops. However, it still can achieve higher than 50° across the load range.

(a)

(b)

Figure 68 Loop Gain and Phase of the Proposed NMOS-LDOs

The simulated results of input rejection of the proposed NMOS-LDOs is shown in figure 69. The input rejection can be achieved as 83dB when output load current 100mA and frequency of 270kHz.

Figure 69 Input Rejection of the Proposed NMOS-LDOs

5.2.3 EXPERIMENTAL RESULTS

The proposed SC converter with integrated LDOs is designed and fabricated in 0.18 μ m CMOS technology. It aims to regulate 1V output voltage from 1.8V input source. The operating frequency is from 1kHz to 320kHz. Figure {70} shows the transient waveform when output load changes from 10mA to 100mA. When load switches from 10mA to 100mA, the settling time for the output voltage is 200ns. On the other hand, when load switches from 100mA to 10mA, the settling time is 150ns. This is because of the fast response of the proposed LDO.

Figure 70 Transient Response with I_{OUT} from 10mA to 100mA

Figure 71 shows the power conversion efficiency w.r.t. load current. The SC converter achieve peak efficiency 83%. It maintains the efficiency higher than 72% throughout the entire load range.

Figure 71 Power Conversion Efficiency of Proposed SC Converter with LDOs

CHAPTER 6: SUMMARY AND FUTURE WORKS

6.1 SUMMARY & CONCLUSION

Energy harvesting is more and more popular, and it became a trend power management research area. It helps human to reduce the world's dependency on conventional energy such as coal, oil, etc. One of the most common renewable energy source is PV energy. PV energy can be captured and converted directly to electricity. However, as the high cost of a PV system as compared to conventional system, it is essential to maximize the cost efficiency. Specifically, it is achieved by maximizing the output power of the PV cell, minimizing hardware cost and maximizing the power conversion efficiency. The main focus of this research is to develop an energy harvesting system that is able to harvest energy from PV source and delivered to the electronic application of IOT, with the improvement on overall cost efficiency.

Chapter two summarizes past literature related to this research topic. Firstly, we reviewed the model and characteristics of the PV cell. The equivalent circuit model must be able to define the entire I-V relationship of the PV cell with high accuracy. One simplest and common use is the single diode model, which is derived from the physical principles of the PV cell. The plots I-V and P-V relationship of the PV model in different illuminations show that the maximum power point is non-linearity. Since the maximum power greatly varies with surrounding condition, the MPPT play an important role in the energy harvesting system. It tracks and locks the PV cell operating at the maximum power point

regardless of the environmental conditions. There are various of MPPT algorithm and they are classified into different groups based on their complexity, algorithms and hardware requirements. With the scale of a low power energy harvesting application, perturb and observe method is favourable due to its ease of implementation, low requirement and good accuracy.

Several kinds of DC-DC converter were briefed such as linear regulator, switching inductor converter and switching capacitor converter. Among these types of converter, switching inductor converter still provided a good solution for energy harvesting system. Despite it has high component count and occupies large area, it can achieve high power conversion efficiency, which is very critical for low power energy harvesting.

A few common second-order inductor-based DC-DC converter were discussed: buck converter, boost converter and buck-boost converter. On top of that, the multi-input multi-output buck-boost topology has the highest conversion efficiency.

Finally, the literature review concludes with some review on the converter's controller and control methods.

To accommodate the demand for self-powered portable device in the IOT area, a H-bridge dual-input dual-output power converter is proposed for indoor energy harvesting system. The power system operates in three different operating modes. To achieve high power conversion efficiency, the H-bridge power stage transfers harvested energy directly to the output load in one conversion stage. In light load

condition, when there is no energy demanding from the load, the excessive amount of energy is transferred and stored in a supercapacitor for backup purpose. When the PV energy is not insufficient, and the load demands high power, the third operating mode is enabled to deliver the backup energy to provide immediate power to the load.

The overall efficiency of the energy harvesting system consists of two parts: the amount of power extracted from the PV source as compared to the maximum available power, the power conversion efficiency.

A perturb-and-observe method is implemented in order to extract the maximum available energy from the PV source. The on-times of all the power switches are stored and manipulated in digital domain. A novel power approximation technique is proposed to make use these digitized on-time values. A digital pulse-width modulation is then designed to control the six power switches. As the converter aims to use in very low power applications, the power consumption from the controller need to be optimized. Using pulse-skipping method and pulse-frequency modulation, the switching power consumption can be reduced significantly. However, changing the operating frequency also leads to the shift of the PV operating point far from its maximum power point. Thus, the extraction efficiency reduces drastically. Another on-time estimation method is proposed to quickly estimate and shift the operating point to the maximum. It is measured that, after changing the frequency, the on-time estimation technique recovers the maximum power point with in 4 switching cycles.

The proposed energy harvesting system was fabricated in 0.18 μ m CMOS process. The proposed system achieves above 60% of conversion efficiency with a peak efficiency of 84.1% while driving 1 μ A to 1mW load current. The controller consumes only 300nW quiescent power.

Chapter Five discussed on the feasibility of switched-capacitor DC-DC converter in self-powered and battery-powered devices. Two design of SC power converter were proposed.

The first design focused on analysing the output voltage ripple of SC. It aims to optimize the output voltage ripple through single boundary hysteretic controller together with frequency modulation. The power converter maintains power conversion efficiency higher than 65% while deliver output loads from 0.1mA to 7mA. It achieves peak conversion efficiency of 86% at 2mA load.

The second design proposed another possible method to suppress the output voltage ripple by combining the low-dropout regulator with the power stage of the switched-capacitor DC-DC converter. The SC converter achieve peak efficiency 83%. It maintains the efficiency higher than 72% throughout the entire load range.

6.2 FUTURE WORKS

Although the proposed DC-DC converter provides a sufficient solution for the energy harvesting application with high conversion efficiency, there are still rooms for improvement.

The major part of the power loss is the conduction loss causing from the accuracy of the dead-time control and zero-current detector. The accuracy of the DTC and ZCD can be improve by increase the digital bit of the delay. However, it results a significant increase in hardware component count. Although the proposed V_x sensor is simple and with low power consumption, it deals with the internal threshold of transistor, which is susceptible to process and temperature variation. Thus, it affects the stability of the detection of undershooting and overshooting. In the future, more work on DTC and ZCD will be carried on.

The converter can be further improved by adopting a variable step-size control for the MPPT. During the steady stage, using small perturbation size is more practical to reduce the ripple current and ripple voltage of the PV source. Since the ripple is reduced, the control efficiency is improved. On contrary, during transient duration, when there is a big change in the lighting condition, the operation is far from the MPP. Larger step size can be selected to allow faster transient and smaller settling time.

6.3 CONTRIBUTIONS

A. K. Bui, Z. Xiao, and L. Siek, "A Digitally-Controlled DC-DC Converter with Fast Predictive MPPT for PV Energy Harvesting System" submitted to The Journal of Engineering

A. K. Bui, Z. Xiao, and L. Siek, "Digitally-Controlled H-Bridge DC-DC Converter for Micropower PV Energy Harvesting System," in 15th Int. Symp. Integrated Circuits (ISIC), 2016.

Z. Xiao, A. K. Bui, and L. Siek, " A Hysteretic Switched-Capacitor DC-DC Converter with Optimal Output Ripple and Fast Transient Response," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 25, Issue: 11, Nov. 2017)

Z. Xiao, A. K. Bui, and L. Siek, " On-chip reconfigurable switched-capacitor DC-DC converter for indoor PV energy harvesting," Electronics Letters. Available: <http://digital-library.theiet.org/content/journals/10.1049/el.2016.3018>.

Z. Xiao, A. K. Bui, and L. Siek, "A Switched-Capacitor DC-DC Converter with Embedded Fast NMOS-LDOs Achieving Low Noise, Low Output Voltage Ripple and Fast Response," in 15th Int. Symp. Integrated Circuits (ISIC), 2016.

6.4 REFERENCES

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