Advanced chemical science-based high-resolution low-cost printing for high performance printed electronics

Shi, Jingsheng

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electronics

SHI JINGSHENG

SHI JINGSHENG

SCHOOL OF CHEMICAL AND BIOMEDICAL ENGINEERING

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process for printed electronics

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SHI JINGSHENG

School of Chemical and Biomedical Engineering

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Abstract

Printing processes are promising alternatives to photolithography for printed electronics. It is essential to applications such as large-area flat-panel displays, electronic paper, radio frequency identification tags (RFID tags), and ultraportable disposable sensors, which have requirements other than operating speeds and increasingly complicated circuits for better manufacturability. The impact of printing processes on device performance is still underexplored. Understanding and advancing the chemical sciences involved in printing electronics is essential to develop new printing technologies or improve existing printing processes for high performance organic semiconductor/CNT-based printed electronics.

UV transfer embossing using selective cross-linking of resins has been improved for lower gate leakage current, and significant roughness reduction at the dielectric-semiconductor interface, leading to improved device performance. The resulting printed OTFT produced one order higher mobility ($0.01 - 0.02 \text{ cm}^2/\text{V s}$) and two orders higher on/off ratio (10^4) compared to top-gated devices.

In-situ polymerization in PDMS-based nanocomposite dielectric material was used to replace cross-linking of UV resins and develop a low-cost adhesive-free direct transfer printing process. The adhesive-absent semiconductor-electrode interface showed width-normalized contact resistance of $\sim 100 \text{ k}\Omega\cdot\text{cm}$. Further

improved device performance with a high mobility of $0.038 \text{ cm}^2/\text{V s}$ and an on/off ratio of $10^4 - 10^5$ was demonstrated.

The first use of spatial control of oxygen-inhibition of photopolymerization in acrylate-based materials was demonstrated as a universal printing technique applicable on different substrates. The new approach eliminates the expensive equipment and materials in the conventional lithography process. This new printing method was also used to fabricate printed TFTs on Si and PET substrates, showing very good device performance.

A single-step transfer printing method to fabricate CNT finFETs with novel PVA dielectric-wrapped CNT network was developed and the printed high performance CNT finFETs with mobility of $27 \pm 10 \text{ cm}^2/\text{V s}$ and 10^2 - 10^4 on/off ratio were fabricated. The method is a versatile low-cost printing technology to mass-produce high performance all-printed CNT-based electronics on flexible large-area substrates for a broad range of electronic applications.

In summary, advances in chemical science for new and improved printing processes were studied to offer better device performance for printed electronic and to address the technological issues in other printing processes while fundamental studies were conducted on how the printing processes would affect the performance of the printed devices from various aspects. This research offers chemical, material and mechanical engineering approaches for better manufacturability and high performance printed electronics, in addition to providing fundamental insights on the effect of the printing process on devices.

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Chapter 1 Introduction

1.1 Background

The conventionally dominant patterning technique for integrated circuits is photolithography in silicon-based microelectronics, which uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical "photoresist" on the substrate and to enable deposition of a new material or removal of the underlying material in the desired pattern on the substrate. Improvements in the resolution of photolithography enable smaller devices, higher operating speeds, and lower power consumption in denser integrated circuits. This down scaling has led to improvements in microelectronics, where the number of transistors in an IC has doubled every 18 months, a scaling known as Moore's law. Photolithography has provided a powerful tool that has helped market growth for traditional microelectronics. However, the cost of the facilities needed to build such systems has increased at similar rates. Photolithography is not capable of creating large-area patterns. Long process time and expensive equipment/materials are disadvantages when fabricating relatively simple circuits.

Various electronic applications, such as large-area flat-panel display/electronic paper ¹, radio frequency identification tags (RFID tags) ², and ultraportable disposable sensors^{3, 4}, have different requirements other than operating speeds and increasingly complicated circuits. For example, amorphous silicon (a-Si)

thin-film, currently used for displays, requires a lower operating speed but larger area coverage in its fabrication process. Other requirements include mechanical flexibility for flexible display, electronic paper and artificial skins; extremely low-cost for product level implementation of RFID tags; and flexibility, ultra-portability, and low-cost for some sensor applications. Therefore, printed electronics are receiving increasing research interest to satisfy the above-mentioned and new requirements from various applications. Printing electronics produces electronic devices using low-cost methods such as screen printing⁵, inkjet printing^{6, 7}, microcontact printing (μcp)^{8, 9}, transfer printing^{10, 11} *etc.*, preferably in combination with solution-processable organic semiconductors¹², carbon nanotubes (CNT)¹³, and semiconductor nanomaterials¹⁴. Research efforts have been and are being spent on many printing methods to meet different requirements from the different applications mentioned above and to offer other advantages such as low manufacturing cost, shorter process time, high brightness and power-efficiency in displays, better integration with semiconductor materials and better device performance over process control.

1.2 Motivations

Although several alternative manufacturing processes have been developed and studied, there are some drawbacks associated with these techniques that limit their widespread industrial application.

μcp ^{8, 15, 16} requires idiosyncratic chemistry, as the best-established μcp system to date is based on alkanethiolates on gold and silver and alkylsiloxanes on hydroxyl-terminated surface⁸, and in this system specific surface chemistry is required between the ink material and substrate, which limits its wide application. In inkjet printing, one obvious challenge is low resolution due primarily to the volume of the ink droplets¹⁷. While electrohydrodynamic inkjet printing can generate smaller droplets and thus better resolution, the equipment setup is more complicated than other printing technologies, and it is unlikely that much smaller droplets could be generated in the near future, limited by the physics of the droplet production process¹⁸. Stringent requirements of substrate surface properties are must be met for better liquid line stability, minimal coffee stain effect¹⁷, and thus resolution.

Study of the chemical science involved in the development of new printing processes and the improvement of existing processes is highly needed to address the above issues, such as the stringent requirements of substrate materials and interfacial chemistries.

New mechanisms that are independent of idiosyncratic chemistry are needed for better portability of the printing processes across different substrates, and new processes that are capable of creating unique nanostructures for better device performance are of high interest for commercially viable applications.

Existing transfer printing processes need to be improved with faster process speed and better reliability, as well as a device structure designed specifically for this process to achieve high device performance.

Printing techniques with new nanocomposite materials capable of performing in-situ chemical processes are required for favorable device physics, simpler device structure, and production. Additionally, it is important to understand the fundamentals of printed devices such as how printing processes affect the electrode-semiconductor and dielectric-semiconductor interfaces in the device structure, and thus further affect device performance, as well as what processing condition should be chosen to optimize printing processes and create unique nanostructures for improved device performance.

1.3 Objectives of the study

1.3.1 New mechanisms for printing techniques

An important task of this project is to discover, develop, and investigate new mechanisms for low-cost printing techniques in printed electronics. As interfacial chemistry, surface treatment, and adhesives are heavily utilized in other printing processes, new mechanisms involving mold-based spatial control of the oxygen-inhibition effect in the chemical science of acrylate materials can be developed to mimic photolithography and to eliminate the above requirements, thus gaining better applicability to different substrate materials.

Solvent vapor treatment, which changes the mechanical properties of polymer films under room temperature and modifies interfacial adhesion strength, can be used as the mechanism of a transfer printing process and replace the requirements mentioned above. Moreover, novel nanostructure can be created with the new physical chemistry in the mechanism for the much-improved device performance.

1.3.2 Improved processes for printed electronics

To improve and develop the existing processes/mechanisms used in printing techniques, UV resin can be used as instant adhesive in transfer printing to improve process speed and reliability. Device structure can then be optimized according to the printing technique for better molecular packing on a smooth dielectric-semiconductor interface and minimized leakage current by thorough cross-linking of polymer dielectric. In-situ polymerization of PDMS-based nanocomposite material for transfer printing processes can be studied and used as an adhesion enhancement mechanism in transfer printing to replace adhesives for simplified production and device structure.

1.3.3 Effect of printing processes on printed electronic devices

Regarding the study of the fundamentals of printed devices and the effect of printing processes, electrode-semiconductor and dielectric-semiconductor interfaces in printed device structures can be characterized in relation to device performance for a deeper understanding of device physics in printed structures. Versatile printing techniques can then be used to create novel finFET-like

nanostructure in high performance all-printed CNT-based electronics on flexible large-area substrates for a broad range of electronic applications.

1.4 Organization

This dissertation is devoted to the study of printing processes in printed electronics to address existing issues (poor device performance caused by printing processes and requirements for idiosyncratic chemistry, *etc.*) and the impact of printing processes on device performance in terms of the electrode-semiconductor interface, dielectric-semiconductor interface, dielectric constant and leakage current. This dissertation is organized in the following manner:

Chapter 1 provides background and overview of the motivation and objectives of this PhD research.

In Chapter 2, the literature on fabrication processes in printed electronics is summarized. In particular, the basic concepts and device physics of organic and CNT TFTs, and the fabrication processes of printed TFTs are reviewed.

Chapter 3 describes the experimental procedure, materials, and instruments used in this study in detail.

For Chapter 4, the UV transfer embossing technique is improved in the fabrication of bottom-gated organic thin-film transistors, and device

performance is much improved with a smooth dielectric-semiconductor interface and thermally cross-linked PVP dielectric.

Chapter 5 presents the development and investigation of an adhesive-free transfer printing process using PDMS-TiO₂ nanocomposite to improve hysteresis behavior and threshold voltage of printed thin-film transistors.

In Chapter 6, spatially controlled oxygen-inhibition in acrylate-based materials is developed as a new mechanism in printing techniques. The mechanism is further developed into a universal printing technique for printed electronics.

Chapter 7 presents novel, printed CNT finFETs with a novel dielectric-wrapped CNT network to produce excellent device performance.

The last chapter provides a general conclusion and some perspectives on future research possibilities.

Chapter 2 Literature Review

Printed electronics are receiving more and more interests in both research and industry due to their cost-efficient fabrication processes at low temperature using printable materials^{14, 19, 20}. Because of this, printed electronics have enabled many applications such as RFID tags², flexible display/e-paper¹ and portable, inexpensive sensors^{3, 4}.

Printed electronics creates electrically functional devices such as thin-film transistors²¹, photo optical devices^{22, 23}, and memory²⁴ by utilizing printing processes on a broad range of substrates. Common printing processes include screen-printing, flexography, gravure, and inkjet printing. There are other processes such as μ cp⁸, transfer printing^{25, 26}, *etc.*, which are currently under active research. Common substrates are polymer films, glass and silicon. Printed electronics utilize many printable materials, including organic semiconductors²⁷, CNTs²⁰, and inorganic semiconductor nanomaterials¹⁴.

Printed thin-film transistors are important electronic components in RFID rectifier and transponder circuits, back-plane driving circuits in displays/electronic papers, and transducer components in sensors. Printed thin-film transistors offer many attractive aspects, including lightweight devices, low-temperature processing, and mechanical flexibility. Innovative printing technologies are under active research with the aim of manufacturing low-cost

devices on large-area substrates, as well as maintaining the best device performance by improving resolution, optimizing device structure, minimizing contact effects, widening applicability on different substrates, etc. This chapter reviews the fundamentals and materials in printed TFTs in section 2.1; section 2.2 reviews several types of printing processes for device fabrication.

2.1 Fundamentals and materials

2.1.1.1 Device structures and operations

There are four common device structures of printed TFTs. Figure 2.1 shows an illustration of these device structures. The position of the gate electrode determines whether the device has a bottom-gate or top-gate structure, while, depending on the position of source and drain electrodes relative to the gate electrode, the device structure can be further specified as top-contact or bottom-contact.

Figure 2.1 Four common device structures of printed TFTs.

The basic operation principle of TFTs is modulation of current in semiconductor materials from source to drain electrode by applying a gate voltage. In more detail, most TFTs operate in accumulation mode and the gate electrode-insulator-semiconductor structure can be considered as a capacitor, and thus a sufficiently high gate voltage is capable of bending the energy band in the semiconductor near the insulator layer such that a negative gate voltage will induce hole carrier in p-type semiconductors and a positive gate voltage will induce electron carrier in n-type semiconductors. When a proper drain voltage is applied, drain current flowing from source electrode to drain electrode will be produced in the semiconductor. Figure 2.2 shows energy-band diagrams to further explain the operation principle of TFTs. At zero gate voltage, the energy bands are approximately in flat-band condition, if one assumes that the work function of the gate metal is similar to the Fermi level of the semiconductor. In this case, if a drain voltage is applied, there is no current generated in the semiconductor, as no charge carriers are induced and the device is in “off-state”. In p-channel TFTs, when a negative gate voltage is applied, the energy band of the semiconductor near the semiconductor-dielectric interface is bent upward, and holes are induced and accumulated at the interface, as the valence band is close to Fermi level. Drain current flows from source to drain electrode through hole transport when drain voltage is applied. When a positive gate voltage is applied in n-channel TFTs, the energy band of the semiconductor near the interface is bent downward, and electrons are induced and accumulated at the interface, as the conduction band is close to

Fermi level and electron transport provides drain current when drain voltage is applied. The drain current is related to the charge carrier concentration, which in turn depends on the gate voltage, and capacitance of gate electrode-insulator-semiconductor structure and equations 2.1 and 2.2 describe the relationship in the linear and saturation regimes, respectively:

$$I_D = \frac{WC_i\mu}{L} \left(V_G - V_T - \frac{V_D}{2} \right) \times V_D, \quad |V_D| \ll |V_G - V_T| \quad (2.1)$$

$$I_D = \frac{WC_i\mu}{2L} (V_G - V_T)^2, \quad |V_D| > |V_G - V_T| \quad (2.2)$$

where W , L , C_i , and μ are channel width, channel length, capacitance per unit area, and field-effect mobility, respectively.

Figure 2.2 Theoretical energy band diagrams for gate-insulator-semiconductor structure in (a) flat-band condition, (b) p-channel operation when negative gate voltage is applied and (c) n-channel operation when positive gate voltage is applied.

2.1.1.2 Device performance evaluation

Field-effect mobility and on/off ratio are two most important parameters when evaluating device performance, as they will affect the working frequency and power consumption of the printed circuits. Threshold voltage is another important device parameter. Equation 2.1 and 2.2 relate the field-effect mobility and experimental data and are commonly used for mobility extraction. In a saturation regime, which is common for organic transistors, equation 2.3 can be obtained by taking the square root of the drain current, and mobility can be obtained from the plot of $I_D^{1/2}$ against V_G , while the on/off ratio can be simply calculated by dividing the “on-state” current by the “off-state” current.

$$\mu = \left(\frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2 \frac{2L}{W} \frac{1}{C_i} \quad (2.3)$$

where I_D is the drain current, C_i is the capacitance per unit area of the gate dielectric film, and V_G is the gate voltage. According to equation 2.3, a straight line can be fit into the $I_D^{1/2}$ - V_G plot, and the intersection between this straight line and the $I_D = 0$ line gives the threshold voltage.

For TFTs using CNTs or semiconductor nanomaterials, the devices are usually characterized in a linear regime and mobility is calculated with equation 2.4, in which the drain voltage V_D has to be taken into consideration.

$$\mu = \frac{\partial I_D}{\partial V_G} \times \frac{L}{W} \times \frac{1}{C_i \cdot V_D} \quad (2.4)$$

where μ is device mobility, I_D is drain current, V_G is gate voltage, L is channel length, W is channel width, C_i is the capacitance of dielectric material over a unit area, and V_D is drain voltage.

The on/off ratio is similarly calculated as described above and threshold voltage is estimated from the linear fit of the $I_D - V_G$ plot, as V_D in a linear regime can be neglected ($|V_D| \ll |V_G - V_T|$).

2.1.1.3 Contact resistance

The interface between source/drain electrodes and semiconductor is very important in printed TFTs and has been studied extensively. Different printing processes have been shown to have different impact on the semiconductor-electrode interface, and contact resistance is commonly used in the evaluation of the semiconductor-electrode interface.

The transmission line model (TLM) can be used to estimate contact resistance. TLM states that the total device resistance between the source electrode and the drain electrode can be divided into channel resistance and contact resistance:

$$R_{total} = R_{sh} + R_C = \frac{L}{W\mu C_i(V_G - V_T)} + R_C \quad (2.5)$$

and after contact resistance is normalized by width,

$$R_{total}W = \frac{L}{\mu C_i(V_G - V_T)} + R_CW \quad (2.6)$$

where R_{ch} is the channel resistance and R_C is the contact resistance. The channel resistance is assumed to be only dependent on the intrinsic property of the semiconductor and thus, linearly dependent on the channel length while contact resistance remains constant. In this way, the plot of total resistance against channel length can be fitted into a straight line. The intersection of this straight line and the $L = 0$ line gives the contact resistance.

Contact resistance is known to limit the performance of printed TFTs. Chemical treatment including self-assembled monolayer (SAM) and piranha treatment to modify or dope the semiconductor-electrode interface can be used to reduce the contact resistance. It is also shown that top-contact devices generally performed better than bottom-contact devices. However, vacuum evaporation used in top contact devices will produce metal penetration into organic semiconductors. Molecular or metallic adhesive used in printing processes have been shown to induce a high contact resistance. Minimized thickness of the adhesive could give better device performance.

2.1.2 Printable semiconductors

Significant progress has been made in material research in the development of printable semiconductor materials over the past decades. Organic semiconductors, CNTs, and inorganic semiconductor nanomaterials have been developed into printable forms and the device performance is continuously improving. This section reviews different types of semiconductor materials that have been applied with printing technology.

2.1.2.1 Organic semiconductors

Organic materials have been part of the electronics industry since the first MOSFET and they have already been applied as active semiconductor material through a demonstration of polythiophene-based thin-film transistors²⁸ as early as 1986. Since then, remarkable progress has been made in printed organic transistors through innovative design of printable organic semiconductors, and applications including flexible displays/e-paper¹, RFID tags², and disposable chemical sensors^{3, 4} become possible for this type of material. Organic semiconductors also have a unique feature to generate additional functionality by intelligent material design through different synthetic approaches, representing the possibility of true material engineering.

Among many printable organic semiconductors that have been synthesized, three commonly used organic semiconductors, poly(3-hexylthiophene) (P3HT)²⁹, poly (3,3'''-didodecylquaterthiophene) (PQT-12)³⁰, and solution-processed pentacene precursor (TIPS-pentacene)³¹ are shown in Figure 2.3.

Figure 2.3 Molecular structures of three commonly used organic semiconductors: poly(3-hexylthiophene) (P3HT), poly(3,3''-didodecylquaterthiophene) (PQT-12), and solution-processed pentacene precursor (TIPS-pentacene).

P3HT is the most widely studied printable organic polymeric semiconductor. When the 3-alkyl substituent is incorporated into a polymer chain with only head-to-tail linkages, the resulting product is regioregular polymer, which self-orientates into a well-ordered lamellar structure. TFTs based on regioregular P3HT show excellent mobility of $0.1 \text{ cm}^2/\text{V s}$ and an on/off ratio about 10^6 in an inert atmosphere. However, this type of polythiophene has a poor on/off ratio in air, because it is sensitive to moisture and ambient oxidative doping. Due to this drawback, there have been efforts to design and synthesize a novel printable polymeric semiconductor other than P3HT, by placing the alkyl side-chains

strategically along the polythiophene backbone, to tune the π -conjugation and thus, increase its ionization potential. PQT-12 is one of the outstanding products resulting from these efforts, and PQT-12 TFTs show better performance (in air: mobility = $0.14 \text{ cm}^2/\text{V s}$, on/off ratio = 10^7) and stability in air. PQT-12 is a class of liquid crystalline regioregular polymeric semiconductor that can be prepared with the quaterthiophene monomer (3,3'''-didodecylquaterthiophene) by FeCl_3 -mediated oxidative coupling polymerization. The material can be dissolved in a proper solvent, and the resulting solution can be used to solution-deposit the polymeric semiconductor on different surfaces using spin coating or drop coating. The semiconductor layer is found to be composed of extensive crystalline domains of lamellar π - π stacks, yielding TFT devices with excellent device performance. TIPS-pentacene is a solution-processed precursor based on pentacene, which is one of the benchmark organic semiconductor materials due to its routinely obtainable TFT mobilities higher than $1 \text{ cm}^2/\text{V s}$. Remarkably, when this precursor is solution-deposited and heated at moderate temperature to produce pentacene TFTs, the devices show mobility as high as $1 \text{ cm}^2/\text{V s}$. For this type of material, thin-film growth, morphology, and substrate property have been shown to have an impact on device performance.

2.1.2.2 Carbon nanotubes

CNTs³² are one-dimensional molecular-scale tubes of graphitic carbon with either semiconducting or metallic electronic states.³³ Both experiments and

theory have shown that SWCNTs possess high mobility^{34, 35} and tube diameter-dependent band gap for semiconducting nanotubes.^{36, 37} CNTs have been fabricated into field-effect transistors and have demonstrated extraordinary carrier mobility. Because of their excellent electronic properties, CNTs have been dispersed into suspension/solution to make printable CNT inks. However, solution phase deposition processes have, so far, not given such good devices, as low-density films with high on/off ratios ($10^4 - 10^5$), don't have very high mobility and densely packed films give poor on/off ratios.^{13, 38} Figure 2.4 shows a schematic of the devices and the corresponding device micrographs taken by AFM or optical microscope.

Figure 2.4 The schematic of the device structure/fabrication procedures and the corresponding device micrographs taken by AFM or optical microscope. (Reproduced with permissions from Ref. 13 Copyright © 2005, American Chemical Society, Ref. 51 Copyright © 2010 WILEY and Ref. 24 Copyright © 2004, American Institute of Physics)

The early demonstrations of solution-deposited CNT TFTs show mobilities lower than $1 \text{ cm}^2/\text{V s}$ and on/off ratios around 100.^{13, 39} Solution-deposited CNTs have also been integrated in stamp-based and inject printing technologies. The performance of TFTs fabricated by a PDMS-stamp-based

transfer printing process in combination with solution-deposited CNTs^{40, 41} is generally the same as the early demonstrations, while the latest inkjet-printed TFTs show better performance ($2 - 5 \text{ cm}^2/\text{V s}$, 10^3 on/off ratio) by fine tuning the density of CNT films as transistor channels.⁴²

In addition to the good semiconductor properties described above, CNTs in the form of thin-films also exhibit extreme mechanical bendability⁴³, excellent optical transparency⁴⁴, and good interfaces with other organic electronic materials⁴⁵, and as a result, this class of materials has been applied in printed electronics as both conductors or semiconductors.

2.1.2.3 Semiconductor nanomaterials

Semiconductor nanomaterials are another class of materials that are considered promising for printed electronics⁴⁶⁻⁴⁹ due to their well-developed synthesis processes and the ability to tailor material properties through shape, size, and atomic-composition control and have attracted much research effort due to their intriguing physical properties and attractive potential as building blocks for nanoscale electronics⁵⁰. Three major types of materials can be included in this class of materials: Si/Ge nanomaterials, group III-V nanowires and nanoribbons (GaAs, InP, GaN), and group II-VI nanomaterials (ZnO). These semiconductor nanomaterials are typically grown with a chemical vapor deposition (CVD) method, and the grown materials have high crystallinity because growth relies on the packing of the atoms/molecules along energetically preferential

directions^{51, 52}. The high quality in the crystal structure in turn renders them with excellent electronic properties for applications in printed TFTs⁴⁸.

As these nanomaterials are typically grown on silicon wafers by CVD method under temperature, the use of them in printed electronics usually involves a deposition/printing step. PDMS-stamp-based dry transfer printing is the most commonly used technique. This approach uses a rubber stamp produced by the methods of soft lithography⁸ to retrieve semiconductor materials from a source substrate and deliver them to target device substrate^{53, 54}. These semiconductor nanomaterials can often be processed in solution, and a solution assembly process is used to deposit semiconductor materials on a variety of substrates, including glass and plastics, to fabricate high-performance printed TFTs and high-frequency circuits. In this approach, nanostructured semiconductors with good crystallinity and controlled dimensions are synthesized using a CVD process with high temperature on silicon wafers, and are then collected and dispersed in an organic solvent. The nanomaterial solution is then used for the subsequent assembly on the target substrate. For example, a fluidic-flow-directed assembly approach incorporates microfluidic channels to enable the directional flow of a solution on the surface of the substrate, resulting in the assembly of nanomaterials^{48, 55, 56}. The assembly of the nanomaterials is then processed and metalized with contacts to produce functional TFTs.

2.2 Printing processes

A variety of printing processes have been used to fabricate printed TFTs. Each process has different attributes with advantages and disadvantages regarding reliability, device performance, resolution, registrations, and limitations in target substrates. For example, contact printing has been demonstrated in fabrication of printed TFTs, but tends to have poor registration accuracy for multilayered devices. In this section, different processes used to fabricate printed TFTs will be reviewed.

2.2.1 Photolithography

Photolithography has a long history in the high-performance silicon based semiconductor electronics industry. Although it is not a printing process, it is widely used in research to benchmark test material properties in printed electronics. It uses light to selectively remove parts of a light-sensitive chemical “photoresist” (a mixture of polymers that becomes soluble or insoluble when exposed to UV light) and transfers a geometric pattern from a photomask to the photoresist. In this process, the substrate of interest is coated with photoresist and irradiated with light projected through the photomask, which is a plate with a defined pattern that allow light to partially shine through with the same pattern. Chemical changes occur in the exposed photoresist, inducing a change in solubility. This latent image is then developed for example by rinsing with an appropriate solvent to remove the exposed photoresist (positive photoresist) or to remove the unexposed photoresist (negative photoresist). The remaining

photoresist forms a stable polymeric pattern on the substrate and areas of the underlying substrate that are not protected by the photoresist pattern may be etched or doped or materials may be selectively deposited on the substrate through a “lift-off” process. After processing, the remaining resist may be stripped and usually many photolithographic processes may be performed to create complex devices (up to 50 times in complex integrated circuits). Due to the large number of photolithographic processes needed in IC manufacturing, photolithography typically accounts for about 30 percent of the cost of manufacturing.

The general sequence of the processing steps for a typical optical lithography process is as follows: substrate preparation, spin-coating of photoresist, exposure, development, and following intended operations such as “lift-off”, etching or doping. The schematic of the photolithography process is shown in Figure 2.5.

Figure 2.5 Schematic of the photolithography process. First, a light sensitive chemical “photoresist” is coated on the substrate. Then, the photoresist is selectively removed using photomask and UV exposure to form the desired pattern on the substrate. Lastly, the pattern can be transferred onto the substrate or other materials on the substrate through lift-off or etching.

The disadvantages of photolithography determine that it’s not suitable as manufacturing process for printed electronics. The cost of photolithography introduced by its requirements for clean room environment, expensive photolithographic tools and photoresists, and intensive labor is too high for printed electronics whose target products are low to medium performance devices. Photolithography is not able to create patterns on large-area substrates.

Photolithography process became technologically mature on 300mm diameter wafer only recently while printed electronics requires even larger-area substrates. The harsh environment in the development step using organic solvents can cause damage to most organic semiconductors²⁷. Photolithography is originally designed for flat substrates and it is not very effective at creating patterns on flexible substrates. Alternative fabrication processes have been developed for printed electronics to overcome the above disadvantages.

2.2.2 Microcontact printing (μ cp)

μ cp is one of the most studied unconventional microfabrication processes. The process uses a soft elastomeric stamp to bring molecules in some ink to a surface and forms a pattern replicating the pattern of the stamp protrusions through conformal contact. The pattern was then used as an etching mask, or a dewetting pattern, or a catalyst to pattern functional device components. Typically, inks employed in μ cp are chosen to form self-assembled monolayers (SAMs) after or during the printing. These materials include alkanethiols on gold, silver and copper^{57, 58}, alkylsiloxanes on hydroxyl-terminated surfaces such as silica⁵⁹ and alkanephosphonic acids on aluminum⁶⁰. Typical application of μ cp in fabrications of printed TFTs is to use SAM layers as ultrathin masks for subsequent wet etching to form metal contacts in TFTs. Figure 2.6 shows a schematic of creating metal contacts for printed TFTs using μ cp.

Figure 2.6 Schematic of creating metal contacts for printed TFTs using μ cp.

Generally, PDMS is used as the material for elastomeric stamps and PDMS stamps can be replicated from silicon master templates. Ink containing SAM molecules is applied to the PDMS stamp. The application of ink onto the PDMS stamp usually has two varieties: ink solution is directly applied onto the PDMS stamp followed by drying; ink solution is applied onto another PDMS slab used as “ink pad”, which is used to apply the ink onto the PDMS stamp. The inked PDMS stamp is then brought into contact with the metal layer to be patterned as metal contacts in printed TFTs. Given some amount of time, SAM layer with the same pattern as stamp protrusions formed on top of metal layer

due to the inherent strong binding between ink molecules and metal layer, and the patterned SAM layer is used as etching mask to remove the exposed metal. The resulting metal patterns are used as contacts in printed TFTs. This process usually defines the source and drain electrodes, normally for printed TFTs in bottom-contact geometries. There are other ways of applying μ cp in fabrication of printed TFTs. High/low energy surface patterns can be used to define the placement of semiconductor islands deposited from a flooding methanol solution by dewetting⁵⁹. μ cp has also been used to deliver the semiconductor layer itself⁶¹. The quality of the semiconductor film is tied to the surface characteristics of the dielectric, as well as the specific delivery method used⁶¹.

Early demonstrations of printed TFTs show that the typical resolution of this process is relatively low ($20\text{ }\mu\text{m}$)⁵. Significant research has been focused on the development of μ cp process. Printed TFTs using P3HT as active semiconductor material using μ cp has been demonstrated⁹. Large-area μ cp has been demonstrated by applications in flexible displays with an array of 256 pentacene transistors¹. μ cp has its own limitations: firstly, specific surface chemistry is required between ink material and substrate, which means different ink molecules have to be selected or designed for different materials to be patterned. The ink molecule must have strong binding onto the underlying materials to be patterned in order to form intact SAM patterns. The best-established system to date for μ cp is based on alkanethiolates on gold and silver and alkylsiloxanes on hydroxyl-terminated surface⁸. Although the resolution capability of μ cp is down to submicron scale, the resolution of large-area μ cp is

still limited¹. Distortions are prone to be introduced and thus, the handling of PDMS stamps is restricted in order to minimize distortions.

2.2.3 Inkjet printing

Beginning shortly after the commercial introduction of inkjet technology in digital-based graphic art printing, there has been interest in developing inkjet printing for manufacturing of physical parts in microelectronics such as etch resists and adhesives^{62, 63}. Inkjet printing has its advantages in (i) purely additive operation, (ii) efficient materials usage, and (iii) scalability to large substrate sizes and continuous processing (e.g., reel to reel). There are generally three types of inkjet printing, namely, thermal, piezoelectric, and electrohydrodynamic inkjet printing.

Thermal inkjet printing uses electrical pulses applied to heaters that reside near the nozzles and generates joule heating to vaporize the ink locally (heating temperature ~ 300 °C for aqueous inks). The bubble forms near the heater and then expands rapidly (nucleate boiling process). The resulting pressure impulse ejects ink droplets through the nozzle before the bubble collapses. Figure 2.7 illustrates how a thermal inkjet printer eject ink droplet using heaters. The process time of bubble formation and collapse is typically within 10 μ s and thus, the heating would not degrade the properties of inks, not even for temperature sensitive inks⁶⁴⁻⁶⁶.

Figure 2.7 Schematic of thermal inkjet printing uses heaters to eject ink droplet.

Piezoelectric inkjet printing uses electrical pulses applied to the piezoelectric element create pressure impulses that rapidly change the volume of the ink chamber to eject droplets without heat generated. The piezoelectric actuation offers considerable control over the shape of the pressure pulse, enabling optimized, mono-dispersed droplet production⁶⁷. Figure 2.8 shows a schematic of piezoelectric inkjet printing using electrical pulses applied to the piezoelectric element and creating pressure impulses to eject droplets.

Figure 2.8 Schematic of piezoelectric inkjet printing using electrical pulses applied to the piezoelectric element create pressure impulses to eject droplets.

The above two types of inkjet printing is often referred to as conventional inkjet printing and the resolution capability of these inkjet printing techniques is limited ($\sim 20 \mu\text{m}$)⁵⁰ since the size of nozzle must be sufficiently large to avoid clogging. Electrohydrodynamic inkjet printing is developed with the capability of generating small jets from big nozzles to improve resolution capability. In this type of inkjet printing, a conducting metal film coats the nozzle in this system, and the substrate rests on a grounded electrode. When a voltage is applied between the metal-coated nozzle and the grounded electrode, surface charges accumulate at the liquid meniscus near the end of the nozzle, deforming the sphere into cone. A jet with a diameter smaller than the nozzle size emerges from the apex of this cone with sufficient voltage⁶⁸. By controlling the applied voltage and substrate position relative to the nozzle, this jet can be used to write patterns of ink onto the substrate with better resolution^{69, 70}. This type of high-

resolution printing has been demonstrated for electronic device fabrications with feature size of $\sim 2 \mu\text{m}$ ⁷⁰.

Figure 2.9 Schematic of electrohydrodynamic inkjet printing using electrical field to generate small jets from big nozzles to improve resolution capability. (Adapted with permission from Ref. 80, Copyright 2007 NATURE PUBLISHING GROUP)

For all types of inkjet printing, the physical properties of the ink are important for high-resolution inkjet-printed patterns. First, to generate droplets with micrometer-scale diameters (picoliter-regime volume), the ink must be provided with sufficiently high kinetic energies^{65, 66} exceeding the interfacial energy. Because of this, printing high-viscosity inks is difficult, due to viscous

dissipation of kinetic energy supplied. Second, high evaporation rates in the inks can locally increase the viscosity at the nozzles, which may lead to clogging. The wetting behavior, together with the volume and positioning accuracy of the ink droplets, influences the resolution. Photolithographic process to creating wetting patterns is sometimes used with inkjet printing for better resolution, but in that case, the fabrication process is not attractive to printed electronics anymore.

Inkjet printing can also be applied to certain organic semiconductors and gate insulators^{71, 72}, where printing of the semiconductor can be more challenging than that of other device components due to the difficulties in controlling morphology, wetting, and evaporation process. Inorganic inks have been inkjet-printed for printed electronics, too. For example, suspensions of Ag, Cu, and Au nanoparticles⁷³⁻⁷⁵, CNT inks⁴² and silicon nanowire inks⁷⁶ has been printed to produce continuous electrode lines, conductive contacts and active semiconductors.

The primary limitation of inkjet printing is its resolution capability. While the conventional inkjet printing has a resolution limit of $\sim 20\text{ }\mu\text{m}$, relatively new electrohydrodynamic inkjet printing pushes the limit down to sub-10 μm range with carefully optimized parameters, but the equipment setup for the new type of inkjet printing is more sophisticated. Inkjet printing also poses stringent requirements on substrate surface properties and ink physical properties for optimized pattern formation and minimized feature size.

2.2.4 Transfer printing

A set of printing methods can be classified as “transfer printing”. This class of printing processes is capable of depositing several types of material including conductors, semiconductors, and dielectrics in printed electronics. Functional TFTs fabricated solely by transfer printing processes have been demonstrated. The process generally involves a stamp, either hard or elastomeric, that can support functional materials and can be contacted to a target substrate. During the contact, some mechanism, including surface chemistry, non-covalent Van Der Waals force, and enhanced adhesion by additional adhesives, is used to transfer the functional materials onto the target substrate. A generalized schematic is shown in Figure 2.10.

Figure 2.10 Generalized schematic for transfer printing.

One of the most studied transfer printing processes that rely on surface chemistry is nanotransfer printing (nTP). It begins with evaporation of metal onto elastomeric stamp. Then, the metal-coated stamp forms conformal contact

with a chemically treated target substrate and chemical bonds such as condensation reactions between hydroxyl groups^{25, 26} and thiol-metal reactions^{77, 78} forms between metal and target substrate. Upon removal of the stamp, the metal remains tightly bonded onto the target substrate, producing the desired pattern for device fabrication. This process, with arguably better resolution than μ CP, reaching sub-100 nm range, has been employed to form source and drain electrodes in printed OTFTs with 1 μ m transistor channel^{10, 40, 79}. The device performances reach levels comparable or nearly identical to those in devices fabricated by conventional means such as shadow-mask evaporation.

Non-covalent transfer printing relies on a physical interfacial energy difference between the interface at the substrate surface and the interface at the stamp surface. The process does not require surface chemistry at the interface or surface treatment to the target substrate, but it seems that the transfer is less reliable and has critical requirements on the conformal contact between stamp and target substrate. Low roughness on the substrate surface, which can provide good contact between the target surface and the transferred materials, is also important for good transfer⁴⁰. It is also believed that the segregation of siloxane oligomers at the interface between functional material and stamp could facilitate release. Because the binding strength between the transferred materials and the substrate is low, there are several ways to enhance the transfer. Sacrificial layer can be introduced between the functional material and the stamp, and then removed after stamp-target substrate contact is established to facilitate the release of the functional materials. CNT network transistors

have been transferred to polymer supports by using silicon oxide as the sacrificial layer for the release of both CNT network and metal contacts. The printed TFTs can be bent through at least 60° angles without damaging device performance. The devices operate as p-type TFTs showing mobilities of 12 cm²/V s⁸⁰. High temperature can be used to enhance the bonding strength between functional materials and polymeric receiving surface. Generally, temperature near glass transition temperature (T_g) of the polymeric receiving surface is sufficient⁸¹ and the mechanism behind is that the polymeric receiving surface behaves like a viscous liquid at T_g and active polymer chain movement on the receiving surface will ensure better penetration of polymer chains into functional material surface, providing intimate contact with the functional materials. A similar approach is to use the vapor of the solvent of the receiving surface material to enhance bonding strength. The receiving surface material is swollen by the vapor treatment and the absorption of the solvent vapor lowers the T_g of the material to have more active polymer chain movement at relatively low temperature to provide intimate contact with the functional materials⁸². In the transfer printing process, there is usually a step of depositing functional materials onto the stamp before the actual transfer step. For metal deposition, vacuum evaporation is used most of the time. For materials such as semiconductor nanomaterials, which usually are produced on another solid substrate, undercut etching can be applied to facilitate the deposition⁸³ because for non-covalent transfer printing, the adhesion between the stamp and

functional material is poor. Kinetic control is another way to temporarily amplify the adhesion on stamp for deposition step⁸⁴.

Adhesives can be applied to improve transfer efficiency on large-area⁸⁵ or to add features such as faster transfer⁸⁶. One type of adhesive is UV resins which polymerize quickly upon UV exposure, normally within seconds, to significantly shorten the transfer time. In the process, before the contact is initiated, a mixture of liquid monomers EB600, SR508, and SR351 is spin-coated onto the flexible substrate and subsequently hardened by UV exposure. The transferred metal contacts are used as source and drain electrodes in printed TFTs with mobility of $0.0016 \text{ cm}^2/\text{V s}$ and 100 on/off ratio using P3HT as the active semiconductor. Because of the application of liquid adhesives, hard silicon mold can be used as the carrier for the functional materials⁸⁶.

Figure 2.11 Schematic for UV transfer embossing using UV resin as adhesive.

2.2.5 Other printing techniques

This section reviews a few unconventional patterning techniques that have been applied in printed electronics. These techniques, though with attractive features such as high-resolution patterning capability, have some obvious disadvantages for printed electronics and thus less studied for applications in printed electronics. Nanoimprint lithography⁸⁷ is a method of fabricating nanometer scale patterns originally for high performance silicon electronics. Compared to photolithography, it is a relatively simple nanolithography process with low-cost, high-throughput, and high-resolution. Patterns are created by mechanical deformation of imprint resist, typically a monomer or polymer formulation that is thermoplastic or UV curable, and subsequent residual resist removal step. When using UV curable resists, the process is often termed as UV embossing. One of the shortcomings that hinder the application of this process in printed electronics is the high pressure and high temperature involved in the process, as well as the resulting high cost of the process. The high-resolution capability is attractive to the high performance silicon electronics industry but it's less attractive in printed electronics as short-channel effect is easily induced in printed electronics where thicker polymer dielectric materials is used⁸⁸

Figure 2.12 Schematic of nanoimprint lithography.

Cold welding is another process with high-resolution patterning capabilities. It occurs when two clean metal surfaces meet with applied pressure (~ 150 MPa), the surfaces conform to each other in vacuum so that the gap between the two surfaces approaches inter-atomic distance and metallic bonding takes place without heating at the interface. Top-contact pentacene TFTs with gold electrodes have been fabricated by cold welding. To achieve top-contact structure, a “strike layer” was deposited directly on top of pentacene and then cold welding was used to define the source and drain electrodes with channel length as short as $1\ \mu\text{m}$ ⁷⁹ the device exhibited significant nonlinear large contact resistance at the gold-pentacene interface. The shortcomings of cold welding in printed electronics includes: firstly, the plasma etching process to remove the “strike layer” from the channel is invasive to pentacene; secondly, the high contact pressures required for cold welding may cause structural damage to the device.

Figure 2.13 Process illustration of cold welding. (Reproduced with permission from Ref. 90, Copyright © 2002, American Institute of Physics)

Capillary molding is a process in which microfluidic channels form by laminating a mold against a flat substrate and liquid materials can be filled into the channels. Capillary molding or external pressure can be used for the filling process. After the liquid is solidified through solvent evaporation and the solid materials are delivered to the substrate surface, the mold is removed to complete the fabrication. This process has been used to pattern source and drain electrodes made of carbon paste and polyaniline in order to fabricate printed P3HT TFTs⁸⁹. The performance of these transistors compares favorably with that of similar devices constructed using conventional methods. This process requires that the microfluidic channels should be liquid-tight and the channel formation is reversible, thus the technique is usually performed with elastomeric stamps, such as PDMS stamps. It is also problematic when

patterning viscous liquids since the filling process can be slow or impossible without additional means such as vacuum application on the other end of the channel⁹⁰ and heat treatment⁹¹.

Figure 2.14 Capillary molding using PDMS mold and liquid materials.
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Chapter 3 Experimental approaches

3.1 Materials and equipments

3.1.1 Materials

Sulfuric acid (H_2SO_4) (ACS reagent, 95.0-98.0%), hydrogen peroxide (H_2O_2) (ACS reagent, solution contains inhibitor, 30 wt. % in H_2O), acetone (Laboratory Reagent, $\geq 99.5\%$), ethanol (Laboratory reagent, $\geq 99.5\%$), isopropyl alcohol (IPA), 1H,1H,2H,2H-Perfluorooctyltriethoxysilane ($\geq 98\%$), Indium tin oxide (ITO) coated PET sheet (surface resistivity $60 \text{ } \Omega/\text{sq}$), *N,N*-Dimethylformamide (DMF) (ACS reagent, $\geq 99.8\%$), hexane (Laboratory Reagent, $\geq 95\%$), toluene (ACS reagent, $\geq 99.5\%$), chloroform (ACS reagent, $\geq 99.8\%$), pentacene (triple-sublimed grade, $\geq 99.995\%$ trace metals basis), poly(vinyl alcohol) (PVA) (average Mw 130,000, 99+% hydrolyzed), poly(4-vinylphenol) (PVP) (average Mw $\sim 25,000$), methylated poly(melamine-co-formaldehyde) (average Mn ~ 432 , 84 wt. % solution in 1-butanol) were purchased from Sigma-Aldrich. Deionized (DI) water ($\geq 18 \text{ M}\Omega \text{ cm}$) from Millipore Q water purification system was used in all experiments. PDMS Sylgard 184 was purchased from Dow Corning (Midland, MI, USA). Silicon wafers were purchased from Bonda Technology (Singapore) and used as substrates/gate electrodes or fabricated into silicon molds. Solution of KI and I₂

in DI water ($\text{KI}:\text{I}_2:\text{H}_2\text{O}=4:1:100$) was used as etchant to remove unprotected gold and produce desired pattern with a typical etching time of 2 minutes. Decon90 purchased from Decon Laboratories Limited (Hove, East Sussex, UK) was used as cleaning agent for ITO. Different components in UV resin were purchased from UCB, Sartomer and Ciba Specialty Chemicals and formulated accordingly in different experiments. SU-8 25 photoresist (MicroChem) was used as the structural material in SU-8 mold. CNT solution was prepared by dispersing commercially available enriched SWCNTs (Nanointegris) of 99% purity in DI water with SDS as surfactant and a concentration of $\sim 0.34 \mu\text{g/mL}$. Preparation of PQT-12 is detailed in Ref ³⁰. Briefly, quaterthiophene monomer (3,3'''-Didodecylquaterthiophene) was polymerized by FeCl_3 -mediated oxidative coupling polymerization and the polymer was then washed with water, precipitated with acidic ethanol and filtered. The product was further extracted and purified with heptane and chlorobenzene to give electrically pure 0.3 wt % PQT-12 solution in chlorobenzene for OTFT fabrication. All chemicals used in PQT-12 synthesis process were also purchased from Sigma-Aldrich.

3.1.2 Equipments

Mask aligner (Karl Suss MA6) was used in photolithography, which combines with Deep Reactive Ion Etcher (Surface Technology Systems, Newport, UK), to fabricate silicon molds.

Oxygen plasma treatment was conducted in a March PX-500 cleaning system to clean or activate different surfaces.

Deposition of gold, aluminum and other metal films was performed on explorer series sputtering system (Denton Vacuum, Moorestown, NJ, USA).

UV irradiation was provided by an UV flood cure system to cure UV resin and cross-link acrylate mixture.

Spin-coating was performed on a G3P-8 spin-coater (Specialty Coating Systems, Indianapolis, IN, USA) to deposit polymeric thin-films.

Atomic force microscopy (AFM) measurements of nanocomposite film thickness were performed on a Dimension 3100/Nanoscope IIIa (Digital Instruments, Santa Barbara, CA, USA) in tapping mode to characterize the morphology of the samples, to measure the thickness of thin-films and to characterize the printed devices.

JSM-6700F field emission scanning electron microscopy (FE-SEM) (JEOL Ltd., Tokyo, Japan) was used to characterize the surface and cross-section of nanocomposite films and to measure the feature size of the printed devices.

Agilent 4284A precision LCR meter (Agilent, Santa Clara, CA, USA) was used to measure the unit area capacitance of different dielectric layers.

Summit series probe station (Cascade Microtech, Beaverton, OR, USA) and Agilent E5270B Semiconductor Parameter Analyzer System (Agilent, Santa

Clara, CA, USA) was used to produce device performance data of printed devices.

Annealing process of PQT-12 was performed in EYELA VOS-201SD vacuum drying oven (Tokyo Rikakikai, Tokyo, Japan).

SMZ1500 optical microscope (Nikon Instruments Inc., Melville, NY, USA) was used to characterize the transferred gold patterns for defect analysis.

3.2 Methodology

3.2.1 Preparation of silicon mold

Silicon mold was fabricated by standard photolithographic procedure described in Chapter 2 followed by deep reactive ion etching (DRIE) process with typical etching depth of 100 – 150 μm . To facilitate the transfer process or minimize the adhesion of undesired particles such as cross-linked acrylate polymer, the mold was modified with a passivation layer produced by immersing the mold in 0.5 – 1 mM solution of 1H,1H,2H,2H-Perfluorooctyltriethoxysilane in ethanol or hexane for 8 hours. The process can produce a self-assembled monolayer (SAM) of the silane molecules on the mold. Figure 3.1 shows a simplified schematic to illustrate the preparation procedure. Water contact angle measurement was used to check the surface property of the mold, which typically had a very hydrophobic surface with a typical water contact angle of close to 120° after creation of the passivation layer. The passivated mold can be used directly or 100-nm-gold was sputtered onto the passivated silicon template

or transfer printing processes. The passivated mold is re-usable after proper removal of metal layers and a simple cleaning step by sonication in acetone.

Figure 3.1 Simplified illustration of the silicon mold preparation procedure.

3.2.2 Surface treatments

Surface treatments are conducted in order to control the adhesion strength between two surfaces as required in different printing processes by modifying one or both of the surfaces. The treatment methods include formation of SAM as passivation layer on silicon mold as described in the previous section and oxygen plasma to activate a surface for better adhesion for PVP and PET substrates or higher reactivity for silicon molds before SAM passivation layer. The reason is that the plasma-introduced polar functional groups including radicals, hydroxyl, carbonyl, and carboxyl groups on different surfaces, which

increase their surface free energies ⁹² to boosts nominal work of adhesion between them and another surfaces for better adhesion⁹³. Before plasma treatment, the surfaces were usually cleaned by ultrasonication in acetone, ethanol and DI water, each for 20 minutes, and then plasma treatment was applied with different parameters for different purposes. The details will be specified in the following chapters.

3.2.3 Materials deposition

Spin coating was used as a common material deposition method for different materials such as photoresists, UV resin, dielectric layer and solution-processable semiconductor layer. The parameters for spin-coating was determined by considering the estimated resulting thin-film thickness and the concentration/viscosity of the solutions and using an empirical formula correlating the thin-film thickness with spin speeds concluded by C. J. Lawrence for polymer solutions as follows (26):

$$h_f \propto \Omega^b, \quad (3.1)$$

where h_f is the resulted polymer film thickness, Ω is the spin speed with unit of revolutions per minute (RPM) and b is an empirical constant of -1/2. The formula was concluded based on the experimental results of spin coating different polymer solutions with different solvents on silicon wafer and measuring film thicknesses with ellipsometry.

Sputtering is a process whereby atoms are ejected from a solid target material due to bombardment of the target by energetic particles (argon plasma) and atoms can be ejected for thin-film deposition when energy exchange between the energetic particles and atoms in the materials exceeds the surface binding energy. Sputtering process performed on Denton Vacuum explorer series sputtering system was used to deposit metal layers such as aluminum and gold, which would be further used as electrodes in transistor or capacitor devices.

Physical vapor deposition (PVD) is a purely physical method to deposit thin films by the condensation of a vaporized form of the material such as metal or small molecular organic semiconductors onto various surfaces. Specifically, pentacene was deposited by evaporative deposition in which pentacene was heated to a high vapor pressure by electrically resistive heating in low vacuum and the thickness of the pentacene thin-film was 60-65nm for a good balance between mobility and on/off ratio.

Deposition of CNT network on gold-coated silicon mold was conducted by drop-coating process, in which CNT solution droplets were placed using a pipette on protrusions of gold-coated silicon mold. The solvent (DI water) was then evaporated in a 70°C oven to leave dry CNT network on Au-coated silicon mold. After that, the mold with coated CNT network was briefly soaked in DI water for 10 seconds to remove surfactants. The drop coating, drying and soaking steps were repeated for three times.

3.2.4 Thin-film transistor characterization

Before the electrical characterization of transistors, printed micropatterns were examined by different microscopic techniques. Optical microscope was used to characterize the printed patterns on a larger scale, mainly for defect analysis purpose, e.g., whether the pattern was intact, were there defects on the printed pattern and the possible reason such as dirt or other microparticles, what was the size of the defects and foreign particles, or were the patterns completely broken or just had minor defects. Due to the resolution capability, the optical microscope was not used as the sole equipment in determination of the feature size of the printed patterns such as channel length, which was on micrometer scale. In this case FE-SEM and AFM was used to precisely determine the micron-scale feature size of the printed patterns and sub-micron scale edge roughness of the patterns for resolution limit.

Printed TFT devices were characterized using Agilent E5270B Semiconductor Parameter Analyzer System and probe station; all characterizations were conducted in ambient air. At two types of device performance curves were obtained after characterization: transfer characteristic curve and output curve. The transfer characteristics curve (I_D - V_G) was obtained by sweeping gate voltage in a range while keeping drain voltage at a constant value and drain current was plotted against gate voltage for the curve. The output curve (I_D - V_D) was obtained by measuring drain current when drain voltage was swept in a

range and gate voltage was stepped on several different voltages. By plotting drain current against drain voltage, the I_D - V_D curve can be obtained.

In order to extract transistor performance parameters such as mobility and on/off ratio, unit area capacitance of dielectric layers was measured separately. In more detail, dielectric layers were deposited with the same spin-coating parameters onto ITO-coated glass and 100 nm Al film was deposited by sputtering on top of the dielectric layers to fabricate ITO-insulator-Al capacitors with a size of 2 mm $\times$ 2 mm. The capacitance was then measured by Agilent 4284A precision LCR meter and adjusted into the unit of F/cm².

In study of contact resistance in printed TFTs, transmission line model was used by measuring drain current with fixed drain voltage and calculating resistance between the source and drain electrodes for different channel lengths. Different gate voltages were usually applied for more accurate estimation of contact resistance.

Chapter 4 Improved UV transfer embossing for bottom-gated organic TFTs^a

4.1 Introduction

To lower the cost of printed organic electronics⁹⁴⁻⁹⁶, it is important to develop fabrication processes that do not rely on clean room and that are compatible with solution processable dielectric materials and organic semiconductors¹². Cold welding methods, both subtractive and additive, developed by Forrest's group^{79, 94, 97} are capable to transfer metallic patterns on submicron scale by applying high pressure to form metallic bonds at the conformal contact area. In the additive cold welding method, a strike layer for facilitating the bonding process requires a gentle etching or simple sputtering process to be removed. Inkjet printing is an alternative technique to photolithography that has recently reached submicron scale resolution⁹⁸; this process, however, requires a chemically modified ink to fabricate ultra-hydrophobic electrodes and post-printing sintering at a high temperature to increase the conductivity of the electrodes. Screen printing and μ cp have been actively investigated by different research groups⁵, but these techniques are limited to low resolution of $\sim 20\text{ }\mu\text{m}$,

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especially on large-area substrates. Nanotransfer printing (nTP), developed by rogers' research group as advances of μ cp, offers a better resolution (~ 100 nm) comparing to μ cp^{10, 11} due to the elimination of vapor phase transport of ink materials. The process utilizes the surface chemistry or noncovalent forces between the receiving surface and transferred metal to form the source and drain electrodes in printed OTFTs^{40, 78}.

Ultraviolet (UV) transfer embossing at room temperature with a resolution (~ 2 μ m) comparable to lithography process⁸⁶ was demonstrated as a fast and efficient printing process OTFT devices. It does not require clean room environment and is capable of achieving high-resolution features on micron-scale. The embossing template fabrication itself does require clean fabrication conditions, but once it is made, it can be used repeatedly to produce printed OTFTs under less stringent conditions. However, the previously fabricated top gate devices, regardless of using P3HT or poly(3,3''-didodecyl quaterthiophene) (PQT-12) as organic semiconductors, have relatively low device performance of mobility (μ) of $0.001\sim 0.002$ $\text{cm}^2/\text{V s}$ and on/off ratio of 10^2 ⁸⁶. The poor performance is attributed principally to the roughness between the PVP dielectric and the semiconductor; this is propagated from the relatively rough PET substrate surface through the thin semiconductor film. The high roughness at the dielectric-semiconductor interface significantly perturbs the structure of the semiconductor and forms many charge carrier traps. Further, the top-gated configuration, which requires deposition of the organic semiconductor prior to the deposition of the poly(4-vinylphenol) (PVP)

dielectric, prevents thermal cross-linking of the dielectric since that would damage the underlying semiconductor (the typical cross-link temperature for PVP is above 150 °C, which would degrade the semiconductor⁹⁹), with the consequence of high leakage current through the dielectric layer.

Here, the UV transfer embossing process was optimized by fabricating bottom gate devices with a resolution of $\sim 2 \mu\text{m}$ which exhibit much improved device performance. Bottom gate devices allow deposition of PVP dielectric before semiconductor deposition. Figure 4.1 shows a schematic illustration of the fabrication process for bottom gate devices by our UV transfer embossing process.

Figure 4.1 Schematic illustration of the UV transfer embossing process in fabrication of bottom gate devices: (I) ITO coated PET films are cleaned in

detergent; (II) PVP with MPMF is spin-coated on top of ITO and cross-linked in an oven followed with O₂ plasma treatment; (III) UV resin is spin-coated on PVP; (IV) Si embossing mold and UV resin coated substrate are brought into contact and exposed to UV light; (V) Source and drain electrodes are transferred onto PVP after demolding; (VI) Semiconducting polymer is drop-coated to complete device fabrication.

4.2 Materials preparation and process details

4.2.1 UV resin

The UV embossing resin was a mixture of epoxy bisphenol-A diacrylate (Ebecryl 600), dipropylene glycol diacrylate (SR 508) and trimethylolpropane triacrylate (SR 351) with weight ratio of 12:5:3 diluted (50 wt %) in isobutylmethylketone (IBMK). Ebecryl 600 was supplied by UCB chemicals and SR 508 and SR 351 were supplied by Sartomer. Our UV resin mixture offers a fast curing response, good adhesion and superior cured film strength. This formulation was chosen also because the contact between UV resin and PVP thin film was good enough for the deposition of UV resin on PVP via spin coating.

4.2.2 PVP dielectric material

PVP and methylated poly(melamine-co-formaldehyde) (MPMF, used as PVP crosslinking agent) with weight ratio of 4:1 were dissolved in dimethyl

formamide (DMF) to give 8 wt % solution. The solution was filtered with a polytetrafluoroethylene (PTFE) syringe filter with 0.2 μm pore size. The embossing template was fabricated, passivated and coated with Au film in the same manner as described in chapter 3.

4.2.3 UV transfer embossing process

Poly(ethylene terephthalate) (PET) films coated with indium tin oxide (ITO) supplied by Sigma-Aldrich were cleaned by sonication in detergent. ITO served as the transistor gate electrode. The PVP solution was spin-coated onto the ITO coated PET substrate at 500 rpm for 3 minutes. The dielectric layer was then cross-linked in air at 200 °C for 2 hours. For high volume production, PVP dielectric could also be sufficiently crosslinked at 200°C for 15 minutes as it turns insoluble in acetone and chlorobenzene. Since reduced crosslinking time is critical for the mass production, we conducted this process and successfully fabricated proper transistor devices. O₂ plasma treatment at power of 400 watt and O₂ pressure of 200 mTorr were applied to PVP dielectric for 10 seconds. UV resin was then spin-coated onto the PVP thin film at 3000 rpm for 2 minutes. The UV resin coated substrate was immediately brought into contact with a gold coated embossing template and exposed to UV light through the transparent substrate, ITO gate electrode and PVP thin film. After removal of the template, the adhered gold patterns formed source and drain electrodes. The whole construct was rinsed with ethanol or isopropyl alcohol to remove the uncured UV resin. The transistor channel formed after removal of the uncured

UV resin which is in the uncontacted areas and inhibited from curing by oxygen. The fabrication process was completed by drop coating of PQT-12 solution in chlorobenzene and annealing at 125 °C for 15 minutes in a vacuum oven.

4.3 Results and discussion

4.3.1 Effect of oxygen plasma treatment

O₂ plasma treatment is a key step for the successful transfer of electrodes onto the hydrophobic PVP surface.

Figure 4.2 (a) Incomplete transfer of source and drain electrodes without plasma activation; (b) Intact source and drain electrodes transferred onto plasma activated PVP; (c) Water contact angle of PVP surface without plasma activation; (d) Water contact angle of PVP surface with brief plasma activation.

(S: source electrode in transistor device; D: drain electrode in transistor device;
channel: a line indicating the position of transistor channel)

Figure 4.2 (a) and (b) show transferred gold electrodes on PVP thin film without (a) and with (b) O₂ plasma treatment. Without plasma treatment, the gold electrodes were only partially transferred. It is known that O₂ plasma treatment can activate a surface, make it hydrophilic and greatly improved the adhesion of cured UV resin to the PVP, which was necessary for the gold electrodes to remain on the construct after removal of the UV embossing template. Figure 4.2 (c) and (d) show micrographs of water droplets on untreated and plasma-activated PVP surfaces. The O₂ plasma treatment reduces the water contact angle from $76 \pm 1^\circ$ to $19 \pm 2^\circ$.

4.3.2 Characterization of transfer embossed electrodes

The transfer embossed electrodes were characterized by high resolution scanning electron microscope (HR-SEM) and atomic force microscope (AFM).

Figure 4.3 (a) High resolution SEM image of a gap between two electrodes; (b) AFM image of a gap between two electrodes.

Figure 4.3(a) shows the top view of the gap between two patterned electrodes on PVP dielectric film. The measured length of the gap, which is the channel length of the transistor device, is $3.0 \pm 0.1\ \mu\text{m}$ and the ratio between the length of the gap and roughness of the electrodes is estimated to be 30:1, resulting in a roughness of around 100 nm. The relatively high roughness is believed to arise from the mechanical breakage in the Au film at the edge of the mold during demolding. Figure 4.3(b) shows a 3D AFM image of the patterned electrodes, focusing on the gap between two electrodes. The measured gap of $3.0 \pm 0.3\ \mu\text{m}$ in length between the two electrodes was obtained. These results indicate that the technology described in this work is capable of achieving a resolution as low as $\sim 3\ \mu\text{m}$.

4.3.3 Device performance of printed OTFT

The device performance of OTFT fabricated by this transfer embossing technology was measured in air using an Agilent E5270B parameter analyzer with a cascade probe station.

Figure 4.4 (a) Output and (b) transfer characteristics of bottom gate OTFTs fabricated by UV transfer embossing.

Figure 4.4(a) shows a representative drain current versus drain voltage (I_D - V_D) curve and Figure 4.4 (b) shows the transfer characteristics (I_D - V_G) curve. The devices achieved a much better performance than the prior top gate devices we have reported. The calculated carrier mobility ranged from 0.01~0.02 $\text{cm}^2/\text{V s}$ in the saturation regime, which is more than 1 order of magnitude higher than the top-gated devices⁸⁶; the on/off ratio reached as high as 10^4 , which is 2 orders of magnitude higher than that in the top-gated devices⁸⁶.

The electrical properties at the interface of transfer embossed Au electrode/semiconducting polymer was studied with standard TLM method¹⁰⁰. The total contact to contact resistance (R_{total}) can be divided into sheet resistance(R_{sh}) in the channel and the contact resistance(R_c) at the electrodes according to equation 2.5¹⁰⁰ and equation 2.6 can be obtained by normalizing resistance with channel width¹⁰¹. The width-normalized contact resistance can be evaluated at $L=0$. Devices with four different channel lengths were fabricated and tested. Figure 4.5 shows the plot of width normalized R_{total} as a function of L .

Figure 4.5 Plot of width normalized total contact to contact resistance as a function of channel length to obtain contact resistance values.

A straight line is fitted to four corresponding total contact-to-contact resistances. The interception between the fitting line and Y-axis gives a width normalized contact resistance of around $500 \text{ K}\Omega \cdot \text{cm}$ when $V_G = -20 \text{ V}$. The moderate contact resistance is believed to be caused by the roughness produced at the demolding step.

To investigate the cause of the improvement in charge carrier mobility, atomic force microscopy (AFM) was used to study the dielectric-semiconductor interface. Figure 4.6(a) and (b) show the surface morphology of ITO coated PET substrate and cross-linked PVP, respectively.

Figure 4.6 AFM morphology of (a) ITO coated PET substrate and (b) cross-linked PVP.

The root mean square roughness (R_{rms}) of ITO coated PET substrate was 3.7 nm. With proper spin-coating parameters for the PVP thin film, R_{rms} of the dielectric surface was reduced to 0.9 nm. It is well-known that the mobility in OTFTs is affected by morphology and grain size of the semiconductor film¹⁰². The semiconductor film morphology is in turn partly driven by the substrate surface¹⁰³. Therefore, substrate roughness, to some extent, determines the quality of interface and further affects transistor characteristics^{104, 105}. In our

earlier top gate devices, the PET substrate showed a regular ripple-like morphology ($R_{\text{rms}} = 6.7 \text{ nm}$), which was a typical surface morphology of a polymer substrate. The spin-coated semiconductor film was very thin and closely conformed to this morphology; the roughness of semiconductor film only reduced modestly to $R_{\text{rms}} = 4.4 \text{ nm}$ ⁸⁶. In the present bottom-gated configuration, the PVP film is thick enough (800 nm ~ 1000 nm) to cover up the rough surface of the ITO film and produce a very smooth ($R_{\text{rms}} = 0.9 \text{ nm}$) dielectric interface. We propose that the increased mobility is a consequence of this significant roughness reduction at the dielectric-semiconductor interface.

The bottom gate device structure makes it possible to cross-link the PVP thin film at high temperature without affecting the quality of semiconductor layer, which is deposited after PVP has been cross-linked. Generically, cross-linking of polymer systems enhances mechanical strength and stiffness and increases the resistance to solvents^{106, 107}. In our experiments, PVP thermally cross-linked with MPMF also shows high solvent resistance to chlorobenzene and, as a result of the cross-linking process, the gate leakage current is reduced below nA scale and the off current is as low as 0.1 nA, leading to the increase of on/off ratio. These results agree well with others' reports in which leakage current through PVP cross-linked with the proper amount of MPMF is more than two orders of magnitude lower than uncross-linked PVP film¹⁰⁸ and transistor off current is found to decrease by 2 orders of magnitude with prolonged cross-linking time¹⁰⁹. Based on our optimized process, real, commercially interesting OTFT applications such as low-cost, large area sensor systems become feasible.

4.4 Conclusions

In summary, the UV transfer embossing process is optimized by using bottom-gated configuration so that the resulting printed OTFT has greatly improved mobility and on/off ratio of $0.01 \sim 0.02 \text{ cm}^2/\text{V s}$ and 10^4 , respectively. The bottom-gated configuration permits thermal cross-linking of the PVP dielectric and hence lower gate leakage current and off current. The increased mobility is proposed to result from significant roughness reduction at the dielectric-semiconductor interface. The improved printed OTFT performance makes this technique feasible for medium performance and/or disposable applications such as electronic paper and large-area environmental sensors.

Chapter 5 Adhesive-free transfer printing with PDMS-TiO₂ nanocomposite^b

5.1 Introduction

Unlike the traditional inorganic semiconductor process, the low-temperature solution-based processes used for printed organic electronics¹¹⁰⁻¹¹³ can deposit various organic semiconductors on a broad range of substrate materials such as plastics to fabricate low-cost electronics under ambient conditions^{59, 114}. The continuous efforts to reduce the cost of organic electronics require a suitable printing process that is independent of expensive photolithography. Inkjet printing^{6, 7}, gravure printing¹¹⁵ and transfer printing^{86, 116} have been reported to meet the needs of the emerging low-cost organic electronics.

In printing technology, the transfer of Au film from the surface of a template onto a substrate for a patterned gold structure has been studied. Much of the efforts have been devoted to print patterned Au films onto rigid substrates by using elastomeric stamps, while the substrates are derivatized with self-

^b Reproduced with permission from [J. S. Shi, M.B. Chan-Park, and C.M. Li, Adhesive-Free Transfer of Gold Patterns to PDMS-Based Nanocomposite Dielectric for Printed High-Performance Organic Thin-Film Transistors. ACS Applied Materials & Interfaces, 2011 <http://dx.doi.org/10.1021/am200058b>], Copyright © 2011, American Chemical Society

assembled monolayers (SAM) of molecules with thiol function group as an adhesive for the Au film^{84, 117, 118}. A few studies have reported the use of rigid stamps such as patterned Si wafers to print patterned Au films onto a cross-linked solid PDMS modified with thiolated SAM as a molecular adhesive or Ti/Cr as a metallic adhesive for Au film transfer^{25, 26}, where the PDMS simply serves as an elastomeric substrate. However, the adhesion between the Au film and substrate such as Ti can adversely affect charge injection in the electrode-semiconductor interface to cause a significantly elevated interfacial contact resistance and deteriorate the device performance¹¹⁹. A direct transfer process of Au film onto PDMS surface without any adhesive interlayer is advantageous for improved device performance since PDMS as a dielectric material, instead of merely substrate material, has its unique advantages. It allows fabricating extremely flat films, provided that the prepolymer is cast and spun over a very flat substrate. More importantly, it has a hydroxyl-free and inert surface after curing, making it an excellent candidate to fabricate organic transistors with possible n-type conduction^{104, 120, 121} and low hysteresis¹²². However, PDMS is a low-K dielectric material, and needs to be fabricated into a very thin film for effective gate modulation and thus elimination of short-channel effect (SCE) becomes very difficult, especially in devices with a short channel length^{123, 124}.

In this work, we demonstrate a novel direct transfer process to fabricate Au pattern for printed electronics without use of any adhesive but by increasing adhesion between Au and nanocomposite surfaces through an in situ PDMS cross-linking process. In the process, the liquid prepolymer surrounding

titanium dioxide nanoparticles cross-links and produce the solid nanocomposite film with higher adhesion to Au surface to facilitate the transfer process. Titanium dioxide nanoparticles of about 4 – 8 nm in size with dielectric constant of about 5.3 has been synthesized with a solution process¹²⁵, which is highly compatible with PDMS by choosing a common solvent for both materials to disperse the nanoparticles uniformly in PDMS and further fabricate the PDMS-based nanocomposite dielectric layer with a higher dielectric constant than plain PDMS. The transferred Au film, with a resolution down to 3 μm (shown in the inset of Figure 5.2) limited by the resolution of master template, can easily survive Scotch Tape test and the bottom-gated organic transistors were fabricated by this process using poly(3,3'''-Didodecylquaterthiophene) (PQT-12) as the active material to demonstrate the advantages of the process and its great potential in organic electronics.

5.2 Materials preparation and printing process

5.2.1 Solution processable PQT-12

PQT-12 was prepared with the quaterthiophene monomer (3,3'''-Didodecylquaterthiophene) by FeCl_3 -mediated oxidative coupling polymerization³⁰. In particular, after the quaterthiophene monomer was added in FeCl_3 suspension with an appropriate solvent at room temperature (typically 6.2 g quaterthiophene monomer to 20.4 g FeCl_3 suspension in 250 mL chloroform), the mixture was stirred for 20 minutes, and then water was added into the reaction vessel to terminate the polymerization. The polymer was then

washed with water, precipitated with acidic ethanol and filtered. The product was further extracted and purified with heptane and chlorobenzene to give electrically pure 0.3 wt % PQT-12 solution in chlorobenzene for printed OTFT fabrication. All chemicals used in PQT-12 synthesis process were also purchased from Sigma-Aldrich.

5.2.2 PDMS-titanium dioxide nanocomposite

Sylgard 184 PDMS prepolymer and curing agent with weight ratio of 1:1 were dissolved in toluene to form a 20 wt % solution. 0.5 g PDMS solution was mixed with 0.5 g 3.5 wt % organic-capped titanium dioxide nanoparticles solution in chloroform. The amount of nanoparticles solution was controlled to obtain different ratio of titanium dioxide nanoparticles to PDMS in nanocomposite solution. The added curing agent was excessive since it was found that a longer curing time than the recommended was often required. The prepared nanocomposite solution was immediately spin-coated on ITO coated PET film to form nanocomposite films with different thicknesses by controlling spin speed. Before spin coating process, ITO coated PET films were cleaned by sonication in decon 90 cleaning agent for 10 minutes, rinsed with DI water to remove the remnant detergent and blown dry by air. The nanocomposite films were then baked at 150 °C for 3 - 5 hours to fully cross-link the nanocomposite into a solid film.

5.2.3 Printing process of organic thin-film transistors

A schematic illustration for the fabrication procedure of an organic transistor device in bottom-gated configuration is shown in Figure 5.1.

Figure 5.1 Schematic illustration of the direct transfer printing process on PDMS-based nanocomposite.

To fabricate the organic transistor, silicon template was firstly fabricated via standard procedures of photolithography and deep reactive ion etching (DRIE). The etching depth was 100 – 150 μm . 1 mM 1H,1H,2H,2H-perfluoro-octyl triethoxysilane in hexane solution was used to form a self-assembled monolayer (SAM) as a passivation layer on the silicon template. 100 nm gold was

sputtered onto the passivated silicon template. 5% PVA solution in DI water was spin-coated on ITO coated PET film to form a PVA dielectric layer of about 200 nm for reduced parasitic gate leakage current. ITO served as the transistor gate electrode. The prepared nanocomposite solution was then spin-coated on the PVA dielectric layer to form an 880 ± 60 nm thick nanocomposite layer, followed by baking at 150 °C for 2 minutes to remove the remnant solvent. Longer baking time should be avoided to prevent excessive curing of PDMS in the nanocomposite before contact with the silicon template. To calculate mobility of device, the unit area capacitance of the dielectric layer stack including PVA and nanocomposite layer (2.68 nF/cm^2) was measured separately by fabricating ITO-insulator-Al capacitors. The coated substrate was carefully brought into contact with the gold-coated silicon template. Gentle pressure was applied to ensure sufficient contact between the nanocomposite film and gold. The whole assembly was then baked at 150 °C for 3 - 5 hours to fully cross-link the nanocomposite into a solid film. The cross-linking process of the nanocomposite could increase the adhesion between gold and nanocomposite after nanocomposite turning from liquid into solid film. This explains why the gold film can be transferred onto the nanocomposite film without need of an additional adhesive. After demolding, the gold film was transferred onto the nanocomposite film to form the transistor source and drain electrodes. PQT-12 solution in chlorobenzene³⁰ with a concentration of 0.3 wt % was drop-casted and annealed at 150 °C for 45 minutes in a vacuum oven as the active layer to complete OTFT fabrication. Apparently, this approach can

provide a low-cost mass printing manufacturing process for printed organic electronics.

5.3 Characterization of materials and devices

5.3.1 Characterization of nanocomposite film

The surface and cross-section of the nanocomposite films were characterized by FE-SEM. The nanocomposite film samples for cross-sectional view were prepared in liquid nitrogen. The thicknesses of the nanocomposite films were measured by AFM. To measure the thickness, a nanocomposite film was partially removed from ITO coated PET film to create a step in the nanocomposite film and AFM tip scanned across the step to measure the height of it, which was taken as the thickness of the nanocomposite film. 100 nm aluminum was deposited on the nanocomposite film using sputtering system to fabricate ITO-nanocomposite-Al capacitors. For each nanoparticle to PDMS ratio, six capacitors were fabricated and the capacitances of these capacitors were measured using probe station and Agilent LCR meter. The average value of the measured capacitances was used to calculate the dielectric constant of the nanocomposite film.

5.3.2 Characterization of organic thin-film transistors.

The OTFTs were characterized in ambient air using an Agilent E5270B semiconductor analyzer and probe station. The output characteristics of the OTFTs was obtained by sweeping the drain voltage from 0 V to -20 V and

stepping the gate voltage from 0 V to -20 V at an interval of 5 V. The transfer characteristics of the OTFTs was obtained by keeping the drain voltage constant at -20 V and sweeping the gate voltage from 10 V to -20V as off-to-on direction and from -20 V to 10 V as on-to-off direction. Study of contact resistance by transmission line model was conducted by measuring resistances between the source and drain electrodes for different channel lengths with different gate voltages applied using the same equipments.

5.4 Results and discussion

5.4.1 Transfer efficiency and nanocomposite film thickness

Based on the experimental results of spin coating different polymer solutions with different solvents on silicon wafer and measuring film thicknesses with ellipsometry, an empirical formula on the dependence was concluded by C. J. Lawrence for polymer solutions correlating the thin-film thickness with spin speeds as shown in equation 3.1¹²⁶. To study whether the spin-coated film thickness can be predicted using this empirical relationship, the thicknesses of nanocomposite films fabricated with different spin speeds were measured by AFM.

Figure 5.2 Thickness of spin-coated nanocomposite film versus different spin speed; (b), (c), (d) gold patterns transferred onto the nanocomposite film with the thickness represented by the corresponding data points; the inset shows an SEM image of the channel between Au electrodes with a resolution of 3 μm .

Figure 5.2(a) shows the thickness against spin speed and the polynomial fit by setting $b = -1/2$, illustrating that the film thickness can be predicted closely by the empirical formula at lower spin speeds, while the measured thickness is higher than that predicted by 20 - 30 nm at higher spin speeds.

By transfer-printing gold patterns onto the nanocomposite film of different thicknesses, a significant dependence of gold transfer efficiency on the nanocomposite film thickness was observed. Figure 5.2(b), (c) and (d) demonstrate that gold pattern transferred onto the 880 ± 60 nm thick nanocomposite film is intact while gold pattern transferred on the 630 ± 60 nm thick nanocomposite film is still almost intact except a minor defect at the edge of the pattern. However, the gold transferred onto the 490 ± 45 nm thick nanocomposite film with a broken pattern is taken as failed transfer. Table 5.1 shows the statistical data of the transfer efficiency in correlation with nanocomposite film with different thickness.

Table 5.1, Transfer efficiency with different nanocomposite film thicknesses.

Nanocomposite film thickness	Total number of samples	Intact patterns transferred (Figure 5.2b)	Patterns with minor defect (Figure 5.2c)
880 ± 60 nm	15	14	1
630 ± 60 nm	15	5	10
490 ± 45 nm	15	2	3

Three batches of gold patterns with 15 gold patterns in each batch were fabricated under the same conditions except the thickness of the nanocomposite film. The intact patterns are the patterns without defect as shown in Figure 5.2(b) while patterns with minor defect are the gold patterns that have minor defect on the edge of the pattern but the transistor channel between source and drain electrodes is successfully created (shown in Figure 5.2(c)). Gold patterns transferred like the one in Figure 5.2(d) are not taken into account as successfully transferred patterns.

The surfaces of nanocomposite thin-films were characterized by FE-SEM as shown in Figure 5.3.

Figure 5.3 (A), (B), (C) FE-SEM images of film surfaces with 880 nm, 630 nm, 490 nm thicknesses, respectively; (D) FE-SEM image of pure titanium dioxide nanoparticle film surface.

In the SEM images, titanium dioxide nanoparticle aggregates can be observed in the nanocomposite films with different thicknesses studied. In the 880 nm thick nanocomposite film, the surface mainly comprises PDMS with a typical ripple-like polymer surface and a few aggregates of titanium dioxide nanoparticles with diameter of about 200 nm. In the 630 nm thick nanocomposite film, more titanium dioxide nanoparticle aggregates sized about 1 μm emerge on the surface and the ripple-like polymer surface becomes less

apparent. In the nanocomposite film with thickness of 490 nm, the surface is mainly composed of titanium dioxide nanoparticle aggregates sized about 5 μm . In fact, the composition and thickness of the nanocomposite film are dependent on the spin speed. More nanoparticles with much lower solubility than PDMS can precipitate to form larger aggregates due to faster solvent evaporation when using higher spin speed to make a thinner film. Good contact between gold pattern and nanocomposite film is crucial for successful transfer. The silicon template used in the process is a hard template, which lacks flexibility and has better contact with only thicker soft films¹²⁷. Furthermore, larger nanoparticle aggregates in a thinner film can impede good contact between the two surfaces, resulting lower transfer efficiency. This explains the dependence of transfer efficiency on nanocomposite film thickness. Thus, a certain thickness of the nanocomposite film as the dielectric layer is necessary to possess good contact and high adhesion for the pattern transfer. This can also explain that a pure PDMS cannot be directly used for an adhesive-free pattern transfer process since thick PDMS film cannot be used as transistor dielectric layer due to its low dielectric constant as discussed in more detail below.

Figure 5.4 (a),(b),(c) SEM image of cross-sectional view of nanocomposite film with thickness of about 900nm,680nm,450nm, respectively; (d) SEM image of cross-sectional view of pure nanoparticle film

The cross-section of 900 nm nanocomposite film shows that the aggregates sized about 200 nm distributed evenly across the thickness of the nanocomposite film. In a thinner 680 nm nanocomposite film, larger aggregates can be observed. The size of the aggregates is from 1 μm to 1.5 μm while some reside inside the bulk of the nanocomposite film and some is located on the top of the film, corresponding to those observed in top view of the film in Figure 5.3(b). For the nanocomposite film with 450 nm thickness, aggregates with size more than 2 μm can be observed to protrude from the nanocomposite film. The cross-section of pure nanoparticle film is also shown as a comparison to the nanocomposite films.

5.4.2 Dielectric constant of nanocomposite

Pure PDMS without titanium dioxide nanoparticles as the dielectric material has been investigated in this work. Due to the low dielectric constant of PDMS (2.3 - 2.8)¹²⁸, a very thin PDMS film (500 - 600 nm) must be used to effectively avoid SCE in transistor devices with a channel length around 3 μm in terms of our experimental results. However, the yield of this process drops to an unacceptable value that cannot be used in a practical manufacturing process since all transfer processes tried with pure PDMS film of about 500 nm thickness failed by results similar to Figure 5.2(d). One approach to solve this dilemma is to increase the dielectric constant of the dielectric material. Solution-processable organic-capped titanium dioxide nanoparticle solution¹²⁵ was mixed with PDMS solution with proper concentration to produce nanocomposite material with a higher dielectric constant. Figure 5.5 shows the dielectric constant of the nanocomposite against the weight ratio of titanium dioxide nanoparticles to PDMS.

Figure 5.5 Dielectric constant of the nanocomposite material with different weight ratio of titanium dioxide nanoparticles to PDMS.

The dielectric constant of the nanocomposite increases with increasing ratio of titanium dioxide nanoparticle to PDMS until achieving a plateau to have the maximum dielectric constant (~ 5.3), which is almost the same as titanium dioxide nanoparticles. Since a thinner film would be fabricated with higher nanoparticle to PDMS ratio under the same spin coating parameters, a weight ratio of 1:6 (titanium dioxide nanoparticle: PDMS) was chosen in order to satisfy the thickness requirement in this process.

5.4.3 Device performance of printed OTFTs

Figure 5.6 shows the output and transfer characteristics of organic transistors fabricated with the direct transfer process.

Figure 5.6 Representative performance of organic transistors fabricated with the reported process (a) source-drain current versus source-drain voltage with different gate voltage applied, the inset shows source-drain current versus source-drain voltage at the linear region, indicating an ideal ohmic contact between the direct transferred gold patterns and the active material; (b) transfer characteristics of the devices; (c) plot of square root of source-drain current against gate-voltage, source-drain current is measured when gate voltage is swept in both off-to-on and on-to-off directions. Linear fits of both directions are shown in order to find the corresponding threshold voltage.

From Figure 5.6(a) and (b), a mobility of $0.038 \text{ cm}^2/\text{V s}$ in saturation regime and on/off ratio of $10^4 - 10^5$ are extracted using,

$$\mu = \left(\frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2 \frac{2L}{W} \frac{1}{C_i}, \quad (2)$$

where I_D is the drain current, C_i is the capacitance per unit area of the gate dielectric film, and V_G is the gate voltage. V_{th} of the device was estimated to be -1.3 V from the intersection between $I_D = 0$ and linear fit of $I_D^{1/2}$ - V_G curve at the saturation regime.

Figure 5.6(c) shows the hysteresis characteristic of the transistor device by measuring root square of drain current while the gate voltage is swept in both off-to-on and on-to-off directions. Two lines are fit to the bidirectional curve and threshold voltages are obtained by extrapolating the fitting lines to $I_D^{1/2} = 0$. The obtained threshold voltage when gate voltage is swept from off-state ($V_G = 10$ V) to on-state ($V_G = -20$ V) is $V_{th(off-to-on)} = -2.5$ V while the corresponding threshold voltage when the gate voltage is swept from on-state to off-state is $V_{th(on-to-off)} = -1.3$ V, which gives a very small $\Delta V_{th} = 1.2$ V. This value, in particular considering that all measurements were conducted in ambient air, is much smaller than ΔV_{th} on silicon dioxide¹²⁹, HMDS treated silicon dioxide¹³⁰, poly(4-vinylphenol)¹³¹ and other different hydroxyl-containing polymer dielectrics¹³² reported in the literature. The small swing of threshold voltage demonstrating the low hysteresis behavior in the device can be attributed principally to the hydroxyl-free nature of dielectric-semiconductor interface suggested by Bao et al¹²².

To demonstrate the low contact resistance between the active material and direct transfer-printed source and drain electrodes without adhesives, the response at small source-drain voltages is shown in the inset of Figure 5.6(a). The good linear response of transistor at the linear region suggests ideal ohmic contacts with low contact effects between the transferred electrodes and active organic semiconductor in the transistor channel. To further study the electrode-semiconductor interface, transmission line model⁴⁵ shown in equation 2.5 and 2.6 relating the channel length and width-normalized total resistance in the device was used to estimate the contact resistance at source and drain contacts:

Figure 5.7 shows width-normalized device resistance versus channel length of transistors and the linear fit of the data points.

Figure 5.7 Dependence of width-normalized total ON resistance on channel length of the devices. Drain voltage is -2 V and gate voltages are -20 V, -15 V, -10 V and -5 V.

According to the transmission line model, the black lines are drawn to represent the linear fits to the 4 groups of red points, which are experimentally measured width normalized resistance. By extrapolating the linear fits to $L = 0$, the contact resistance in the transistor devices is estimated to be on the order of $\sim 100 \text{ k}\Omega\cdot\text{cm}$. This value is less than or comparable to the contact resistance at gold-semiconductors interface optimized by reduced adhesive thickness, hole injection layer or sulfuric acid treatment on electrodes^{119, 133-135}.

5.5 Conclusion

In summary, a low-cost adhesive-free direct transfer printing process onto PDMS-based nanocomposite dielectric material with a resolution down to 3 μm was developed and successfully applied in fabrication of organic thin-film transistors. Dielectric constant of the nanocomposite was observed to vary with the ratio of titanium dioxide nanoparticle to PDMS. With optimized nanocomposite thickness, the transfer efficiency of gold patterns can achieve a very high level while avoiding short-channel effect in the fabricated organic transistors. The organic transistors fabricated by this process showed a high mobility of $0.038 \text{ cm}^2/\text{V s}$ and on/off ratio of $10^4 - 10^5$. Due to the inert nature of the dielectric-semiconductor interface, transistor devices also demonstrate low hysteresis ($\Delta V_{\text{th}} = 1.2 \text{ V}$) and low threshold voltage (-1.3 V). Width-normalized contact resistance between the transfer-printed gold patterns and active material in organic transistors is on the order of $\sim 100 \text{ k}\Omega\cdot\text{cm}$, which is due to the absence of SAM or metallic adhesive at the electrode-semiconductor interface. This technique can be readily adapted into low-cost mass manufacturing process for printed electronics.

Chapter 6 Printing process by spatially controlled oxygen-inhibition effect in acrylate-based materials^c

6.1 Introduction

Photolithography has a long history in the high-performance silicon based semiconductor electronics industry but is not particularly well-suited for low-end applications^{6, 94-96, 136} in printed electronics because of its requirements for delicate photolithographic tools, expensive photo-masks/resists and intensive labour. Several categories of alternative printing processes such as microcontact printing (μcp)^{8, 9}, transfer printing^{25, 26, 137}, inkjet printing^{6, 138} *etc* have been developed. μcp is a very powerful printing technique and has been studied intensively. It has been successfully applied in printed OTFTs. The best established system to date for μcp is based on alkanethiolates on gold and silver and alkylsiloxanes on hydroxyl-terminated surface⁸, in which specific surface chemistry is required between ink material and substrate. This requires a specific ink material to be used for printing on certain substrate material and

^c Reproduced with permission from [J. S. Shi, M. B. Chan-Park, C. Gong, H. B. Yang, Y. Gan, C. M. Li*: Spatially controlled oxygen-inhibition of acrylate photopolymerization as a new lithography method for high performance OTFTs. *Chem Mater*, 22 (7), 2341–2346, 2010.], Copyright © 2010, American Chemical Society

new inks must be designed accordingly to print each new material; this involves significant re-design work and limits the applicability of this printing technique. In transfer printing, interface chemistry is also necessary when a molecular adhesive is used²⁶, and a thick metallic adhesive has proved to limit the device performance even when conventional patterning techniques are used¹¹⁹. Inkjet printing, a convenient printing method that has been applied in different research areas¹³⁸, is another low-cost fabrication process which has advantages of additive operation, on demand deposition and compatibility with flexible and large-area substrates¹¹. However, conventional inkjet printing suffers from low resolution capability, and thus is inadequate for direct printing of source and drain electrodes for OTFTs¹³⁹; The recently reported electrohydrodynamic jet printing approach offers impressive single micron resolution but requires a conductive support to generate an electric field between the nozzle and the conductive support, making the process more complicated^{140, 141}. Thus, there is a great need to develop an economic micropatterning method for printing electronics with resolutions on the few microns, submicron and nanoscales.

Here a low-cost printing process which employs a reusable silicon mold associated with UV exposure to spatially modulate oxygen-inhibition in the UV polymerization process in acrylate-based monomer or oligomers is developed. This is the first demonstration of spatial control of oxygen-inhibition in the UV polymerization process and the use of this effect to produce a pattern in acrylate polymer. The fabrication process does not rely on any surface/interfacial chemistry or additional adhesives, and is capable of achieving a high resolution

of 3 μm and potentially higher. The fabrication process replaces the elaborate infrastructure of photolithographic tools, photoresist and photomasks with simple UV illumination of low-cost acrylate-based material as “resist” in contact with a reusable silicon mold, making itself well-suited in low-end applications of printed organic electronics and the printing process is applied here to print the etch masks for the electrodes of top- and bottom-gated organic thin film transistors.

Furthermore, as various substrate materials such as silica¹⁴², polyimide¹⁴³ and polyethylene terephthalate (PET)¹¹⁶ have been used in printed electronics, a universal micropatterning technique is in need to produce patterns on different substrates. Photolithography is portable across these substrates, but not particularly well suited for low-cost printed electronics as stated above. For other unconventional processes such as microcontact printing^{9, 144, 145}, transfer printing^{40, 137} and ink jet printing^{6, 146, 147}, they are also limited to specific type of substrate materials. When applying μCP ⁸ to polymeric substrates, new inks and surface chemistry have to be studied and designed according to the substrate material. Transfer printing has the similar limitation, in which adhesive is used to facilitate the transfer and should be specifically selected for a substrate material in terms of interfacial chemistry²⁶. If the substrate or transferred material is too hydrophobic, surface modification is required and makes the fabrication process complicated¹³⁷. Inkjet printing¹⁴⁸ imposes stringent requirement on the substrate surface properties, which should be compatible

with the ink for good resolution^{6, 149}, making printing difficult on other substrates.

Therefore, this printing process by spatially controlled oxygen-inhibition of acrylate polymerization is further developed into a universal micropatterning method by using SU-8 mold and other low-cost materials to mimic conventional photolithography and print patterns on different substrate materials without any modification. The reason why SU-8 is selected as the mold material instead of PDMS, a widely used mold material in μ cp, is because PDMS is highly porous and oxygen inside PDMS prevents acrylate polymerization even at the contacted area, leading to failure of pattern creation.

The process and its mechanism are illustrated in Figure 6.1. It is worthy of a note that a rigid silicon mold is difficult to have conformal contact with a hard substrate, thus limiting this process from being applicable to large-area hard substrates.

(a)

(b)

Figure 6.1 (a) Schematic illustration of the process to create a pattern on substrate by spatially controlling oxygen inhibition in the photopolymerization of acrylate-based material to create a polymer mask over metal electrodes in a FET; (b) schematic illustration (magnified area 1 in (a)) of the mechanism of spatially controlled oxygen inhibition

There are three stages of reactions in an acrylate-based, free radical polymerization process: initiation, polymerization and termination. The overall reaction scheme may be represented by the following equations¹⁵⁰, which are

Initiation,

Polymerization,

Termination,

The oxygen inhibition effect occurs through the scavenging of free radicals by oxygen molecules to form oxidized radicals, which are ineffective in the polymerization process. The difference between reaction processes on contacted and uncontacted regions with dissolved oxygen in the acrylate mixture under low incident light intensity can be expressed as the following diagram (5),

and the reaction between radicals and oxygen molecules can be further detailed into the following equations:

where $ROO\cdot$ and $RM_nOO\cdot$ are not capable of initiating the polymerization process¹⁵⁰.

The oxygen molecules that produce the inhibition effect are provided by dissolved oxygen in the acrylate mixture and diffused ambient oxygen from the depressions of the silicon mold into the acrylate mixture (Figure 6.1(b)). Upon UV exposure, as shown in Figure 6.1(b), the portions of acrylate mixture thin-film in contact with the silicon mold protrusions are protected from the ambient air and would not experience oxygen inhibition after consumption of dissolved oxygen in acrylate mixture. This would result in photopolymerization of the thin film in contact with the mold while the uncontacted regions of the thin film would not polymerize. After removal of the silicon mold and rinsing away of the uncross-linked acrylate mixture, an acrylate polymer pattern replicating the elevated relief of mold is created on the surface of the substrate.

6.2 Process details

6.2.1 Molds fabrication

Silicon mold was fabricated as described in Chapter 3 and for fabrication of SU-8 mold, PET film were cleaned by ultrasonication in acetone, ethanol and DI water, each for 20 minutes, and were treated with 300 W oxygen plasma at pressure of 270-300 mTorr for 2 minutes. SU-8 25 photoresist was deposited by

spin coating followed by pre-exposure baking at 65 °C for 2 hours. SU-8 was then photolithographically patterned with 98 mJ/cm² UV exposure using Karl Suss MA6 followed by post-exposure baking at 50 °C for 1 hour and 95 °C for 2 minutes. During UV exposure, a silicon wafer was placed under the PET substrate to increase the backside exposure by reflection. Lastly, the fabrication was complete after placing the samples in SU-8 developer for 5 - 7 minutes with gentle agitation to remove the uncross-linked SU-8 photoresist. The SU-8 molds were examined with field emission scanning electron microscopy.

6.2.2 Procedure

The detailed procedure is illustrated in Figure 6.2(a). During fabrication, a mixture of acrylate monomer and oligomer is spin-coated on a sputtered gold surface on PET substrate. The mixture is comprised of a monomer, styrene, an oligomer, ethoxylated bisphenol A diacrylate (SR-349 purchased from Sartomer) with a ratio of styrene to SR-349 of 1:3 and 0.3 wt % photoinitiator, 2,2-Dimethoxy-1,2-diphenylethan-1-one (IRGACURE 651 purchased from Ciba Specialty Chemicals). The low concentration of the photoinitiator used was to maintain a pronounced oxygen-inhibition effect during the polymerization. The molecular structures are shown in Figure 6.2(b).

(a)

(b)

Figure 6.2 (a) Schematic illustration of polymer mask pattern fabrication on gold surface and the following gold etching step; (b) molecular structure of styrene and ethoxylated bisphenol A diacrylate and 2,2-Dimethoxy-1,2-diphenylethan-1-one

After coating the gold substrate with acrylate mixture, the mold is carefully brought into contact with the thin film of acrylate mixture. UV exposure is applied through the transparent PET substrate and semi-transparent gold layer to cross-link the acrylate mixture. UV irradiation was provided by an UV flood cure system. Gold-coated PET film could filter out wavelengths below 310 nm, resulting in a low effective intensity to avoid suppression of oxygen-inhibition at the uncontacted region. The intensity and spectral distribution of the UV irradiation and transmittance through gold-coated PET film is provided in Figure 6.3. After removal of the mold, the uncross-linked acrylate mixture, which was exposed to oxygen and thus did not cross-link, is removed by soaking the substrate in IPA (isopropyl alcohol); the cross-linked acrylate polymer remains on the gold surface forming the desired pattern. The exposed gold is removed by etching in a solution of KI and I₂ in DI water (KI:I₂:H₂O=4:1:100) for 2 minutes.

(a)

(b)

Figure 6.3 (a) Normalized spectral distribution of the UV flood cure system which provides incident light, (b) transmittance of gold (25 nm) coated PET film; wavelengths below 310 nm is effectively filtered out by gold coated PET film; at wavelength of 340 nm, the most absorbed wavelength by IRGACURE 651, the transmittance is ~26 %; wavelengths above 400 nm could not be effectively absorbed by IRGACURE 651

6.3 Patterning and OTFT fabrication

6.3.1 Characterization of polymer patterns

The region of the polymer pattern formed by this method that would be most critical in FET performance, the area destined to become the active channel after application of semiconductor material, was characterized by optical microscopy and field-emission scanning electron microscopy (FE-SEM).

Figure 6.4 shows optical (Figure 6.4(a) and (b)) and FE-SEM (Figure 6.4(c) and (d)) images of the acrylate polymer on gold surface in the area of the transistor channel (area 2 in Figure 6.1(a)). Polymer patterns with feature sizes of 20 μm and 3 μm are shown, demonstrating the relatively high resolution capability (3 μm) of this process.

Figure 6.4 (a) Optical image of polymer pattern on gold with resolution of 20 μm at the transistor channel (area 2 in Figure 6.1(a)); (b) optical image of polymer pattern on gold with resolution of 3 μm ; (c) SEM image of polymer pattern with resolution of 20 μm ; (d) SEM image of polymer pattern with resolution of 3 μm

6.3.2 Top-gated PQT-12 transistor

The microstructure printing by this new printing process was used to fabricate organic thin-film transistors (OTFTs) with both bottom-gated and top-gated configurations. To fabricate top-gated PQT-12 OTFTs, PQT-12 dissolved in dichlorobenzene with a concentration of 0.3%, was spin-coated at 1000 RPM for 2 minutes on gold source and drain electrodes and active channel gap produced by etching out the regions of the gold film not protected by the polymer mask. PQT-12 was then annealed in vacuum at 125 °C for 45 minutes. Solution processable TiO₂ nanoparticles with a concentration of 35 mg/mL in chlorobenzene fabricated in our lab were then spin-coated coated at 800 RPM for 1 minute as primary dielectric material¹²⁵, followed by spin-coating PVP solution on the TiO₂ nanoparticle thin film as additional dielectric material to reduce the gate leakage current. The PVP solution was 8 wt % PVP in dimethylformamide. The channel dimensions of the PQT-12 transistor were W/L=700 μm / 20 μm. Finally, a 100 nm aluminum gate electrode was deposited by physical vapor deposition, to complete fabrication of the OTFT. The fabrication process is illustrated in Figure 6.5(a). OTFT device performance data are shown as I_D - V_D and I_D - V_G curves in Figure 6.5(b). Device mobility in the saturation regime was extracted from equation 2.3. The capacitance per unit area of the gate dielectric was separately measured to be 4.8 nF/cm². The field effect mobility, μ , was calculated to be 0.06 cm²/V s. The device performance is comparable to that of OTFT devices fabricated using photolithographically defined source and drain electrodes¹²⁵.

(a)

Figure 6.5 (a) The fabrication process of top-gated PQT-12 organic thin-film transistor; (b) device performance, as I_D - V_D and I_D - V_G curves, of the fabricated top-gated PQT-12 organic thin-film transistor

6.3.3 Bottom-gated pentacene transistor

The bottom-gated transistor configuration requires some adjustments in the fabrication process to put transparent ITO gate electrode and PVP dielectric under the gold. The adjusted process is illustrated in Figure 6.6(a). ITO coated PET substrate purchased from Sigma-Aldrich was cleaned with detergent and deionized water. 12 wt % PVP solution in dimethylformamide was spin-coated and cross-linked at 200 °C for 15 minutes. The cross-linking agent for the PVP dielectric was methylated poly(melamine-co-formaldehyde). Gold was then

deposited using a sputtering system to a thickness of 35 nm. Acrylate mixture was spin-coated on the gold surface, brought into contact with the mold and cross-linked with UV exposure to create a mask pattern of acrylate polymer. The channel dimensions of the pentacene transistor were $W/L=240\text{ }\mu\text{m} / 20\text{ }\mu\text{m}$. After removal of the uncross-linked acrylate and etching away of the unprotected gold, the cross-linked acrylate polymer mask was removed with acetone, followed by deposition of 65 nm of pentacene using PVD system to complete the OTFT. Although the device structure is different from top-gated transistor, the process only requires an adjustment of the sequence of deposition of gate electrode, dielectric material and definition of source and drain electrodes while the process for creation of polymer pattern is the same as that in fabrication of top-gated transistor, demonstrating the capability of this process to pattern devices with different structures without modification. After fabrication, the OTFT devices were characterized and the device performance is shown in Figure 6.6(b). The capacitance per unit area of gate dielectric was separately measured to be 1.7 nF/cm^2 . The field effect mobility, μ , was calculated to be $1.02\text{ cm}^2/\text{V s}$ using equation 2.3 while the on/off ratio of the transistors was calculated to be slightly above 10^3 . The transistor performance is adequate for applications such as rectifier circuits of RFID tags in lower bands and driver circuits for displays^{151, 152}. The device performance can be further improved by optimizing the properties of interfaces and contacts in the transistor structures such as self-assembled monolayer treated interface and contact^{153, 154}.

(a)

(b)

Figure 6.6 (a) The fabrication process of bottom-gated pentacene organic thin-film transistor; (b) device performance, as I_D - V_D and I_D - V_G curves, of the fabricated bottom-gated pentacene organic thin-film transistor

6.4 Universal micropatterning with SU-8 mold

6.4.1 Optimization of SU-8 mold fabrication

SU-8 is known to have poor adhesion to unmodified PET but although a high UV exposure can improve adhesion, excessive UV exposure should be avoided to have good photomask pattern reproduction, thus PET surface treatment is required¹⁵⁵. Oxygen plasma was used to treat the PET substrate to improve adhesion of the SU-8 structure as described in experimental section.

Figure 6.7 SEM imagery of (a) SU-8 structures on oxygen plasma-treated PET substrate, showing that the SU-8 structures are tightly adhered onto the substrate, (b) SU-8 structures on PET substrate without oxygen plasma treatment, in which the narrow parts of SU-8 structures have detached from the substrate.

Figure 6.7(a) and (b) show SEM micrographs of SU-8 molds fabricated with and without oxygen plasma treatment, respectively, indicating that SU-8 structures can well adhere to the PET substrate with oxygen plasma treatment while the narrower parts of the SU-8 structures are detached from the untreated substrate. The magnified SEM images at the bottom of Figure 6.7 illustrate the dramatic improvement produced by oxygen plasma treatment. This can be attributed to the plasma-introduced polar functional groups including hydroxyl, carbonyl, and carboxyl groups on the surface of PET substrate, which increase

the surface free energy of PET substrate⁹² to boost nominal work of adhesion between SU-8 resist and PET substrate for better adhesion⁹³.

Thickness of SU-8 structure have to be optimized because certain thickness of the SU-8 film in the mold is necessary to effectively control oxygen-inhibition effect, but a deeply trenched mold is difficult to have uniform UV exposure along the thickness. Previous study shows that UV transmission of 100 μm uncross-linked SU-8 photoresist layer is 46% at 365 nm wavelength¹⁵⁶. This may lead to under-exposed SU-8 photoresist on the bottom and the photoinitiator in SU-8, triaryl sulfonium salt, could not generate sufficient acid to catalyze polymerization during post-baking. Figure 6.8(a) shows SU-8 microstructure with a height of 70 μm , which is distorted at the bottom (at the PET substrate, distal from the UV source), indicating that SU-8 at the bottom is under-exposed and insufficiently cross-linked. Simply extending the UV exposure time cannot be used to improve the cross-linking process of SU-8 resist on the bottom since a feature size reduction of 3 μm could be observed with additional 100 mJ/cm^2 UV exposure due to UV diffraction at the slit of photomask and the air gap between photomask and SU-8 resist¹⁵⁵. Thus, optimization of the thickness of SU-8 resist instead of increasing UV exposure is carried out to produce good photomask pattern and it shows that 30 μm thickness of SU-8 resist (Figure 6.8(b)) achieves a good compromise between adequate cavity depth and uniformity of SU-8 crosslinking.

Figure 6.8 SEM imagery of (a) 70 μm thick SU-8 underexposed at the base of the structures, leading to imprecise or completely failed mold fabrication, (b) intact and normally-shaped SU-8 mold structure of 30 μm height.

6.4.2 Patterning on silicon wafer

To demonstrate that this universal printing technique can be applicable for different substrate materials, an array of polymer patterns was first created on thermal oxide capped silicon wafer, a type of substrates commonly used in both industry and research. Figure 6.9(a) shows an optical micrograph of the produced polymer pattern array. Figure 6.9(b) and (c) are magnified micrographs to show the patterns more clearly.

Figure 6.9 (a) Optical micrograph of an array of polymer patterns on a nontransparent silicon substrate, (b) and (c) magnified optical micrographs of indicated regions in (a).

In fact, the silicon wafer used in the demonstration can stand for a class of substrate materials that are opaque and rigid. With this patterning method, other substrate materials such as glass, silica and metals can be printed since the method is based on a low-cost printing material system comprising acrylate mixture, SU-8 mold and UV exposure to mimic the conventional photolithography and eliminates the stringent requirements of surface chemistry and surface property in other patterning techniques such as μ cp, transfer printing and inkjet printing, thus becoming a universal printing technique being widely applicable to different substrate materials.

6.4.3 Patterning on PET substrates

A polymer pattern array on flexible polymer substrates such as PET has been printing using this printing process with SU-8 mold to demonstrate a universal printing technique applicable on different substrate materials. Figure 6.10(a) shows an optical micrograph of an acrylate polymer array patterned on PET substrate over an area of $4\text{ mm} \times 3\text{ mm}$, demonstrating the specific advantage of the flexibility of SU-8 mold for flexible substrates as illustrated in Figure 6.10(b) and (c).

Figure 6.10 (a) Optical micrograph of an array of acrylate polymer patterned on PET flexible substrate over an area of $4\text{ mm} \times 3\text{ mm}$, (b) schematic illustration of the poor contact between a rigid silicon mold and substrate (not drawn to scale), (c) schematic illustration of improved contact between a flexible SU-8 mold and substrate (not drawn to scale).

Flexible substrates are usually slightly curved, which is caused by production and storage conditions. Clearly, if a rigid mold were used in the technique, it

would not be able to bend and conform to the slightly curved surface of a flexible substrate (Figure 6.10(b)), and consequently the oxygen-inhibition effect could be controlled over only small areas where the mold-substrate contact was established. However, a flexible mold has demonstrated its capability in producing patterns on curved surfaces such as optical fiber and glass lens^{84, 157}. Similarly, SU-8 mold fabricated on flexible PET substrate can bend on its own weight and conform to the slightly curved flexible substrate, forming much better contact with the substrate to produce patterns over a larger area. Our experimental results show that a rigid silicon mold can only produces individual isolated patterns due to the poor contact between the rigid silicon mold and flexible substrates. The new mold demonstrated here is formed of SU-8 on PET film; other patternable UV-transparent materials and flexible substrates with low porosity could also be employed.

6.4.4 OTFT fabrication and characterization

The universal printing technique was further applied to fabricate OTFTs to demonstrate its feasibility in organic electronic application. Figure 6.11 illustrates the OTFT fabrication procedure.

Figure 6.11 Schematic illustration of OTFT fabrication procedure.

During fabrication, the silicon wafer was used as both substrate and gate electrode. PVP was spin-coated onto the wafer and thermally cross-linked at 200 °C in air for 15 minutes as the dielectric layer. A 50 nm gold thin-film was deposited with a sputtering system, which was patterned by illuminating UV light through SU-8 mold and spatially controlling the oxygen-inhibition in the acrylate mixture. After patterning the source and drain electrodes as described in experimental section, a 60 nm pentacene layer was then deposited on the top

by using PVD. The OTFTs were characterized using an Agilent E5270B Semiconductor Parameter Analyzer System and CASCADE probe station in ambient air. The performance of the OTFTs is shown by I_D - V_D and I_D - V_G curves in Figure 6.12.

Figure 6.12 OTFT I_D - V_D and I_D - V_G curves with a micrograph of one transistor device, inset shows a micrograph of a complete OTFT device.

Device mobility in the saturation regime is given by equation 2.3. The capacitance per unit area of the PVP dielectric was separately measured to be 4.25 nF/cm^2 . The field-effect mobility, μ , and the on/off ratio were calculated to be $1.3 \text{ cm}^2/\text{V s}$ and 1.2×10^4 respectively. The performance is comparable to that of devices made from other electrode patterning techniques including thermal evaporation^{158, 159}.

6.5 Conclusion

In conclusion, the first use of spatial control of oxygen-inhibition of photopolymerization in acrylate-based materials have been demonstrated as fabrication process for printed electronics and the use of the printed micropattern so created as an etch mask in the fabrication of high performance top- and bottom-gated OTFTs. The process has been further developed into a universal printing technique using SU-8 molds as a widely applicable and a promising low-cost fabrication process on different substrates for printed organic electronics. This new approach eliminates the delicate photolithographic tools, expensive photo-masks and resist required by the conventional lithography process, thus providing a much simpler manufacturing process. No surface/interfacial chemistry or adhesives are required in the process, and so it can be used in patterning a wide range of materials with high resolution (3 μm) for printed organic electronics without the necessity of idiosyncratic chemistry or surface modifications. The OTFT devices fabricated with this new lithography method demonstrate very good device performance for organic electronics applications such as RFID tags, data storage devices and sensors could be fabricated with this technique. Arrays of polymer patterns printed on thermal oxide capped silicon wafer and PET substrates were produced to demonstrate its universal patterning capability for different types of substrate materials. It may serve as enabling technology in low-cost medium-

performance printed organic electronics. Other semiconductors like CNTs and ZnO nanowires could readily replace the organic semiconductors to assist many other research areas in the future.

Chapter 7 All-printed CNT finFETs on plastic substrates for high performance flexible electronics

7.1 Introduction

The great attraction of printed electronics relies on the possibility to mass-manufacture flexible large-area electronics in a more simple and cost-effective way than conventional silicon-based ones. Printing electronics as potential low-cost alternatives to the silicon-based devices have wide applications from large-area electronics^{160, 161} such as active-matrix LCDs, organic light emitting diodes, e-paper to ultra-low-cost and flexible electronic devices^{162, 163} including wearable electronics, smart labels, radio frequency identification tags. Diverse types of materials including organic semiconductors, inorganic semiconductors and carbon nanotubes (CNT) have been made solution-processable for printing electronics on flexible substrates, but the poor performance is the major blockage in the potential applications. The highest mobilities reported for all-printed organic transistors ($0.1 - 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) are still inferior to that of a-Si^{163, 164}. Printable inorganic semiconductors exhibit better performances ($< 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)¹⁶², but the metal-organic precursors are difficult to prepare and a higher processing temperature ($200 \text{ }^\circ\text{C} - 400 \text{ }^\circ\text{C}$) is required^{162, 165}, which is apparently not suitable to use flexible plastic substrate.

CNTs possess excellent intrinsic electronic properties^{35, 166-168} and the pristine CVD grown CNT network transistors^{167, 169} have achieved mobilities of 10 - 100 cm² V⁻¹ s⁻¹ and on/off ratio of 100 - 1000. CNTs are also developed as printable inks to form conducting channels in transistors¹³ for low-cost, large-scale fabrication of printed electronics. However, the printed CNT transistor still displays mobility below 10 cm² V⁻¹ s⁻¹ mobility and on/off ratio less than 1000.^{13, 41, 42, 80, 170, 171} Most importantly, these are not an all-printed device since the fabrication still requires metal contacts produced by vacuum deposition and photolithography^{13, 80, 161, 166, 169, 171}, and thus are less attractive for printing electronics applications.

FinFET¹⁷² is a type of transistor developed in silicon electronics with dielectric and gate wrap around a silicon “fin” to have higher channel conduction while suppressing the short-channel effect. Here we describe a single-step transfer printing method to directly print a novel dielectric-wrapped CNT network structure similar to finFET for high performance flexible all-printed CNT transistors on a plastic substrate, which have demonstrate mobilities of 27 ± 10 cm² V⁻¹ s⁻¹ and on/off ratio of 10²-10⁴. The mobility is higher than that of transfer printed¹⁷⁰ and the ink-jet printed CNT transistors⁴² by one order and six times respectively. This direct printing technology only requires 95 °C heat-treatment at the most, and has fabricated transfer-printed metal patterns on a plastic substrate with dimensions of 4 cm × 2.5 cm, exhibiting a simple, cost effective and scalable process to produce flexible CNT based all-printed electronics for broad practical applications.

7.2 Process details

The transfer printing method is illustrated in Figure 7.1. Preparation of silicon mold is described in Chapter 2 and then Au film with a thickness of 100nm was sputtered on the passivated silicon mold by sputtering system. CNT solution was prepared by dispersing commercially available enriched SWCNTs (Nanointegris) of 99% purity in DI water with SDS as surfactant. The concentration is estimated to be 0.34 $\mu\text{g/mL}$. Brief sonication is used to assist CNT dispersion before deposition of CNT network on Au-coated mold. No further purification or functionalization is required in preparation of CNT solution and the resulted CNT network did not contain any specific alignment. The deposition of CNT network was conducted by using a pipette to place CNT solution droplets on protrusions of Au-coated silicon mold (Figure 7.1). After drying in a 70 °C oven, the mold was briefly soaked in DI water for 10 seconds to remove surfactants and the drop-coating, drying and soaking steps were repeated for 3 times.

For the transfer printing step, the substrate, poly (butylene succinate) (PBS) polymer film, was coated by sputtering Au film with a thickness of 100nm as the gate electrode in the transistor. Two layers of polyvinyl alcohol (PVA) dielectric thin-film were spin-coated (2000 RPM for 15 seconds using 5 wt % PVA solution in DI water) on top and dried in a 70 °C oven as dielectric layer in the transistor. Au-coated silicon mold with CNT network on top was brought

into contact with the substrate coated with Au and PVA thin-film. After contact is established, the whole construct was kept in a sealed chamber heated to 95 °C with DI water on the bottom for 90 minutes. After the “steaming” step, the sample was cooled down to room temperature and the mold was removed while the metal contacts together with CNT network on silicon mold were transferred onto the PVA layer. In the transfer printing process, the PVA thin-film has two functional rolls: dielectric layer in transistors and adhesive material for transfer printing process. During the “steaming” step, water vapor could help rearrange the polymer chain entanglement in PVA thin-film to produce intimate contact between PVA thin-film and Au surfaces, raising the noncovalent adhesive strength and facilitate the transfer printing process. In the resulted structure, CNT network was wrapped by dielectric and metal contacts and partially embedded in PVA dielectric as illustrated in Figure 7.1(c) in which the metal contacts were intentionally drawn as semi-transparent to show the CNT network underneath.

Figure 7.1 Schematic of the single-step transfer printing process. (a) Drop-coating carbon nanotube network and brought into contact with plastic substrate, (b) “steaming” treatment while mold-substrate contact is established. PVA thin-film behaves like an adhesive for transfer printing during “steaming”, (c) source and drain electrodes along with carbon nanotube network simultaneously transfer-printed on PVA thin-film, with carbon nanotube network embedded in PVA thin-film while wrapping the CNTs around by PVA to form finFET structure; the electrodes are intentionally drawn as semitransparent to display the carbon nanotube network underneath.

7.3 Characterization of printed CNT network

The transferred metal contacts on the plastic PBS substrate were shown in Figure 7.2(a). The dimensions of the PBS substrate as shown were 4 cm × 2.5 cm, which can be scaled up to larger substrates without any obvious difficulties.

The inset image in the figure shows a pair of source and drain electrodes with channel observable due to different light reflection in the channel area. The width of the channel is $2000\ \mu\text{m}$ defined by the dimension of silicon mold protrusions. It should be noted that the transfer printing process was carried out in a non-clean-room environment and some dust particles can be observed on the sample, but all the transfer printed metal contact pads are functional as source and drain electrodes in the transistors.

The transferred CNT network was characterized by field emission scanning electron microscopy (FE-SEM) (Figure 7.2(a) and (b)). The results show that the transferred CNT network has densely and randomly distributed CNT bundles connected with the source and drain electrodes to form the conducting channel with a length of $5\ \mu\text{m}$, and the well-networked CNTs are embedded in the dielectric layer, clearly confirming the finFET structure in the all-printed devices.

Figure 7.2 Characterization of all-printed CNT network finFET structure. (a) Transferred metal contacts on the plastic PBS substrate, the dimensions of the

PBS substrate as shown were $4\text{ cm} \times 2.5\text{ cm}$, the inset image shows a pair of source and drain electrodes with channel observable due to different light reflection in the channel area, (b) transferred CNT network embedded in the PVA dielectric layer, showing the finFET structure in the all-printed device and channel length is $5\text{ }\mu\text{m}$, (c) magnified FE-SEM image of the CNT random network wrapped around by the PVA dielectric.

7.4 Characterization of printed TFT

The transfer-printed CNT network transistor was characterized using CASCADE Microtech probe station and Agilent E5270B measurement system. Figure 7.3(a) shows the transfer characteristics curve by sweeping gate voltage from 1V to -4V while keeping drain voltage at constant of -0.2 V and the curve is plotted using drain current against gate voltage while Figure 7.3(b) shows the drain current plotted against drain voltage with gate voltage stepped at 0V, -2V and -4V showing that the conductance of the channel is increasing with higher gate voltage. The mobility of the device is extracted from equation 2.4. C_i is separately measured to be 17.5 nF/cm^2 by fabricating 12 ITO-PVA-silver capacitors and averaging the capacitance of all 12 capacitors. For the 20 all-printed devices, the estimated hole mobility is $27 \pm 10\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ and on/off ratio is within $10^2 - 10^4$, of which the mobility is higher than the reported best all-printed CNT transistors by six times⁴². The variation in mobilities for different devices is also reported by other printed CNT devices^{169, 173, 174} and should be able to be improved by quality control during mass production.

Figure 7.3(c) shows an FE-SEM image of a defect along the edge of a transferred metal contact. The defect reveals the CNT network sandwiched between the transferred metal contact and PVA dielectric layer and furthermore, it can be observed more clearly that the CNT network is embedded in PVA dielectric layer. The CNT network embedded in PVA dielectric layer, which is structurally similar to the finFET¹⁷² devices in silicon electronics, should play a critical role in achieving the high mobility. The mobility enhancement mechanism can be schematically illustrated in Figure 7.3(d), in which hole carrier generation in a printed finFET is presented in comparison to that in a normal top-contact device. Similar to the working concept of finFET, hole carriers can be induced all around CNT bundles at proper gate bias when the dielectric layer wraps around CNT bundles in printed CNT finFETs, thus all CNTs on the surface of bundles contribute to the effective conduction channel and generate high device mobility; whereas in a normal top-contact device, CNT bundles lie on top of the dielectric layer and hole carriers can be induced only at the small bottom part of the bundle adjacent to the dielectric interface.

Figure 7.3 Transistor devices: performance and structure. (a) Transfer characteristics of the CNT network transistor, (b) output characteristics by plotting drain current versus drain voltage of the device, (c) FE-SEM image of a defect along the edge of a transferred metal contacts, showing that the CNT network is embedded in PVA dielectric layer, (d) comparison of hole carrier generation in a printed finFET in which CNT bundles are embedded in dielectric and a normal top-contact device in which CNT bundles are on top of dielectric.

7.5 Conclusion

In conclusion, a single-step transfer printing method has been demonstrated to fabricate all-printed CNT transistors structurally similar to finFET to have high performance with mobility of $27 \pm 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and on/off ratio 10^2 - 10^4 . It is believed that the enhancement mechanism is similar with the finFET structure

in silicon transistors. This simple, cost-efficient and low-temperature transfer printing method can be scaled up for large-area plastic substrates, thus providing versatile manufacturability of all printed flexible CNT-based electronics for wide practical applications.

Chapter 8 General conclusion and future work

8.1 General conclusion

In this dissertation, unconventional printing processes for printed electronics, especially printed TFTs, have been reviewed thoroughly. Device basics, materials applied, and issues in printing processes with organic and CNT TFTs are presented. It remains challenging to have a fast, low-cost, and reliable printing process on large-area substrates with wide applicability, and the impact of printing processes on device performance from different aspects is still underexplored. Developing new printing processes and improving existing processes can boost the performance and manufacturability of organic semiconductor/CNT-based printed electronics.

A UV transfer embossing process (few-micron resolution limited by master template) using a selective cross-linking process in resin was improved by adapting the process into fabrication of bottom-gated printed TFTs so that the resulting printed OTFT showed one order higher mobility ($0.01 - 0.02 \text{ cm}^2/\text{V s}$) and two orders higher on/off ratio (10^4) when compared to top-gated devices. Study on the effect of the printing process on electronic devices has shown lower gate leakage current and off current, as well as significant roughness reduction at the dielectric-semiconductor interface, all of which contribute to improved device performance. The improved printing technique with faster

process speed and better reliability can be feasible for medium-performance and/or disposable applications such as electronic paper and large-area environmental sensors.

Using PDMS-based nanocomposite dielectric material capable of performing in-situ polymerization process, the transfer embossing process was further improved into a low-cost adhesive-free direct transfer printing process (resolution down to 3 μm). The effect of an adhesive-absent semiconductor-printed electrode interface was studied by width-normalized contact resistance, which is measured to be on the order of $\sim 100 \text{ k}\Omega\cdot\text{cm}$, and further improved device performance with a high mobility of $0.038 \text{ cm}^2/\text{V s}$ and on/off ratio of $10^4 - 10^5$ was demonstrated. The printed devices also demonstrate low hysteresis ($\Delta V_{\text{th}} = 1.2 \text{ V}$) and low threshold voltage (-1.3 V) due to the inert nature of the dielectric-semiconductor interface. By varying the ratio of titanium dioxide nanoparticle to PDMS, dielectric constant of the nanocomposite was optimized for the printing process. With optimized dielectric constant and thickness of nanocomposite, the transfer efficiency of gold patterns can reach a very high level while avoiding the short-channel effect in the printed transistors.

The above transfer printing processes were found to be limited by the interfacial properties between the contacted surfaces, so the first use of spatial control of oxygen-inhibition of photopolymerization in acrylate-based materials

has been demonstrated as a printing-like process, which was further developed into a universal printing technique using SU-8 molds as a widely applicable process on different substrates for printed electronics. The new approach eliminates the delicate photolithographic tools, expensive photo-masks and resist required by the conventional lithography process, thus providing a much simpler manufacturing process. No surface/interfacial chemistry or adhesives are required in the process, so it can be used in patterning a wide range of materials with high resolution (3 μm limited by the master template) for printed electronics without the necessity of idiosyncratic chemistry or surface modifications. Arrays of polymer patterns printed on thermal oxide capped silicon wafer and PET substrates were produced to demonstrate its universal patterning capability for different types of substrate materials. The printed organic TFTs fabricated with this new printing method demonstrate very good device performance. Other semiconductors like CNTs and ZnO nanowires could readily replace the organic semiconductor to be of use in many other research areas in the future.

The above printing-like process, though simpler than photolithography, is still more complicated than other unconventional printing processes. Therefore, a single-step transfer printing method to transfer both semiconductor and metal contacts at the same time directly onto a PVA dielectric layer was developed for simple, low-temperature fabrication of printed TFTs. In addition, taking advantage of the versatile printing process, all-printed CNT finFETs with a unique dielectric-wrapped CNT network were fabricated, demonstrating high

performance with mobility of $27 \pm 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an on/off ratio 10^2 - 10^4 . This simple, cost-efficient, and low-temperature transfer printing method can be scaled up for large-area plastic substrates, thus improving manufacturability of all printed flexible CNT-based electronics for wide practical applications.

In summary, the chemical sciences involved in newly developed or improved printing technologies were studied to improve existing printing processes for high performance organic semiconductor/CNT-based printed electronics and to address the issues in other printing processes. Systematic investigations of how the printing processes would affect the fundamental device physics of the printed devices were conducted. This research offers chemical, electronic, material, and mechanical engineering approaches to greatly improve the performance and manufacturability of printed electronics, in addition to providing fundamental insights into the effect of the printing process on devices.

8.2 Future research opportunities

Printed electronics are of great interest to low-cost, disposable, medium-performance electronic applications. For this type of application, even though the resolution requirement is not as high as for high-speed electronics, miniaturization of devices would always contribute to further reduction of cost. With the use of a master template with nanoscale feature sizes, it is fundamentally interesting to observe how the printing processes would evolve

into nanoscale. In the printing process by spatially controlled oxygen-inhibition effect in acrylate materials, the diffusion of oxygen into acrylate mixture will ultimately affect the resolution capability of this process when feature size approaches 10 – 100 nm. The study of the oxygen diffusion process from mold trenches into acrylate mixture is of fundamental importance. It is also technologically significant to fully control the diffusion process for the production of patterns with feature sizes smaller than the master template.

There also remain many challenging issues in the integration of printed devices into printed circuits and further packaging into products. First, roll-to-roll manufacturing is a very promising technique for high throughput, large-area applications. All the printing processes developed in this project should be studied for integration into roll-to-roll processes. Flexible/soft molds should be developed with appropriate choices of mold material, as the roller of the process and the material deposition method should be adapted accordingly instead of using a spin-coating technique. Second, the drive current of the printed transistors has to be increased, possibly by further reduction in critical feature size in the printed transistors or by searching for other materials such as semiconductor nanomaterials with better intrinsic electronic properties. Third, the printed devices should be fully patterned including gate electrode and dielectric layer, to reduce parasitic capacitance for high frequency applications.

In the single-step transfer printing process to fabricate printed CNT transistors, PVA and water vapor were used to enhance the adhesion between metal

contacts and the PVA surface. As enhanced adhesion was observed using other polymers and their solvent vapors, this transfer printing process can be further generalized into using a series of polymers and the corresponding solvent vapors. The success of this research can provide much broader material availability, which is needed in order to print materials that are sensitive to water vapors and to have more surface engineering options to the surfaces of the polymers. Systematic study may also lead to identification of the best combination of polymer and solvent vapor for patterning techniques, depending on surface roughness, vapor dissolution, *etc.*

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Publications

Journal papers

1. **J. S. Shi**, M. B. Chan-Park, C. M. Li*: Bottom gate organic thin-film transistors fabricated by ultraviolet transfer embossing with improved device performance. *Organ. Electron*, 10, 396–401, **2009**.
2. **J. S. Shi**, M. B. Chan-Park, C. Gong, H. B. Yang, Y. Gan, C. M. Li*: Spatially controlled oxygen-inhibition of acrylate photopolymerization as a new lithography method for high performance OTFTs. *Chem Mater*, 22 (7), 2341–2346, **2010**.
3. **J. S. Shi**, M.B. Chan-Park, and C.M. Li, Adhesive-Free Transfer of Gold Patterns to PDMS-Based Nanocomposite Dielectric for Printed High-Performance Organic Thin-Film Transistors. *ACS Applied Materials & Interfaces*, 3 (6), 1880–1886, **2011**.
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Electronics. *Advanced Materials*, published online 2011, DOI:
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7. G.C. Yuan, Z. Xu, C. Gong, Q.J. Cai, Z.S. Lu, **J.S. Shi**, F.J. Zhang, S. L. Zhao, N. Xu, C. M. Li*: High performance organic thin-film transistor with phenyltrimethoxysilane-modified dielectrics. *Applied Physics Letters*, 94, 153308, **2009**.
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9. Y.H. Xiao, C. M. Li*, S.Q. Wang, **J.S. Shi**, C. P. Ooi: Incorporation of collagen in poly(3,4-ethylenedioxythiophene) for a bifunctional film with high bio- and electrochemical activity. *Journal of Biomedical Materials Research: Part A*, 92A (2), 766-772, **2010**.

Conference papers

J. S. Shi, M.B. Chan-Park, and C.M. Li, Low-cost fabrication processes for printed electronics. *ICMAT 2011*.

Patents

1. Spatially controlling oxygen-inhibition in photopolymerization process for low-cost patterning of organic transistors (filed)
2. Solution processed, transfer-printed carbon nanotube network sandwich structure for high performance printed ambipolar transistors (filed)