Multilevel diode clamped converter with space vector modulation and DC-link capacitor voltage balancing

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**MULTILEVEL DIODE CLAMPED CONVERTER
WITH SPACE VECTOR MODULATION AND DC-
LINK CAPACITOR VOLTAGE BALANCING**

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**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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Multilevel Diode Clamped Converter with Space Vector Modulation and DC-Link Capacitor Voltage Balancing

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List of Abbreviations

Acronyms

AC	Alternating current
ANPC	Active neutral-point-clamped
CMI	Cascaded multilevel inverter
CSI	Current source inverter
DC	Direct current
EMI	Electromagnetic interference
EV	Electric vehicle
FACTS	Flexible ac transmission system
GTO	Gate turn off thyristor
HVDC	High voltage direct current
IGBT	Insulated-gate bipolar transistor
JFET	Junction gate-field transistor
LS-PWM	Level shifted pulse width modulation
MDCI	Multilevel diode-clamped inverter
MFCI	Multilevel flying capacitor inverter
M2DCI	Multiple-pole multilevel diode-clamped inverter
MMI	Modular multilevel inverter
MOSFET	Metal-oxide-semiconductor field-effect transistor
NPC	Neutral-point-clamped
NPP	Neutral-point-potential
PCC	Point of common coupling
PI	Proportional + Integrator
PLL	Phase lock loop
PMSM	Permanent magnet synchronous motor
PS-PWM	Phase shifted pulse width modulation
PWM	Pulse width modulation
RMS	Root-mean-square
SCR	Silicon-controlled rectifier
SiC	Silicon Carbide
SVM	Space vector modulation
THD	Total harmonic distortion

UPF	Unity power factor
VSD	Variable speed drive
VSI	Voltage source inverter
3D	Three dimensional

Variables

C_{tot}	Equivalent capacitance value in the DC-link
E_{dc}	DC-link voltage
i_A, i_B, i_C	Output current of the inverter circuit for phase (A,B,C)
$i_{C1}, i_{C2}, i_{C3}, i_{C4}$	Dc-link capacitor currents
i_1, i_2, i_3, i_4, i_5	The currents of five-level inverter through the top and bottom terminals of the dc-link and mid-point between the capacitors.
K_p	Proportional gain of the controller
K_i	Integral gain of the controller
L_1, L_2, L_3	STATCOM inductance of phase (A, B, C)
$L(s)$	Open-loop transfer function of the controller
m_A, m_B, m_C	Modulation control signal
m	Modulation amplitude
n	Number of voltage level
R_g	Grid resistance
R_s	STATCOM resistance
$S_{X1}, S_{X2}, S_{X3}, S_{X4}$	Switching states of five- level inverter switches
V_{An}, V_{Bn}, V_{Cn}	Output phase (A, B and C) voltages referenced to ground 'n'
V_s	Space vector generated by three phase voltage
$V_{C1}, V_{C2}, V_{C3}, V_{C4}$	DC-link Capacitor voltages
$\Delta V_{Cj}(k)$	Voltage error of jth capacitor C_j at the beginning of the sampling interval
θ_0	Initial phase angle of voltage
θ_L	Initial phase angle of PCC voltage
δ	Power factor

Abstract

Multilevel converters are very popular in medium/high power conversions due to their capability to generate high quality voltage magnitudes with low harmonics while employing devices of smaller voltage ratings. The output voltage waveform of multilevel inverter consists of multiple steps of smaller magnitudes designed to reduce electromagnetic interference (EMI) commonly produced by rapid switching that generate lesser common mode currents at motor shaft and bearings due to reduced dv/dt . The neutral point clamped (NPC), cascaded H-bridge (CHB) and flying capacitor (FC) converters are considered as the three classical multilevel converter topologies which have found their way to industrial applications almost two decades ago. To expand the application field of multilevel converters by overcoming the challenges associated with classical topologies, new multilevel topologies and modulation techniques are developed.

In this thesis, various NPC multilevel inverter topologies and its modulation techniques are investigated. Diode-clamped multilevel inverter (DCMI) for more than three-level operation is less attractive due to dc-link capacitor voltage unbalancing issues and increased conduction losses caused by the commutation of $(n-1) \times (n-2)$ clamping diodes connected in series per-leg of an n -level diode clamped inverter. A converter topology with minimum number of series connected devices which balance the total voltage equally between the semiconductors and new multilevel modulation schemes, which on more number of levels, redundant voltage vectors and zero common mode voltage vectors available in higher level DCMI, can be used together to solve the above mentioned issues.

In this thesis, the voltage unbalance issues and capacitor voltage balancing techniques in DCMI are studied in detail. An extensive analysis of two modulation techniques, level-shifted PWM (LS-PWM) and space vector modulation (SVM) are presented and a SVM based voltage balancing strategy for three-level and five-level diode clamped inverters are developed by utilizing redundant switching vectors without the need of any additional controls or auxiliary circuits. The proposed balancing strategy is tested on a five-level reduced device topology. Multiple-pole multilevel diode-clamped inverter (M2DCI) which is derived from three-level DCMI topology and uses lesser number

of clamping diodes compared to the classic five-level DCMI. The capacitor currents as well as dc-link intermediate branch currents are obtained from the switching function model of five-level M2DCI, which reduces the number of calculations at each sampling periods while implementing the voltage balancing strategy when compared to sector based methods. The stability limits of the proposed voltage balancing strategy for M2DCI based on load power factor angle and modulation indices have been obtained at various load conditions. The investigations shown here are modelled in Matlab/Simulink® and PSIM environment and verified using experimental results.

It is found that to achieve capacitor voltage balancing, modulation index is restricted to about 60% of its maximum value when loads of high power factor i.e $PF \geq 0.8$ is connected at the converter terminals. Hence the proposed reduced device topology with SVM technique, which self-balances the dc-link capacitors has been extended for reactive power control in a grid connected environment. Additionally, the application of five-level multiple-pole multilevel diode-clamped converter (M2DCC) as STATic synchronous COMpensator (STATCOM) is investigated with the proposed space vector modulation based balancing strategy. The proposed scheme maintains a balanced voltage across the dc-link capacitors and exchange reactive power at various load conditions. Further, the performance of STATCOM and controllers are investigated through modelling done in Matlab/Simulink® and PSIM environment. The proposed reduced device topology together with SVM based voltage balancing technique is expected to give good performance for reactive power applications by reducing the converter losses, size, weight and THD.

Chapter 1

Introduction

1.1. Overview of Research in Power Electronics

Power electronics deals with the conversion and control of electric power using power semiconductor devices. It is widely used in recent applications such as smart grid, renewable energy, electric/hybrid electric systems and high-efficiency energy systems. Research in power electronics focus mainly on four areas; power semiconductor devices, converter systems, motor drives and general energy systems, to expand the range of applications and to improve the energy efficiency (Figure 1. 1). The voltage and current ratings and switching characteristics of power semiconductor devices can be improved with the development of new devices based on silicon and large band gap power semiconductor devices [1, 2]. Wide band gap semiconductors like silicon carbide (SiC) possess high breakdown voltage, high temperature operation capability, and high thermal conductivity properties when compared to silicon which gives significant improvement on system performance [3-5].

Power converter can be treated as a network consisting of power semiconductor devices which can be uncontrolled, partially controlled or fully controlled for power conditioning. They can be classified as: ac to dc, ac to ac, dc to dc and dc to ac converters. Researchers are continuously focusing on improving the performance of the power conversion system either by deriving new converter topologies or by modifying the control techniques. Multilevel converters are very popular in medium-high power conversions due to their capability to generate high voltage magnitudes with low output harmonics while using devices of smaller voltage ratings. They are employed in a wide range of products which is being used in applications such as Power systems [6, 7] (AF, STATCOMs, DVRs and UPQC), Traction [8-10], Ship propulsion [11], Automotive [12], Alternative energy sources

Figure 1. 1: Research areas in power electronics.

and Hydro pumped energy storage [13-15]. Though multilevel converter was introduced for reducing the magnitude of harmonics in motor drive system; they have found a remarkable place as power converters in high-voltage high-power applications.

Another promising application of power electronics is electrical drives or adjustable speed drives (ASD) [16-20]. The range of power, speed and torque requirements in drive system varies based on the type of application. Traction drives need to operate over a wide range of frequencies and require medium-voltage and high-power. Ship propulsion deals with megawatt power and it is necessary to improve the dynamic performance and input power quality to have more efficient and smaller power system. Transportation, wind power generation, pumps, etc., usually require medium-power range. An appropriate selection of converter, machine and control is important to achieve higher energy efficiency, and higher reliability drive system. New techniques like multilevel and multiphase power converters have been developed in the past decade for providing higher reliability and fault tolerant control of ASD in applications like automotive, aerospace, nuclear plant and ship propulsion. Matrix converters are used to improve the power density of electrical drives. The sensorless control, multiphase machines and fault-tolerant control algorithms are also to be addressed to increase the reliability of drive system for diverse applications.

Figure 1. 2: General system for electric power conversion.

The conventional energy sources like fossil fuel and hydroelectric generators are replaced or integrated with alternative energy sources such as wind and PV along with large energy storage devices to meet the energy demand. Batteries, ultra-capacitors, hydrogen and super conducting magnetic storage (SMES) are some examples of energy storage devices. Sophisticated control functions (e.g., active/reactive power control, harmonic compensation, power quality assurance, frequency and voltage regulations, dc-link control) are involved while integrating energy systems with the utility systems. Innovations in the field of power electronics, mainly converters as an interface with the grid and control bring new solutions for providing a reliable, robust and manageable power system network.

1.2. Motivation for Research: Multilevel Converters - Current and Future Power Applications

The general system for electric power conversion shown in Figure 1. 2: employs a power converter along with a controller to convert power from source to load based on application. If the source is DC and an AC motor is connected as a load then a two-level voltage source inverter (VSI) as shown in Figure 1. 3 is used to convert fixed DC to variable voltage and variable frequency AC at the motor terminals. By controlling the inverter, the DC can be converted to variable voltage and variable frequency AC as demanded by the motor speed. The two-level inverter pole voltage (voltage at the inverter poles A, B, C with respect

Figure 1. 3: Two-level VSI fed AC motor drive.

to negative DC bus terminal ‘N’ in Figure 1. 3) can attain only two distinct values ($+ E_{dc}$ or zero) if the switches in an inverter leg are switched in complimentary manner. The inverter generates pulsed voltage at the output terminals which consists of fundamental component and harmonics centered on the switching frequency and its multiples. The output voltage of the inverter can be controlled by proper PWM controller. The higher switching frequency operation of the inverter power devices leads to higher waveform quality in output voltage and current, faster dynamics but increased switching loss. But due to various problems, the switching frequency cannot be increased beyond a certain limit especially in high power application. Hence a new class of inverters called multilevel inverter can be used for solving all these problems. Multilevel inverters generate staircase-type output voltage waveform from several levels of dc-voltage sources. The single leg representation of n-level inverter shown in Figure 1. 4 consists of a single- pole- multiple-throw switch. Based on the switching state value S_x , the pole voltage with respect to the negative DC bus (V_{AN}) can attain any of the n levels $V_{AN} = \{0, \frac{E_{dc}}{n-1}, \frac{2E_{dc}}{n-1}, \frac{3E_{dc}}{n-1}, \dots, E_{dc}\}$ corresponding to the switching state ‘ S_x ’ values $S_x = \{1, 2, 3, 4, \dots, n\}$ respectively. The number of steps in line-to-line voltage is given by

Figure 1. 4: Representation of one leg of n-level inverter.

$$k = 2n - 1 \quad (1.1)$$

And number of steps in line-to-neutral (phase) voltage is given by

$$p = 4n - 3 \quad (1.2)$$

When the number of levels increases, the multilevel inverter configuration consists of higher number of switching devices and the voltage stress across the each device will reduce, which makes this topology suitable for high voltage application where low voltage rating devices can be used. Hence they can reach high voltages with reduced harmonic distortion and lesser EMI emissions using devices of smaller voltage ratings which make them suitable in medium-to-high power applications.

The “neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC) converters are considered as the three classical multilevel converter topologies. The recent topologies are either derived from the classical topologies or hybrid of the classical topologies [21]. Table 1. 1 gives a comparison of multilevel converter topologies depending on implementation factors [22]. They are used for practical applications such as utility interface for renewable energy systems, marine propulsion, static var generator (SVG), back-to-back intertie system for the UPFC (unified power flow controller), and for wide-range

Figure 1. 5: An illustration showing the applications of multilevel converter.

Table 1. 1: Comparison of Multilevel Converter Topologies depending on Implementation Factors

	NPC	FC	CHB
Specific Requirement	Clamping diodes	Additional capacitors	Isolated dc sources
Modularity	Low	High	High
Design and implementation complexity	Low	Medium (capacitors)	High (input transformer)
Control concern	Voltage balancing	Voltage setup	Power sharing
Fault tolerance	Difficult	Easy	Easy

variable-speed drive systems. The overview of multilevel converter applications [22] is shown in Figure 1. 5. Among the three classical multilevel converter topologies NPC has become quite popular in high-power AC drive applications, regenerative applications as back-to-back configuration (conveyors for mining industry) and grid interface for renewable energy sources like wind power. The main challenge in operating with n-level NPC converter is to retain the voltage across the dc-link capacitors to ' $1/(n-1)$ ' times the total dc-link voltage during steady state and transient operations. Also, the high reverse recovery current through the clamping diodes in NPC will increase switching loss in other semiconductor

devices and can affect the efficiency of the converter. The efficiency of the converter can be improved by reducing the switching losses, conduction losses and harmonics generated by the converter by selecting a suitable topology and modulation technique which motivates further development in multilevel technology.

1.3. Research Objectives

The voltage imbalance in dc-link capacitors of classical NPC multilevel inverters generates lower order harmonics in the output voltage and increases the voltage stress on the switching devices which may result in permanent damage to the semiconductor devices. The converter topology which minimizes the series connected devices and shares the total voltage equally among the devices during a valid switching state is required for achieving improved efficiency.

The main objective of this research is to study the dc-link capacitor voltage unbalance in classical NPC multilevel converter topology and to implement a space vector modulation (SVM) based voltage balancing strategy at reduced computational efforts compared to the conventional sector based SVM methods. A new NPC topology with reduced number of clamping diodes compared to classical five-level NPC topology is also investigated to implement SVM based voltage balancing strategy. This will significantly reduce the number of clamping diodes/phase and eliminates the need of balancing circuit which will improve the performance of the system by reducing the converter losses, size, weight, cost and THD. The possibility of the proposed methodology for STATCOM application and the performance evaluation during transient and steady-state operating conditions are also included in this research.

1.4. Organization and Contributions of the Thesis

This thesis investigates the dc-link capacitor unbalancing problems associated with NPC multilevel converters and how the issues are addressed with the introduction of lesser computational required SVM using redundant voltage vector property. The proposed SVM

algorithm has been initially simulated using Matlab/Simulink® and PSIM environments and then experimentally verified on a 1.5 kW laboratory prototype. A new five-level multiple-pole multilevel diode clamped inverter (M2DCI) based STATCOM using SVM for dc-link capacitor voltage balancing is proposed and performance evaluation during various operating conditions are also done. The studies are presented as separate chapters in this thesis and the contributions are provided in Chapters 3-5.

Chapter 2 presents a detailed literature review of multilevel inverter structures, modulation techniques, operational and technological issues. Classical multilevel inverter structures and some newly developed multilevel topologies derived from basic topologies for various industrial applications are presented. Some of the popular PWM schemes for multilevel inverter control like *sine-triangle* modulation in time domain and *space vector* modulation in stationary reference frame are also presented. Furthermore, the capacitor voltage fluctuations in multilevel inverters and balancing techniques are also described.

Chapter 3 presents an extensive analysis of neutral point potential (NPP) unbalance issues and balancing techniques for three-level NPC. Here balancing methods based on level-shifted PWM (LS-PWM) and space vector modulation (SVM) are proposed. It is shown that LS-PWM has higher harmonic distortions and high losses when compared to SVM. The experimental results are presented to validate both simulation and theoretical results.

In Chapter 4, the capacitor balancing of five-level NPC multilevel inverter by means of balancing circuit and LS-PWM technique is verified through simulation done in Matlab/Simulink® and PSIM environments. Then a space vector modulation (SVM) based voltage balancing strategy has been proposed for a new five-level multiple-pole multilevel diode-clamped inverter (M2DCI) topology which consists of lower number of clamping diodes compared to the classic 5-level NPC inverter. The control method utilizes the redundant voltage vector property to balance the dc-link capacitor voltages without using any auxiliary hardware.

A simple switching function model is derived to predict the capacitor currents and dc-link intermediate branch currents; this will help to implement the voltage balancing strategy in a reduced number of calculations at each sampling period compared to the sector based methods. The dependence of the capacitor voltage variation on the load power factor and modulation index has been extensively studied and the stability plot for proposed system is also shown. The voltage control strategy under various operating conditions is evaluated and the results are experimentally verified on a 1.5 kW laboratory prototype.

Chapter 5 investigates the performance of five-level M2DCI for STATCOM application using the proposed lesser computational required SVM to balance the dc-link capacitor voltages. STATCOM steady-state model and controller design are also presented. The reactive power compensation of ac system in transient and steady-state conditions under balanced, unbalanced and non-linear operating conditions are achieved by controlling the five-level M2DCI. It is shown that, the individual dc-link capacitor voltages remain stable and balanced during all operating conditions. The simulation results obtained using Matlab/Simulink® and PSIM environments are also presented to validate the proposed system.

Chapter 6 gives an overview of the research work and the suggestions for future work.

Chapter 2

A Review of Multilevel Converters- Structure, Modulation Methods and Operational Issues

2.1. Introduction

For better understanding the concept of multilevel converters and their advantages over the conventional two-level VSI, a brief operation and analysis of general n -level inverter is presented below. The classical and various commercialized multilevel topologies, multilevel modulation techniques, operational and technological issues are presented in the subsequent sections. The single leg representation of two-level inverter shown in Figure 2. 1 (a) consists of a single pole double through (SPDT) switch. Based on the switching state value S_A , the pole voltage with respect to the negative DC bus (V_{AN}) can attain any of the two levels $V_{AN}=0$ and $V_{AN}=E_{dc}$ when switching state ' S_A ' becomes 1 and 2 respectively. The other two phases can also be represented in the similar way. The three-level inverter shown in Figure 2. 1 (b), consists of three switching states, $S_A = \{1, 2, 3\}$ and $V_{AN} = \{0, \frac{E_{dc}}{2}, E_{dc}\}$ are the corresponding pole voltage magnitudes. For a general n -level inverter, as shown in Figure 2. 1 (c), the switching states have a range from 1 to n .

The pole voltages of the inverter with respect to bottom (negative) node of the DC bus are defined as

$$\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \frac{E_{dc}}{n-1} \begin{bmatrix} S_A - 1 \\ S_B - 1 \\ S_C - 1 \end{bmatrix} \quad (2.1)$$

where n is the number of levels and $S_A, S_B, S_C = \{1, 2, 3\}$.

The load phase voltages can be expressed in terms of the inverter pole voltages by

Figure 2. 1: Representation of one leg of the inverter (a) two- level (b) three- level (c) n - level.

$$\begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} \quad (2.2)$$

Similarly the inverter line-to-line voltages can be written as

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} \quad (2.3)$$

The inverter pole voltages contain third harmonic components, which are absent in the line-to-line voltage and line-to - neutral voltage. The number of steps in the line-to-line voltage is given by

$$k = 2n - 1 \quad (2.4)$$

and number of steps in the line-to-neutral (phase) voltage is given by

$$p = 4n - 3 \quad (2.5)$$

As the number of levels increases, the multilevel inverter configuration consists of larger number of switching devices and the voltage stress across the each device will reduce, which makes this topology suitable for high voltage application where low voltage rating devices can be used.

The advantages of using the multilevel inverter fed systems can be summarized as:

- Lower Total Harmonic Distortion (THD)
- Reduced electromagnetic interference problems
- Lower blocking voltage rating for the switching devices

The following section describes the classical multilevel inverter topologies and some newly developed topologies.

2.2. Multilevel Converter Topologies Overview

The classification of high-power converters is given in Figure 2.2 [22]. The high power two-level VSI requires high power semiconductor devices whereas multilevel converters are operated using medium power semiconductors. The “neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC)” are the three classical multilevel converter structures which are commonly applied in industrial applications. The multilevel converters can be operated as an inverter or rectifier circuit. This chapter mainly focuses on multilevel inverter structures. The concept of stepped output wave generation was developed and patented by W.McMurry in 1971, by connecting H-bridges in series [23]. The Flying Capacitor and Diode Clamped converter were subsequently developed and patented by J.A Dickerson *et al* [24] and R.H.Baker [25], respectively. In 1980s the current source inverters are the main research focus for developing high power converters by increasing the inverter current. And the idea of increasing the voltage instead of current by developing new converter topologies produced the first NPC three-level inverter for medium voltage applications by Nabae *et al* in 1981 [26]. The following sections discuss various multilevel inverter structures in detail.

Figure 2. 2: Classification of high-power converters.

2.2.1. Cascaded H-bridge Multilevel Inverters

The single phase full bridge inverters are connected as shown in Figure 2. 3 to form a per leg configuration of a cascaded multilevel structure. Each full bridge cell generates 3 voltage levels ($+\frac{E_{dc}}{2}$, 0 or $-\frac{E_{dc}}{2}$) and by connecting 2 such cells as in Figure 2. 3 (a) provide 5 different voltage magnitude (E_{dc} , $+\frac{E_{dc}}{2}$, 0, $-\frac{E_{dc}}{2}$ or $-E_{dc}$) at the pole of the inverter, V_{A0} . Though this topology requires large number of isolated DC supply, the inverter structure is simple without any capacitor unbalancing issues, clamping diodes and can easily extend to any level of operation. In general, the number of steps in the output pole voltage for cascaded inverter structure is given by $n = (2m + 1)$, where m is number of isolated DC supplies per phase [27].

Figure 2. 3: Single phase structure of cascaded H-bridge configuration (a) five-level inverter (b) seven-level inverter.

The cascaded H-bridge (CHB) configuration has been used for medium voltage drives with output voltage ranges from 2.3kV-7.2kV and output power of 200kW to 12MW [28]. The phase-shifting PWM (PS-PWM) technique used for cascaded H-bridge shifts the harmonics to higher frequency side and enables the converter devices to operate at low average switching frequency [29]. This allows air cooling and reduces the losses. The main disadvantage of cascaded H-bridge multilevel converter is the requirement of large phase-shifting transformer used for providing isolated dc sources which will increases the system size and cost [21, 29].

2.2.2. Neutral Point Clamped Multilevel Inverters

Here the dc-bus voltage is divided among the series connected capacitors to generate small voltage levels [26] . Figure 2. 4 shows the schematic of a three-level diode clamped

inverter where clamping diodes and capacitors are used to produce multiple levels in the AC output voltage waveform. Each leg consists of four active switches with anti-parallel diodes where IGBT can be used as switching device. The midpoint of the dc-bus capacitors is called the neutral point '0'. Depending on current direction in each phase, inverter output terminals can be clamped to this neutral point by means of the respective diodes (D_{x1} and $D_{x1'}$, where $x = \{A, B, C\}$) connected to the neutral point in the leg [26]. In Figure 2. 4, the inverter switches are operated in complementary manner, such as, in leg-A, S_{A3} is switched complementary to S_{A1} and S_{A4} is switched complementary to S_{A2} .

Figure 2. 4: The circuit schematic of three-level diode clamped inverter (DCI).

If the two capacitors are equally charged to half of the dc-bus voltage and S_{A1} and S_{A2} are turned on, the inverter output terminal 'A' is connected to positive dc-bus terminal and the pole voltage V_{AO} is equal to half of the dc-bus voltage $\frac{E_{dc}}{2}$. And if S_{A2} and S_{A3} are on then the terminal 'A' is connected to neutral point '0' through any of the clamping diodes, D_{A1} and $D_{A1'}$ depending on the direction of load current in phase 'A', hence 'zero' voltage level is generated.

Table 2. 1: Switching States and Pole Voltages of three-level Inverter (X=A,B,C)

Switching symbol	Voltage Level L_X	Switching states		Pole Voltage (V) V_{X0}
		S_{X1}	S_{X2}	
P	3	ON	ON	$E_{dc}/2$
O	2	OFF	ON	0
N	1	OFF	OFF	$-E_{dc}/2$

The third level ($V_{A0} = -\frac{E_{dc}}{2}$) is obtained by turning on S_{A3} and S_{A4} . The switches S_{A1}

and S_{A3} act in a complementary manner. That means when one switch is turned on the other must be turned off. And S_{A2} and S_{A4} are also act as complementary pair. Table 2. 1 gives the relationship between operating status of the switches, the switching state value and the inverter terminal voltage of the inverter. Since two switches are always on at any level of operation, the other two non-conducting switches shares the voltage stress equally which reduces the voltage rating of the devices to half of the DC bus voltage when compared to two-level VSI.

The three-level NPC topology is extended to generate higher levels of operation [30] . The per-phase diagram of five-level diode clamped inverter is shown in Figure 2. 5 and the switching status and inverter terminal voltage is summarized in Table 2. 2 [30]. The inverter switches S_{X5}, S_{X6}, S_{X7} and S_{X8} , are switched complementary to S_{X1}, S_{X2}, S_{X3} and S_{X4} respectively.

Figure 2. 5: The five-level DCI scheme with (a) diodes of different ratings, (b) diodes of equal ratings.

The clamping diodes share unequal voltages during each switching states. For instance, when leg

Table 2. 2: Switching States and Pole Voltages of five-level DCI (X=A,B,C)

Voltage Level L_X	Switching states				Pole Voltage (V) V_{X0}
	S_{X1}	S_{X2}	S_{X3}	S_{X4}	
5	ON	ON	ON	ON	$E_{dc}/2$
4	OFF	ON	ON	ON	$E_{dc}/4$
3	OFF	OFF	ON	ON	0
2	OFF	OFF	OFF	ON	$-E_{dc}/4$
1	OFF	OFF	OFF	OFF	$-E_{dc}/2$

‘A’ switches are operated to generate a pole voltage of $-\frac{E_{dc}}{2}$ (level-1), the reversed biased voltage across clamping diodes D_{A1} , D_{A2} , D_{A3} are $3E_{dc}/4$, $E_{dc}/2$, $E_{dc}/4$ respectively. Hence to use equal rating devices, a diodes having voltage rating $E_{dc}/4$ are connected in series as shown in Figure 2. 5 (b).

In general for n-level NPC inverter topology, each capacitor has voltage equal to $E_{dc}/(n-1)$ and the voltage stress on each switching device is equal to $E_{dc}/(n-1)$. The number of diodes required per phase is given by $2(n-2)$.

The total number of diodes of same rating required to maintain equal voltage distribution across them is given by $(n-1) \times (n-2)$ which is a substantial increase [21].

2.2.3. Flying Capacitor Multilevel Inverters

An n-level FC multilevel inverter requires $[(n-1)(n-2)]/2$ clamping capacitors in per phase leg and (n-1) number of dc-bus capacitors if capacitors having voltage rating same as the power electronic switch are to be selected. The flying capacitor topology was introduced in 1991 by Meynard [31] in his paper titled “Multilevel conversion: high voltage choppers and voltage-source inverters”, in which he has compared the proposed one with the conventional diode clamped three-level inverter based on the performance factors like output harmonic spectrum and dv/dt generated at commutation. Flying capacitor topology uses

Figure 2. 6: Flying capacitor multilevel inverter configuration (a) three-level scheme (b) five-level scheme.

capacitors to generate different voltage level instead of using clamping diodes. FC topology gives same voltage level for different switching combinations. These redundant switching states will automatically balance the DC-bus capacitors. The per-phase configuration of a

Table 2. 3: Switching States and Pole Voltages of three-level FC Inverter (X=A,B,C)

Level	S_{A1}	S_{A2}	Pole voltage, V_{X0}	Effect on flying capacitor voltage (C)
2	ON	ON	$E_{dc} / 2$	No effect
1	ON	OFF	0	Charging
1	OFF	ON	0	Discharging
0	OFF	OFF	$-E_{dc} / 2$	No effect

three- level FC inverter and five-level FC inverter are shown in Figure 2. 6 (a) and (b), respectively. Table 2. 3 shows the switching state and the corresponding pole voltage ' V_{X0} ' of the three-level FC inverter. The pairs shown in dotted lines in Figure 2. 6 (a) act as complementary switches and two different switching combinations generate same voltage level (level 1) as given in Table 2. 3. In the case of 5 level FC topology as shown in Figure 2. 6 (b) the switching state redundancies of voltage levels $E_{dc} / 2$, $E_{dc} / 4$, 0, $-E_{dc} / 4$, or $-E_{dc} / 2$ are 1, 3, 6, 3, 1, respectively [21]. In order to maintain balanced capacitor voltages, this topology requires higher switching frequency of operation (with or without the aid of

Figure 2. 7: (a) three-level Active NPC converter (leg ‘a’) (b) three phase 5-level HNPC and (c) MMC with series connected 2-level VSI.

controller). But for high power applications the switching frequency is limited in the range of 500-700 Hz, which makes FC multilevel inverter less suitable for Industry applications [21].

2.2.4. Recent Multilevel Inverter Topologies

The NPC, FC and CHB are the classic topologies which are commercially available from different manufacturers in the related application area. Apart from that, five-level H-bridge NPC (5L-HNPC) [32-34], three-level Active NPC (3L-ANPC) [35, 36], and Modular Multilevel Converter (MMC) [37-40] are some newly derived topologies which are on their way to commercial market (Figure 2. 7).

Two three-level NPC are connected as H-bridge to generate five-level output waveform in 5L-HNPC [41] converter. The problems of unequal loss distribution between the outer and inner switching devices in three-level NPC converter has been solved by introducing 3L-ANPC [42] topology where clamping diodes have been replaced by active switches in each leg. MMC, which was invented in 2001 [43], is popular in HVDC applications [38, 44] due to its property to attain high voltage levels maintaining good power quality at ac side. Each leg in MMC is formed by series connection of single phase half bridge converter as shown in Figure 2. 7(c).

The medium voltage drives supplied by ABB in the range of 250kW to 36MW uses three-level NPC and five-level ANPC converters for a wide range of applications across all industries [45, 46] . Toshiba Mitsubishi-Electric Industrial Systems Corporation (TMEIC) uses classical 3L-NPC, CHB and the hybrid topologies in MW power range for drive products (TMdrive) and utility scale solar inverters (Solar Ware) [47]. Alston produces 4-L FC multilevel inverter fed drives [48]. Yaskawa [49] manufactures medium voltage AC drives (2.4kV/4.16kV) in the range from 130kW to 12MW using enhanced CHB configuration which generates motor friendly 9/17 level output waveforms.

2.3. PWM Strategies for Multilevel Inverters

The main idea of the pulse width modulation is to produce the fundamental voltage of required amplitude and frequency as desired by the controller and to shift the harmonic components to higher frequency band. The era of multilevel inverter started when Nabae et al introduced the three-level NPC inverter for medium voltage applications in 1981 [26]. Thereafter, a number of modulation schemes have been proposed in [21, 50-52] for three-level operation. Since most of the applications are related to high power, the modulation scheme used in commercial converters are intended to give good power quality and reduced switching frequency [53]. The level-shifted PWM (LS-PWM), Phase shifted PWM (PS-

PWM) and selective harmonic elimination (SHE) techniques are the classic and commercially available modulation techniques employed in multilevel inverters [54, 55].

But the increased number of levels, voltage vector redundancies and zero common mode voltage vectors present in multilevel inverters have not completely been utilized by the carrier-based PWM schemes which eventually drives for other modulation strategies like Space vector modulation(SVM) [56]. The direct power control based SVM (DPC-SVM) can be used in real and reactive power control for better efficiency with robust operation. For three-level inverter operation, LS-PWM generates the gating signal in each phase by comparing its reference sine wave with two identical but level shifted triangular waves. In SVM the voltage space vector obtained from the three phase reference voltages is sampled and three nearest voltage vectors surrounding the reference vector are selected for switching [57].

The general requirements for a PWM scheme for inverters are as follows [58]

- Wider linear modulation range
- minimum number of pole voltage transitions to reduce the switching loss
- Lower harmonic content in the output voltage and current
- Elimination of low frequency (sub) harmonics to avoid torque pulsations in motors
- Reduction in the EMI
- Operation in the over-modulation extending up to square-wave mode
- Simplicity of implementation
- Reduction of common mode voltages and dc-link capacitor voltage balancing, in the case of multilevel inverters.

The classification of modulation techniques used for multilevel inverters are shown in Figure 2. 8.

Figure 2. 8: Classification of modulation techniques of multilevel inverters.

The most popular modulation methods, i.e., *sinusoidal pulse width modulation* (SPWM) and *space vector modulation* (SVPWM) schemes for multilevel inverters are presented in the following sub-sections.

2.3.1. Multilevel Sinusoidal Pulse Width Modulation

The sine triangle comparison used in two-level VSI is extended to generate PWM in multilevel converters. Carrara in [54] used $(n-1)$ carrier waves to compare with three phase reference waveforms. The level-shifted carrier waves have amplitude $\frac{E_{dc}}{(n-1)}$ and they divide

the vertical plane of reference signal into $(n-1)$ regions of operation to generate stepped voltage waveform. In the case of five-level inverter, PWM generation is shown in Figure 2.

9. If the reference vector ' v_{AN} ' lies in Sector 'C1' over one sampling period, the pole voltage

' V_{A0} ' will switch from $\frac{E_{dc}}{2}$ to $\frac{E_{dc}}{4}$. The pole voltage switching in each sector is illustrated in

Figure 2. 9 (b). This method is similar to the two-level SPWM [54].

Figure 2. 9: Carrier based PWM for five-level inverter (a) level-shifted triangular waves and three phase reference signals (b) Pole voltage waveform generation in phase- A.

Based on the carrier waves structure used, there are different carrier based PWM methods have been proposed [54]. They are

- Alternate Phase Opposition Disposition (APOD): each carrier wave is shifted by 180° from the adjacent carrier.

- Phase Opposition Disposition (POD): The carriers in positive half of reference signal are shifted by 180° from the carriers in the negative half.
- Phase Disposition (PD): All carriers are in phase as shown in Figure 2. 9 (a).

Steinke *et al* in [59] have added an offset voltage with the reference waveforms to increase the linear range of PWM method. The magnitude of offset voltage v_{offset} is given by

$$v_{offset} = (v_{max} - v_{min}) / 2 \quad (2.6)$$

where v_{max} and v_{min} are the maximum and minimum values among the instantaneous amplitude of the reference signals over one sampling period. But the multilevel carrier based techniques for PWM generation in NPC topology leads to unequal switch utilization.

2.3.2. Space Vector Modulation Technique

The SVPWM has been derived for achieving various goals like switching frequency reduction, DC-Link capacitor voltage balancing [60, 61], optimal switching transitions to reduce switching loss [52, 62] reduction in common mode voltage, and reduce THD. The multilevel SVPWM methods are initially proposed for three-level neutral-point clamped GTO inverters [52, 60, 61, 63]. The process of reference voltage generation in SVM has three sections; the first one is to select the three nearest vectors surrounding the reference vector and the next stage involves the calculation of duty ratios of the selected vectors over one sampling period. The final stage is to arrange the voltage vectors in an optimum sequence. When the number of levels increases, larger number of vectors will be there and the vectors become closer as in Figure 2.10 and the whole process become more complicated. Though SVPWM has advantages over the conventional carrier based PWM method, it is not the perfect choice for Industrial applications due to the extensive offline computations and look up table involved during implementation.

The traditional sector identification and look-up table method used for SVPWM schemes cannot be extended to higher level of multilevel configurations. Hence generalized

Figure 2. 10: Space vector locations for (a) two-level inverter (b) three-level inverter, and (c) five-level inverter.

SVPWM techniques for n -level converters are developed by various methods [51, 64, 65]. These include mapping the sector of outer sub hexagon to the inner sub hexagon, and calculating switching vector duration and sequence using two-level algorithm. In [66], the switching time functions are obtained from reference signal sampling. The algorithm presented in [59] involves the same number of computational steps for selecting voltage vectors and calculating their duty ratio for any level of converter operation. The advantages of techniques presented in [67] are the reduction in calculation efforts, reduction in the memory size of the controller and that the scheme can be extended to multilevel topologies easily. But based on the control regions (depending on the number of phases and the coordinates used) the SVM technique and algorithm are different which demands a new SVM technique which can be applied to multilevel converters with any number of levels and phases.

2.4. Operational Issues

In NPC inverter, depending on switching state the neutral point current can charge or discharge the capacitors, which will produce an unequal voltage distribution in capacitors. With higher voltage unbalance, the switching device gets damaged because of uneven voltage distribution and can also generate high output voltage harmonics. In the case of three-level NPC inverters, the unbalance operation may charge one capacitor to full dc voltage while switches are rated for half the dc-link voltage. This will not only damage the diodes and switches due to the voltage stress but also inject even-order harmonics which will affect the motor load in terms of increased machine loss and high torque pulsations [63]. These issues are discussed in [60] [63, 68] [69, 70] [50, 63, 71-75] where different control methods are suggested to overcome the NPP unbalance problem. The literature [66 – 67] studies the effect of NPP variation on load current, load power factor and dc-link capacitors in three-level NPC inverter. The effect of the zero sequence voltage on the neutral-point variation is established in [74] and the theoretical minimum capacitance of the capacitors required for neutral-point balancing is studied in [61]. The neutral-point balancing schemes, for the three-level neutral-point clamped inverter, are based on effective use of the redundant switching states of the inverter voltage vectors. The redundant switching states are used alternately such that the neutral-point voltage unbalance caused by the first switching state combination is compensated by another state, thus, bringing the total unbalance, in one switching cycle, to zero [70, 76] . The neutral-point voltage control scheme presented by Newton in [70] adds a dc offset voltage to the modulating signals before comparing with the carriers. Adding the dc offset in such manner does not change the effective voltage across the machine phases, but results in the change in the average current drawn from middle rail of the dc-link. The capacitor voltage imbalance can also be corrected by adding a dc offset and a third harmonic component to the modulating waves combined along with the switching circuit [70]. This additional hardware will increase the complexity of the power circuit as well as the system

cost, especially at high power levels. The cost function which uses capacitor voltages and average value of dc-link intermediate branch currents is introduced in the references [52, 77, 78] to achieve voltage balancing using SVM. The above method also requires the sector information where the reference space vector is located at each sampling period and involves lots of calculations which makes the system more complex. Khajehoddin *et al* in [79] used a current flow model to predict the capacitor voltages corresponding to each switching state and hence to minimize the voltage deviation based on the cost functions.

The self-balancing of capacitors in FC multilevel inverters requires high frequency operation which is not possible for high-power applications. Also all the capacitors are to be pre-charged to their nominal values by controlling the inverter switches by connecting and disconnecting the capacitors to the source. When applied to real power conversions, FC multilevel converters possess poor efficiency and switch utilization. The capacitors present in FC are bulky and more expensive than NPC topology which also limits the industrial application of FC topology to maximum of four levels. The phase-shifting transformer present in CHB is huge in size and costly than the one used in NPC. Also, the regenerative application of CHB requires more devices, making the NPC topology more suitable for regenerative application [29].

Chapter 3

Space Vector Based PWM Technique for Three-Level Neutral Point Clamped Inverter with DC-Link Voltage Balancing

3.1. Introduction

Multilevel inverters generate staircase-type output voltage waveform from several levels of dc-voltage sources. They can reach high voltages with reduced harmonic distortion and lower EMI emissions using devices of smaller voltage ratings which make them suitable in medium to high power applications. Three-level neutral-point-clamped PWM inverter (NPC- PWM inverter) was invented by Nabae et al. [26] in the late 1970s for high efficiency motor drive applications and generates output voltage with fewer harmonic compared to conventional two-level inverters. Therefore, three-level NPC-PWM inverters are preferred over two-level inverters for practical applications such as utility interface for renewable energy systems, marine propulsion, static var generator (SVG) ,back-to-back intertie system for the UPFC (unified power flow controller), and for wide-range variable-speed drive systems [29, 80-82]. Level shifted PWM (LS-PWM) and Space Vector Based PWM (SVPWM) are the most commonly used PWM techniques for multilevel inverters. SVPWM can be programmed to synthesize multiple voltage levels with reduced switching loss and harmonic losses and utilizes higher number of levels, redundant voltage vectors and zero common mode voltage vectors available in higher level NPC inverters.

This chapter presents an analysis of neutral point potential (NPP) unbalance issues and balancing techniques for three-level NPC inverter. The NPP control of three-level NPC inverter operating with two different PWM techniques are studied comprehensively. A time-

Figure 3. 1: Three-level Diode Clamped Inverter (DCI).

domain analysis is performed first to propose the relationship between switching functions and reference modulating signals in three-level NPC inverter. Thereafter, Fourier series representation of neutral point current is derived and NPP control schemes for LS-PWM are discussed. The method of using space vector concept to generate multilevel output voltage and elimination of NPP variation by selecting redundant switching states and adjusting duty ratio is also studied. The balancing methods using LS-PWM and SVPWM controls are compared by considering THD in inverter output voltage and current as a performance indicator. It can be verified from experimental results that the SVPWM gives reduced harmonic content in output and lower loss compared to LS-PWM.

3.2. Three-level Diode Clamped Inverter

The configuration of a three-level diode-clamped inverter (DCI) connected to a three phase load is shown in Figure 3. 1. In Figure 3. 1, the neutral point with respect to dc source

Table 3. 1: Switching States and Pole Voltages of Three-level Inverter (X=A,B,C)

Switching symbols	Voltage Level L_X	Switching states		Pole Voltage (V) V_{XO}
		S_{X1}	S_{X2}	
P	2	ON	ON	$E_{dc}/2$
O	1	OFF	ON	0
N	0	OFF	OFF	$-E_{dc}/2$

is indicated as ‘O’; diodes D_{A1} to D'_{C1} are used for clamping the terminal voltage to neutral point potential. The output voltage between the inverter terminal and neutral point can vary between $+\frac{E_{dc}}{2}$ and zero or $-\frac{E_{dc}}{2}$ and zero. Table 3. 1 shows the valid switching states and the corresponding inverter output voltages for three-level NPC. The PWM techniques used for generating three-level output voltage are presented below.

3.2.1. LS-PWM Technique

The SPWM technique used in two-level VSI can be extended to multilevel inverter structures for signal generation. LS-PWM for three-level inverter involves the comparison of three phase reference waveforms of fundamental frequency with two high frequency level-shifted triangular waves. The switching signal generation for phase-A are shown in Figure 3. 2 . The bottom switches present in each leg operate in complimentary manner with respect to

Figure 3. 2: Switching signal generation of three-level NPC using LS-PWM.

Figure 3. 3: Switching pattern of three-level DCI for phase-A.

upper switches. When S_{A2} and S'_{A1} are on, the inverter terminal voltage $V_{AO} = 0$ and the neutral point is connected to the phase-A of load causing a current flows through the neutral point and unbalanced voltage across the dc-link capacitors.

3.2.1.1. Neutral Point Control for Three-level DCI

To derive the control scheme for eliminating the voltage unbalance, the current through the top and bottom terminals of the dc-link and neutral point are derived as a function of switching signals and load currents from the PWM pattern shown in Figure 3. 3. The low frequency sinusoidal modulating signal magnitude remains constant in a sampling period T_s , and to do the analysis in positive and negative half cycles, it is assumed as a square wave as shown in Figure 3. 3. In Figure 3. 3, Let λ_{x1} , λ_{x2} , and λ_{x3} represent the logic signals when the respective switching combinations $(S_{x1}S_{x2})$, $(S_{x2}S'_{x1})$, $(S'_{x1}S'_{x2})$ in Figure 3. 1 are true.

Then, based on the PWM strategy (Figure 3. 3) for the switches in each leg, the logic signals

$\lambda_{X1}, \lambda_{X2}, \lambda_{X3}$ are represented as:

$$\begin{aligned}\lambda_{X1} &= S_{X1} \\ \lambda_{X2} &= \bar{S}_{X1} = S'_{X1} \text{ for } m_X(t) > 0 \text{ else } \lambda_{X2} = S_{X2} \\ \lambda_{X3} &= \bar{S}_{X2} = S'_{X2}\end{aligned}\quad (3. 1)$$

Then the currents drawn from the top, neutral point and bottom terminals (Figure 3. 1) of dc-link are expressed as

$$\begin{aligned}i_l &= \lambda_{A1}i_A + \lambda_{B1}i_B + \lambda_{C1}i_C \\ i_2 &= \lambda_{A2}i_A + \lambda_{B2}i_B + \lambda_{C2}i_C \\ i_3 &= \lambda_{A3}i_A + \lambda_{B3}i_B + \lambda_{C3}i_C\end{aligned}\quad (3. 2)$$

where

$$\begin{aligned}i_A &= I_m \cos(\omega t + \theta_0 - \delta) \\ i_B &= I_m \cos(\omega t + \theta_0 - \delta - 2\pi/3) \\ i_C &= I_m \cos(\omega t + \theta_0 - \delta + 2\pi/3)\end{aligned}\quad (3. 3)$$

I_m is the amplitude of the load current, θ_0 is the initial phase angle of voltage and δ is the power factor angle.

From Figure 3. 3, during the positive and negative half cycles of modulating signal, the reference signal $m_A(t)$ can cross the upper triangular carrier $tri_{up}(t)$ and lower triangular carrier $tri_{lower}(t)$, respectively, at different instants in a sampling period. The modulating signal can be expressed as:

$$m_{A^+}(t) = -\frac{2t}{T_s} + 1 \quad (3. 4)$$

$$m_{A^-}(t) = -\frac{2t}{T_s} \quad (3. 5)$$

where $0 \leq t \leq \frac{T_s}{2}$, $m_{A^+}(t)$ and $m_{A^-}(t)$ are the positive and negative sections of modulating signal, respectively.

To derive the neutral point current i_2 , the analysis is done in phase-A based on Figure 3. 3 and (3.2), and results are used to obtain expression for the other two phases. Let $D_{\lambda_{A2}}$ is the duty ratio for neutral point current flowing through phase-A, then the magnitude of modulating signal during the positive half cycle is obtained by substituting $t = D_{\lambda_{A2}} \left(\frac{T_s}{2} \right)$ in (3.4)

$$M_{A+} = -\frac{2D_{\lambda_{A2}} T_s}{2T_s} + 1 = 1 - D_{\lambda_{A2}} \quad (3.6)$$

When modulating signal is negative, the magnitude of modulating signal is obtained by substituting $t = (1 - D_{\lambda_{A2}}) \left(\frac{T_s}{2} \right)$ in (3.5).

$$M_{A-} = -\frac{2(1 - D_{\lambda_{A2}}) T_s}{2T_s} + 1 = D_{\lambda_{A2}} - 1 \quad (3.7)$$

Then the conduction pattern for neutral point current in phase-A can be written as

$$\begin{aligned} \lambda_{A2}(t) &= 1 - m_A(t) \text{ for +ve modulating signal} \\ \lambda_{A2}(t) &= 1 + m_A(t) \text{ for -ve modulating signal} \end{aligned} \quad (3.8)$$

Let $\text{sgn}[m_X(t)]$ represent the sign function, then applying the same analysis in other two phases

$$\lambda_{X2}(t) = 1 - m_X(t) \times \text{sgn}[m_X(t)] \text{ for } X = A, B, C. \quad (3.9)$$

Substituting (3.9) in (3.2), the neutral point current emerges in the following form:

$$\begin{aligned} i_2(t) &= \{[1 - m_A(t) \times \text{sgn}[m_A(t)]]i_A + [1 - m_B(t) \times \text{sgn}[m_B(t)]]i_B \\ &\quad + [1 - m_C(t) \times \text{sgn}[m_C(t)]]i_C \\ i_2(t) &= i_A + i_B + i_C - \{m_A(t) \times \text{sgn}[m_A(t)]\}i_A - \{m_B(t) \times \text{sgn}[m_B(t)]\}i_B \\ &\quad - \{m_C(t) \times \text{sgn}[m_C(t)]\}i_C \end{aligned} \quad (3.10)$$

The Fourier series expansion of functions $\text{sgn}[m_X(t)]$ for X=A, B and C are given by

$$\begin{aligned}
sgn[m_A(t)] &= \frac{4}{\pi} \sum_{n=1,3,5,\dots,\infty} \frac{1}{n} \sin\left(\frac{n\pi}{2}\right) \cos\left(n(\omega t + \theta_0)\right) \\
sgn[m_B(t)] &= \frac{4}{\pi} \sum_{n=1,3,5,\dots,\infty} \frac{1}{n} \sin\left(\frac{n\pi}{2}\right) \cos\left(n\left(\omega t + \theta_0 - \frac{2\pi}{3}\right)\right) \\
sgn[m_C(t)] &= \frac{4}{\pi} \sum_{n=1,3,5,\dots,\infty} \frac{1}{n} \sin\left(\frac{n\pi}{2}\right) \cos\left(n\left(\omega t + \theta_0 + \frac{2\pi}{3}\right)\right)
\end{aligned} \tag{3.11}$$

Assuming balanced voltage across the dc-link capacitors, and substituting (3. 11) in analysis to (3. 10), the neutral point current becomes

$$\begin{aligned}
i_2(t) = 0 - & \left\{ \frac{MI_m}{\pi} \sum_{n=1,3,5,\dots,\infty} \frac{1}{n} \sin \frac{n\pi}{2} \begin{pmatrix} 2 \cos \delta \cos(n(\omega t + \theta_0)) \\ + \cos((n+2)(\omega t + \theta_0) - \delta) \\ + \cos((n-2)(\omega t + \theta_0) + \delta) \end{pmatrix} \right\} \\
& - \left\{ \frac{MI_m}{\pi} \sum_{n=1,3,5,\dots,\infty} \frac{1}{n} \sin \frac{n\pi}{2} \begin{pmatrix} 2 \cos \delta \cos\left(n\left(\omega t + \theta_0 - \frac{2\pi}{3}\right)\right) \\ + \cos\left((n+2)\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) - \delta\right) \\ + \cos\left((n-2)\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) + \delta\right) \end{pmatrix} \right\} \\
& - \left\{ \frac{MI_m}{\pi} \sum_{n=1,3,5,\dots,\infty} \frac{1}{n} \sin \frac{n\pi}{2} \begin{pmatrix} 2 \cos \delta \cos\left(n\left(\omega t + \theta_0 + \frac{2\pi}{3}\right)\right) \\ + \cos\left((n+2)\left(\omega t + \theta_0 + \frac{2\pi}{3}\right) - \delta\right) \\ + \cos\left((n-2)\left(\omega t + \theta_0 + \frac{2\pi}{3}\right) + \delta\right) \end{pmatrix} \right\}
\end{aligned} \tag{3.12}$$

$$i_2(t) = - \frac{MI_m}{\pi} \sum_{n=1,3,5,\dots,\infty} \frac{1}{n} \sin \frac{n\pi}{2} \begin{pmatrix} 2 \cos \delta \cos(n(\omega t + \theta_0)) \left(1 + 2 \cos \frac{n2\pi}{3}\right) \\ + \cos((n+2)(\omega t + \theta_0) - \delta) \left(1 + 2 \cos \frac{(n+2)2\pi}{3}\right) \\ + \cos((n-2)(\omega t + \theta_0) + \delta) \left(1 + 2 \cos \frac{(n-2)2\pi}{3}\right) \end{pmatrix} \tag{3.13}$$

$$i_2(t) = \frac{-3MI_m}{\pi} \left\{ \sum_{n=3,9,15,\dots,\infty} \sin \frac{n\pi}{2} \left[\frac{2 \cos \delta \cos(n(\omega t + \theta_0))}{n} - \frac{\cos(n(\omega t + \theta_0) - \delta)}{n-2} - \frac{\cos(n(\omega t + \theta_0) + \delta)}{n+2} \right] \right\} \quad (3.14)$$

It can be observed from (3. 14) that, the NPC inverter will experience triplen harmonic current and zero dc-components at the neutral point. The neutral point current expression can be derived by considering the dominant harmonic current i.e., 3rd order harmonic components of (3. 14).

$$i_2(t) = 0.764MI_m \left(-0.67 \cos \delta \cos 3(\omega t + \theta_0) - \sin \delta \sin 3(\omega t + \theta_0) \right) \quad (3.15)$$

It can be seen that the neutral point current is a function of modulating signal amplitude M , amplitude of the load current I_m , initial phase angle of voltage θ_0 and the power factor angle δ . Under normal operating condition, the mean current drawn from the neutral point over one modulation cycle is zero and neutral point potential (NPP) is kept at the center potential of the dc link voltage.

When there is a variation in NPP due to transients, component imperfections and other imbalances, a non-zero mean neutral current flows into and away from the floating neutral point leading to capacitor voltage unbalances. The subsequent neutral point current expression contains an additional component which is a function of zero sequence voltage output [69]. Hence, the principle of neutral potential control is to control the zero sequence output voltage of NPC VSI such that current drawn from the neutral point becomes zero. The two common technique used for achieving NPP control in LS-PWM are described below.

3.2.1.1.1. Active Balancing by Adding Offset Voltage to Modulating Signals

The zero sequence voltage at the NPC three-level VSI output can be controlled to eliminate/reduce the NPP variation. Injecting a zero sequence voltage in to the three phase

Figure 3. 4: System model of three-level inverter with offset voltage addition for NPP control.

modulating waves generates same effective voltage at the load terminals, but changes the effective current path through the capacitors. The zero sequence voltage (v_{offset}) is selected in such a way that the neutral point current is forced to be zero [69]. The basic principle of active balancing is to measure the voltage difference between two dc-link capacitors and add the offset voltage required to eliminate the NPP variation to three phase modulating signal. Figure 3. 4 shows the NPP control scheme using offset voltage addition to the modulating reference signals.

The new modulating reference signals are obtained as

$$m_x^*(t) = \frac{V_{xo}(t)}{(E_{dc}/2)} - \left(\frac{V_{C1}(t) - V_{C2}(t)}{E_{dc}} \right) = m_x(t) - offset \quad (3.16)$$

Then the new modulating signals are compared with level shifted carrier waves to generate gating signals for three-level DCI.

3.2.1.1.2. Passive Balancing by using Star Connected RC Filter

With star connected RC filter circuit as shown in Figure 3. 5, the zero sequence component causing voltage unbalance can be diverted in to RC filter circuit. Also, to prevent an excessive high voltage across the switching devices, any dc component in zero sequence voltage should be eliminated [83, 84]. The RC filter phase voltages are given by

$$\begin{aligned} V_{Af}(t) &= V_{AO}(t) - V_{fo}(t) \\ V_{Bf}(t) &= V_{BO}(t) - V_{fo}(t) \\ V_{Cf}(t) &= V_{CO}(t) - V_{fo}(t) \end{aligned} \quad (3.17)$$

The zero sequence voltage (v_{fo}) between RC filter and inverter neutral point 'O' is expressed as:

$$V_{fo}(t) = \frac{V_{AO}(t) + V_{BO}(t) + V_{CO}(t)}{3} \quad (3.18)$$

Figure 3. 5: System model of three-level inverter with RC filter for NPP control.

Substituting (3. 18) in (3. 17)

$$\begin{aligned}
V_{Af} &= \frac{2V_{AO}(t) - V_{BO}(t) - V_{CO}(t)}{3} \\
V_{Bf} &= \frac{-V_{AO}(t) + 2V_{BO}(t) - V_{CO}(t)}{3} \\
V_{Cf} &= \frac{-V_{AO}(t) - V_{BO}(t) + 2V_{CO}(t)}{3}
\end{aligned} \tag{3. 19}$$

The output pole voltages given in (3. 19) are easily calculated from capacitor voltages and switching functions. Then replacing switching functions by modulating signals the pole voltages becomes

$$\begin{aligned}
V_{AO}(t) &\approx \frac{V_{C1}(t)}{2} [m_A(t) + 1] - \frac{V_{C2}(t)}{2} [1 - m_A(t)] \\
V_{BO}(t) &\approx \frac{V_{C1}(t)}{2} [m_B(t) + 1] - \frac{V_{C2}(t)}{2} [1 - m_B(t)] \\
V_{CO}(t) &\approx \frac{V_{C1}(t)}{2} [m_C(t) + 1] - \frac{V_{C2}(t)}{2} [1 - m_C(t)]
\end{aligned} \tag{3. 20}$$

Substituting (3. 20) in (3. 19) gives

$$\begin{aligned}
V_{Af}(t) &\approx \frac{1}{3} \left\{ \begin{aligned} &[V_{C1}(t) + V_{C2}(t)] \left[m_A(t) - \frac{1}{2} m_B(t) - \frac{1}{2} m_C(t) \right] \\ &+ [V_{C1}(t) - V_{C2}(t)] \left[1 - \frac{1}{2} - \frac{1}{2} \right] \end{aligned} \right\} \\
V_{Bf}(t) &\approx \frac{1}{3} \left\{ \begin{aligned} &[V_{C1}(t) + V_{C2}(t)] \left[-\frac{1}{2} m_A(t) + m_B(t) - \frac{1}{2} m_C(t) \right] \\ &+ [V_{C1}(t) - V_{C2}(t)] \left[1 - \frac{1}{2} - \frac{1}{2} \right] \end{aligned} \right\} \\
V_{Cf}(t) &\approx \frac{1}{3} \left\{ \begin{aligned} &[V_{C1}(t) + V_{C2}(t)] \left[-\frac{1}{2} m_A(t) - \frac{1}{2} m_C(t) + m_C(t) \right] \\ &+ [V_{C1}(t) - V_{C2}(t)] \left[1 - \frac{1}{2} - \frac{1}{2} \right] \end{aligned} \right\}
\end{aligned} \tag{3. 21}$$

The RC filter output voltages given in (3. 21) contain zero dc components which provide balanced capacitor voltages and removes the high frequency current components from the load side.

3.2.2. SVM with Self-Balancing Technique

The output phase voltages V_{An}, V_{Bn} , and V_{Cn} in Figure 3. 1 are given by

$$V_{Xn} = V_{XO} - V_{nO} \text{ for } X = A, B, C. \quad (3. 22)$$

And the equivalent space vector generated by the phase voltages is

$$V_s = \frac{2}{3} \left(V_{An} + V_{Bn} e^{j\frac{2\pi}{3}} + V_{Cn} e^{j\frac{4\pi}{3}} \right) = V_r e^{j\theta} \quad (3. 23)$$

Substituting (3. 18) in (3. 19),

$$V_s = \frac{2}{3} \left(V_{AO} + V_{BO} e^{j\frac{2\pi}{3}} + V_{CO} e^{j\frac{4\pi}{3}} \right) = V_r e^{j\theta} \quad (3. 24)$$

Pole voltages V_{AO}, V_{BO}, V_{CO} in (3. 20) can take three distinct levels based on the switching states as shown in Table 3. 1. The resulting 19 voltage space vectors and 27 inverter switching states can be arranged in three-dimensional representation as shown in Figure 3. 6.(a). The distribution of voltage vectors forms two hexagons that are divided in to six triangular sections of 60° each for analysis. In Figure 3. 6.(a), (A-F) are the sectors and each sectors are divided in to four sub-sectors S-1,S-2,S-3,S-4. The voltage vectors are distributed in to four groups: large vector (LV), medium vector (MV), small vector (SV) and zero vector (ZV) based on their magnitudes. And the magnitudes of voltage vectors are:

$$LV(V_1, V_2, V_3, V_4, V_5, V_6) = \frac{2}{3} E_{dc}; MV(V_{12}, V_{23}, V_{34}, V_{45}, V_{56}) = \frac{E_{dc}}{\sqrt{3}};$$

$$SV(V_{01}, V_{02}, V_{03}, V_{04}, V_{05}, V_{06}) = \frac{E_{dc}}{3} \text{ and } ZV(V_0) = \text{zero}.$$

Three phase reference voltage output at the inverter can be synthesized by generating the equivalent space vector by switching three voltage vectors where the tip of the vectors becomes the vertex of a triangle in which the reference space vector resides [85] . The reference voltage space vector is rotating with uniform speed and traces a circle. To generate V_s , the rotating reference voltage space vector V_s is sampled at low sampling period(T_s) such that the average voltage variation is sinusoidal. During a sampling period we assume that V_s is stationary. Then the sampled V_s can be generated by switching the

Figure 3. 6: (a) Space vector locations for three-level DCI (b) Voltage space vector lying in sector-A.

nearest three voltage vectors (For example, in Figure 3. 6.(b): the reference space vector V_s lying in sub-sector $S-4$ is synthesized by selecting V_2, V_{02} and V_{12}) so that the volt-second component of V_s along the orthogonal axis $\alpha\beta$ and volt-second component of three nearest vectors along $\alpha\beta$ axis are equal. The switching duration of each selected vector is obtained by time-averaging of V_s over one sampling time T_s . Let V_i, V_j and V_k represent the left side vector, right side vector and middle vector in each sub-sectors and t_i, t_j and t_k be their respective time period in one sampling instant. Then,

The volt-second balance equation is given as

$$\begin{aligned} T_s \cdot V_s &= (t_i \cdot V_i + t_j \cdot V_j + t_k \cdot V_k) = V_r e^{j\theta} \\ V_s &= (d_i \cdot V_i + d_j \cdot V_j + d_k \cdot V_k) = V_r e^{j\theta} \end{aligned} \quad (3. 25)$$

where d_i, d_j and d_k are the duty ratios of V_i, V_j and V_k , respectively.

For example, in Figure 3. 6.(b) the location of V_s during one sampling instant is shown and switching duration of selected vectors V_2, V_{02} and V_{12} are calculated as follows

$$V_s = (d_i \cdot V_{02} + d_j \cdot V_{12} + d_k \cdot V_2) \quad (3. 26)$$

Substituting the values of voltage vectors and separating the real and imaginary parts,

$$V_s = \left(d_i \cdot \frac{E_{dc}}{3} e^{j60} + d_j \cdot \frac{E_{dc}}{\sqrt{3}} e^{j30} + d_k \cdot \frac{2E_{dc}}{3} e^{j60} \right) = V_r e^{j\theta} \quad (3. 27)$$

$$V_r \cos \theta = \frac{E_{dc}}{3} \left(\frac{d_i}{2} + \frac{3}{2} d_j + d_k \right) \text{ and } V_r \sin \theta = \frac{E_{dc}}{2\sqrt{3}} (1 + d_k)$$

Also, from Figure 3. 6.(b),

$$V_x = V_r \left(\cos \theta - \frac{1}{\sqrt{3}} \sin \theta \right) \quad (3. 28)$$

$$V_y = V_r \frac{2}{\sqrt{3}} \sin \theta$$

Let

$$d_x = \frac{V_x}{\frac{2}{3} E_{dc}} \text{ and } d_y = \frac{V_y}{\frac{2}{3} E_{dc}} \quad (3. 29)$$

From (3. 27) and (3. 29)

$$d_i = (1 - d_j - d_k); d_j = 2d_x \text{ and } d_k = 2d_y - 1. \quad (3. 30)$$

The switching vectors and their respective duty ratios are obtained in the same manner as described above for synthesizing the reference space vector lying in any of the sub-sectors in sector-A. The calculated duty ratios of voltage vectors are given in Table 3. 2.

Table 3. 2: Relative on- times of voltage vectors in Sector-A

Duty ratio	Sub-sector			
	S-1	S-2	S-3	S-4
d_i	$1 - d_j - d_k$			
d_j	$2d_x$	$2d_x - 1$	$2d_x + 2d_y - 1$	0
d_k	$2d_y$	$2d_y$	$1 - 2d_y$	$2d_y - 1$

The subsector identification is related to d_x and d_y as follows:

$$\begin{aligned}
& \text{if } (d_x + d_y) \leq 0.5 \text{ then } S - 1 \\
& \text{if } d_x > 0.5 \text{ then } S - 2 \\
& \text{if } d_y > 0.5 \text{ then } S - 4 \\
& \text{else } S - 3.
\end{aligned} \tag{3. 31}$$

The reference vector V_s residing in any of the sectors can be synthesized by switching the nearest three vectors over one sampling period where the duty ratios of the respective vectors are obtained by virtually transferring V_s to sector-A and applying Table 3.

2 . While transferring V_s lying in any other sectors to sector-A to calculate the duty ratios, the angle θ should vary between 0° to 60° .

3.2.2.1. Neutral Point Potential Balancing using SV Switching Scheme.

The effect of switching states on dc-link capacitor voltages are evaluated and summarized in Table 3. 3. The equivalent circuit representations of three-level DCI while switching various vector groups are shown in Figure 3. 7. It can be seen from Figure 3. 7.(b) that, when SV with switching state 211 is selected, the load is connected between positive dc-link terminal and neutral point which will discharge top capacitor and charge the bottom other. And when SV with switching state 100 (Figure 3. 7.(c)) is selected for switching, the load is

Table 3. 3: Effect of switching states on dc-link capacitors

Vector Group		Voltage Vector	Switching States	Capacitor C_1	Capacitor C_2
ZV		V_0	222,111,000	No effect	
SV	+veSV (PSV)	$V_{01}^+, V_{02}^+, V_{03}^+, V_{04}^+, V_{05}^+, V_{06}^+$	211,221,121,122,112,212	discharging	charging
	--ve SV (NSV)	$V_{01}^-, V_{02}^-, V_{03}^-, V_{04}^-, V_{05}^-, V_{06}^-$	100,110,010,011,001,101	charging	discharging
MV		$V_{12}, V_{23}, V_{34}, V_{45}, V_{56}$	210,120,021,012,102,201	Less charging or discharging(depends on load current)	
LV		$V_1, V_2, V_3, V_4, V_5, V_6$	200,220,020,022,002,202	No effect	

distributed between neutral point and negative dc-link terminal and the neutral point current i_2 flows in the opposite direction when compared to switching state 211. Both states generates same voltage vector however their effect on dc-link capacitors are opposite. This redundant property of SVs can be used for NPP control [86]. And the SV are classified in to +ve SV

Figure 3. 7: Current model of three-level DCI showing the effect of switching vectors on dc-link capacitors. (a) LV [$V_l:200$] (b) PSV [$V^+_{oi}:211$] (c) NSV [$V^-_{oi}:100$] (d) ZV [$V_0:222$] (e) MV [$V_{l2}:210$].

(PSV) and -ve SV (NSV) based on the direction of NP current generated during switching. It is seen from Figure 3. 7 that the SV and MV affect the neutral point current and other two vector groups do not control neutral point current. Hence to control the NPP, the voltage difference

Table 3. 4: Switching sequence in Sectors-A and B

<i>Sector</i>	<i>Sub-sector</i>		<i>Switching Sequence</i>
<i>A</i>	<i>S-1</i>	$\theta < \frac{\pi}{6}$	$V_{01}^- V_{02}^- V_0 V_{01}^+ V_0 V_{02}^- V_{01}^-$
		$\theta > \frac{\pi}{6}$	$V_{02}^- V_0 V_{01}^+ V_{02}^+ V_{01}^+ V_0 V_{02}^-$
	<i>S-2</i>		$V_{01}^- V_1 V_{12} V_{01}^+ V_{12} V_1 V_{01}^-$
	<i>S-3</i>	$\theta < \frac{\pi}{6}$	$V_{01}^- V_{02}^- V_{12} V_{01}^+ V_{12} V_{02}^- V_{01}^-$
		$\theta > \frac{\pi}{6}$	$V_{02}^- V_{12} V_{01}^+ V_{02}^+ V_{01}^+ V_{12} V_{02}^-$
	<i>S-4</i>		$V_{02}^- V_{12} V_2 V_{02}^+ V_2 V_{12} V_{02}^-$
<i>B</i>	<i>S-1</i>	$\theta < \frac{\pi}{6}$	$V_{02}^- V_0 V_{03}^+ V_{02}^+ V_{03}^+ V_0 V_{02}^-$
		$\theta > \frac{\pi}{6}$	$V_{03}^- V_{02}^- V_0 V_{03}^+ V_0 V_{02}^- V_{03}^-$
	<i>S-2</i>		$V_{02}^- V_{23} V_2 V_{02}^+ V_2 V_{23} V_{02}^-$
	<i>S-3</i>	$\theta < \frac{\pi}{6}$	$V_{02}^- V_{23} V_{03}^+ V_{02}^+ V_{03}^+ V_{23} V_{02}^-$
		$\theta > \frac{\pi}{6}$	$V_{03}^- V_{02}^- V_{23} V_{03}^+ V_{23} V_{02}^- V_{03}^-$
	<i>S-4</i>		$V_{03}^- V_3 V_{23} V_{03}^+ V_{23} V_3 V_{03}^-$

between the top and bottom capacitor is obtained and the duty ratio calculated for ZV is distributed among PSV and NSV over one sampling period to minimize the voltage error. The selection of redundant vectors and switching sequence in each sub-sectors of sectors-A and B over one sampling interval are shown in Table 3. 4. In other sectors the sequence is replaced with equivalent switching vectors.

Let d_{SV} be the relative on-time of the SV over one sampling interval T_s . Then, to control the neutral point potential to half of the dc-link voltage, d_{SV} is distributed among PSV and NSV as follows through a weighting coefficient k .

$$\begin{aligned} d_{PSV} &= \frac{1+k}{2} d_{SV} \\ d_{NSV} &= \frac{1-k}{2} d_{SV} \end{aligned} \quad (3.32)$$

where $-1 < k < 1$; d_{PSV} and d_{NSV} are the duty ratios for PSV and NSV respectively.

3.3. Comparative Evaluation of LS-PWM and SVM based Voltage Balancing Techniques for three-level DCI

The two different PWM techniques-namely, LS-PWM with star connected RC filter and SVM utilizing redundant voltage vector property for achieving neutral point potential control for three-level DCI are evaluated and compared in this section. The operation of three-level DCI shown in Figure 3. 1 connected to a three-phase RL load is investigated using Matlab/Simulink® and PSIM environments initially and verified using experimental results.

3.3.1. Simulation Studies

The main circuit parameters are the following:

- dc-link Voltage (E_{dc}) : 300V
- dc-link capacitors (C_1, C_2): $1000\mu F$ with $\pm 20\%$ tolerance and $ESR=100m\Omega$.
- Sampling frequency (f_s), carrier frequency ($f_{tri_{up}}, f_{tri_{lower}}$) : 2.5 kHz.

The variation in the capacitor voltages, V_{C1} and V_{C2} are shown in Figure 3. 8. It can be seen that initially the capacitors are unbalanced and after that capacitor voltages are regulated to 150V. Both control methods effectively maintain balanced voltages across the capacitors; however, SVM-based active balancing control regulates the capacitor voltages more rapidly than LS-PWM with RC filter. Figure 3. 9 shows the pole voltage of the three-level DCI which has three distinct levels +150, 0 and -150. The line-to-line voltage V_{AB} is shown in Figure 3. 10. The pole voltage and line-to-line voltage of three-level DCI using SVM based active balancing technique are shown in Figure 3. 11 and Figure 3. 12, respectively.

Figure 3. 13 (a) and (b) show the normalized FFT of pole voltage and line voltage of three-level DCI respectively for LS-PWM with RC filter balancing technique. The harmonic spectrum obtained while using SVM based active balancing technique for three-level DCI is shown in Figure 3. 14. From the FFT comparison made between two control techniques

Figure 3. 8: DC-Link capacitor voltages V_{C1} and V_{C2} of three-level DCI (a) LS-PWM with RC filter balancing (b) SVM with active balancing technique.

Figure 3. 9: Output voltage of three-level DCI measured between inverter terminal 'A' and neutral point 'O' using LS-PWM with RC filter balancing technique.

(Figure 3. 13 and Figure 3. 14), it is observed that the SVM based active balancing control gives a larger fundamental component and significant improvement in THD of output voltage

Figure 3. 10: Line voltage output of three-level DCI for LS-PWM with RC balancing technique.

Figure 3. 11: Output voltage of three-level DCI measured between inverter terminal 'A' and neutral point 'O' using SVM with active balancing technique.

Figure 3. 12: Line voltage output of three-level DCI for LS-PWM using SVM with active balancing technique.

for the three-level DCI. Even though THD is improved in SVM with active balancing

Figure 3. 13: FFT of Output voltage of three-level DCI for LS-PWM with RC filter balancing technique. (a) Pole voltage, V_{AO} (b) Line voltage, V_{AB}

Figure 3. 14: FFT of Output voltage of three-level DCI for SVM with active balancing technique. (a) Pole voltage, V_{AO} (b) Line voltage, V_{AB} .

technique, a rather large 3rd harmonic appears in pole voltage waveforms; this is a disadvantage, as wanted and unwanted components get close to each other, making filtering difficult.

It is desirable to investigate the dynamic performance of the neutral point potential control of three-level DCI using SVM based voltage balancing technique. The next section will focus on the performance of SVM based active balancing of three-level DCI while driving a motor.

3.3.1.1. Dynamic Performance

Figure 3. 15 shows the schematic of three-level DCI driving a Permanent magnet synchronous motor (PMSM) incorporating SVM based capacitor balancing control and field

Figure 3. 15: Schematic of three-level DCI PMSM drive.

oriented control (FOC). The FOC block generates the sinusoidal reference voltage required at the motor terminals based on the speed demand and space vector modulator provides the corresponding gating signals for three-level DCI as well as maintaining a constant voltage of magnitude $E_{dc}/2$ across the individual dc-link capacitors during transient and steady state

operating conditions. The three-level DCI will convert the DC voltage to a stepped output voltage waveforms with a fundamental component equivalent to the sinusoidal reference voltage which will drive the PMSM at the given reference speed.

The mathematical model of PMSM can be derived from the wound rotor synchronous motor model. Since the position of rotor magnets determines the instantaneous induced emfs, stator currents and torque, the rotor reference frame is chosen to develop the state space model of PMSM [87].

The state space modeling of PMSM motor is given by

$$\begin{aligned}
 p i_{ds}^r &= \frac{(V_{ds}^r - R i_{ds}^r + \omega_r L_q i_{qs}^r)}{L_d} \\
 p i_{qs}^r &= \frac{(V_{qs}^r - R i_{qs}^r - \omega_r L_d i_{ds}^r - \omega_r \lambda_{af})}{L_q} \\
 p \omega_r &= \frac{\left(\left(\frac{P}{2}\right)(T_e - T_l) - B \omega_r\right)}{J} \\
 p \theta_r &= \omega_r
 \end{aligned} \tag{3.33}$$

where i_{ds}^r, i_{qs}^r and V_{ds}^r, V_{qs}^r are the direct and quadrature axis component of stator currents and voltages respectively; L_d and L_q are the stator inductances; λ_{af} is the flux linkage due to rotor magnets linking the stator; R is stator resistance; ω_r is rotor speed in rad/s; P is the number of poles; T_e represents the electromagnetic torque developed by the motor and T_l is the load torque.

If $i_{ds}^r = 0$ then $T_e = k_t i_{qs}^r$, where k_t is the motor torque constant. Hence, the torque can be controlled by controlling the quadrature component of stator current i_{qs}^r . Also, a negative value of i_{ds}^r will weaken the air-gap flux.

The control scheme for the speed FOC of PMSM drive is shown in Figure 3. 15. The rotor speed ω_r is compared with the reference speed ω_r^* and the error is given to a PI controller to generate the reference current i_{qs}^{r*} to drive the motor at desired speed. To get an

Table 3. 5: Circuit and controller parameters of three-level DCI drive

<i>Three-level DCI</i>	
DC-Link voltage, E_{dc}	400V
DC-Link capacitor, C_j , $j=1,2$.	1000 μ F $\pm$ 20% tolerance and ESR=100m Ω
Sampling Frequency, f_s	2.5kHz
<i>PI controllers</i>	
Rotor speed controller	Gain=0.05; time constant=0.1s
dq-axis current loop controller	Gain=10; time constant=0.0005s

optimum torque, the flux reference is set to zero by forcing $i_{ds}^* = 0$. The output of the current controllers gives the reference stator voltages V_{ds}^{r*} and V_{qs}^{r*} in dq model using (3. 33). Then, the reference stator voltages are transformed to stationary reference frame $\alpha\beta$ and the equivalent space vector is given to the SV modulator to generate gating signals for three-level DCI. The SV modulator block also requires the individual dc-link capacitor voltages and dc-link voltage to implement the redundant voltage vector based NPP control to ensure three-level output voltage at the inverter terminal through all operating conditions.

3.3.1.1.1. Performance of three-level DCI Drive

The steady-state and transient operation of the system shown in Figure 3. 15 is evaluated using Matlab/Simulink® and PSIM. The circuit and controller parameters considered for simulation are given in Table 3. 5:. A PMSM motor with parameters $R=4.3\Omega$, $L_d=23\text{mH}$, $L_q=67\text{mH}$, $J=1.7\text{mkgm}^2$, $B=0.179\text{Nm/rad}$, $P=4$ and $\lambda_{af}=0.2719\text{V/rad/s}$ has been selected for simulation. Initially, a load of 3Nm is applied to the motor and a speed of 170rad/s is selected as reference speed. At $t=1\text{s}$, load at the motor is increased to 5Nm. The dc-link capacitor voltages are shown in Figure 3.16. The SVM based voltage balancing control maintains the voltage across each capacitor to an average value of 200V. The increased ripple in capacitor voltages after 1s is due to the increase in load current. The pole voltage and line voltage of three-level DCI are shown in Figure 3.17.(a) and (b),

Figure 3.16: DC-Link capacitor voltages V_{C1} and V_{C2} of three-level DCI PMSM drive with SVM based voltage balancing technique.

Figure 3.17: Output voltage of three-level DCI PMSM drive with SVM based voltage balancing technique. (a) Pole voltage in phase-A, V_{AO} (b) Line voltage, V_{AB} .

Figure 3.18: Motor line currents i_A , i_B and i_C of three-level DCI PMSM drive with SVM based voltage balancing technique.

Figure 3.19: Three-level DCI PMSM drive waveforms with SVM based balancing technique. (a) Load torque T_l and developed torque T_e of motor. (b) Reference speed ω_r^* and rotor speed ω_r .

Figure 3. 20: Photograph of the three phase prototype model of three-level DCI.

respectively. The pole voltage has three distinct levels 200V, 0V and -200V. Line voltage has five distinct levels +400V, 200V, 0V, -200V and -400V. When the applied torque has increased to $T_l = 5\text{Nm}$ at 1s, the speed controller and current controllers operate in such a way that the motor tracks the reference speeds $\omega_r^* = 170\text{rad/s}$ and develops a torque equal to applied load torque plus mechanical losses. Motor line currents are shown in Figure 3.18.

Figure 3.19 shows the simulation results of rotor speed ω_r and electromagnetic torque T_e developed by the PMSM. The torque spikes are caused by the corresponding spikes in the quadrature component of stator current which can be improved by tuning the PI controller.

3.4. Experimental Results

The operation of voltage balancing control for three-level DCI based on LS-PWM and SVM techniques described in the above sections are verified experimentally by implementing dSPACE-DS1103 PPC controller for three-level DCI prototype (Figure 3. 20).

The main circuit parameters are the following:

- dc-link Voltage (E_{dc}) : 300V
- dc-link capacitors (C_1, C_2) : $1000\mu F$ with $\pm 20\%$ tolerance and $ESR=100m\Omega$.
- Sampling frequency (f_s), carrier frequency ($f_{tri_{up}}, f_{tri_{lower}}$) : 2.5 kHz.
- 3 ϕ load of $R_{/phase}=150\Omega$ and $L_{/phase}=122mH$.

Figure 3.21 shows the capacitor voltages when the balancing control is turned off. The capacitor voltages give a difference of 20V between them. Figure 3. 22 and Figure 3. 23 show the steady-state voltage across the capacitors when LS-PWM and SVM based NPP controls are implemented, respectively. It is seen that the two capacitors are able to maintain

Figure 3. 21: DC-Link capacitor voltages V_{C1} and V_{C2} of three-level DCI when NPP controller is turned off.

Figure 3. 22: DC-Link capacitor voltages V_{C1} and V_{C2} of three-level DCI for LS-PWM with RC filter balancing technique.

Figure 3. 23: DC-Link capacitor voltages V_{C2} and V_{C2} of three-level DCI for SVM with active balancing technique.

Figure 3. 24: Output voltage of three-level DCI measured between inverter terminal ‘A’ and neutral point ‘O’ using LS-PWM with RC filter balancing technique ($m=0.8$).

close to perfectly balanced voltage of magnitude 150V across them, ensuring three-level operation of the DCI. The pole voltage, V_{AO} , and the line voltage, V_{AB} , of the three-level DCI for LS-PWM with RC filter balancing technique for $m=0.8$ are also measured and shown in Figure 3. 24 and Figure 3. 25, respectively. The pole voltage of the three-level DCI has three

Figure 3. 25: Line voltage output of three-level DCI for LS-PWM with RC balancing technique ($m=0.8$).

Figure 3. 26: FFT of Output voltage of three-level DCI for LS-PWM with RC filter balancing technique ($m=0.8$). (a) Pole voltage, V_{AO} (b) Line voltage, V_{AB} .

Figure 3. 27: Experimental results of three-level DCI for LS-PWM with RC filter balancing technique ($m=0.8$). (a) Line current, i_A (b) FFT of line current.

Figure 3. 28: Output voltage of three-level DCI measured between inverter terminal ‘A’ and neutral point ‘O’ using SVM based active balancing technique ($m=0.8$).

Figure 3. 29: Line voltage output of three-level DCI for SVM based active balancing technique ($m=0.8$).

distinct levels +150, 0, and - 150; and line voltage has five distinct levels +300, +150, 0, -150 and -300. Figure 3. 26. (a) and (b) show the normalized FFT of pole voltage and line voltage of three-level DCI, respectively, for LS-PWM with RC filter balancing technique. The inverter current output in phase-A and its harmonic spectrum are shown in Figure 3. 27.(a)

(a)

(b)

Figure 3. 30: FFT of Output voltage of three-level DCI for SVM with active balancing technique. (a) Pole voltage, V_{AO} (b) Line voltage, V_{AB} .

(a)

(b)

Figure 3. 31: Experimental results of three-level DCI for SVM with active balancing technique ($m=0.8$). (a) Line current, i_A (b) FFT of line current.

and (b), respectively. The pole voltage, V_{AO} and the line voltage, V_{AB} of the three-level DCI operating at modulation index, $m=0.8$ for SVM based active balancing control are shown in Figure 3. 28 and Figure 3. 29, respectively. The pole voltage has three distinct levels and line voltage waveform contains five levels. And their respective normalized FFTs are shown in Figure 3. 30.(a) and (b). The inverter current output in phase-A and its harmonic spectrum are depicted in Figure 3. 31. (a) and (b), respectively. The THD of pole voltage, line voltage and line current obtained for three-level DCI with LS-PWM control are 39%, 26% and 3% respectively, whereas respective THDs obtained with SVM based control are 24%, 8% and

1%. Hence there is a significant improvement in THD when SVM based control is implemented. The ratio of output fundamental voltage to the dc-link voltage i.e., The DC bus utilization of SVM is better than LS-PWM. From the FFT of output voltage waveforms shown in Figure 3. 26 and Figure 3. 30, it can be noted that, the SVM gives higher fundamental voltage as compared to LS-PWM. Also, the maximum value of peak pole voltage generated when LS-PWM used is $0.5 E_{dc}$ whereas the SVM gives $0.577 E_{dc}$. i.e., SVM enhances the DC bus utilization by 15.47%.

3.5. Conclusion

In this chapter, the NPP variation and control techniques of the classical three-level NPC inverter were analyzed on the basis of current flowing into and out of neutral point. The Fourier series representation of neutral point current was derived and the influence of zero sequence output voltage on potential variation was also discussed. It is shown that, an RC filter connected at the inverter terminals eliminates the NPP variation when LS-PWM is used. The SV modulation based switching scheme presented in this chapter eliminates the need of RC filter and gives balanced neutral point potential by selecting redundant switching states and adjusting its duty ratio. It was observed that SVM gives low harmonic distortions and reduced losses than LS-PWM due to the complete utilization of increased number of levels, voltage vector redundancies and optimum switching sequence generation. Simulation and experimental results were shown to validate the theoretical analysis.

Chapter 4

Voltage Balancing Scheme for Five-level Neutral Point Clamped Inverter based on Space Vector Modulation Technique

4.1. Introduction

Neutral point clamped five-level inverter schemes discussed in literature are associated with inherent capacitor voltage balancing issues. The unequal voltage distribution across the capacitors will damage the semiconductor devices as well as generate harmonics at inverter output. To eliminate this voltage unbalancing phenomenon, some auxiliary hardware and/or modification in control techniques are usually implemented [70, 77, 88, 89] . The hardware modifications will increase the power circuit complexity and cost especially at high power levels. The classical modulation schemes cannot utilize the more number of levels, redundant voltage vectors and zero common mode voltage vectors available in five-level DCI for achieving switching frequency reduction, common mode voltage elimination, capacitor voltage balance and reduction in THD, etc. Hence new modulation techniques like SVM are developed for utilizing the above mentioned properties of multilevel converters [64, 66, 90]. The clamping diodes in five-level DCI share unequal voltages for a given switching state and to distribute voltage stress equally among the diodes, 12 clamping diodes of equal voltage ratings $\left(\frac{E_{dc}}{4} \right)$ are required per leg. Converter topology which minimizes the series connected devices and shares the total voltage equally among the devices during a valid switching state is required for achieving improved efficiency.

Figure 4. 1: Schematic of five-level diode clamped inverter (DCI) with three phase load.

The objective of this chapter is to propose an SVM-based voltage balancing strategy for a new five-level reduced device DCI topology which uses lower number of clamping diodes compared to classical five-level DCI. A simple switching function model of the new topology is derived which predicts the dc-link capacitor currents by sensing load currents for given switching state. This will significantly reduce the computational efforts while implementing voltage balancing strategy compared to the sector based method presented in [78]. Here, the redundant voltage vectors present in five-level inverter are utilized to provide a balanced voltage across the four dc-link capacitors and the need for balancing circuit is eliminated.

4.2. Conventional Voltage Balancing Technique in Five-level Diode Clamped Inverter

The configuration of a five-level diode-clamped inverter (DCI) connected to a three phase load is shown in Figure 4. 1. The switching states of five-level DCI and output voltage at the inverter terminal with respect to mid-point terminal 'O' are given in Table 4. 1. The

Table 4. 1: Switching States and Pole Voltages of five-level DCI (X=A,B,C)

Voltage Level L_X	Switching states				Pole Voltage (V) V_{XO}
	S_{X1}	S_{X2}	S_{X3}	S_{X4}	
4	ON	ON	ON	ON	$E_{dc}/2$
3	OFF	ON	ON	ON	$E_{dc}/4$
2	OFF	OFF	ON	ON	0
1	OFF	OFF	OFF	ON	$-E_{dc}/4$
0	OFF	OFF	OFF	OFF	$-E_{dc}/2$

clamping diodes share unequal voltages during each switching states. For instance, when leg-

A switches are operated to generate a pole voltage of $\frac{E_{dc}}{2}$ (level-4), the reversed biased

voltages across clamping diodes D_{A1} , D_{A2} and D_{A3} are $\frac{E_{dc}}{4}$, $\frac{E_{dc}}{2}$ and $\frac{3E_{dc}}{4}$, respectively. If

clamping diodes of voltage ratings $\frac{E_{dc}}{4}$ are used, then the total number of clamping diodes

required/leg is 12 as shown in Figure 4. 2. The current flowing through the clamping diodes

generates dc current in the capacitors and creates an unbalanced voltage across the dc-link

Figure 4. 2: Per-phase schematic of five-level diode clamped inverter (DCI) with diodes of equal voltage ratings.

capacitors. It is proved theoretically in [91] that the LS-PWM technique is not able to balance the capacitors and capacitors C_1, C_4 are charged and C_2, C_3 are discharged continuously. Also the average value of capacitor currents $(-\bar{i}_{C1} = \bar{i}_{C2} = \bar{i}_{C3} = -\bar{i}_{C4} = \bar{i}_C)$ presented in [78] for five-level DCI operating at modulation index $m > 0.5$, are

$$\bar{i}_C = \frac{3}{4\pi} I_m \cos(\delta) \times \left(-m\pi + 4m \sin\left(\frac{1}{2m}\right) + \sqrt{\frac{4m^2 - 1}{m^2}} \right)$$

functions of modulation index (m) and power factor ($\cos(\delta)$). When $\cos(\delta) \neq 0$ there is change in capacitor voltages and output voltage gets three-level waveform leads to unbalanced power losses of IGBT modules. Hence, when operating conditions involve large modulation indices and active load currents, five-level DCI requires an extra balancing circuit to maintain a balanced voltage across the capacitors.

4.2.1. Voltage Balancing Control and Circuit

An auxiliary converter together with voltage balancing control can be used to maintain a balanced voltage across four dc-link capacitors in all operating conditions [89]. The voltage

Figure 4. 3: Circuit schematic of five-level diode clamped inverter (DCI) with balancing circuit.

Figure 4. 4: Control block schematic of positive chopper.

balancing circuit connected to the five-level DCI is shown in Figure 4. 3. Two independently operated choppers (positive and negative) in the balancing circuit provide controlled voltages across dc-link capacitors. The positive and negative choppers control the voltage across capacitors C_1, C_2 and C_3, C_4 , respectively. The control block for positive chopper is shown in Figure 4. 4. The current through inductor L_1 is indicated as ' i_{L1} '. A similar control is done for negative chopper to reduce the error between C_3 and C_4 voltages. In addition to that, an offset voltage is added to the modulation signal to implement neutral point potential balancing. The voltage error between the positive and negative dc-bus terminals with respect to mid-point 'O' is given to a PI controller and the corresponding offset voltage is given by

$$offset = K_p [(V_{C1} + V_{C2}) - (V_{C3} + V_{C4})] + K_i \int [(V_{C1} + V_{C2}) - (V_{C3} + V_{C4})] \quad (4.1)$$

The modified modulating signals are obtained as follow:

$$m_x^*(t) = m_x(t) + offset \quad \text{for } X = A, B \text{ and } C. \quad (4.2)$$

4.2.2. Simulation Results

The capacitor balancing of five-level DCI by means of balancing circuit and LS-PWM technique is verified through simulation done in Matlab/Simulink® and PSIM environment. The three-phase PMSM is connected as a load to check the dynamic performance of voltage balancing circuit and Figure 4. 5 shows the control block schematic.

The balancing circuit parameters are the following:

Figure 4. 6: DC-Link capacitor voltages V_{C1} , V_{C2} , V_{C3} and V_{C4} of five-level DCI drive for LS-PWM with voltage balancing circuit.

- Carrier frequency (f_{tri}) : 2.5 kHz.

A PMSM with parameters $R=4.3\Omega$, $L_d=23\text{mH}$, $L_q=67\text{mH}$, $J=1.7\text{mkgm}^2$, $B=0.179\text{Nm/rad}$, $P=4$; and $\lambda_{af}=0.2719\text{V/rad/s}$ has been selected for simulation. A load of 5Nm is applied at the motor and a speed of 200rad/s is selected as reference speed. A detailed modeling of PMSM and FOC was presented in the previous chapter. PI controller with proportional and integral gains of values 1 and 12, respectively, are used for mid-point potential balancing control. The FOC block generates the sinusoidal reference voltage required at the motor terminals based on the speed demand and is added with an offset voltage from mid-point potential balancing controller to generate the reference signals for LS-PWM block.

Initially the balancing control is disabled and at 0.1s the controller is enabled. Figure 4. 6 shows the dc-link capacitor voltage waveforms. When the control is disabled, the top and bottom capacitors will charge continuously to reach 250V and the two middle capacitor swill discharge towards 0V. It can be seen from Figure 4. 6 that after 0.1s the capacitor voltages reach a steady state value around 125V with balancing control. The pole voltage and motor

Figure 4. 7: Five-level DCI drive waveforms with balancing circuit and LS-PWM technique. (a) Pole voltage V_{AO} measured between inverter terminal 'A' and neutral point 'O'. (b) Motor line currents. (c) Motor phase voltage and current.

Figure 4. 8: Five-level DCI PMSM drive waveforms with balancing circuit and LS-PWM technique. (a) Load torque T_l and developed torque T_e of motor. (b) Reference speed ω_r^* and rotor speed ω_r .

line currents are shown in Figure 4. 7. The pole voltage has five distinct levels +250V, 125V, 0, -125 and -250V. Figure 4. 8 shows the simulation results of rotor speed ω_r and electromagnetic torque T_e developed by the PMSM. The PMSM is started from standstill with an applied torque of $T_l = 5\text{Nm}$ and a reference speed of $\omega_r^* = 200\text{rad/s}$. The speed controller and current controllers operate in such a way that the motor tracks the reference speed in 0.35s and develops a torque equal to applied load torque plus the counter torque due to mechanical losses. Figure 4. 7.(c) shows the phase voltage and current of PMSM. The power factor of operation is 0.7 and modulation index is 0.8. Hence, an active balancing circuit with NPP control eliminates the voltage unbalancing issues in five-level DCI for operating conditions which involves large modulation indices and active load currents. The SVM technique selecting redundant vectors can be used to provide balanced voltage across the capacitors without extra circuit.

Next section proposes an SVM-based voltage balancing strategy for a new five-level multiple-pole multilevel diode-clamped inverter (M2DCI). The new topology is derived from three-level DCI and uses lower number of clamping diodes compared to classical five-DCI. A simple switching function model of new topology is derived to implement the voltage balancing strategy at reduced computational efforts compared to the conventional sector-based SVM methods. The voltage balancing limits of the inverter for which capacitor balancing is impossible are also obtained.

4.3. Five-Level Multiple-Pole Multilevel Diode-Clamped Inverter

The classical five-level DCI shown in Figure 4. 1 consists of four capacitors of voltage rating equal to $E_{dc}/4$ to split the dc-link. Each leg of the inverter consists of four complementary switching pairs and the switching devices share voltage stress equally ($E_{dc}/4$) while generating different levels of output voltages. But the reverse biased voltages across the clamping diodes in five-level DCI are different during each switching states. The total

Figure 4. 9: Five-level multiple-pole multilevel diode-clamped inverter (M2DCI) configuration.

number of clamping diodes required per-leg of the five-level DCI to maintain equal voltage distribution across them is 12, which is a substantial increase.

The multiple-pole multilevel diode-clamped inverter (M2DCI) proposed in [92] uses lower number of clamping diodes to generate per-phase multilevel structure by combining two poles of three-level DCI as shown in Figure 4. 9. Table 4. 2 shows the valid switching states and pole voltages of five-level M2DCI. Table 4. 3 presents the maximum switching stress on semiconductor devices present in five-level DCI and M2DCI topology. It can be noticed that the clamping diodes in M2DCI share voltage stress equally and the total number of clamping diodes required per-phase is four, whereas in five-level DCI it was 12.

Table 4. 2: Switching States and Pole Voltages of five-level M2DCI (X=A,B,C)

Voltage Level L_X	Switching states				Pole Voltage (V) V_{XO}
	S_{X1}	S_{X2}	S_{X3}	S_{X4}	
4	ON	ON	ON	ON	$E_{dc}/2$
3	OFF	ON	ON	ON	$E_{dc}/4$
2	OFF	OFF	ON	ON	0
1	OFF	OFF	OFF	ON	$-E_{dc}/4$
0	OFF	OFF	OFF	OFF	$-E_{dc}/2$

Table 4. 3: Maximum Voltage Stress on Semiconductor Devices

Multilevel Inverter Topology	Power Semiconductor Device, X= {A, B, C}.	Voltage stress magnitude (V)
Five-level DCI	$S_{X1}, S_{X2}, S_{X3}, S_{X4}, S'_{X1}, S'_{X2}, S'_{X3}, S'_{X4}, D_{X1}, D'_{X3}$	$E_{dc}/4$
	D_{X2}, D'_{X2}	$2 E_{dc}/4$
	D_{X3}, D'_{X1}	$3 E_{dc}/4$
Five-level M2DCI	$S_{X2}, S_{X3}, S'_{X2}, S'_{X3}, D_{X1}, D_{X2}, D'_{X1}, D'_{X2}$	$E_{dc}/4$
	S_{X4}, S'_{X1}	$2 E_{dc}/4$
	S_{X1}, S'_{X4}	$3 E_{dc}/4$

4.3.1. Proposed Current Model for Five-level M2DCI

The capacitor currents of five-level M2DCI are derived as a function of switching states and three phase output currents by writing the mathematical model of the system. Let λ_{X1} (X=A, B, C) represent the logic 1 when the switching function $S_{X1}S_{X2}S_{X3}S_{X4}$ in Figure 4. 9 are true. And from Figure 4. 10, when $\lambda_{X1}=1$ the inverter terminal 'X' is connected to top dc-link, generating a pole voltage of magnitude $E_{dc}/2$ (level 4). Similarly, λ_{X2} , λ_{X3} , λ_{X4} and λ_{X5} represents the logic signals when the respective combinations $(S_{X2} \text{ to } S'_{X1}), (S_{X3} \text{ to } S'_{X2}), (S_{X4} \text{ to } S'_{X3})$ and $(S'_{X1} \text{ to } S'_{X4})$ in Figure 4. 9 are true, which will connect the inverter terminal to the capacitor mid-points 3, 2, 1 and the bottom terminal of the dc-link, respectively, as shown in Figure 4. 10.

Figure 4. 10: Current model of five-level M2DCI.

The currents of the inverter through the top and bottom terminals of the dc-link and mid- point between the capacitors are

$$\begin{aligned}
 i_1 &= \lambda_{A1}i_A + \lambda_{B1}i_B + \lambda_{C1}i_C \\
 i_2 &= \lambda_{A2}i_A + \lambda_{B2}i_B + \lambda_{C2}i_C \\
 i_3 &= \lambda_{A3}i_A + \lambda_{B3}i_B + \lambda_{C3}i_C \\
 i_4 &= \lambda_{A4}i_A + \lambda_{B4}i_B + \lambda_{C4}i_C \\
 i_5 &= \lambda_{A5}i_A + \lambda_{B5}i_B + \lambda_{C5}i_C
 \end{aligned} \tag{4.3}$$

And the dc-link capacitor currents are

$$\begin{aligned}
 i_{C1} &= i_1 - i_{in} \\
 i_{C2} &= i_1 + i_2 - i_{in} \\
 i_{C3} &= i_1 + i_2 + i_3 - i_{in} \\
 i_{C4} &= i_1 + i_2 + i_3 + i_4 - i_{in}
 \end{aligned} \tag{4.4}$$

The voltage at inverter neutral point 'O' with respect to terminal 'A' and negative dc-bus

terminal ‘N’ are given in (4. 5) and (4. 6), respectively.

$$V_{AO} = (V_{C1} + V_{C2})\lambda_{A1} + V_{C2}\lambda_{A2} - V_{C3}\lambda_{A4} - (V_{C3} + V_{C4})\lambda_{A5} \quad (4. 5)$$

$$V_{ON} = V_{C3} + V_{C4} \quad (4. 6)$$

Applying KVL at dc-link and taking its derivative

$$\frac{1}{C_1}i_{C1} + \frac{1}{C_2}i_{C2} + \frac{1}{C_3}i_{C3} + \frac{1}{C_4}i_{C4} = 0 \quad (4. 7)$$

Substituting (4. 3) and (4. 4) in (4. 7) gives

$$i_{in} = C_{tot} \left\{ \begin{aligned} &\left(\frac{\lambda_{A1}}{C_1} + \frac{\lambda_{A1} + \lambda_{A2}}{C_2} + \frac{\lambda_{A1} + \lambda_{A2} + \lambda_{A3}}{C_3} + \frac{\lambda_{A1} + \lambda_{A2} + \lambda_{A3} + \lambda_{A4}}{C_4} \right) i_A \\ &+ \left(\frac{\lambda_{B1}}{C_1} + \frac{\lambda_{B1} + \lambda_{B2}}{C_2} + \frac{\lambda_{B1} + \lambda_{B2} + \lambda_{B3}}{C_3} + \frac{\lambda_{B1} + \lambda_{B2} + \lambda_{B3} + \lambda_{B4}}{C_4} \right) i_B \\ &+ \left(\frac{\lambda_{C1}}{C_1} + \frac{\lambda_{C1} + \lambda_{C2}}{C_2} + \frac{\lambda_{C1} + \lambda_{C2} + \lambda_{C3}}{C_3} + \frac{\lambda_{C1} + \lambda_{C2} + \lambda_{C3} + \lambda_{C4}}{C_4} \right) i_C \end{aligned} \right\} \quad (4. 8)$$

where $C_{tot} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$

For a valid switching state given in Table 4. 2,

$$\begin{aligned} \lambda_{X1} &= S_{X1}, \quad \lambda_{X2} = S_{X2} - S_{X1}, \quad \lambda_{X3} = S_{X3} - S_{X2}, \\ \lambda_{X4} &= S_{X4} - S_{X3}, \quad \text{and} \quad \lambda_{X5} = \bar{S}_{X1}. \end{aligned} \quad (4. 9)$$

Substituting (4. 9) in (4. 8)

$$i_{in} = C_{tot} \sum_{j=1}^4 \frac{S_{Aj} + S_{Bj} + S_{Cj}}{C_j} \quad (4. 10)$$

And the dc-link capacitor currents in (4. 4) can be written as

$$\begin{aligned} i_{C1} &= S_{A1}i_A + S_{B1}i_B + S_{C1}i_C - i_{in} \\ i_{C2} &= S_{A2}i_A + S_{B2}i_B + S_{C2}i_C - i_{in} \\ i_{C3} &= S_{A3}i_A + S_{B3}i_B + S_{C3}i_C - i_{in} \\ i_{C4} &= S_{A4}i_A + S_{B4}i_B + S_{C4}i_C - i_{in} \end{aligned} \quad (4. 11)$$

Hence, from (4. 10) and (4. 11), the dc-link capacitor currents can be predicted from the load current values for any valid inverter switching states. This will significantly reduce the

computational steps while implementing SVM based voltage balancing strategy for the five-level M2DCI.

Applying (4. 9) in (4. 5) and (4. 6),

$$V_{AO} = V_{C1}S_{A1} + V_{C2}S_{A2} + V_{C3}S_{A3} + V_{C4}S_{A4} - (V_{C3} + V_{C4}) \quad (4. 12)$$

$$V_{AN} = V_{C1}S_{A1} + V_{C2}S_{A2} + V_{C3}S_{A3} + V_{C4}S_{A4} \quad (4. 13)$$

where V_{AN} is the inverter terminal voltage at phase-A with respect to negative dc-bus terminal.

The voltage across the dc-link capacitors can be written as

$$\begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \end{bmatrix} = \int \left\{ \begin{bmatrix} \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 \\ 0 & 0 & 0 & \frac{1}{C_3} \end{bmatrix} \begin{bmatrix} i_{C1} \\ i_{C2} \\ i_{C3} \\ i_{C4} \end{bmatrix} dt \right\} \quad (4. 14)$$

Substituting the values of capacitor currents from (4. 4) into (4. 14)

$$\begin{aligned} \Delta V_1 &= V_{C2} - V_{C1} = \frac{1}{C_2} \int (i_1 + i_2 - i_{in}) dt - \frac{1}{C_1} \int (i_1 - i_{in}) dt \\ \Delta V_2 &= V_{C3} - V_{C2} = \frac{1}{C_3} \int (i_1 + i_2 + i_3 - i_{in}) dt - \frac{1}{C_2} \int (i_1 + i_2 - i_{in}) dt \\ \Delta V_3 &= V_{C4} - V_{C3} = \frac{1}{C_4} \int (i_1 + i_2 + i_3 + i_4 - i_{in}) dt - \frac{1}{C_3} \int (i_1 + i_2 + i_3 - i_{in}) dt \end{aligned} \quad (4. 15)$$

Hence the current through the mid-point between dc-link capacitors are responsible for capacitor voltage change and the voltage unbalancing can be minimized by controlling the average value of mid-point currents (close to zero) over one sampling time.

Also, from (4. 4) and (4. 11) the mid-point currents can be derived as

$$\begin{aligned} i_2 &= (S_{A2} - S_{A1})i_A + (S_{B2} - S_{B1})i_B + (S_{C2} - S_{C1})i_C \\ i_3 &= (S_{A3} - S_{A2})i_A + (S_{B3} - S_{B2})i_B + (S_{C3} - S_{C2})i_C \\ i_4 &= (S_{A4} - S_{A3})i_A + (S_{B4} - S_{B3})i_B + (S_{C4} - S_{C3})i_C \end{aligned} \quad (4. 16)$$

The switching states and inverter output currents control the average value of mid-point currents and hence the capacitor currents over one sampling time.

If all the capacitors are assumed to have equal magnitudes, (4. 7) becomes

$$i_{C1} + i_{C2} + i_{C3} + i_{C4} = 0 \quad (4. 17)$$

Then from (4. 4) and (4. 17) , the current through the capacitors are calculated from mid-point currents as

$$i_{Cj} = \frac{1}{4} \sum_{x=1}^3 x i_{x+1} - \sum_{x=j+1}^4 i_x \quad for \ j = 1, 2, 3, 4. \quad (4. 18)$$

This can be used for deriving the voltage control for the new five-level M2DCI, which is explained in following section.

4.4. DC-Link Capacitor Voltage Balancing Strategy

The voltage balancing principle uses the minimum energy property of capacitor banks for selecting the switching vector to maintain a balanced voltage across the capacitors [93]. When voltages across all capacitors are equal, the total energy of capacitors in Figure 4. 10 will reach its minimum value at voltage balance. Assuming the capacitors have equal capacitance (C), the minimum energy is

$$E_{min} = \frac{1}{2} \times C \times \frac{E_{dc}^2}{4} \quad (4. 19)$$

To drive the capacitors towards this minimum energy condition, a positive definite cost function ($G(t)$) with zero as absolute minimum is defined

$$G(t) = \sum_{j=1}^4 (V_{Cj} - V_{dc})^2 = \sum_{j=1}^4 \Delta V_{Cj}^2 \quad (4. 20)$$

where V_{dc} is the balanced voltage across the capacitors with a magnitude of $E_{dc}/4$.

A switching state which gives minimum value for (4. 21) is selected from the available redundant states to drive the capacitor towards the minimum energy condition as well as to provide desired three phase voltage at the inverter terminals.

$$\frac{dG(t)}{dt} = C \sum_{j=1}^4 \Delta V_{Cj} i_{Cj} \leq 0 \quad (4.21)$$

Also,

$$\Delta V_{C1} + \Delta V_{C2} + \Delta V_{C3} + \Delta V_{C4} = 0 \quad (4.22)$$

Applying (4. 18) in (4. 21) and eliminating ΔV_{C4} using (4. 22) the derivative of the cost function becomes

$$\sum_{j=1}^3 \Delta V_{Cj} \left(\sum_{x=j+1}^4 i_x \right) \geq 0 \quad (4.23)$$

where i_x can be calculated from (4. 16).

During one sampling period T_s , the voltage across the capacitors are assumed to be constant and (4. 23) is expressed as follows,

$$\sum_{j=1}^3 \Delta V_{Cj}(k) \left(\sum_{x=j+1}^4 \bar{i}_x \right) \geq 0 \quad (4.24)$$

$\Delta V_{Cj}(k)$ is the voltage error of j^{th} capacitor C_j at the beginning of the sampling interval T_s , and $\bar{i}_x(k)$ is the average value of mid-point current over that period. Hence from the available switching combination obtained in five-level SVM, the switching combination which gives maximum value for (4. 24) can be selected to achieve capacitor voltage balancing. The proposed SVM based voltage balancing strategy for five-level M2DCI is given below.

4.5. SVM of Five-level M2DCI

Let V_{AB} , V_{BC} and V_{CA} represent the reference three-phase balanced voltage generated at the inverter terminals. Then, the equivalent space vector can be written in terms of inverter output voltages as

$$\mathbf{V}_s = \sqrt{\frac{2}{3}} \left(V_{AB} + V_{BC} e^{j\frac{2\pi}{3}} + V_{CA} e^{j\frac{4\pi}{3}} \right) = V_r e^{j\theta} \quad (4.25)$$

where V_r is the magnitude of space is vector and θ is the angle of the space vector from the reference voltage V_{AB} .

Figure 4. 11: Space vector representation of switching states of five-level inverter.

A total of $5^3=125$ switching states are possible for five-level inverter. The switching states and their 61 equivalent space vector locations forms a five-level inverter space vector structure as shown in Figure 4. 11. However, for simplicity the redundant switching states are not marked in Figure 4. 11. In Figure 4. 11, ‘4’, ‘3’, ‘2’, ‘1’ and ‘0’ indicates pole voltages $E_{dc}/2$, $E_{dc}/4$, 0, $-E_{dc}/4$ and $-E_{dc}/2$, respectively. Hence, at each sampling instant, the reference voltage space vector V_s can be approximated by switching the three nearest voltage vectors which forms a triangle containing the tip of reference space vector. The relative switching time of the neighboring voltage vectors are determined using

$$V_s = (d_1 \cdot V_1 + d_2 \cdot V_2 + d_3 \cdot V_3) \quad (4. 26)$$

$$d_1 + d_2 + d_3 = 1 \quad (4. 27)$$

Here V_1 , V_2 , V_3 are the nearest three voltage vectors and d_1 , d_2 , d_3 are their respective duty ratios.

4.5.1. Redundant Voltage Vectors and their Effect on Capacitor Voltages

Switching vectors shown in Figure 4. 11 which have equal number of redundant vectors are grouped in one group. A total of 5 groups can be used to distribute the 125 switching states available for five-level inverter. Switching vector groups, redundant vectors, mid-point currents generated and dc-link capacitor currents are given in Table 4. 4. The current model of five-level M2DCI while switching 433,422,411,400 and 444 from groups G4,G3,G2,G1 and G5 are shown in Figure 4. 12. (a),(b),(c),(d) and (e), respectively. Switching vectors with 5 redundancies are given in G5. Groups G4, G3 and G2 contain voltage vectors with redundancies 4, 3 and 2, respectively. Switching states and their redundant vectors given in G4 connects the load across one capacitor while switching a specific voltage vector. And vectors and redundant states given in G3, G2 and G1 distribute the load across 2, 3 and 4 capacitors while switching a specific vector. The zero voltage vectors present in group G5 do not charge or discharge the dc-link capacitors and cannot be used for voltage balancing control.

Also, from Table 4. 4 it can be noticed that the redundant vectors can charge or discharge the dc-link capacitors depending on the load currents direction and this can be utilized for achieving voltage balancing especially at low modulation index. When the reference space vector is residing inside the hexagon formed by group G3 vectors, then redundant voltage vectors from group G4 can effectively control the dc-link capacitors and voltage balancing can be achieved. But when the modulation index is high it is difficult to balance the four dc-link capacitors using only redundant vectors. As the number of levels increases, the calculation effort required by conventional SVM becomes devastating. Hence,

for five-level inverters, the switching states represented in three-dimensional system are transformed in to hexagonal co-ordinate system and nearest three vectors and duty ratios are obtained as follows [64].

Figure 4. 12: Current model of five-level M2DCI showing the effect of switching vectors on dc-link capacitors. (a) [G4:433] (b) [G3:422] (c) [G2:411] (d) [G1:400] (e) [G5:444].

Table 4. 4: Mid-point currents and capacitor currents generated by switching states of five-level M2DCI

Group	Switching States	mid-point currents			capacitor currents			
		i_2	i_3	i_4	$(1/4)i_{C1}$	$(1/4)i_{C2}$	$(1/4)i_{C3}$	$(1/4)i_{C4}$
G1	400	0	0	0	0	0	0	0
	410	0	0	i_B	$-i_B$	$-i_B$	$-i_B$	$3i_B$
	420	0	i_B	0	$-2i_B$	$-2i_B$	$2i_B$	$2i_B$
	430	i_B	0	0	$-3i_B$	i_B	i_B	i_B
	440	0	0	0	0	0	0	0
	340	i_A	0	0	$-3i_A$	i_A	i_A	i_A
	240	0	i_A	0	$-2i_A$	$-2i_A$	$2i_A$	$2i_A$
	140	0	0	i_A	$-i_A$	$-i_A$	$-i_A$	$3i_A$
	040	0	0	0	0	0	0	0
	041	0	0	i_C	$-i_C$	$-i_C$	$-i_C$	$3i_C$
	042	0	i_C	0	$-2i_C$	$-2i_C$	$2i_C$	$2i_C$
	043	i_C	0	0	$-3i_C$	i_C	i_C	i_C
	044	0	0	0	0	0	0	0
	034	i_B	0	0	$-3i_B$	i_B	i_B	i_B
	024	0	i_B	0	$-2i_B$	$-2i_B$	$2i_B$	$2i_B$
	014	0	0	i_B	$-i_B$	$-i_B$	$-i_B$	$3i_B$
	004	0	0	0	0	0	0	0
	104	0	0	i_A	$-i_A$	$-i_A$	$-i_A$	$3i_A$
	204	0	i_A	0	$-2i_A$	$-2i_A$	$2i_A$	$2i_A$
	304	i_A	0	0	$-3i_A$	i_A	i_A	i_A
	404	0	0	0	0	0	0	0
	403	i_C	0	0	$-3i_C$	i_C	i_C	i_C
	402	0	i_C	0	$-2i_C$	$-2i_C$	$2i_C$	$2i_C$
	401	0	0	i_C	$-i_C$	$-i_C$	$-i_C$	$3i_C$
G2	411	0	0	$-i_A$	i_A	i_A	i_A	$-3i_A$
	300	i_A	0	0	$-3i_A$	i_A	i_A	i_A
	421	0	i_B	i_C	i_A-i_B	i_A-i_B	i_A+3i_B	$-3i_A-i_B$
	310	i_A	0	i_B	$-3i_A-i_B$	i_A-i_B	i_A-i_B	i_A+3i_B
	431	i_B	0	i_C	i_A-2i_B	i_A+2i_B	i_A+2i_B	$-3i_A-2i_B$
	320	i_A	i_B	0	$-3i_A-2i_B$	i_A-2i_B	i_A+2i_B	i_A+2i_B
	441	0	0	i_C	$-i_C$	$-i_C$	$-i_C$	$3i_C$
	330	$-i_C$	0	0	$3i_C$	$-i_C$	$-i_C$	$-i_C$
	341	i_A	0	i_C	$-2i_A+i_B$	$2i_A+i_B$	$2i_A+i_B$	$-2i_A-3i_B$
	230	i_B	i_A	0	$-2i_A-3i_B$	$-2i_A+i_B$	$2i_A+i_B$	$2i_A+i_B$
	241	0	i_A	i_C	$-i_A+i_B$	$-i_A+i_B$	$3i_A+i_B$	$-i_A-3i_B$
	130	i_B	0	i_A	$-i_A-3i_B$	$-i_A+i_B$	$-i_A+i_B$	$3i_A+i_B$
	141	0	0	$-i_B$	i_B	i_B	i_B	$-3i_B$
	030	i_B	0	0	$-3i_B$	i_B	i_B	i_B

G2	142	0	i_C	i_A	i_A+2i_B	i_A+2i_B	$-3i_A-2i_B$	i_A-2i_B
	031	i_B	0	i_C	i_A-2i_B	i_A+2i_B	i_A+2i_B	$-3i_A-2i_B$
	143	i_C	0	i_A	$2i_A-3i_B$	$-2i_A-i_B$	$-2i_A-i_B$	$2i_A-i_B$
	032	i_B	i_C	0	$2i_A-i_B$	$2i_A-3i_B$	$-2i_A-i_B$	$-2i_A-i_B$
	144	0	0	i_A	$-i_A$	$-i_A$	$-i_A$	$3i_A$
	033	$-i_A$	0	0	$3i_A$	$-i_A$	$-i_A$	$-i_A$
	134	i_B	0	i_A	$-i_A-3i_B$	$-i_A+i_B$	$-i_A+i_B$	$3i_A+i_B$
	023	i_C	i_B	0	$3i_A+i_B$	$-i_A-3i_B$	$-i_A+i_B$	$-i_A+i_B$
	124	0	i_B	i_A	$-i_A-2i_B$	$-i_A-2i_B$	$-i_A+2i_B$	$3i_A+2i_B$
	013	i_C	0	i_B	$3i_A+2i_B$	$-i_A-2i_B$	$-i_A-2i_B$	$-i_A+2i_B$
	114	0	0	$-i_C$	i_C	i_C	i_C	$-3i_C$
	003	i_C	0	0	$-3i_C$	i_C	i_C	i_C
	214	0	i_A	i_B	$-2i_A-i_B$	$-2i_A-i_B$	$2i_A-i_B$	$2i_A+3i_B$
	103	i_C	0	i_A	$2i_A+3i_B$	$-2i_A-i_B$	$-2i_A-i_B$	$2i_A-i_B$
	314	i_A	0	i_B	$-3i_A-i_B$	i_A-i_B	i_A-i_B	i_A+3i_B
	203	i_C	i_A	0	i_A+3i_B	$-3i_A-i_B$	i_A-i_B	i_A-i_B
	414	0	0	i_B	$-i_B$	$-i_B$	$-i_B$	$3i_B$
	303	$-i_B$	0	0	$3i_B$	$-i_B$	$-i_B$	$-i_B$
	413	i_C	0	i_B	$3i_A+2i_B$	$-i_A-2i_B$	$-i_A-2i_B$	$-i_A+2i_B$
	302	i_A	i_C	0	$-i_A+2i_B$	$3i_A+2i_B$	$-i_A-2i_B$	$-i_A-2i_B$
	412	0	i_C	i_B	$2i_A+i_B$	$2i_A+i_B$	$-2i_A-3i_B$	$-2i_A+i_B$
	301	i_A	0	i_C	$-2i_A+i_B$	$2i_A+i_B$	$2i_A+i_B$	$-2i_A-3i_B$
G3	422	0	$-i_A$	0	$2i_A$	$2i_A$	$-2i_A$	$-2i_A$
	311	i_A	0	$-i_A$	$-2i_A$	$2i_A$	$2i_A$	$-2i_A$
	200	0	i_A	0	$-2i_A$	$-2i_A$	$2i_A$	$2i_A$
	432	i_B	i_C	0	$2i_A-i_B$	$2i_A+3i_B$	$-2i_A-i_B$	$-2i_A-i_B$
	321	i_A	i_B	i_C	$-2i_A-i_B$	$2i_A-i_B$	$2i_A+3i_B$	$-2i_A-i_B$
	210	0	i_A	i_B	$-2i_A-i_B$	$-2i_A-i_B$	$2i_A-i_B$	$2i_A+3i_B$
	442	0	i_C	0	$-2i_C$	$-2i_C$	$2i_C$	$2i_C$
	331	i_C	0	i_C	$2i_C$	$-2i_C$	$-2i_C$	$2i_C$
	220	0	$-i_C$	0	$2i_C$	$2i_C$	$-2i_C$	$-2i_C$
	342	i_A	i_C	0	$-i_A+2i_B$	$3i_A+2i_B$	$-i_A-2i_B$	$-i_A-2i_B$
	231	i_B	i_A	i_C	$-i_A-2i_B$	$-i_A+2i_B$	$3i_A+2i_B$	$-i_A-2i_B$
	120	0	i_B	i_A	$-i_A-2i_B$	$-i_A-2i_B$	$-i_A+2i_B$	$3i_A+2i_B$
	242	0	$-i_B$	0	$2i_B$	$2i_B$	$-2i_B$	$-2i_B$
	131	i_B	0	$-i_B$	$-2i_B$	$2i_B$	$2i_B$	$-2i_B$
	020	0	i_B	0	$-2i_B$	$-2i_B$	$2i_B$	$2i_B$
	243	i_C	i_A	0	i_A+3i_B	$-3i_A-i_B$	i_A-i_B	i_A-i_B
	132	i_B	i_C	i_A	i_A-i_B	i_A+3i_B	$-3i_A-i_B$	i_A-i_B
	021	0	i_B	i_C	i_A-i_B	i_A-i_B	i_A+3i_B	$-3i_A-i_B$
	244	0	i_A	0	$-2i_A$	$-2i_A$	$2i_A$	$2i_A$

G3	133	$-i_A$	0	i_A	$2i_A$	$-2i_A$	$-2i_A$	$2i_A$
	022	0	$-i_A$	0	$2i_A$	$2i_A$	$-2i_A$	$-2i_A$
	234	i_B	i_A	0	$-2i_A-3i_B$	$-2i_A+i_B$	$2i_A+i_B$	$2i_A+i_B$
	123	i_C	i_B	i_A	$2i_A+i_B$	$-2i_A-3i_B$	$-2i_A+i_B$	$2i_A+i_B$
	012	0	i_C	i_B	$2i_A+i_B$	$2i_A+i_B$	$-2i_A-3i_B$	$-2i_A+i_B$
	224	0	$-i_C$	0	$2i_C$	$2i_C$	$-2i_C$	$-2i_C$
	113	i_C	0	$-i_C$	$-2i_C$	$2i_C$	$2i_C$	$-2i_C$
	002	0	i_C	0	$-2i_C$	$-2i_C$	$2i_C$	$2i_C$
	324	i_A	i_B	0	$-3i_A-2i_B$	i_A-2i_B	i_A+2i_B	i_A+2i_B
	213	i_C	i_A	i_B	i_A+2i_B	$-3i_A-2i_B$	i_A-2i_B	i_A+2i_B
	102	0	i_C	i_A	i_A+2i_B	i_A+2i_B	$-3i_A-2i_B$	i_A-2i_B
	424	0	i_B	0	$-2i_B$	$-2i_B$	$2i_B$	$2i_B$
	313	$-i_B$	0	i_B	$2i_B$	$-2i_B$	$-2i_B$	$2i_B$
	202	0	$-i_B$	0	$2i_B$	$2i_B$	$-2i_B$	$-2i_B$
	423	i_C	i_B	0	$3i_A+i_B$	$-i_A-3i_B$	$-i_A+i_B$	$-i_A+i_B$
	312	i_A	i_C	i_B	$-i_A+i_B$	$3i_A+i_B$	$-i_A-3i_B$	$-i_A+i_B$
	201	0	i_A	i_C	$-i_A+i_B$	$-i_A+i_B$	$3i_A+i_B$	$-i_A-3i_B$
G4	433	$-i_C$	0	0	$3i_A$	$-i_A$	$-i_A$	$-i_A$
	322	i_A	$-i_A$	0	$-i_A$	$3i_A$	$-i_A$	$-i_A$
	211	0	i_A	$-i_A$	$-i_A$	$-i_A$	$3i_A$	$-i_A$
	100	0	0	i_A	$-i_A$	$-i_A$	$-i_A$	$3i_A$
	443	i_C	0	0	$-3i_C$	i_C	i_C	i_C
	332	$-i_C$	i_C	0	i_C	$-3i_C$	i_C	i_C
	221	0	$-i_C$	i_C	i_C	i_C	$-3i_C$	i_C
	110	0	0	$-i_C$	i_C	i_C	i_C	$-3i_C$
	343	$-i_B$	0	0	$3i_B$	$-i_B$	$-i_B$	$-i_B$
	232	i_B	$-i_B$	0	$-i_B$	$3i_B$	$-i_B$	$-i_B$
	121	0	i_B	$-i_B$	$-i_B$	$-i_B$	$3i_B$	$-i_B$
	010	0	0	i_B	$-i_B$	$-i_B$	$-i_B$	$3i_B$
	344	i_A	0	0	$-3i_A$	i_A	i_A	i_A
	233	$-i_A$	i_A	0	i_A	$-3i_A$	i_A	i_A
	122	0	$-i_A$	i_A	i_A	i_A	$-3i_A$	i_A
	011	0	0	$-i_A$	i_A	i_A	i_A	$-3i_A$
	334	$-i_C$	0	0	$3i_C$	$-i_C$	$-i_C$	$-i_C$
	223	i_C	$-i_C$	0	$-i_C$	$3i_C$	$-i_C$	$-i_C$
	112	0	i_C	$-i_C$	$-i_C$	$-i_C$	$3i_C$	$-i_C$
	001	0	0	i_C	$-i_C$	$-i_C$	$-i_C$	$3i_C$
	434	i_B	0	0	$-3i_B$	i_B	i_B	i_B
	323	$-i_B$	i_B	0	i_B	$-3i_B$	i_B	i_B
	212	0	$-i_B$	i_B	i_B	i_B	$-3i_B$	i_B
	101	0	0	$-i_B$	i_B	i_B	i_B	$-3i_B$

G5	444	0	0	0	0	0	0	0
	333	0	0	0	0	0	0	0
	222	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0
	000	0	0	0	0	0	0	0

4.5.2. Coordinate Transformation

The three-dimensional switching states of five-level inverter can be transformed using (4. 28) in to two-dimensional representation. Figure 4. 13 shows the switching states of the five-level inverter in hexagonal coordinate system after transformation.

$$\begin{aligned}
 \mathbf{V}_{gh} &= \begin{bmatrix} V_g & V_h \end{bmatrix}^T \\
 V_g &= \frac{V_r}{\sqrt{2}V_{dc}} \left(\cos \psi - \frac{1}{\sqrt{3}} \sin \psi \right) \\
 V_h &= \sqrt{\frac{2}{3}} \times \frac{V_r}{V_{dc}} \sin \psi
 \end{aligned} \tag{4. 28}$$

where $V_{dc}=E_{dc}/4$ and $\psi = \theta - 30^\circ$.

4.5.3. Selection of Nearest Vectors

The three nearest vectors can be selected from a set of four nearest vectors obtained

Figure 4. 13: Space vector representation of switching states of five-level inverter in hexagonal coordinate system.

from upper and lower rounded integer values of V_g and V_h .

$$\mathbf{V}_{ul} = \begin{bmatrix} V_{gu} \\ V_{hl} \end{bmatrix}; \quad \mathbf{V}_{lu} = \begin{bmatrix} V_{gl} \\ V_{hu} \end{bmatrix}; \quad \mathbf{V}_{uu} = \begin{bmatrix} V_{gu} \\ V_{hu} \end{bmatrix}; \quad \mathbf{V}_{ll} = \begin{bmatrix} V_{gl} \\ V_{hl} \end{bmatrix} \quad (4.29)$$

Then

$$\begin{aligned} \mathbf{V}_1 &= \mathbf{V}_{ul} \\ \mathbf{V}_2 &= \mathbf{V}_{lu} \end{aligned} \quad (4.30)$$

And the third vector can be selected based on the following rule.

$$\begin{aligned} \text{if } \mathbf{V}_g + \mathbf{V}_h - (V_{gu} + V_{hl}) > 0 \quad \text{then } \mathbf{V}_3 &= \mathbf{V}_{uu} \\ \text{else } \mathbf{V}_3 &= \mathbf{V}_{ll} \end{aligned} \quad (4.31)$$

4.5.4. Duty Cycle Calculation

The duty ratio values are computed based on the selection of third nearest vector $\mathbf{V}_3$ as follows.

$$\begin{aligned} \text{if } \mathbf{V}_3 &= \mathbf{V}_{uu} \\ d_1 &= V_g - V_{gl} \quad \text{and} \quad d_2 = V_h - V_{hl} \end{aligned} \quad (4.32)$$

$$\begin{aligned} \text{if } \mathbf{V}_3 &= \mathbf{V}_{ll} \\ d_1 &= -(V_h - V_{hu}) \quad \text{and} \quad d_2 = -(V_g - V_{gu}) \end{aligned} \quad (4.33)$$

4.5.5. Selection of Switching States in Three Dimensional System

The switching vectors $\mathbf{V}_x = [g, h]^T$ for $x=1,2$ and 3 in two-dimensional coordinate system are transformed back to inverter switching states by evaluating

$$\begin{bmatrix} k \\ k - V_x(1,1) \\ k - V_x(1,1) - V_x(2,1) \end{bmatrix} \quad (4.34)$$

where $k, k - V_x(1,1), k - V_x(1,1) - V_x(2,1) \in [0, 4]$

For example, the vector $\mathbf{V}_x = [1, 2]^T$ when transformed back to the inverter switching states gives two possible switching states $[3, 2, 0]^T$ and $[4, 3, 1]^T$. The selection of switching state from available redundant switching state vectors is based on dc-link capacitor voltage balancing strategy which is explained in the following section.

4.6. Proposed SVM based Balancing Strategy for Five-level M2DCI

The nearest three voltage vectors and their duty ratios over one sampling period are obtained using fast SVM technique as explained above. Let r_1, r_2, r_3 represent the number of switching states available and $V_{1-r1}, V_{2-r2}, V_{3-r3}$ be the valid switching states obtained from (4. 34) for V_1, V_2 and V_3 , respectively, during each sampling period. Then the total number of switching combinations available by taking one redundant vector from each vector group will be $(r_1 \times r_2 \times r_3)$. The average mid-point current $\bar{i}_x$ corresponding to each set of switching combinations is obtained by

$$\bar{i}_x = i_{x,V_{1-r1}} \times d_1 + i_{x,V_{2-r2}} \times d_2 + i_{x,V_{3-r3}} \times d_3 \text{ for } x = 2, 3, 4. \quad (4. 35)$$

$i_{x,V_{1-r1}}, i_{x,V_{2-r2}}, i_{x,V_{3-r3}}$ are the mid-point currents generated while switching one redundant vector from each vector group V_1, V_2, V_3 , respectively. From the switching signal model of five-level M2DCI, the mid-point currents i_x can be calculated by sensing the load currents for any valid switching combination. From (4. 16),

$$i_x = (S_{Ax} - S_{Ax-1})i_A + (S_{Bx} - S_{Bx-1})i_B + (S_{Cx} - S_{Cx-1})i_C \text{ for } x = 2, 3, 4. \quad (4. 36)$$

With the proposed SVM technique, the dc-link capacitor currents, as well as mid-point currents, are predicted from the switching function model of five-level M2DCI, which reduces the number of calculations required in each sampling period compared to the sector-based methods in [78, 94]. The switching combination which gives maximum value for (4. 37) is selected to achieve voltage balancing, and switching states of the selected three vectors are arranged in a sequence to ensure minimum switching of inverter legs.

$$\sum_{j=1}^3 \Delta V_{Cj}(k) \left(\sum_{x=j+1}^4 \bar{i}_x \right) \geq 0 \quad (4. 37)$$

For example, in Figure 4. 13, $V_1 = [1, 2]^T$, $V_2 = [2, 1]^T$ and $V_3 = [2, 2]^T$. The three dimensional switching states obtained from (4. 34) are shown in Figure 4. 14. V_1 has two redundant switching states : $V_{1-r1} = [3, 2, 0]^T$ and $V_{1-r2} = [4, 3, 1]^T$. The two possible switching

Figure 4. 14: Triangular section of space vector representation of five-level inverter.

states of v_2 are: $V_{2-1} = [3, 1, 0]^T$ and $V_{2-2} = [4, 2, 1]^T$. The only valid state for the third vector v_3 is $V_{3-1} = [4, 2, 0]^T$. First, the mid-point currents generated by all switching states are computed using (4. 36) and Table 4. 2. Then, the average mid-point current and the cost function (4. 37) are obtained for each set of switching combinations while taking one redundant vector at a time.

Here the four possible $(2 \times 2 \times 1)$ switching combinations are

- 310,320,420
- 310,431,420
- 421,431,420
- 421,320,420

The average mid-point currents for the first switching combination are obtained as

$$\begin{aligned}
 \bar{i}_2 &= i_{2,310} \times d_1 + i_{2,320} \times d_2 + i_{2,420} \times d_3 \\
 \bar{i}_3 &= i_{3,310} \times d_1 + i_{3,320} \times d_2 + i_{3,420} \times d_3 \\
 \bar{i}_4 &= i_{4,310} \times d_1 + i_{4,320} \times d_2 + i_{4,420} \times d_3
 \end{aligned} \tag{4. 38}$$

The mid-point currents for switching state [310] are obtained from (4. 39) with the help of Table 4. 2 , and are given by

Figure 4. 15: Flow chart of the proposed SVM based voltage control scheme for five-level M2DCI

$$\begin{bmatrix} i_{2,310} \\ i_{3,310} \\ i_{4,310} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \quad (4.39)$$

Similarly the mid-point currents for other switching functions are obtained.

The flow chart and control block schematic of the proposed method are shown in Figure 4. 15 and Figure 4. 16.

Figure 4.16: Control block schematic of the proposed SVM based voltage control scheme for five-

In sector based methods [78, 94], the average mid-point currents are calculated using

$$\begin{bmatrix} \bar{i}_2 & \bar{i}_3 & \bar{i}_4 \end{bmatrix}^T = D S_T I_{dq} \text{ where } D \text{ is the duty ratio matrix, } S_T = S T_{dq}^T \text{ is the transformed sector}$$

matrix and $I_{dq} = T_{dq} i_{abc}$ is the transformed output current matrix in rotating reference frame

(d-q frame). In each sampling period, the method requires minimum 56 multiplications, 38

summations and a number of comparisons to find the average mid-point currents. With the

proposed method, there is at least 30% reduction in number of calculations and contains no

comparisons.

Table 4. 5: Specification of five-level M2DCI system

DC-Link voltage, E_{dc}	340V
DC-Link capacitor, C_j , $j=1,2,3,4$.	2200 μ F $\pm$ 20% tolerance and ESR=100m Ω
Sampling Frequency, f_s	4kHz
Load current Amplitude, I_L^{peak}	5A
Frequency	50Hz

4.7. Performance Evaluation of SVM-based Voltage Balancing control of five-Level M2DCI

To evaluate the performance of the proposed SVM based voltage control strategy of five-level M2DCI, a constant DC source is connected at the dc side of the inverter and a three phase RL load is connected at the ac side of the inverter. The whole system is co-simulated between Matlab/Simulink® and PSIM environments. The system parameters are given in Table 4. 5. To obtain the limits of the proposed voltage balancing strategy for the M2DCI, simulation is done at various load power factor angles and modulation indexes. The stability region obtained is shown as shaded area in Figure 4. 17. The solid line gives the boundary under which the proposed control provides balanced capacitor voltages. The area under solid line is called stable region. When five-level M2DCI operating points are located above the solid line (unstable region) the proposed voltage control strategy cannot provide balanced capacitor voltages. The stability limit shown in Figure 4. 17 for various modulation indices and power factors are obtained by simulation studies. The stability region obtained for the proposed M2DCI topology lies within the theoretical voltage balance limits for classical diode clamped topology. The boundary in classical higher order diode clamped topology is defined by

$$m = \frac{\sqrt{3}}{\pi \times |PF|} \quad (4. 40)$$

Figure 4. 17: Voltage balance limits for SVM-based capacitor voltage balancing strategy of proposed five-level M2DCI.

When the converter is operating in an unstable region shown in Figure 4. 17 the capacitor voltages cannot maintain balanced steady state values and the voltage balancing control fails to provide equal voltage sharing of dc capacitors. In Figure 4. 17, when five-level M2DCI is operating at a unity power factor (UPF) and modulation index $m = 0.5$ (operating point “A”) the capacitor are balanced. And for converter operating point “B” (PF=1 and $m = 0.65$) the capacitors becomes unbalanced. When the converter operates at low PF, the voltage balancing control has the capability of providing balanced voltages for high modulation indices. In Figure 4. 17, operating points “C” (PF=0.6 and $m = 0.7$) and “D” (PF=0.9 and $m = 0.35$) are stable operating points; the SVM based voltage control provides a balanced voltage across dc-link capacitors. The operation of the proposed system described in

Figure 4. 18: Five-level M2DCI waveforms with balanced load operating at PF=1 and $m = 0.5$ (Stable operating point “A”). (a). Line voltage, V_{AB} .(b).) Line current, i_{ABC} (c) DC-Link capacitor voltages V_{Cj} for $j=1,2,3,4$.(d) FFT of Line voltage.

Figure 4. 16 is evaluated using Matlab/Simulink® and PSIM for various operating conditions and results are presented below.

4.7.1. Balanced Load Condition

When load is assumed as linear and balanced at unity power factor (PF=1), the control algorithm will provide a balanced voltage across dc-link capacitors for $m = 0.5$ (point “A” on Figure 4. 17) as shown in Figure 4. 18 . When modulation index is increased above $m = 0.53$, the capacitor voltages are uncontrollable and hence line voltages are distorted. The inverter waveforms corresponding to unstable operating point “B” on Figure 4. 17 ($m = 0.65$ and PF=1) are shown in Figure 4. 19. As the load power factor angle is increased to 69.51° (PF=0.35) with $m = 0.9$ (point “D” on Figure 4. 17), the dc-link

Figure 4. 19: Five-level M2DCI waveforms with balanced load operating at PF=1 and $m=0.65$ (Unstable operating point “B”). (a). Line voltage, V_{AB} . (b). Line current, i_{ABC} . (c) DC-Link capacitor voltages V_{Cj} for $j=1, 2, 3, 4$. (d) FFT of Line voltage.

capacitors converge to a voltage of $E_{dc}/4$, which is equal to 85V [Figure 4. 20.(c)] ensuring that, when the converter operates at stable operating points, the balancing algorithm eliminates the voltage drift phenomena in M2DCI. Figure 4. 20 shows the inverter waveforms at operating point $m=0.9$ and PF=0.35. The capacitors are balanced and converter output voltage V_{AB} gives 9 levels.

4.7.2. Unbalanced Load Condition

The operating points mentioned in the balanced load conditions are simulated with unbalanced load currents (12% unbalance) of amplitudes $\hat{I}_A = 5.6A$, $\hat{I}_B = 5A$ and $\hat{I}_C = 4.4A$ to verify the effectiveness of proposed SVM based capacitor voltage balancing control. It was observed that the stability region remains the same even for unbalanced load condition. The

Figure 4. 20: Five-level M2DCI waveforms with balanced load operating at PF=0.35 and (Stable operating point “D”). (a). Line voltage, V_{AB} .(b) Line current, i_{ABC} .(c) DC-Link capacitor voltages V_{Cj} for $j=1,2,3,4$. (d) FFT of Line voltage.

inverter waveforms corresponding to operating point “D” on Figure 4. 17 (PF=0.35 and $m = 0.9$) are shown in Figure 4. 21.

4.7.3. Effect of Harmonics

Non-linear loads connected at inverter terminals generate harmonics in output currents. Hence to study the performance of the proposed SVM-based balancing strategy, three phase current sources are connected at the ac side of the inverter to generate distorted load currents. Figure 4. 22 shows the M2DCI waveforms with 20% third order harmonic current injection. The fundamental component amplitude is 5A. Figure 4. 23 depicts the converter waveforms with 20% of third order harmonic and 10% of fifth order harmonic

(d)

(e)

(f)

(g)

Figure 4. 21: Five-level M2DCI waveforms with unbalanced load operating at PF=0.35 and $m=0.9$ (Stable operating point “D”). (a) Line voltage, V_{AB} . (b) Line current, i_{ABC} . (c) DC-Link capacitor voltages V_{Cj} for $j=1,2,3,4$. (d) FFT of Line voltage. (e) FFT of i_A . (d) FFT of i_B . (e) FFT of i_C . current injection. In both cases, the dc-link capacitor voltages are balanced and give a steady state voltage of 85V.

Figure 4. 22: Five-level M2DCI waveforms with distorted load (20% of 3rd harmonic) operating at PF=0.35 and $m = 0.9$ (Stable operating point “D”). (a) Line voltage, V_{AB} (b) Line current, i_{ABC} . (c) DC-Link capacitor voltages V_{Cj} for $j=1,2,3,4$. (d) FFT of Line voltage. (e) FFT of i_A .

From the FFT comparison made between the proposed SVM technique and conventional balancing circuit technique (Table 4.6), it is observed that the proposed SVM based technique gives larger fundamental component and improved THD of output voltage for five-level M2DCI. However, the operation range is not wide when as compared to conventional balancing technique. With the proposed technique, the modulation index allowed for high power factor operation is less and hence to produce necessary output voltage higher dc-link voltage is required as compared to conventional balancing technique.

Figure 4. 23: Five-level M2DCI waveforms with distorted load (20% of 3rd and 10% of 5th harmonics) operating at PF=0.35 and $m=0.9$ (Stable operating point "D"). (a) Line voltage, V_{AB} . (b) Line current, i_{ABC} (c) DC-Link capacitor voltages V_{Cj} for $j=1,2,3,4$. (d) FFT of Line voltage. (e) FFT of i_A .

Table 4. 6: Comparison of Proposed Modulation method with Conventional Balancing**Technique using Balancing circuit**

Operating Condition	Proposed Modulation Method			Conventional Balancing Technique		
	THD of V_{AB} (%) , V_{AB} (fun)*	THD of i_{ABC} (%) , i_{ABC} (fun)	V_{Cj} for $j=1,2,3,4$.	THD of V_{AB} (%) , V_{AB} (fun)	THD of i_{ABC} (%) , i_{ABC} (fun)	V_{Cj} for $j=1,2,3,4$.
PF=1, m=0.5	26.92 % , 169.4V	0.32% , 5A	Balanced	35.13% , 145V	0.32% , 4.33A	Balanced
PF=1, m=0.65	29.12% , 311V	0.32% , 5A	Unbalanced	24.36% , 193.4V	0.32% , 4.33A	Balanced
PF=0.35, m=0.9 (balanced load)	16.92% , 305.8V	0.32% , 5.01A	Balanced	17.37% , 263.5V	0.32% , 4.34A	Balanced
PF=0.35, m=0.9 (12% unbalanced load)	17.03% , 305.6V	0.32% , 5.26A, 5A, 4.67A	Balanced	17.3% , 263.5V	0.2% , 4.55A, 4.34A, 4.04A	Balanced
PF=0.35, m=0.9 (20% of 3 rd harmonic load)	16.85% , 305.6V	20% , 5A	Balanced	17.34% , 263.4V	20% , 4.3A	Balanced
PF=0.35, m=0.9 (20% of 3 rd and 10% of 5 th harmonic load)	16.85% , 305.7V	22.36% , 5A	Balanced	17.36% , 263.4V	22.36% , 4.3A	Balanced

*(fun) represents the fundamental component

4.7.4. Dynamic Response Evaluation

The five-level M2DCI is operated at PF=0.3 and m=0.9, i.e., point “D” on Figure 4. 17 under various load changes. Initially, the inverter is supplying a balanced linear load of amplitude 1.4A. Figure 4. 24.(a) shows the inverter waveforms when load is increased to 2.3A at 0.5s. Figure 4. 24.(b) shows the inverter waveforms when the load has changed from balanced to unbalanced. In Figure 4. 24.(c), at 0.5 s some non-linear loads are connected at the inverter output terminals. It is seen from Figure 4. 24 that the SVM based voltage control is able to maintain balanced capacitor voltages though there is a change in load at 0.5s. The increased voltage ripples present in the capacitor voltages are due to increase in load current

Figure 4. 24: Dynamic performance of dc-link voltage balancing scheme of five-level M2DCI operating at PF=0.3 and $m = 0.9$ (Stable operating point “D”).

Upper: dc-link capacitor voltages V_{Cj} for $j=1,2,3,4$; Lower: Line current i_A

- (a) sudden change in balanced linear load from 1.4 to 2.3A.
- (b) sudden change in linear load from balanced to un-balanced.
- (c) sudden change in balanced load from linear to non-linear.

amplitude. And by increasing the capacitance value the ripple magnitude can be reduced. The transient change in capacitor voltages from their nominal values owing to the change in load are 1.6%, 3% and 2.8% as shown in Figure 4. 24. (a), (b) and (c) respectively.

Figure 4. 25: Switching scheme to protect the system during unbalanced operation.

When the inverter operating conditions are above the stability limit shown in Figure 4. 17 the balancing algorithm cannot provide balanced voltage across the capacitors and this will create unequal distribution of power loss in in IGBT modules and may damage the semiconductor components. To protect the system during such unbalanced operation (like the case study shown in Figure 4. 19) the capacitor voltages are monitored within a limit as shown in Figure 4.25 and switching signals are modified. Hence during unbalanced operations the gating signals are zero and IGBTs are protected.

4.8. Experimental Verification

The performance of the proposed SVM balancing control of five-level M2DCI system shown in Figure 4. 16 was tested experimentally for balanced and unbalanced load conditions at various load PF and modulation indices using a 1.5kW prototype (Figure 4. 26). dSPACE-DS1103 PPC controller was used to implement the proposed control strategy.

Figure 4. 26: Laboratory prototype of five-level M2DCI.

Voltage and current sensors were used to sense dc-link capacitor voltages and load currents required by the controller for generating gating signals for inverter switches.

The main circuit parameters are the following:

- dc-link Voltage (E_{dc}): 200V
- dc-link capacitors (C_1, C_2, C_3, C_4): $2200\mu F$ with $\pm 20\%$ tolerance and $ESR=100m\Omega$.
- Sampling frequency (f_s): 2.5 kHz.
- Load current amplitude (i_{ABC}^{peak}): 2.3A.

The results obtained ensure the effectiveness of SVM based voltage balancing control in the stability region shown in Figure 4. 17. The results are presented below.

4.8.1. Balanced Load Condition

To verify the results presented in section 4.7.1, the M2DCI was operated at $PF=0.6$ and $m=0.7$ (point “C” on Figure 4. 17) with a balanced RL load of value $R/\text{phase}=21\Omega$ and $L/\text{phase}=90mH$. Figure 4. 27.(a) shows, the individual capacitor voltages when 200V is

(a)

(b)

Figure 4. 27: Experimental results of five-level M2DCI operating at PF=0.6 and m=0.7 (Stable operating point “C”) with balanced load.

(a) dc-link capacitor voltages V_{Cj} for $j=1,2,3,4$ [20V/div].(Mean values: $V_{C1}=50.17$, $V_{C2}=50.96$, $V_{C3}=50.75$, $V_{C4}=48.22$)

(b) Upper trace: Line voltage, V_{AB} [100V/div]. Lower trace: Line current i_A [5A/div].

applied at the dc-link, while the line voltage and load current waveforms are shown in Figure 4. 27.(b). The individual dc-link capacitors are balanced around 50V and the line voltage has 7 distinct levels. Figure 4. 28 (a) and (b) show the individual capacitor voltages, line voltage and load current waveforms when M2DCI is operated at PF=0.3 and m=0.9 with three phase RL load of value $R/\text{phase}=13.5 \Omega$ and $L/\text{phase}=137\text{mH}$. Since the system is operated at stable operating point “D” on Figure 4. 17, the dc-link capacitors achieved a balanced voltage of 50V across them as shown in Figure 4. 28 (a). The line voltage waveform shown inFigure 4.

(a)

(b)

Figure 4. 28: Experimental results of five-level M2DCI operating at PF=0.3 and m=0.9 (Stable operating point “D”) with balanced load.

(a) dc-link capacitor voltages V_{Cj} for $j=1,2,3,4$ [20V/div].(Mean values: $V_{C1}=47.84$, $V_{C2}=51.83$, $V_{C3}= 50.10$, $V_{C4}=50.18$)

(b) Upper trace: Line voltage, V_{AB} [20V/div]. Lower trace: Line current i_A [5A/div].

28 .(b) has greater number of distinct levels when compared with Figure 4. 27. (b) due to the higher value of modulation index.

4.8.2. Unbalanced Load Condition

To verify the effectiveness of the proposed voltage balancing control strategy during unbalanced load currents of amplitudes $i_A^{peak} = 2.05A$, $i_B^{peak} = 2.3A$ and $i_C^{peak} = 2.1A$, three RL loads of different values are connected at the ac side of the M2DCI, and the inverter is

(a)

(b)

Figure 4. 29: Experimental results of five-level M2DCI operating at PF=0.3 and m=0.9 (Stable operating point “D”) with unbalanced load.

- (a) dc-link capacitor voltages V_{Cj} for $j=1,2,3,4$ [20V/div].(Mean values: $V_{C1}=49.04$, $V_{C2}= 50.62$, $V_{C3}= 49.50$, $V_{C4}=50.13$)
- (c) Upper trace: Line voltage, V_{AB} [200V/div]. Lower trace: Line currents i_A , i_B , and i_C [1A/div] with peak to peak values 4.10,4.62 and 4.20 respectively.

operated at various power factors and modulation indices. The M2DCI waveforms corresponding to PF=0.3 and m=0.9, i.e., point “D” on Figure 4. 17 is shown in Figure 4. 29. The dc-link capacitor voltages V_{C1} , V_{C2} , V_{C3} , and V_{C4} , and their average values are shown in Figure 4. 29. (a), while Figure 4. 29.(b) shows the line voltage V_{AB} and load currents i_A , i_B , and i_C . The line voltage waveform has 9 levels and load currents i_A , i_B , and i_C peak to peak amplitudes are 4.10, 4.62 and 4.20A respectively. DC-link capacitor voltages converge to steady state value of 50V (Figure 4. 29.(a)). This ensures that when the converter operates at

stable operating points, the balancing algorithm eliminates the voltage drift phenomena in M2DCI even for some unbalanced load conditions.

4.9. Conclusion

In this chapter, SVM-based dc-link capacitor voltage balancing technique for five-level multiple-pole multilevel diode-clamped inverter (M2DCI) was proposed. The switching signal model of five-level M2DCI was derived to predict the dc-link capacitor currents by sensing the load currents, which reduced the number of calculations (at least 30%) per sampling period to implement the proposed voltage control technique when compared to conventional sector based SVM techniques. The stability region for the proposed scheme was verified using both simulation and experimental results at various load conditions. It was noted that to achieve capacitor balancing, modulation index was restricted to about 60% of its maximum value when loads of high power factor, i.e., $PF \geq 0.8$ were connected at the inverter terminals. Hence, the proposed reduced device topology with SVM technique, which self-balances the dc-link capacitors without any voltage balancing circuit, can be very attractive for reactive power control in a grid connected environment to enhance the performance and efficiency.

A Space Vector Modulated Five-Level Multiple-pole Multilevel Diode Clamped Based STATCOM Application

5.1. Introduction

The voltage-sourced converters (VSC) are commonly used for most of the Flexible AC Transmission System (FACTS) controllers due to low overall cost and good performance. The STATic synchronous COMpensator (STATCOM) is a shunt connected advanced FACTS controller used for voltage control, VAR compensation, and for stabilizing voltage in electric power system [6, 95, 96]. The VSC based STATCOM generates a controllable synchronous three phase output voltage from an energy storage capacitor that forces reactive power exchange with the ac system required for compensation. The transformer used in conventional two-level VSC based STATCOM for voltage matching between converter AC output voltage and utility grid contributes major power losses and increases the system size and cost. Multilevel inverters generate high voltages with less harmonics and EMI emissions by using devices of smaller voltage ratings which makes them suitable in STATCOM application [21, 29]. Hence multilevel inverter based STATCOM eliminates the need of transformer and can be directly connected to the utility grids for improved efficiency. In [7, 97, 98], multilevel inverter based commercial STATCOM systems are presented. Special attention has to be given to maintain constant voltage across the dc-link capacitors during all operating conditions. The voltage balancing circuit presented in [89] consists of two bidirectional buck-boost choppers connected on the dc-link of the converter together with mid-point control employing 6th harmonic zero sequence voltage injection techniques and provides well-balanced capacitor voltages for a 200V,10kVA

STATCOM based on five-level NPC. However the need for this additional hardware increases the system size and cost. The voltage balancing issues in classical diode clamped multilevel inverters (DCMI) and some voltage equalization methods are addressed in [7, 88, 99, 100]. The space vector modulation (SVM) based voltage balancing strategy in [101] utilizes the redundant voltage vector property of five-level NPC inverters to maintain constant voltage across the dc-link capacitors in all operating conditions. Although this method eliminates the auxiliary hardware, it requires the information on which sector the reference space vector is located in and involves increased number of calculation during each sampling interval which makes the system more complex.

The objective of this chapter is to investigate the performance of five-level M2DCI for STATCOM application using the proposed SVM with lower computational requirement to balance the dc-link capacitor voltages. The proposed methodology greatly reduces number of calculations required at each sampling time and the need for voltage balancing circuit is eliminated. With lower number of power diodes compared to the classical five-level DCI, the proposed topology together with SVM technique allows better efficiency and enhance the performance of STATCOM.

5.2. Five-Level Multiple-Pole Multilevel Diode-Clamped STATCOM Converter

The five-level M2DCI presented in the previous chapter can be used as STATCOM converter, as shown in Figure 5. 1. Figure 5. 2 shows current model of STATCOM converter. From Figure 5. 2 the dc-link capacitor currents can be written as

$$\begin{aligned} i_{C2} &= i_{C1} + i_2 \\ i_{C3} &= i_{C2} + i_3 \\ i_{C4} &= i_{C3} + i_4 \end{aligned} \tag{5.1}$$

In general, the sums of the capacitor voltages are equal to the dc-link reference voltage of magnitude E_{dc} . Hence by applying KVL at the dc-link and then taking the derivative,

Figure 5. 1: Schematic of five-level multiple-pole multilevel diode-clamped STATCOM converter.

$$\frac{1}{C_1} i_{C1} + \frac{1}{C_2} i_{C2} + \frac{1}{C_3} i_{C3} + \frac{1}{C_4} i_{C4} = 0 \quad (5.2)$$

If all the capacitors are assumed to have equal capacitances, (5. 2) becomes

$$i_{C1} + i_{C2} + i_{C3} + i_{C4} = 0 \quad (5.3)$$

Then from (5. 1) and (5. 3), the current through the capacitors are calculated from mid-point currents as

Figure 5. 2: Current model of five-level multiple-pole multilevel diode-clamped STATCOM

$$i_{Cj} = \frac{1}{4} \sum_{x=1}^3 x i_{x+j} - \sum_{x=j+1}^4 i_x \quad \text{for } j=1,2,3,4. \quad (5.4)$$

And the mid-point currents are given by

$$\begin{aligned} i_2 &= (S_{A2} - S_{A1})i_A + (S_{B2} - S_{B1})i_B + (S_{C2} - S_{C1})i_C \\ i_3 &= (S_{A3} - S_{A2})i_A + (S_{B3} - S_{B2})i_B + (S_{C3} - S_{C2})i_C \\ i_4 &= (S_{A4} - S_{A3})i_A + (S_{B4} - S_{B3})i_B + (S_{C4} - S_{C3})i_C \end{aligned} \quad (5.5)$$

The detailed modeling of the converter and SVM based voltage balancing control have been presented in the previous chapter. The cost function used for implementing voltage balancing is given by

$$\sum_{j=1}^3 \Delta V_{Cj}(k) \left(\sum_{x=j+1}^4 \bar{i}_x \right) \geq 0 \quad (5.6)$$

The SVM based voltage balancing algorithm presented in the previous chapter will select the switching vector combination during each sampling interval and the converter switches are controlled in such a way that the voltage across the four dc-link capacitors are balanced at a reference value of $\left(\frac{E_{dc}}{4}\right)$.

From the stability plot (Figure 5. 3) obtained for five-level converter, it can be noted that, at low power factor operation, the SVM based balancing control eliminates the voltage

Figure 5. 3: Voltage balance limits for SVM based capacitor voltage balancing strategy of five-level M2DCI.

drift phenomena for a range of linear modulation index. Hence, it can be used for controlling the reactive power in transmission/distribution line.

5.3. STATCOM Modeling and Controller Design

STATCOM is a shunt connected reactive power compensator capable of generating or absorbing desired amount of reactive power at its ac terminals when an energy storage device is connected at its dc terminals. It consists of a VSC which generates desired three-phase voltages and currents from an energy-storage capacitor to improve power system

Figure 5. 4:: single-line diagram of five-level M2DCI based STATCOM connected to the ac system.

performance. In this paper five-level M2DCI is employed instead of conventional two-level VSC, which will also reduce the harmonic pollution of power system caused by addition of STATCOM into power system. Furthermore, STATCOM output is coupled to the ac system through a small reactance, as shown in Figure 5. 4.

5.3.1. Steady-State Model

The first-order differential equation for the ac-side of the system in Figure 5. 4 can be written as

$$\begin{aligned} p i_{sA} &= \frac{1}{L_s} (-R_s i_{sA} + V_{sA} - V_{LA}) \\ p i_{sB} &= \frac{1}{L_s} (-R_s i_{sB} + V_{sB} - V_{LB}) \\ p i_{sC} &= \frac{1}{L_s} (-R_s i_{sC} + V_{sC} - V_{LC}) \end{aligned} \quad (5.7)$$

where p is the (d/dt) operator and STATCOM terminal voltages can be defined as follows:

$$\begin{bmatrix} V_{sA} \\ V_{sB} \\ V_{sC} \end{bmatrix} = \frac{m E_{dc}}{\sqrt{3}} \begin{bmatrix} \sin(\omega t + \theta_1) \\ \sin\left(\omega t + \theta_1 - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \theta_1 + \frac{2\pi}{3}\right) \end{bmatrix} \quad (5.8)$$

From Figure 5. 5, the dc-side circuit equation is expressed as

$$p E_{dc} = \frac{-1}{C_{equ}} \left(I_{dc} + \frac{E_{dc}}{R_p} \right) \quad (5.9)$$

Figure 5. 5: Simplified equivalent circuit of STATCOM .

where R_p represents capacitor losses and switching losses and $C_{equ} = \frac{I}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$.

The ac-side equations are converted on a synchronous rotating reference frame using the transformation

$$\begin{bmatrix} f_{dq0} \end{bmatrix} = T \cdot \begin{bmatrix} f_{ABC} \end{bmatrix} \quad (5. 10)$$

where

$$T = \sqrt{2/3} \begin{bmatrix} \sin(\theta_{pcc}) & \sin\left(\theta_{pcc} - \frac{2\pi}{3}\right) & \sin\left(\theta_{pcc} + \frac{2\pi}{3}\right) \\ \cos(\theta_{pcc}) & \cos\left(\theta_{pcc} - \frac{2\pi}{3}\right) & \cos\left(\theta_{pcc} + \frac{2\pi}{3}\right) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}; \begin{bmatrix} f_{dq0} \end{bmatrix} = \begin{bmatrix} f_d & f_q & f_0 \end{bmatrix}^T,$$

$\begin{bmatrix} f_{ABC} \end{bmatrix} = \begin{bmatrix} f_A & f_B & f_C \end{bmatrix}^T$ and $\theta_{pcc} = \omega t + \theta_L$. Note that θ_L is the initial phase angle of PCC voltage V_L .

STATCOM terminal voltages and load terminal voltages in $d-q$ frame are given by

$$\begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \frac{mE_{dc}}{\sqrt{2}} \begin{bmatrix} \cos(\theta_1 - \theta_L) \\ \sin(\theta_1 - \theta_L) \end{bmatrix} \quad (5. 11)$$

$$\begin{bmatrix} V_{Ld} \\ V_{Lq} \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} V_{Lpeak} \\ 0 \end{bmatrix} \quad (5. 12)$$

V_{Lpeak} is the amplitude of PCC voltage V_L . (5. 7) is converted in to $d-q$ reference frame

as follows:

$$\begin{bmatrix} p i_{sd} \\ p i_{sq} \end{bmatrix} = \begin{bmatrix} -R_s/L_s & \omega \\ -\omega & -R_s/L_s \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \frac{1}{L_s} \begin{bmatrix} V_{sd} - V_{Ld} \\ V_{sq} - V_{Lq} \end{bmatrix} \quad (5. 13)$$

The power balance equation of the converter is given by

$$E_{dc} I_{dc} = (V_{sd} \times i_{sd} + V_{sq} \times i_{sq}) \quad (5.14)$$

Substituting (5. 11) in (5. 14),

$$I_{dc} = \frac{m}{\sqrt{2}} [\cos(\theta_l - \theta_L) i_{sd} + \sin(\theta_l - \theta_L) i_{sq}] \quad (5.15)$$

The dc-side circuit equation expressed in (5. 9) can be modified to

$$pE_{dc} = \frac{-1}{C_{equ}} \left(\frac{m}{\sqrt{2}} [\cos(\theta_l - \theta_L) i_{sd} + \sin(\theta_l - \theta_L) i_{sq}] + \frac{E_{dc}}{R_p} \right) \quad (5.16)$$

5.3.2. STATCOM Control

The i_{sd} and i_{sq} are coupled with each other through an inductive reactance as presented in the state-space model of STATCOM given in (5. 13). To provide a decoupled control, the STATCOM terminal voltage vector is controlled as follows:

$$\begin{aligned} V_{sd} &= -\omega L_s i_{sq} + V_{Ld} + L_s V_{sd}^* \\ V_{sq} &= \omega L_s i_{sd} + V_{Lq} + L_s V_{sq}^* \end{aligned} \quad (5.17)$$

Substituting (5. 17) and (5. 12) in (5. 13) gives

$$\begin{bmatrix} p i_{sd} \\ p i_{sq} \end{bmatrix} = \begin{bmatrix} -R_s/L_s & 0 \\ 0 & -R_s/L_s \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \begin{bmatrix} V_{sd}^* \\ V_{sq}^* \end{bmatrix} \quad (5.18)$$

The corresponding transfer function is

$$G_s(s) = \frac{I_{sd}(s)}{V_{sd}^*(s)} = \frac{I_{sq}(s)}{V_{sq}^*(s)} = \frac{1}{s + (R_s/L_s)} \quad (5.19)$$

Two independent PI controllers can be used to produce the control signals V_{sd}^* and V_{sq}^* , as shown by (5. 20).

The STATCOM control defined in (5. 17) is implemented and the block diagram is shown in Figure 5. 6.

$$\begin{aligned} V_{sd}^* &= K_{pd} (i_{sd}^* - i_{sd}) + K_{id} \int (i_{sd}^* - i_{sd}) \\ V_{sq}^* &= K_{pq} (i_{sq}^* - i_{sq}) + K_{iq} \int (i_{sq}^* - i_{sq}) \end{aligned} \quad (5.20)$$

The STATCOM is used to compensate for the reactive power required by the load at PCC, so that ac power system does not have to supply the load's reactive power demand.

The reactive current reference i_{sq}^* is obtained from quadrature component of load current and the dc-link voltage control loop provides the direct axis current reference i_{sd}^* to regulate dc-link voltage of the STATCOM to its reference magnitude.

5.4. Performance Evaluation of Five-level M2DCI STATCOM

The reactive power compensation of ac system in transient and steady-state conditions is achieved by controlling the five-level M2DCI as described in Figure 5. 6. The performance of the proposed system is evaluated using Matlab/Simulink® and PSIM for various operating conditions. The circuit and controller parameters are given in Table 5. 1.

Table 5. 1: Control Parameters of the System

UTILITY	
SOURCE VOLTAGE, V_{GAB}	190.52V
RESISTANCE, R_G	0.5Ω
REACTANCE, X_{LG}	0.031 Ω
supply frequency, f	50Hz
STATCOM	
dc-link voltage, E_{dc}	400V
dc-link capacitor, C_j , j=1,2,3,4.	8800uF
inductor reactance, X_{LS}	1.57 Ω
inductor resistance, R_s	0.9 Ω
sampling Frequency, f_s	2.5kHz
PI CONTROLLERS	
dc-link voltage controller	$K_p=1;K_i=30$
d-axis current loop controller	$K_{pd}=2.5;K_{id}=25$
q-axis current loop controller	$K_{pq}=10;K_{iq}=200$

Figure 5. 6: Control scheme for five-level M2DCI based STATCOM connected to the ac system.

5.4.1. Performance of STATCOM with Inductive Load

The system in Figure 5. 4 is initially at no-load and STATCOM connected to the grid supplies no reactive power. At 0.1s a balanced three-phase load of value $R_L/\text{phase}=1.4\Omega$ and $L_L/\text{phase}=22\text{mH}$ (load PF=0.47) is connected and the system response to the reactive power change is shown in Figure 5. 7. Figure 5. 7.(a) shows, the individual capacitor voltages when 400V is given as dc-link voltage reference. The control algorithm provides a balanced voltage of magnitude 100V across the dc-link capacitors and M2DCI line-to-line voltage shown in Figure 5. 7.(b) has 9 distinct levels due to increase in modulation index. Since the reactive current is provided by the STATCOM, the grid voltage and current waveforms are in-phase with each other and are shown in Figure 5. 7.(c). The reference reactive current component and the STATCOM reactive current component are shown in Figure 5. 7.(d). The STATCOM delivers the reactive current demand of the load and hence the source reactive current component is zero as shown in Figure 5. 7.(e).

5.4.2. Step change from Lagging to Leading Load

Figure 5. 8 shows the system performance with a change in load from lagging to leading at 0.4s. When the load is changed at 0.4s the compensating current tracks the reference and the SVM based balancing control gives balanced voltage across the dc-link capacitors. Figure 5. 8.(a) and (b) show the individual dc-link capacitor voltages while Figure 5. 8.(c) shows grid voltage and current in phase-A. The STATCOM controller generates the desired reactive current component such that it maintains unity power factor at the grid after change in load. The reactive current component of STATCOM and grid are shown in Figure 5. 8.(d) and (e), respectively.

5.4.3. With Unbalanced Source Condition

To verify the effectiveness of the proposed voltage balancing control strategy during unbalanced source condition, three-phase source voltage of amplitudes $V_{gA} = 147.78\text{V}$,

Figure 5. 7: System response for an addition of inductive load at 0.1s.

- (a) DC-link capacitor voltages V_{Cj} for $j=1, 2, 3, 4$
- (b) Line voltage of M2DCI, V_{AB}
- (c) Grid voltage V_{gA} and grid current I_{gA} in phase 'A'
- (d) STATCOM reactive current component i_{qs}
- (e) Grid reactive current component, i_{qg}

$V_{gB} = 155.55\text{V}$ and $V_{gC} = 163.32\text{V}$ (Figure 5. 9.(c)) is applied with the same conditions

Figure 5. 8: System response for a step change in load from lagging to leading at 0.4s.

- (a) DC-link capacitor voltages V_{Cj} for $j=1, 2, 3, 4$
- (b) Zoomed waveforms of dc-link capacitor voltages
- (c) Grid voltage V_{gA} and grid current I_{gA} in phase 'A'
- (d) STATCOM reactive current component i_{qs}
- (e) Grid reactive current component, i_{qg}

described in section 5.4.1. The dc-link capacitor voltages V_{C1} , V_{C2} , V_{C3} , and V_{C4} are shown in Figure 5. 9.(a). DC-Link capacitor voltages converge to steady state value of 100V which ensures that balancing algorithm eliminates the voltage drift phenomena in M2DCI even for

some unbalanced source conditions. Grid voltages are shown in Figure 5. 9.(b). The grid voltage and current waveforms are in-phase with each other and are shown in Figure 5. 8.(c). The reactive current component of STATCOM and source are shown in Figure 5.9.(d) and (e) respectively. The ripple present in the respective reactive current component compared to Figure 5.7 (d) and (e) are due to the imbalance in source voltages.

5.4.4. Change in Linear Load from Balanced to Unbalanced

To verify the effectiveness of the proposed voltage balancing control strategy during unbalanced load currents, the load at the PCC is changed from balanced to unbalanced at 0.4s. And the corresponding system response is shown in Figure 5. 10. Though there is a change in load at 0.4s, the capacitor voltages remain stable and balanced around 100V and the M2DCI line-to-line voltage has 9 distinct levels. The low frequency oscillations present in the reactive current components shown in Figure 5. 10.(e) and (f) after 0.4s is due to unbalanced load currents.

5.4.5. Change in Balanced Load from Linear to Non-linear

Prior to 0.4s, the operating condition of the system shown in Figure 5. 4 is as described in section 5.4.1(Performance of STATCOM with Inductive Load). At 0.4s, three-phase non-linear load is also connected to the system which generates some harmonics in load currents (Figure 5. 11.(c)). The system response due to the change in load is shown in Figure 5. 11. The individual dc-link capacitor voltages shown in Figure 5. 11.(a) remain stable and balanced and the M2DCI line-to-line voltage given in Figure 5. 11.(b) has 9

Figure 5. 9: System response for unbalanced source condition.

- (a) DC-link capacitor voltages V_{Cj} for $j=1, 2, 3, 4$.
- (b) Grid voltage waveforms, V_{gA} , V_{gB} and V_{gC}
- (c) Grid voltage V_{gA} and grid current I_{gA} in phase 'A'
- (d) STATCOM reactive current component i_{qs}
- (e) Grid reactive current component, i_{qg}

Figure 5. 10: System response for a change in load from balanced to unbalanced at 0.4s..

- (a) DC-link capacitor voltages V_{Cj} for $j=1, 2, 3, 4$
- (b) Line voltage of M2DCI, V_{AB}
- (c) Load current waveforms i_{LA} , i_{LB} and i_{LC}
- (d) Grid voltage V_{gA} and grid current i_{gA} in phase 'A'
- (e) STATCOM reactive current component i_{qs}
- (f) Grid reactive current component, i_{qg}

distinct levels. The STATCOM delivers the reactive power demand of the load and provides unity displacement power factor at the source as shown in Figure 5. 11.(d)-(f).

Figure 5. 11: System response for a step change in balanced load from linear to non-linear at 0.4s.

- (a) DC-link capacitor voltages V_{Cj} for $j=1, 2, 3, 4$
- (b) Line voltage of M2DCI, V_{AB}
- (c) Load current waveforms i_{LA} , i_{LB} and i_{LC}
- (d) Grid voltage V_{gA} and grid current i_{gA} in phase 'A'
- (e) STATCOM reactive current component i_{qs}
- (f) Grid reactive current component, i_{qg}

5.5. Conclusion

Multilevel inverter based STATCOM configuration is preferred over two-level VSC due to several advantages such as improved power quality, and high efficiency utilizing devices of smaller power ratings to connect directly to the grid in high power conversions. The proposed five-level M2DCI based STATCOM greatly reduces the number of power diodes compared to the classical five-level DCI. The SVM based voltage balancing strategy presented in the work reduces the number of calculations required at each sampling period by predicting the dc-link capacitor current. The performance of the five-level M2DCI based STATCOM in transient and steady-state conditions, for example: balanced, unbalanced and no-linear operating conditions were evaluated using Matlab/Simulink® and PSIM environments. Results ensure that, the voltage balancing control maintains balanced voltage across dc-link capacitors in all operating conditions. The proposed methodology provides better efficiency and enhances the performances of the STATCOM.

Conclusions and Recommendations

6.1. Conclusions of the Thesis

The research work presented in this thesis mainly focused on neutral point clamped multilevel inverter (NPC) and space vector based modulation technique. The major contributions of the research carried out in this thesis are

- Time-domain analysis of three-level DCI is carried out to derive an expression for neutral point current. It can be seen that the neutral point current is a function of modulating signal amplitude, amplitude of the load current, initial phase angle of voltage and the power factor angle. It can be used for developing NPP control scheme.
- DC-Link capacitor voltage balancing scheme for three-level DCI configuration using LS-PWM and SVM techniques are compared and verified experimentally.
- Switching function model of the five-level M2DCI is derived. Hence the dc-link capacitor currents can be predicted from the load current values for any valid inverter switching states. This will significantly reduce the computational steps while implementing SVM based voltage balancing strategy for the five-level M2DCI.
- A five-level SVM scheme with dc-link capacitor balancing is presented which require lower computational efforts compared to conventional sector-based techniques. With the proposed method, there is at least 30% reduction in number of calculations and contains no comparisons.
- SVM-based voltage balancing strategy is implemented for a new five-level multiple-pole multilevel diode clamped inverter (M2DCI) and the stability plot is verified

using both simulation and hardware results at various load conditions. And with the proposed method THD of output voltage was improved.

- It is observed that the operation range for the proposed balancing technique is not sufficient when power factor is high. And it can be suitable for applications that involve reactive power.
- The performance of five-level M2DCI for STATCOM application using the proposed SVM with lower computational requirement is evaluated during transient and steady-state operating conditions.

6.2. Recommended for Future Work

The SVM algorithm presented in Chapter 4 can be tested for back-to-back high-voltage direct-current (HVDC) converter system by using five-level M2DCI configuration. The five-level M2DCI based HVDC converter will greatly reduce the number of power diodes compared to the classical five-level DCI. Furthermore, the need for any auxiliary power circuit and control methods are eliminated by implementing SVM based voltage balancing strategy which provides a balanced voltage across the four dc-link capacitors.

The back-to-back five-level M2DCI configuration, with suitable modification of SVM based balancing strategy can be used for medium-voltage, variable-frequency AC drives used in cement plants, oil and gas industry, mining application, power generation utility industry and steel plants. The conventional drive consists of an input transformer with phase-shifted secondary windings connected to diode-bridge rectifiers. The output of the rectifier is given to a single phase inverter through the dc-bus and supplies the power to the motor. With The back-to-back five-level M2DCI configuration, the input transformer and the inverter cell module (diode rectifier and inverter) can be eliminated. Also, the front end rectifier can be controlled using SVM technique for providing balanced voltage across the dc-link capacitors.

The objective of the STATCOM presented in the thesis is to supply the reactive power required by the load. In order for STATCOM to work as a harmonic compensator it

has to deal with active component of current. The operation range for the proposed balancing technique is not sufficient when power factor is high. However, this may require extensive analysis which can be considered for future research work.

Author's Publications

Conference

- [1] A. I. Maswood, P. H. Raj, and P. L. A. Vu, "Efficiency of silicon carbide based power inverters- analytical results," in *Developments in Renewable Energy Technology (ICDRET), 2012 2nd International Conference on the*, 2012, pp. 1-4.
- [2] P. H. Raj ,A. I. Maswood,and Venkataraman, A., "Space vector based field oriented control of Permanent Magnet Synchronous motor with a 3-Level Scheme.", *IEEE Transportation Electrification Conference and Expo (ITEC)*,2013. vol., no., pp.1,6, 16-19 June 2013
- [3] P. H. Raj, A. I. Maswood, Gabriel Ooi H.P, and Ziyou Lim, "Analysis of 3-Level Inverter Scheme with DC-Link Voltage balancing using LS-PWM & SVM Techniques", *ICRERA 2013*. vol., no., pp.1036,1041, 20-23 Oct. 2013.
- [4] P. H. Raj , A. I. Maswood, Gabriel Ooi H.P, and Hossein Dehghani Tafti, "Multiple-Pole Multilevel Diode Clamped Inverter for Permanent Magnet Synchronous Motor Drive" in *IEEE International Conference on Power Electronics and Drive Systems (PEDS) 2015* , accepted for publication.
- [5] Hossein Dehghani Tafti, Ali I. Maswood, Ziyou Lim, Gabriel H. P. Ooi, and P. H. Raj, "NPC Photovoltaic Grid-Connected Inverter with Ride-Through Capability under Grid Faults" in *IEEE International Conference on Power Electronics and Drive Systems (PEDS) 2015* , accepted for publication.
- [6] Hossein Dehghani Tafti, Ali I. Maswood, Ziyou Lim, Gabriel H. P. Ooi , and P. H. Raj, "Proportional-Resonant Controlled NPC Converter for More-Electric-Aircraft Starter-Generator" in *IEEE International Conference on Power Electronics and Drive Systems (PEDS) 2015* , accepted for publication.

- [7] P. H. Raj , A. I. Maswood, and Gabriel Ooi H.P, "Five-Level Multiple-Pole Multilevel Diode-Clamped Inverter Scheme for Reactive Power Compensation" in *IEEE PES Innovative Smart Grid Technologies in Asia 2015 Bangkok International Conference (ISGT Asia 2015 Bangkok)*, submitted.
- [8] P. H. Raj , A. I. Maswood, Ziyu Lim, and Venkataraman, A., "A Space Vector Modulated 5-Level Multiple-pole Multilevel Diode Clamped Based STATCOM Application". *Asia Clean Energy Summit 2015*. Submitted.

Journal

- [1] P. H. Raj, A. I. Maswood, G. H. Ooi, and Z. Lim, "Voltage balancing technique in a space vector modulated 5-level multiple-pole multilevel diode clamped inverter," *Power Electronics, IET*, vol. 8, pp. 1263-1272, 2015.
- [2] P. H. Raj, A. I. Maswood, and G. H. Ooi, "Space Vector Modulated Five-level Multiple-pole Multilevel Diode Clamped Inverter Based STATCOM," *IEEE Transactions on Energy Conversion* . Submitted for publication.

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