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Jiang, Yushan

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**A CMOS LOW DROPOUT REGULATOR FOR
INTERNET OF THINGS**

JIANG YUSHAN

**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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ABSTRACT

With the growing demand of portable devices or the emergence of Internet-of-Things (IoT) applications, the push for small-size and ultra-low-power Low Dropout (LDO) Regulators becomes the key design agenda. Unfortunately, when approaching ultra-low power, the transient performance metrics of the regulator are often significantly reduced. Moreover, the parasitic poles of regulator's devices, which are located at low frequencies, can lead to the instability issue. As such, these undesirable effects pose the serious design challenges in the context of ultra-low quiescent power design constraints.

To tackle the stated problems, an ultra-low quiescent power capacitorless LDO regulator is proposed with employment of the transistor degeneration frequency compensation (TDFC) in the adaptive frequency compensation scheme. It can deliver a full loading current range from 0 to 100 mA and provide a 1 V output voltage from a 1.2 V power supply at a capacitive load of 100 pF whilst consuming only 407 nA for the entire regulator architecture. The total on-chip capacitance is 6.5 pF. On top of that, a distributed overshoot reduction (DOVSR) topology is also proposed to tackle the overshoot reduction problem under ultra-low quiescent circuit design. By incorporating the TDFC scheme and the feedforward biasing design, this results in reduced settling time and overshoot voltage with respect to that of the conventional circuit technique.

The proposed design was fabricated using CMOS 0.18 μm technology for proof of concept. The measurement results have shown that the regulator output can settle within 1.56 μs with 35.33 mV in overshoot voltage at a load current transition step from 0 A to 100 mA. Besides, through the use of adaptively-biased design in conjunction with multiple loop feedback architecture, the undershoot voltage attains 117 mV despite of very limited regulator's system bandwidth at ultra-low quiescent biasing state. The regulator has achieved the output-capacitorless based transient Figure-of-Merit (FOM) of 1.42 mV and output capacitor based transient FOM of 0.475 fs, demonstrating that it can offer excellent transient performance even under

ultra-low quiescent biasing condition and zero minimum load current. Furthermore, the proposed work also achieves comparable result in terms of undershoot/overshoot voltage, settling time, PSR and so forth. The performance comparison has validated that the regulator outperforms that of the representative reported works, advancing state-of-the-art result.

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Chapter 1 Introduction

1.1 Motivations

Nowadays, Internet of Things (IoT) is also rising rapidly, it integrates the technologies of computer science, communication and hardware [1]. As an important part, the front-end hardware layer which is shown in Figure 1.1 illustrates various integrated circuit (IC) blocks in the IoT System-on-Chip (SoC). It features the sensing layer consist of physical devices [2], sensors, actuators [3], [4] , RFID and so forth. They are responsible of sensing and actuating functions, which includes sensing information, performing environmental monitoring on factors such as humidity, motion, blood pressure, temperature, computing function through data acquisition [5] and so on. Processing units process data and information. Communication layer which may make use of Wi-Fi, 4G/5G and so forth, can transmit and receive data to or from either the cloud or the users. Among the blocks, the power management unit (PMU) are delivering the necessary power to the respective blocks.

Figure 1.1 Block diagram of the IoT interface networking [1]–[8]

The front-end sensing devices together with built-in electronic interfaces often require a quality power supply with features of less noise and ripple [9]. The PMUs in each case supports the important devices like sensors, microprocessors and so

forth, as shown in Figure 1.1. Due to the need to detect minute change of physical signals, these devices are very sensitive to power supply noise. To further illustrate another IoT example, Figure 1.2 shows a low-power integrated system for environmental monitoring.

Figure 1.2 Exemplary ultra-low power regulator dedicated to energy harvesting based sensor system for environmental monitoring application [9]

As seen from Figure 1.2, the primary power supply which is generated by the energy harvesting power source presents noise as well as ripple. Therefore, a clean and highly-stable regulated supply is imperative to avoid the potential errors during measurements in potential harsh environment. Although the voltage reference can provide an accurate voltage with low power consumption, but its load current is quite limited. In order to tackle the stated problem, the DC-DC converter becomes another choice in the PMU design due to its merit on good efficiency but at the expense of external filter components. The DC-DC converter can provide a DC supply as well as a large range of load current. However, based on the switching mode operation, the subsequent circuit will suffer from the switching noise, which is undesirable for the noise-sensitive circuits such as sensors and front-end interfaces. Besides, the usual large time-constant output filter associated with the DC-DC converter will hinder its response time to electronic circuits. To tackle both the noise and response time issues whilst maintaining good efficiency, a DC-DC converter incorporating a

LDO regulator, as shown in Figure 1.3, is usually adopted as a popular solution in PMU design.

Figure 1.3 LDO regulator application example

Refer to Figure 1.3, a LDO regulator can support the specific subsystems with fast load current transitions or switchings. As such, it avoids large voltage fluctuations in high performance applications. Therefore, a LDO regulator turns out to be a reliable source to provide a clean supply to the noise-sensitive subsystems. At the same time, it can offer small size due to its simple topology.

As stated above, there is a significant push on the application-driven LDO regulators dedicated to IoT system, mixed-signal system [10] and low-power mobile battery system devices like mobile phones, tablets, wearable devices, biomedical implantable devices [11] and so forth. Their common main features are to meet the requirements for low-power, low supply voltage and low-dropout voltage in order to maintain good efficiency. Turning to LDO regulators' pertaining to IoT applications such as Wireless Sensor Network (WSN), smart sensor technologies and so forth, both power consumption and miniaturization [8] are regarded as the key factors to be addressed in power management system.

Various issues are addressed in the research of the LDO regulators. Firstly, in conventional LDO regulator design, a large output capacitor can be in μF level [12]–[13]. The purposes of using the large off-chip capacitor are to ensure the stability through the generation of Equivalent Series Resistor (ESR) zero from the capacitor

and to reduce the spike at the output by serving as a charging or discharging reservoir. However, the large off-chip capacitor requires an external capacitor component to be implemented, causing an extra pin and the increase of cost. These drawbacks are unfavorable for embedded systems such as ultra-low power biomedical implants and wearable devices. Therefore, the output capacitor-less LDO (OCL-LDO) regulators [11]–[28] have received much attention, especially in the IoT applications.

Secondly, the current development on LDO regulator also focuses on minimizing power consumption down to 1- μ A level for system operating at green mode or stand-by mode [34], whilst aiming to achieve good performance metrics. Since the operation time can be significantly extended in view of applications such as thermostats, security system and MCUs because they stay in idle state in majority of time [35] whilst the low-quiescent LDO regulator benefits the low-current consumption system.

Figure 1.4 Loop Responses of a multi-stage LDO regulator under different biasing currents

Unfortunately, when pushing for ultra-low power and output capacitorless designs, stability and transient performance will be significantly degraded. In this scenario, all poles and zeros are easily located at lower frequencies and close to each other. Refer to Figure 1.4, reducing biasing current and load current will result in a left

shifting of poles and zeros. Furthermore, complex poles [36] may be introduced, leading to the drop of phase margin. Both cases will degrade the overall stability of the feedback system. Another issue is that the settling time will be substantially increased due to smaller bandwidth, resulting in longer response time. Besides, the output voltage spikes may suffer from the difficulty to settle well within the tolerance, leading to the inaccuracy of the output voltage. These problems will cause the regulator to operate unreliably which contributes potential errors in the subsequent system. Finally, the LDO regulator may suffer from poor PSR performance due to lower loop gain and poor frequency response [9]. These raise the motivation of this project for the investigation of a sub-1 μA level output-capacitorless LDO regulator that addresses the above stated problems.

1.2 Objectives and Scope

The objectives of the work are to design, analyze, implement and test an output capacitor-less LDO regulator with fast transient whilst consuming ultra-low quiescent current at the no-load current condition. More importantly, stability is addressed over the whole load current range. The AMS CMOS 0.18 μm technology process design kit (PDK) together with the Cadence tool is used in the project. The design specifications of this work are stated in Table 1.1.

Table 1.1 Specifications of proposed LDO regulator

Parameter	Specification
Supply Voltage, V_{DD} (V)	1.2
Output Voltage, V_{OUT} (V)	1
Dropout Voltage, V_{DO} (mV)	200
Quiescent Current (μA)	< 1
Maximum Load Current, $I_{L(MAX)}$ (mA)	100
Minimum Load Current, $I_{L(MIN)}$ (mA)	0
Load Capacitance Range, C_L (pF)	0 - 100pF
Settling time (μs)	< 3

The design scope of the regulator aims to achieve a typical 200 mV dropout voltage under a supply voltage of 1.2 V. At the same time, the regulator can provide a maximum load current of 100 mA and dissipates the quiescent current of less than 1 μA whilst attaining a settling time less than 3 μs . Besides ultra-low quiescent current consumption, the minimum load current is required to start from 0 mA. This poses the design challenge, particularly the stability concern of LDO regulator at both the ultra-low quiescent bias current and zero minimum load current criteria.

1.3 Contributions

The key contributions are stated as follows:

- (1) An adaptive frequency compensation technique is proposed for an improved adaptive-stage based LDO regulator architecture. This involves the new transistor degeneration frequency compensation (TDFC) topology in the adaptively-biased input differential stage, the Q-reduction frequency compensation between the second adaptively-biased non-inverting gain stage and the differential input stage and the Miller-RC frequency compensation in the power-transistor stage.
- (2) A distributed overshoot reduction (DOVSR) circuit is proposed to reduce the settling time from that of conventional overshoot reduction circuit.
- (3) The employment of feedforward topology between the differential input stage and the second non-inverting gain stage to reduce the biasing branch for saving quiescent power of LDO regulator.
- (4) The design, analysis, implementation and testing of the chips are conducted for proof-of-concept.

1.4 Organization

Chapter 1 presents the motivations, objectives and scope, organization and contributions of the report.

Chapter 2 reviews the fundamental issues in the LDO regulator. This covers the key performance parameters, the prior-art works of LDO regulators and the commonly-used frequency compensation techniques in regulator design.

Chapter 3 presents the CMOS circuit implementation of each sub-block. This includes the core circuit topology of proposed LDO regulator using adaptive frequency compensation and the biasing circuit.

Chapter 4 focuses on the stability analysis of proposed LDO regulator. This includes derivation of the respective transfer function at different load current conditions in the feedback system together with the verification of the system loop stability through the simulation study.

Chapter 5 presents the simulation results and discussions. This includes the investigation of transient responses under different loading conditions together with other key performance metrics pertaining to the LDO regulator. Besides, the proposed distributive overshoot reduction circuit and the adaptive frequency compensation technique are shown to compare with the conventional counterparts.

Chapter 6 presents the measured results. Discussions on the performance comparison is conducted with the state-of-art reported works.

Chapter 7 gives the concluding remarks and future works.

Chapter 2 Literature Review

This Chapter will firstly review the conventional LDO regulator and its key performance parameters. This is then followed by the review of different low-quiescent current LDO regulators such as Flipped-Voltage-Follower (FVF) LDO regulator, dynamically-biased, assistant push-pull and adaptive-stage LDO regulators. Apart from that, the commonly-used frequency compensation techniques in LDO regulator design will be reviewed. Finally, other key circuit and layout issues pertaining to the LDO regulator design are also described.

2.1 Conventional LDO Regulator

A conventional LDO regulator consists of a biasing circuit, a reference voltage, an error amplifier, a power transistor and a feedback network. Figure 2.1 has shown the block diagram of a conventional LDO regulator [12].

Figure 2.1 Conventional LDO regulator [12]

In a conventional LDO regulator, the feedback network will sense any variation at the output. The error amplifier will generate an error signal by comparing the feedback signal and the constant voltage reference. The power transistor will adjust its transconductance according to the load current and the error signal. In this way, the output voltage will be stabilized from the variation. In the whole regulation process, the LDO regulator will keep the output voltage close to the reference voltage whilst providing a range of load current, irrespective of the environment, arising from the change of supply voltage and transitions of load current.

In this architecture, the output variation can be suppressed by the big output capacitor C_O during load current transitions. On top of that, the output capacitor will ensure the stability by defining the low-frequency dominant pole. Since the output capacitor is usually in several μF level, the regulator needs an external capacitor, thus increasing the cost and an extra output pin to accommodate the external capacitor.

2.2 Key Performance Specifications

To further explore the performance metrics, the following key performance specifications are presented with discussion.

2.2.1 Dropout Voltage

The dropout voltage of LDO regulators is defined as the minimum voltage difference between the unregulated supply V_{DD} with the output voltage V_{OUT} [12]. The dropout voltage V_{DO} can also be described as a voltage drop from supply to the output node of regulation, which is stated as follows:

$$V_{DO} = V_{DD} - V_{OUT} = I_L \times R_{ON} \quad (1)$$

where R_{ON} is the equivalent switch-on resistance at the output or the regulation node.

2.2.2 Line Regulation and Power Supply Rejection (PSR)

Line regulation performance refers to a steady-state (dc) variation of output voltage, which arises from dc change in power supply voltage. Line regulation is defined as follows [12]:

$$LNR = \frac{\Delta V_{OUT}}{\Delta V_{DD}} \quad (2)$$

Power supply rejection (PSR) measures the ability of the circuit to reject variation of supply in a whole spectrum range. PSR is usually quoted at a dc frequency or at a specified frequency (e.g. 1 kHz). The sources of the variation include the direct supply of the regulator and the indirect source through the voltage reference. PSR_{REF} induced by voltage reference is assumed better than that of the direct supply.

2.2.3 Load Regulation

Load regulation refers to the dc variation of output voltage arising from the change of output load current I_L . The performance can be measured by load-regulation resistance R_{LDR} described in [12] as follows:

$$\text{LDR} = R_{\text{LDR}} = \frac{\Delta V_{\text{OUT}}}{\Delta I_{\text{L}}} = R_{\text{O-REG}} + R_{\text{PAR}} = \frac{r_{\text{OP}}}{1 + A_{\text{OL}}\beta} + R_{\text{PAR}} \quad (3)$$

where $R_{\text{O-REG}}$ is the closed-loop output resistance of regulated loop [12], r_{op} is the open-loop output resistance, A_{OL} is the open-loop gain and β is the closed-loop feedback factor[12].

R_{PAR} is related to the devices' parasitic parameters, which includes resistance induced by PCB. According to (3), reducing PCB resistance will help the load regulation. However, increasing A_{OL} is the main solution to reduce load regulation.

2.2.4 Temperature Drift

The temperature changes will cause variations at the output of regulator. The variation is measured by temperature coefficient. It can be introduced by the reference voltage and the input-referred offset voltage of the regulator when the temperature changes. The temperature coefficient (T.C.) [12] is calculated as follows:

$$\text{T.C.} = \frac{1}{V_{\text{OUT}}} \left(\frac{dV_{\text{OUT}}}{dT} \right) \approx \frac{1}{V_{\text{OUT}}} \left(\frac{\Delta V_{\text{OUT}}}{\Delta T} \right) \quad (4)$$

2.2.5 Efficiency

Current efficiency η_{I} [12] is one of the vital parameters of the regulator. It can be described as follows:

$$\eta_{\text{I}} = \frac{I_{\text{L}}}{I_{\text{TOTAL}}} = \frac{I_{\text{L}}}{I_{\text{L}} + I_{\text{Q}}} \quad (5)$$

The total power dissipated by the regulator includes the output power $V_{\text{OUT}}I_{\text{L}}$, the power $(V_{\text{IN}} - V_{\text{OUT}})I_{\text{L}}$ dissipated in power transistor by load current and the power $V_{\text{IN}}I_{\text{Q}}$ dissipated by quiescent current I_{Q} . Power efficiency can be further derived to obtain a relationship between the input supply and the output. The efficiency [12] is defined as follows:

$$\eta = \frac{V_{OUT} I_L}{V_{OUT} I_L + (V_{IN} - V_{OUT}) I_L + V_{IN} I_Q} = \frac{V_{OUT} \eta_I}{V_{IN}} \quad (6)$$

According to (6), power efficiency firstly is largely dependent on the dropout voltage, which relies on the difference between supply and output voltage. The efficiency usually plays an important role which will determine the battery life in portable applications. For example, a cellular phone will be at idle state in most of the time and with a very short burst time for operation during talking on the phone [12]. Therefore, minimizing the quiescent current at zero-to-low loading condition is vital for prolonging the battery life.

2.2.6 Transient Response

Due to switching load current conditions, the output will suffer from variation in transitions. The worst case is that of a sudden transition of load current from zero to the peak I_{LMAX} , and vice versa. The typical transient behavior of a LDO regulator when facing a sudden step change is depicted in Figure 2.2 [12].

Figure 2.2 Typical transient behavior of a LDO regulator

The transient output variation ΔV_{TR} refers to the larger value of ΔV_{TR+} and ΔV_{TR-} . ΔV_{TR+} and ΔV_{TR-} denote the undershoot voltage V_{UNS} and overshoot voltage V_{OVS} respectively. The undershoot voltage is generated by a positive load current step.

Upon a sudden rise of load current, the regulator will not response immediately. This causes a discharge of the capacitor at the output node. Thus, an undershoot will happen. The response time [12] is approximated as

$$\Delta t_1 \approx \frac{1}{BW_{CL}} + C_{PAR} \left(\frac{\Delta V_{PAR}}{I_{SR}} \right) \approx \frac{1}{BW_{CL}} + C_{PAR} \left(\frac{\Delta I_L}{g_{mMP} I_{SR}} \right) \quad (7)$$

where g_{mMP} is the transconductance of power transistor, BW_{CL} is the closed-loop bandwidth, C_{PAR} is the parasitic capacitance that appears at the gate of the large power transistor, I_{SR} is the slewing current that slews the parasitic capacitance C_{PAR} [12].

It can be observed that Δt_1 is related to the reciprocal of the closed-loop bandwidth [12]. Besides, it is also related to the internal slew rate at the gate parasitic of the power transistors. Turning to the settling time Δt_2 of undershoot, it depends on the phase margin of the closed-loop frequency response [12].

During a negative load current step, the regulator continues to source current until the loop responses for regulation, which results in a charge accumulation at output node. During the process, the output variation ΔV_2 [12] is described as follows:

$$\Delta V_2 \approx \frac{I_{LMAX}}{C_{OUT}} \Delta t_3 \approx \frac{I_{LMAX}}{C_{OUT}} \times \frac{1}{BW_{CL}} \quad (8)$$

The time Δt_3 [12] that the regulator takes to stop the source current is approximated as

$$\Delta t_3 \approx \frac{1}{BW_{CL}} \quad (9)$$

Finally, the response time Δt_4 [12] to discharge the output capacitor is obtained as

$$\Delta t_4 \approx C_{OUT} \times \frac{\Delta V_2}{I_{PULL-DOWN}} \quad (10)$$

where $I_{PULL-DOWN}$ is the discharge current at the LDO regulator output.

From (7) - (10), it is clear that a larger closed-loop bandwidth, a large output capacitor and large charging and discharging current at each node will provide the benefit for a smaller output voltage variation, smaller settling and response time.

2.2.7 Figure-Of-Merits (FOMs)

As discussed in the above performance parameters, in order to achieve good line and load regulation, a larger loop gain is preferred. In transient performance, the maximum load current is proportional to the output voltage spikes. To reduce both output voltage spike and settling time, a larger closed-loop bandwidth and large output capacitor is preferred as well as large charging and discharging current at each node. First of all, large output capacitor is not suitable for SoC applications due to area occupation. Secondly, large gain and large bandwidth cannot be achieved concurrently due to the limitation of finite GBW. In addition, the broad bandwidth requires increase of quiescent current to increase the g_m of each gain stage. To maintain certain loop gain at ultra-low quiescent current criteria, poles and zeros will be located to lower frequency. This will cause the potential stability problem. The above stated problems will contribute the design challenges in the design of ultra-low quiescent LDO regulator.

In order to evaluate the overall transient performance of the regulator, several transient Figure-of-Merits (FOMs) are introduced. They are given as follows:

- a) A common FOM [30] dedicated to output capacitor-less LDO regulator design is given as

$$\text{FOM}_1 = K \left(\frac{\Delta V_{\text{OUT}} \times I_Q}{\Delta I_L} \right) \quad (11)$$

$$K = \frac{t_{\text{edge}} \text{ used in the measurement}}{\text{the smallest } t_{\text{edge}} \text{ among designs for comparison}} \quad (12)$$

where K is the ratio of edge time in the proposed design with respect to the minimum edge time among the designs in the comparison [37]. ΔV_{OUT} denotes the larger value of undershoot and overshoot voltage. This FOM focuses on quiescent current consumption, output load current step as well as the worst voltage spike from either undershoot or overshoot voltage. A smaller FOM indicates a better performance metric. Therefore, minimizing quiescent current

and small output voltage variation whilst supporting large current step are the key parameters for this FOM.

b) Another FOM₂ [38] dedicated to capacitor-based regulator is given as follows:

$$\text{FOM}_2 = \frac{C_L \times \Delta V_{\text{OUT}}}{\Delta I_L} \times \frac{I_Q}{\Delta I_L} \quad (13)$$

This FOM₂ includes the effect of the output capacitance, worst voltage spike coming from either undershoot or overshoot as well as the current ratio between the quiescent current and the maximum load current.

When the load current is small, V_{SG} of power transistor M_P is small. This may push M_{C2} into triode because of the following relationship.

$$V_{SGMP} = V_{DSMP} + V_{DSMC2} \quad (15)$$

Another issue is that the small loop gain and the mismatch of the error amplifier may cause systematic offset which will finally appears at the output node. Furthermore, V_{DS} of M_{C2} varies with the load current, the matching between M_{C2} and M_{C1} will also be affected. The output will be altered if such the condition is not maintained.

On the other hand, various performance metrics such as load regulation and line regulation are degraded due to its small loop gain. Other architectures [40], [42] and [43], which are based on the FVF LDO regulator have been developed. They are cascaded FVF (CAFVF) and buffered FVF (BFVF). Due to the additional gain stages to overcome the above-stated drawbacks, frequency compensation becomes another design issue to overcome the stability issue. However, it leads to the increase of quiescent power consumption. From the reported work [39], the circuitry may demand large quiescent current of 95 μA to support its operation, and 20 - 40 μA from [40]. Therefore, it is desirable to explore the regulator architecture with ultra-low quiescent current efficiency for IoT applications.

2.3.2 Dynamically-Biased LDO Regulator

The reported works discussed in the previous contents are not suitable for ultra-low quiescent current designs. Further low-power LDO regulator is reported in [44] which relies on the dynamically-biased current boosting technique. The schematic is depicted in Figure 2.4.

Figure 2.4 Dynamically-biased LDO regulator [44]

The output voltage variation will be detected by the slewing detection and amplified by amplification circuit followed. As such, it generates the control signal to boost the bias current of the amplifier in the regulator core. Therefore, it allows the ultra-low power consumption under the idle or no-load current condition while maintaining the transient performance during the load current step transitions. The regulator is reported with $1.3 \mu A$ quiescent current and to provide a maximum load current of 50 mA. It is reported to reduce the settling time from $300 \mu s$ to $9 \mu s$. Unfortunately, during the transient response, the voltage variation need to go through the slew detection, amplification circuit and RC networks to provide bias boosting. The delay introduced by the stated circuits can cause the overshoot and undershoot voltage larger than 500 mV.

2.3.3 Assistant Push-pull LDO Regulator

Alternative low-power LDO regulator with a push-pull output stage is reported in [22]. Figure 2.5 shows its simplified circuit topology.

Figure 2.5 Assistant push-pull LDO regulator [22]

It consists of operational amplifier stage and an assistant push-pull output stage circuit. The assistant push-pull output stage circuit aims to enhance the transient performance under low quiescent power by boosting the slew rate at the gate of the power transistor. It is reported to have $1.2 \mu\text{A}$ of quiescent current whilst providing 100 mA load current. However, it relies on a minimum load current of $100 \mu\text{A}$ to provide enough headroom for the transistor M_{A11} in the previous stage of the power transistor. It is reported to recover the output voltage within $2.7 \mu\text{s}$, however it also suffers from a large undershoot and overshoot voltage of 270 mV during load current steps.

2.3.4 Adaptive-stage LDO Regulator

Another LDO regulator architecture that takes advantages of adaptively-biased is reported in [45]. Figure 2.6 depicts its schematic.

Figure 2.6 Adaptive-stage LDO regulator [45]

The architecture, which performs as a two-stage regulator, consumes only 0.9 μA at no load current condition. The second stage of the regulator will be turned on when the load current increases to a certain level. In this way, the concept of ultra-low power is achieved. Furthermore, when the load current increases, the biasing current also adaptively increases, thus improving the g_m of each gain stage and extending the bandwidth.

As discussed in earlier section, devices such as mobile phones and tablets are usually at idle state and require large power during the talk mode [12]. In this case, the adaptive-stage concept provides an excellent solution in prolonging the battery life. Based on the self-configurable architecture with the load current, further scaling down the current consumption can benefit the ultra-low quiescent power design. Unfortunately, the undesired low-frequency poles and zeros will hinder the process of continual scaling down the quiescent current in the LDO regulator design. Furthermore, the transient metrics related to output voltage spikes and settling time will also be degraded due to lower speed.

2.4 Review of Frequency Compensation

Techniques

As discussed, conventional LDO regulator utilizes a large output capacitor to ensure a stable system. Regarding capacitor-less regulator design, the compensation techniques become one of the key design issues. In this section, basic and advanced frequency compensation techniques, which are commonly adopted in LDO regulators, will be reviewed.

2.4.1 Miller Compensation

Miller Compensation is the simplest way to achieve compensation in an amplifier or a regulator design. Without compensation, a two-stage system exhibits two poles, in which their locations may be close to each other. As such, the two-pole system is subject to instability. Figure 2.7 shows a two-stage amplifier with simple Miller compensation scheme.

Figure 2.7 Miller compensation in a two-stage amplifier

The system exhibits two LHP (left half plane) poles and one RHP (right half plane) zero. The transfer function [46] is described as follows:

$$A_v = \frac{g_{m1}g_{m2}R_1R_O \left(1 - s \frac{C_m}{g_{m2}}\right)}{\left(1 + sC_m g_{m2}R_1R_O\right) \left(1 + s \frac{C_O}{g_{m2}}\right)} \quad (16)$$

$$\omega_{p_1} = -\frac{1}{C_m g_{m2} R_1 R_O} \quad (17)$$

$$\omega_{p_2} = -\frac{g_{m2}}{C_O} \quad (18)$$

$$\omega_{z_1} = +\frac{g_{m2}}{C_m} \quad (19)$$

The compensation capacitor C_m will create a dominant pole by pushing one of the poles to lower frequency. The other pole p_2 becomes non-dominant. It will be pushed to a higher frequency. The frequency of non-dominant pole should exceed the unity gain frequency (UGF) to ensure the stability. The presence of C_m will cause the pole splitting process, resulting in the reduction of gain-bandwidth-product (GBW) in exchange of stability. Therefore, a proper selection of the value of C_m is important because of the trade-off among the quiescent power, response time, stability and silicon area. Figure 2.8 shows an improved Miller compensation, which is Miller-RC compensation.

Figure 2.8 Miller-RC compensation in a two-stage amplifier [46]

An additional nulling resistor is added in series with Miller capacitor. As mentioned above, the compensation capacitor C_m will contribute a feedforward path, leading to a RHP zero. An RHP zero will introduce a -90 degree phase shift without rolling off the gain. Therefore, the phase margin is degraded, and the loop will be unstable. With the addition of a nulling resistor, the location of the zero is obtained as follows:

$$\omega_{z_1} = \frac{1}{C_m(R_m - 1/g_{m2})} \quad (20)$$

The RHP zero can be eliminated by choosing the R_m value equal to $1/g_{m2}$. If the R_m value [46] is made larger than $1/g_{m2}$, the zero will be located in the LHP to contribute phase lead effect for better stability.

2.4.2 Cascode Compensation

The effectiveness of pushing the output pole of the Miller-compensated amplifier or regulator to high frequency may not be effective. In order to effectively stabilize the loop response and improve the transient response, cascode compensation or current buffer Miller compensation [47] can be adopted.

Figure 2.9 Cascode compensation in a two-stage amplifier

The poles and the second pole with unity gain frequency relationship are obtained as follows:

$$p_1 \cong -\frac{1}{(g_{m2}R_2)C_cR_1} \quad (21)$$

$$p_2 \cong -\frac{g_{m2}C_c}{C_1(C_c + C_o)} \quad (22)$$

$$\frac{p_2}{UGF} = \frac{g_{m2}}{g_{m1}} \times \frac{C_c}{C_1} \times \frac{C_c}{C_c + C_o} \quad (23)$$

The dominant pole is widely separated with the second pole in cascode compensation. According to [47], the ratio of second pole and unity gain bandwidth can also be determined by ratio C_C/C_1 with a certain amount of tolerance of output capacitor load. In addition, a zero [48] can be obtained as

$$\omega_z = \frac{g_{\text{mc}}}{C_{\text{C}}} \quad (24)$$

Meanwhile, the circuitry with cascode compensation presents good PSR results. However, complex poles in cascode compensation contribute a larger multiplication factor, which results in a large Q factor [49]. The result of which will create an undesirable peaking effect in the frequency response of LDO regulator. Therefore, the cascade factor C_C/C_1 should be carefully chosen to achieve the tradeoff between the peaking effect and multiplication factor for shifting the second pole to a high frequency.

2.4.3 Indirect Feedback Frequency Compensation

The indirect feedback frequency compensation is reported in [50],[51] and shown in Figure 2.10 [50].

Figure 2.10 Examples of indirect feedback frequency compensation [50]

The indirect feedback frequency compensation makes uses of the current i_{C_c} to achieve pole splitting. Compared to Miller compensation. The poles and zero [50] are obtained as follows:

$$p_1 = -\frac{1}{g_{m2}R_1R_2C_C} \quad (25)$$

$$p_2 = -\frac{g_{m2}R_1C_C}{C_L(R_C C_C + R_1 C_1)} \quad (26)$$

$$p_3 = -\frac{R_C C_C + R_1 C_1}{R_1 C_1 R_C C_C} \quad (27)$$

$$z = -g_{mc} / C_C \quad (28)$$

where $R_C = 1/g_{mc}$.

According to (28), the RHP zero is eliminated without placing the nulling resistor [50] compared with Miller compensation. It is quite close to the performance of cascode compensation. It permits the adoption of small C_C which will consume small area.

2.4.4 Q-Reduction Compensation

In three-stage LDO regulator design, the pole-splitting process is usually adopted to ensure the stability. Apart from the dominant pole, a pair of the non-dominant complex pole may be present in the system. Since the location of the non-dominant poles is related to the value of the transconductance of power transistor. When the load current is high, the poles are located far beyond the UGF so that they will not affect the stability of regulator. However, when the load current decreases, the non-dominant complex poles will cause the rise in loop gain, and a -180 degree phase shift, which leads to a reduction in phase margin. Hence, the loop response becomes unstable with a pair of complex pole that leads to large Q and smaller phase margin.

A Q-reduction topology is reported in [36] and the block diagram is shown in Figure 2.11.

Figure 2.11 Q-reduction circuit in a multi-stage amplifier [36]

A capacitor C_{cf} , a current buffer having low-resistive R_{cf} input and transconductance stage form the Q-reduction circuit, where g_{mcf} is the transconductance of the current buffer. The frequency of the complex pole is obtained as

$$\omega_0 = \sqrt{\frac{g_{m2}g_{m3}}{(C_{gd} + C_2)C_3}} \quad (29)$$

and the Q is obtained as follows:

$$Q = \sqrt{\frac{(C_{gd} + C_2)C_3}{g_{m2}g_{m3}}} \times \left[\frac{C_{m1}g_{m2}g_{m3}}{C_{m1}C_{gd}(g_{m3} - g_{m2}) + C_{cf}C_3g_{m2} + (C_{m1}C_{cf}g_{m2}g_{m3}/g_{mcf})} \right] \quad (30)$$

By choosing a smaller g_{mcf} and a large capacitor C_{cf} , the Q will be reduced. This offers more phase margin and wider load current range.

2.5 Review of Overshoot Reduction Circuit

Techniques

Due to the limited discharging capability of the output power stage under low quiescent current, the LDO regulator tends to suffer from a large overshoot voltage and a long settling time. Several overshoot reduction techniques [20], [30], [52], [53], which are based on the capacitor to provide the ac coupling, have been reported.

Figure 2.12 Simplified ac coupling RC network for voltage spike detection [54]

Figure 2.12 depicts the simplified ac coupling RC network for voltage spike detection [54]. Of particular noted, when there is an overshoot voltage spike, the RC network will sense the voltage spike by C_c to the gate of driving transistor M_2 . This results in an instantaneous discharging current I_d , which helps to reduce the overshoot voltage and allows a fast settling time for the output voltage. However, a large resistor and capacitor are required for effective signal coupling as well as isolation from the static bias node. This may increase the chip area as the trade-off.

On the other hand, a constant-on-time dynamic biasing technique is reported in [26] with aid of digital circuits. It ensures a constant on-time for the dynamic bias current in the error amplifier used in the LDO regulator as shown in Figure 2.13. Although the settling time can be reduced, the overshoot voltage remains high. Therefore, it

gives the motivation for investigating a new circuit for overshoot voltage reduction in this project.

Figure 2.13 Simplified schematic of Guo's constant-on-time biasing technique [26]

2.6 Layout Issues in LDO Regulator

2.6.1 MOS Transistors

Figure 2.14 shows a simplified structure of a NMOS and PMOS device in p-type substrate, on which transistors are usually fabricated in CMOS IC processing [51]. The substrate is the body or the bulk of the NMOS devices. In order to implement NMOS devices, two diffusion areas are formed by n-type impurities doped into the substrate, which are known as the drain and the source terminals. A layer of silicon dioxide (SiO_2) insulates the gate of the device, which is formed by a piece of polysilicon [55]. On the other hand, to implement PMOS devices, as shown in Figure 2.14, n-type impurities are doped into the substrate to form N-Wells. The N-Wells refer to the body or bulk of PMOS devices. Two diffusion areas doped with p-type impurities in the N-Well form the drain and source terminal of PMOS devices. The gate of PMOS devices is also implemented with silicon dioxide and polysilicon on top of it. In this work, twin-well process is only supported by the AMS 0.18 μm CMOS process. There is no triple-well process for transistor layout. As such, body effect will appear in NMOS device in stacked structure due to shared p- substrate. The nominal threshold voltage for short channel PMOS transistor and NMOS transistor is around 350 mV and 430 mV, respectively. As such, 1.2V supply is chosen in the LDO regulator design.

Figure 2.14 Simplified structure of NMOS and PMOS device in p-type
substrate[51]

Fabrication is also one of the factors that will affect the performance of the circuit and chip. Good layout techniques will help to minimize the effects related to fabrication and reliability issues. In the layout process, matching of transistors are very important. Two layout techniques of matched transistors will help to reduce mismatch and achieve reliable performance. When two matched transistors are connected at one node in common, interdigitation will help to reduce the mismatch. One of the possible interdigitation layout is shown in Figure 2.15, where A and B are two transistors with even number of fingers and multiplicity. Transistor A and B are symmetrically located with the axis.

Figure 2.15 Interdigitation layout

The other technique is common centroid, which is shown in Figure 2.16. The transistors A and B are symmetrical with the center. Due to the cross coupled placement, common centroid layout needs more complex connection with different metal layers and polysilicon between devices.

Figure 2.16 Common centroid layout

Apart from the connection techniques, dummy devices are important to be placed at the boundaries of the devices to protect inner devices or elements, which is shown in Figure 2.17. Dummy devices can be identical to the inner devices and their terminals are shorted. Of particularly noted, the dummy transistors may cause parasitic effect, therefore the number of dummy devices used should be carefully chosen.

Figure 2.17 Dummy devices usage

2.6.2 Resistors and Capacitors

Passive devices such as resistors and capacitors also need to be placed with care. Similar to MOS transistors, capacitors can also be placed in common centroid placement to achieve good matching. In sizing the device, it is better to use large identical geometries ($W=L$) as unit capacitor.

In the circuit, resistors could be size up to few hundred $K\Omega$ or more. In this circumstance, identical long unit strips are used as shown in Figure 2.18. The black squares denote as the pins of the two terminals of the resistor. Dummy devices also can be used to protect the inner elements in the layout of passive devices.

Figure 2.18 Resistor layout

2.6.3 Power Transistor Layout

The layout of the power transistor is critical because it directly affects the performance of the chip. Firstly, since the power transistor needs to be capable of delivering large amount of current under full load current condition, the on-resistance of the power transistor should be kept small. As such, the length of the power transistor adopts the minimum process channel length and the width is made large to yield a large aspect ratio of (W/L) . Secondly, due to large-size power transistor, the parasitic capacitor and resistance of the gate will be big. This is translated to reducing the pole location in frequency response. Minimizing the parasitic factors becomes the key issue in power transistor layout. Multiple fingers are used to reduce the resistance by paralleling the unit transistors. Furthermore, higher layer metal should be used to connect the drains and sources of unit transistors because higher layer metals have smaller sheet resistance. Figure 2.19 shows the layout of the power transistor. The lower layers of combined sources and drain terminals are connected from Metal 1 to Metal 4 by vias from Via 2 to Via 4. The left-upper portion of combined sources are connected by Metal 4 to Metal 6 and they are finally routed to the supply V_{DD} through the paralleled Metal 5 and Metal 6. Regarding the right-lower portion of the combined drains, they are paralleled from Metal 4 to Metal 6. Then they are connected to the output node V_{OUT} through the paralleled Metal 5 and Metal 6.

Figure 2.19 Layout of power transistor

Chapter 3 Circuit Design and Analysis

In this Chapter, the design, analysis and implementation of the proposed LDO regulator are given. The details of each sub-block will be described.

3.1 Adaptive-Stage Architecture with Adaptive Frequency Compensation

Figure 3.1 depicts the simplified schematic of the proposed LDO regulator without the bias circuit. The topology consists of a differential input stage, a non-inverting stage, a dual-power-transistors stage, a distributed overshoot reduction (DOVSR) circuit. Transistors M_1 - M_6 form the differential input stage, with the composite transistor input pair comprising M_1 - M_4 . One of the inputs of differential stage is tied to the reference voltage V_{REF} whereas the other input is tied to the feedback point. The second non-inverting gain stage is composed by transistors M_7 and M_{10} - M_{12} . Incorporating with the output stage, it serves as an adaptive-stage which is either off for forming two-stage architecture or on for forming three-stage architecture, depending on the load current level. Besides, the adaptively-biased current technique is employed to both the input differential input stage and the second non-inverting gain stage. The feedforward bias path formed by M_5 and M_{12} reduces the bias branch for saving quiescent power whilst providing fast signal path. The output stage is made up of the dual power transistors, M_{P1} and M_{P2} . And the feedback network constituted by three diode-connected PMOS transistors to realize a feedback factor β of $2/3$. The auxiliary power transistor M_{P1} conducts light current for full load range whereas the main power transistor M_{P2} conducts from moderate to heavy load current. The DOVSR circuit will be discussed in sub-section. Regarding the adaptive frequency compensation technique, it is proposed in this work so that different compensation frequency schemes are self-configured on the basis of the load current level under ultra-low quiescent current design. These frequency compensation schemes include transistor degeneration frequency compensation (TDFC), indirect feedback frequency compensation [50] [51], the Q-reduction compensation [36] and the

Miller-RC compensation. The indirect feedback frequency compensation capacitor C_Y effectively pushes the output pole to high frequency with low quiescent power. Refer to the proposed TDFC scheme, the components C_X and R_X are added to the composite transistors to form a dynamic zero in the adaptively-biased differential input stage. Besides, the dynamic zero is able to partially cancel the phase shift introduced by the second pole of regulator system. As such, the stability of regulator will not be significantly degraded even if the frequency of all the poles are reduced by the reduced biasing current for low quiescent design. Turning to the Q reduction compensation, it deals with the capacitor C_Q [36] and the low input impedance path of the current buffer in the input differential stage. It aims to reduce the peaking effect arising from the complex poles formed by the pole at the gate of main power transistor and the pole at the output of regulator in the three-stage configuration. The complex poles will influence the stability during low-to-moderate level load current. The Q-reduction compensation will be activated in three-stage topology. Furthermore, due to significant increase of transconductance in the power transistor at high load current, a high-frequency complex poles formed by the parasitic poles contributed by the gate of auxiliary power transistor and the gate of main power transistor. Therefore, a high-frequency based Miller-RC compensation, which employs a small resistor R_M and a small capacitor C_M , is applied to the power-transistor output stage so that the stability at high load current condition can be maintained.

Figure 3.1 Transistor-level schematic of the proposed LDO regulator

3.2 Bias Circuit

A self-biased circuit will exhibit two operating states. One is the undesired condition in off state, in which no current will flow in the circuit. The other operating condition is that all the transistors operating in the defined region. Due to a self-biased configuration, a start-up circuit is required to force the circuit from the undesired off state to the operating state. Figure 3.2 shows the constant transconductance (G_m) bias circuit with the start-up circuit.

Refer to Figure 3.2, M_{B7} , M_{B8} , C_{B1} and C_{B2} form the start-up circuit to force the circuit into the desired state. Under the undesired off state, the gate voltage of M_{B1} and M_{B2} denoted as V_B will be forced to be close to the supply V_{DD} whereas the gate voltage of M_{B5} and M_{B6} , denoted as V_C , is forced to be close to the ground.

Figure 3.2 Self-biased circuit with start-up circuit

During start-up transition, the supply voltage increases from zero to V_{DD} , the charges will be stored in C_{B1} whereas V_A will increase with the supply voltage. When the gate voltage V_A has reached a value greater than the transistor's threshold voltage (V_{TH}), M_{B8} will be turned on and start to conduct current. The common gate voltage V_B of M_{B1} and M_{B2} will be pulled away from V_{DD} to a lower value. Consequently, M_{B1} and M_{B2} will start to draw current in each branch of the bias circuit. M_{B3} - M_{B6} will be turned on whereas the gate voltage V_C of M_{B5} will be pulled up to a higher value from the ground. With the rising voltage V_C , M_{B7} will start to conduct and V_A will be forced to be connected to the ground. At this juncture, the start-up circuit will no longer to conduct any static current. Hence, it is isolated from the bias circuit. The start-up circuit benefits low power consumption from zero static current after turning on the bias circuit.

The bias circuit adopts a constant G_m circuit, which is described in the following operation. The current mirror pair M_{B1} and M_{B2} , and the voltage mirror pair, formed

by M_{B3} and M_{B4} , are designed with the relationship that $(W/L)_{B1} = (W/L)_{B2}$, and $(W/L)_{B3} = (W/L)_{B4}$. The current flows through each branch in the bias circuit is therefore identical. By applying Kirchhoff's Voltage Law (KVL) [55], the equations are obtained as follows:

$$V_{GS_MB6} = V_{GS_MB5} + I_{MB5} R_{B1} \quad (31)$$

$$I_{MB5} = I_{MB6} \quad (32)$$

To meet the low power constraint, M_{B5} and M_{B6} are biased in weak inversion region. Therefore, by rearranging (31) and assuming the devices M_{B5} and M_{B6} operating in weak inversion [55], this yields

$$R_{B1} I_{MB6} = \Delta V_{GS} \approx \eta V_T \ln(N) \quad (33)$$

where N denotes the ratio of the device aspect ratio and equals to $(W/L)_{B5}/(W/L)_{B6}$. As a result, the transconductance of M_{B6} can be expressed as

$$g_{m_MB6} = \frac{I_{MB6}}{\eta V_T} = \frac{\ln(N)}{R_{B1}} \quad (34)$$

By applying $(W/L)_{B5} = 4 (W/L)_{B6}$, this gives the approximation as follows:

$$g_{m_MB6} \approx 1.39 / R_{B1} \quad (35)$$

Since the circuit targets for ultra-low quiescent power SoC application, the bias current flowing through each branch is designed to be 50 nA in the bias circuit. The lengths of the transistors used in bias circuit are implemented with at least 4 times of the minimum length of the process. This permits good matching whilst minimizing the channel-length modulation effect.

3.3 Circuit Implementation

The core circuit is implemented using the adaptively-biased and adaptive-stage topology with the addition of frequency compensation techniques together with a feedforward path. It targets for transient response improvement and elimination of biasing current for reduction of static power dissipation. Figure 3.3 shows the schematic of the core circuit without biasing current.

Figure 3.3 Schematic of the proposed LDO regulator

In the architecture, M_7 serves as a current sensor, which senses the current flowing through the auxiliary power transistor M_{P1} at $1/N$ ratio. M_{11} and M_{12} will compare adaptively-biased currents, named I_{M11} and I_{M12} . I_{M11} is the output sensing current which is obtained from the sensing device M_7 and the current mirror M_{10} and M_{11} . I_{M12} is the adaptively-biased current in M_{12} which is feedforward biased by the first stage. In no-load or light load current condition, where $I_{M12} > I_{M11}$ from the intended bias design, the transistor M_{12} is forced to operate in triode region. Therefore, the drains of M_{11} and M_{12} will be pulled close to the supply V_{DD} . Thus, M_{P2} works in off state due to small V_{SG} whereas M_{P1} remains active to provide the regulation function. As such, the architecture is regarded as a two-stage topology as shown in Figure 3.4. The two-stage regulator consists of a differential input stage with one input tied to the reference V_{REF} and an auxiliary power transistor M_{P1} stage.

Figure 3.4 LDO regulator in two-stage configuration

Figure 3.5 Variation of I_{M11} and I_{M12} , and I_L during positive load current step

Figure 3.5 shows both I_{M11} and I_{M12} are built up in the off-state second gain stage upon the transient excitation. When the load current I_L increases to 254 μA , both I_{M11} and I_{M12} simultaneously increase fast while I_{M11} increases faster than I_{M12} . Therefore, it turns out that $I_{M11} > I_{M12}$ and the gate voltage of M_{P2} , V_{G2} , will be discharged

towards lower value by the current I_{M11} . In this way, M_{12} does not work in triode region and this permits the main power transistor M_{P2} to conduct. As such, the non-inverting amplifier is turned on, forming a three-stage amplifier topology as depicted in Figure 3.6.

Figure 3.6 Three-stage configuration with indicated current ratios

The equilibrium point is established at the condition that $I_{M11}=I_{M12}$. The first gain stage drives the auxiliary power transistor M_{P1} . The adaptively-biased current source transistor M_9 in the first differential gain stage will continuously increase with the load current. Subsequently, the g_m of the input pair will increase, thus extending the bandwidth to yield fast transient response. Of particularly noted, the bias current in the differential stage at no load current condition is $2I_{BF}$ in M_8 and zero bias current in M_9 . Refer to Figure 3.6, the current ratios for each current mirror pair are stated. Therefore, defining the maximum current in M_{P1} as I_{MP1_max} , the relationship between the current through the sensing transistor M_7 and M_{P1} is obtained as

$$I_{M7} = \frac{I_{MP1_max}}{N} \quad (36)$$

For transistor group M_7 , M_{10} and M_{11} , we have

$$I_{M7} = I_{M10} = \frac{I_{MP1_max}}{N} \quad (37)$$

$$I_{M11} = M \times I_{M10} = M \times I_{M7} = \frac{M \times I_{MP1_max}}{N} \quad (38)$$

For transistor group M_5 , M_8 , M_9 , and M_{10} , we have

$$I_{M9} = \frac{I_{M10}}{A} \quad (39)$$

$$I_{M5} = \frac{1}{2}(I_{M8} + I_{M9}) \frac{1}{2}(2I_{BF} + I_{M9}) = \frac{1}{2} \left(2I_{BF} + \frac{I_{M10}}{A} \right) \quad (40)$$

For transistor pair M_5 and M_{12} , we have

$$I_{M12} = K \times I_{M5} = \frac{K}{2} \left(2I_{BF} + \frac{I_{M10}}{A} \right) \quad (41)$$

By equalizing I_{M11} and I_{M12} from (38) and (41), we obtain,

$$I_{MP1_max} = N \times I_{BF} \left(\frac{2KA}{2AM - K} \right) \quad (42)$$

Refer to the schematic shown in Figure 3.3, I_{BF} is designed to be a 100nA. $I_{MFB1,2,3}$ in the feedback network is 65 nA. The bias circuit, which is not indicated in Figure 3.3, contributes 100 nA. In this design, $N=30$, $K=31$, $M=5/2$, $A=13/2$. This gives $I_{M7} = 2$ nA, $I_{M11} = 5$ nA, and $I_{Ma1,2} = 3$ nA. The calculated value of I_{MP1_max} is 806 μ A whereas the simulated value is about 716 μ A. The discrepancy is caused by the channel length modulation arising from the minimum channel length employed for M_7 , M_{P1} and M_{P2} . Besides, I_{MP1_max} is designed to avoid V_{SG} of M_{P1} to stress M_4 . As such, the maximum bias current I_{M5_max} is approximately 2.6 μ A at full load current. This provides adequate headroom for M_8 and M_9 in whole load current range. The

maximum current delivered by the auxiliary power transistor M_{P1} is 806 μA in this design.

The calculation pertaining to headroom issue, which is related to the maximum adaptive bias current in the first differential stage and the maximum current that the auxiliary power transistor M_{P1} can deliver, are stated in the following.

Regarding the maximum adaptive bias current in the first stage, the drain voltage of M_8 is defined as

$$V_{D_M8} = V_{REF} - V_{GS_M1} = V_{REF} - \ln\left(\frac{I_{M8}}{I_0}\right)V_T - V_{TH_M1} \quad (43)$$

During no-load current condition, we have

$$V_{D_M8|no-load} = V_{REF} - \ln\left(\frac{I_{BF}}{I_0}\right)V_T - V_{TH_M1} \quad (44)$$

where I_0 is the characteristic current [55].

When turning on the second non-inverting stage under full-load case, the current flowing in the differential input stage has increased to the maximum value. We have,

$$V_{D_M8|full-load} = V_{REF} - \ln\left(\frac{I_{M5_max}}{I_0}\right)V_T - V_{TH_M1} \quad (45)$$

where I_{M5_max} is defined as the maximum adaptive bias current that flows in each branch of the input stage. Subtracting (44) by (45), we get

$$\Delta V_{D_M8} = \Delta V_{D_M8|no-load} - \Delta V_{D_M8|full-load} = \ln\left(\frac{I_{M5_max}}{I_{BF}}\right)V_T \quad (46)$$

In the initial condition, V_{D_M8} is approximately equal to 200 mV. ΔV_{D_M8} should be chosen to provide at least $3V_T$ which is 75 mV for M_8 to operate in weak-inversion region. In this design, I_{M5_max} is approximately 2.6 μA , so that the change of the drain voltage across the transistor M_8 under full-load current condition is

$$\Delta V_{D_M8} = \ln\left(\frac{I_{M5_max}}{I_{BF}}\right)V_T \approx 3V_T \approx 75mV \quad (47)$$

This indicates that there is at least 125 mV (200 mV - 75 mV) of V_{DS} for M_8 when the second non-inverting stage is turned on,

The corresponding I_{MP1_max} , which is the maximum current delivered by the auxiliary power transistor M_{P1} , is designed such that the V_{DS} of M_4 will not be stressed.

$$V_{DS_M4} = (V_{DD} - V_{GS_MP1}) - (V_{REF} - V_{GS_M4}) \quad (48)$$

Rearranging (48), we get

$$\begin{aligned} V_{DS_4} &= (V_{DD} - V_{REF}) - (V_{GS_MP1} - V_{GS_M4}) \\ &= (1.2 - 2/3) - (V_{GS_MP1} - V_{GS_M4}) \approx 533.3 - \ln\left(\frac{I_{MP1_max}}{I_{M5_max}}\right)V_T \end{aligned} \quad (49)$$

where I_{M5_max} is designed to be 2.6 μA in full load current, $V_{REF} = 2/3$ V and $V_T = 25$ mV at room temperature.

In this design, I_{MP1_max} is designed to be 806 μA , such that the input device M_4 will have at least 380 mV of headroom. This ensures that $V_{DS_M4} > 3V_T$ to meet worst case variation from V_{SG_MP1} .

Furthermore, refer to the output current sensing pair M_7 and M_{P1} , V_{DS_M7} will be much larger than V_{DS_MP1} . The same goes for the current mirror pair, M_5 and M_{12} . The difference of V_{DS} of the current mirror transistor pairs will cause mismatch from the channel length modulation. In practice, the actual obtained current of I_{MP1_max} is about 716 μA . Nevertheless, it is within the range of design.

3.4 Overshoot Reduction

3.4.1 Overshoot Reduction by Core Circuit

Overshoot is encountered during high-to-low load current transitions. When the load current steps from high to low, the loop cannot respond immediately and the power transistors continues to deliver current to the output node. The output capacitor will be overcharged, since the discharging current from the output node is small and close to zero. This voltage spike is known as overshoot voltage, which is strong in output capacitor-less and ultra-low power designs.

Figure 3.7 Large-signal transient response during high-to-low load current step

In the normal loop response, the overshoot will be fed back to the input of the first stage. In the path that the signal passes from the first stage to the auxiliary power transistor M_{P1} , the gate voltage of M_{P1} will increase. As V_{SG} of M_{P1} is reduced, the current delivered by the power transistor M_{P1} will be reduced. However, as discussed in the earlier section, the maximum current that M_{P1} can deliver is limited.

At the same time, the signal will continue travel through the other path from M_6 to M_7 and M_{10} . The gate voltage of M_{10} and M_{11} will decrease. Thus, the output of the second stage at the gate of the main power transistor M_{P2} will increase. Since V_{SG} of

M_{P2} reduces, less current will flow to the output through M_{P2} . The output voltage will be settled. Due to the long delay path along the feedback mechanism in the circuit and large parasitic capacitor at the gate of power transistors, the transient response may not be effective or tends to be very slow, significantly slow under ultra-low quiescent designs.

3.4.2 DOVSR and Transient g_m in TDFC

Figure 3.8 Transient response using DOVSR circuit

As mentioned, the normal overshoot settling response by the entire feedback loop of core circuit will cause large overshoot effect and longer settling time. To improve the transient response time or speed of regulator, an improved distributed overshoot reduction (DOVSR) circuit is introduced. Refer to the dotted box in Figure 3.8, the distributed overshoot reduction network consists of two networks. The first network is formed by R_{a1} , C_{a1} and M_{a1} to provide a fast-local feedback loop. The signal will be coupled from the gate of M_{a1} in a form of ac spike signal. The gate voltage of M_{a1} will increase at the overshoot and M_{a1} will draw the excess current from the output node. Therefore, the overshoot is reduced. Pertaining to the second network, it comprises R_{a2} , C_{a2} and M_{a2} . This additional RC network will produce further delay for the ac spike signal to arrive at the gate of M_{a2} . In this case, M_{a2} will continue to sustain the discharging when M_{a1} decreases its conduction of current. Therefore, the

total conduction time of discharging current will be prolonged. As such, the settling time becomes shortened. In brief, the distributed overshoot reduction circuit formed by the components R_{a1} , C_{a1} , M_{a1} , R_{a2} , C_{a2} and M_{a2} shows an improved overshoot reduction result than that of the conventional counterpart formed by standalone R_{a1} , C_{a1} and M_{a1} only.

Apart from this, the effective impedance at the source node of M_3 in TDFC is reduced under transient condition, which causes the decrease of degeneration resistance value and the increase of transconductance value during transitions. Figure 3.9. illustrates the variation of g_{m1} in the differential stage during the negative load current step from 100 mA to 0 A. It shows that g_{m1} is larger with C_X and R_X in TDFC technique.

Figure 3.9 Variation of g_{m1} with transient time with/without C_X and R_X

It can be seen that the compensation network, formed by C_X and R_X in TDFC, reduces the effective impedance at the source node of M_3 under transient condition, causing the decrease of degeneration resistor R_{on} . As the transconductance is boosted during transition, the speed is enhanced.

Chapter 4 Stability Analysis

Figure 4.1 Proposed LDO regulator with indicated break point for loop gain analysis

To analyze the loop response, the analysis is conducted at the breakpoint shown in Figure 4.1. The stability of this LDO regulator will be analyzed based on three scenarios: (i) Low load current condition ($I_L < I_{MP1_max}$), (ii) Moderate load current condition ($I_L > I_{MP1_max}$), and (iii) High load current condition ($I_L \gg I_{MP1_max}$). In the following analysis, g_{mi} , C_i and R_i will denote the transconductance, the equivalent output parasitic capacitance and the equivalent output resistance of each gain stage, respectively. The small-signal model for two-stage and three-stage topologies are depicted in Figure 4.2(a) and (b).

Figure 4.2 Simplified small-signal model of equivalent circuit (a) when $I_L < I_{MP1_max}$ (two-stage topology) and (b) when $I_L > I_{MP1_max}$ (three-stage topology).

4.1 Low Load Current Case ($I_L < I_{MP1_max}$)

In this case, the main power transistor M_{P2} maintains in off state due to small I_L and the LDO regulator is self-configured as a two-stage topology as depicted in Figure 4.2(a). It is noted that g_{m1} represents the effective transconductance of first gain stage. Refer to Figure 4.3, the composite transistor is formed by M_1 and M_3 . The composite transistor is part of half circuit of the composite transistor pair as shown in Figure 4.3, which includes the other composite transistor formed by M_2 and M_4 .

Figure 4.3 (a) Half circuit of input stage and (b) Equivalent small-signal model

The transistors M_1 and M_2 operate in the triode region whereas M_3 and M_4 operate in the subthreshold region. In this case, the $g_{m1}(s)$ of input stage in Figure 4.3(a) can be obtained by analyzing the equivalent small-signal model as illustrated in Figure 4.3(b). As such, $g_{m1}(s)$ can be expressed as follows:

$$g_{m1}(s) \approx \frac{g_{mM3}}{(g_{mM3}R_{on} + 1)} \frac{(C_X(R_{on} + R_X)s + 1)}{\left(C_X\left(R_X + \frac{1}{g_{mM3}}\right)s + 1\right)} = \frac{g_{mM3}}{(g_{mM3}R_{on} + 1)} \frac{(1 + s/z_{TDFC})}{(1 + s/p_{TDFC})} \quad (50)$$

where R_{on} , defined as $1/g_{ds1}$, denotes the on-resistance of the transistor M_1 . $g_{m1} = g_{mM3}/(1 + g_{mM3}R_{on})$ represents the effective dc transconductance which involves the degeneration factor of $(1 + g_{mM3}R_{on})$. Pertaining to the frequency response, a relatively low-frequency LHP zero, $z_{TDFC} = -1/(C_X \times (R_{on} + R_X))$, appears first followed by a higher-frequency LHP pole, $p_{TDFC} = -1/(C_X \times (R_X + 1/g_{mM3}))$. Based on the weak inversion current equation [55], R_{on} can be approximated as follows:

$$R_{on} = \frac{1}{g_{ds_M1}} = \frac{1}{I_{M3}/V_T} \left(e^{\left(\frac{V_{DS_M1}}{V_T} \right)} - 1 \right) \approx \frac{1}{g_{mM3}} \left(e^{\left(\frac{V_{DS_M1}}{V_T} \right)} - 1 \right) \quad (51)$$

where $I_{M3} = I_{M1} = I_{M5} = I_{M6}$, in this work, V_{DS1} is designed close to the thermal voltage V_T at room temperature, leading to $R_{on} \approx 2/g_{mM3}$. From the analytical result, the degenerated transconductance $g_{m1}(s)$ will increase first before it starts to decrease when increasing the signal frequency.

Refer to Figure 4.2(a), which shows the two-stage topology of LDO regulator under low load current condition together with the replacement of the first transconductance input stage by the equivalent model obtained from (46), the transfer function of loop gain can be obtained as follows:

$$A_{2_stage}(s) \approx \frac{-\beta A_{DC_2stage} \left(C_X (R_{on} + R_X) s + 1 \right) \left(\frac{C_Y}{g_{mY}} s + 1 \right)}{\left(R_O (C_Y g_{mMP1} R_1 + C_O) s + 1 \right) \left(\frac{C_O (g_{mY} C_1 R_1 + C_Y)}{g_{mY} (C_Y g_{mMP1} R_1 + C_O)} s + 1 \right) \left(\frac{C_Y C_1 R_1}{g_{mY} C_1 R_1 + C_Y} s + 1 \right) \left(C_X \left(R_X + \frac{1}{g_{mM3}} \right) s + 1 \right)} \quad (52)$$

where β is the feedback factor and equals to $2/3$ in this work. g_{mY} is the transconductance of M_4 . Refer to (52), the two-stage dc gain is obtained as follows:

$$A_{dc_2stage} = g_{m1} g_{mMP1} R_1 R_O \quad (53)$$

Further inspecting the transfer function (52), there are four poles and two zeros in the 2-stage LDO regulator system. They are given as follows:

$$p_{-3dB} = p_1 = -\frac{1}{R_o(C_Y g_{mMP1} R_l + C_o)} \quad (54)$$

$$p_2 = -\frac{g_{mY}(C_Y g_{mMP1} R_l + C_o)}{C_o(g_{mY} C_l R_l + C_Y)} \quad (55)$$

$$z_1 = z_{TDFC} = -\frac{1}{C_X(R_{on} + R_X)} \quad (56)$$

$$z_2 = -\frac{g_{mY}}{C_Y} \quad (57)$$

$$p_3 = -\frac{g_{mY} C_l R_l + C_Y}{C_Y C_l R_l} \quad (58)$$

$$p_4 = p_{TDFC} = -\frac{1}{C_X(R_X + 1/g_{mM3})} \quad (59)$$

In this work, the proposed TDFC scheme enables the generation of an extra z_1 (z_{TDFC}) which is located slightly above UGF. This aims to partially compensate the phase lag introduced by the output pole p_2 which is located slightly below UGF. Besides, the high-frequency z_2 , arising from indirect feedback frequency compensation [50], [51], tends to counteract the phase lag introduced by the high-frequency p_3 and p_4 (p_{TDFC}) which are located much above UGF. Furthermore, since $g_{mMP1} \approx I_L/V_T$, when the load current increases, p_2 moves towards high frequency through the increase of g_{mMP1} . According to (38) and (40), I_{M3} is adaptively biased and proportional to I_L . Therefore, R_{on} is inversely proportional to I_L as interpreted from (51). Therefore, z_1 can partially track p_2 during the change of load current. They will move to higher frequencies when the load current increases. In this way, the bandwidth of the system at higher load current will not be jeopardized. Consequently, the proposed TDFC pole-zero compensation arrangement improves the overall phase margin of LDO regulator system without significantly compromising the settling time.

4.2 Moderate load current case ($I_L > I_{MP1_max}$)

In this scenario, M_{P2} turns on and its transconductance, g_{mMP2} becomes comparable with g_{mMP1} .

Figure 4.4 Small-signal model for moderate load current case

Following the analysis of three-stage topology using the small-signal model as depicted in Figure 4.2 (b), the transfer function of loop gain can be obtained as follows:

$$A_{3stage_Mod}(s) \approx \frac{-\beta \times A_{dc_3stage} \left(C_X (R_{on} + R_X) s + 1 \right) \left(\frac{C_Y}{g_{mY}} s + 1 \right) \left(\frac{C_Q}{g_{mB}} s + 1 \right) \left(\left(\frac{C_2 g_{mMP1}}{g_{m2} g_{mMP2}} + \frac{C_1 g_{mFF}}{g_{m1} g_{m2}} \right) s + 1 \right) \left(C_M \left(R_M - \frac{1}{g_{mMP2}} \right) s + 1 \right)}{\left(g_{m2} R_1 R_2 (C_Y g_{mMP2} R_O + C_Q) s + 1 \right) \left(C_X \left(R_X + \frac{1}{g_{mM3}} \right) s + 1 \right) \left(1 + \left(\frac{C_2 g_{mMP1}}{g_{m2} g_{mMP2}} + \frac{C_Q}{g_{mB}} \right) s + \left(\frac{C_O C_Q}{g_{mY} g_{mMP2}} + \frac{C_2 C_Q g_{mMP1}}{g_{m2} g_{mB} g_{mMP2}} \right) s^2 \right) \left(\left(\frac{C_1}{g_{mMP1} g_{mY} R_O} + C_M R_M \right) s + 1 \right)} \quad (60)$$

where g_{m2} is the transconductance obtained from the second non-inverting stage, g_{mB} is the transconductance of transistor M_5 and g_{mFF} is the feedforward transconductance of transistor M_{12} . The three-stage dc gain in moderate load current becomes

$$A_{\text{dc_3stage}} = g_{\text{m1}} g_{\text{m2}} g_{\text{mMP2}} R_1 R_2 R_{\text{O}} \quad (61)$$

From (60), there are five poles and five zeros in the three-stage LDO regulator system. They are given as follows:

$$p_{-3\text{dB}} = p_1 = -\frac{1}{g_{\text{m2}} R_1 R_2 (C_{\text{Y}} g_{\text{mMP2}} R_{\text{O}} + C_{\text{Q}})} \quad (62)$$

$$z_1 = z_{\text{TDFC}} = -\frac{1}{C_{\text{X}} (R_{\text{on}} + R_{\text{X}})} \quad (63)$$

$$p_2 = p_{\text{TDFC}} = -\frac{1}{C_{\text{X}} (R_{\text{X}} + 1 / g_{\text{mM3}})} \quad (64)$$

$$z_2 = -\frac{g_{\text{mY}}}{C_{\text{Y}}} \quad (65)$$

$$z_3 = -\frac{g_{\text{mB}}}{C_{\text{Q}}} \quad (66)$$

$$z_4 = -\frac{1}{\frac{C_2 g_{\text{mMP1}}}{g_{\text{m2}} g_{\text{mMP2}}} + \frac{C_1 g_{\text{mFF}}}{g_{\text{m1}} g_{\text{m2}}}} \quad (67)$$

$$|p_{3,4}| = \frac{1}{\sqrt{\frac{C_{\text{O}} C_{\text{Q}}}{g_{\text{mY}} g_{\text{mMP2}}} + \frac{C_2 C_{\text{Q}} g_{\text{mMP1}}}{g_{\text{m2}} g_{\text{mB}} g_{\text{mMP2}}}}} \quad (68)$$

$$p_5 = -\frac{1}{\left(\frac{C_1}{g_{\text{mMP1}} g_{\text{mY}} R_{\text{O}}} + C_{\text{M}} R_{\text{M}} \right)} \quad (69)$$

$$z_5 = -\frac{1}{C_{\text{M}} (R_{\text{M}} - 1 / g_{\text{mMP2}})} \quad (70)$$

It is noted that z_1 is out-band and close to UGF. z_2 is above UGF. The out-band high-frequency pole p_2 can be partially compensated contributed by the degenerated transistor in $g_{m1}(s)$. Since the out-band high frequency pole p_5 and zero z_5 can compensate each other. They have no significant effect to the system stability under moderate current condition. Refer to the second-order term in the denominator of (60), it implies that the complex poles, $|p_{3,4}|$, exists because g_{mMP2} is not strong in this moderate load condition. To relax the peaking issue, a small Q-reduction capacitor C_Q is used. The frequency of complex poles is obtained in (68) and they are above UGF in this design. Since the Q-reduction z_3 and the feedforward path z_4 are located beyond the UGF, they will not affect the overall stability.

4.3 High load current case ($I_L > I_{MP1_max}$)

At high load current case, g_{mMP2} becomes a very large value.

Figure 4.5 Small-signal model for high load current case

Following the analysis of 3-stage topology using the small-signal model as depicted in Figure 4.5. The transfer function of loop gain can be expressed as

$$A_{3stage_High}(s) \approx \frac{-\beta \times A_{dc_3stage} (C_X (R_{on} + R_X) s + 1) \left(\frac{C_Y}{g_{mY}} s + 1 \right) \left(\frac{C_Q}{g_{mB}} s + 1 \right) \left(\left(\frac{C_2 g_{mMP1}}{g_{m2} g_{mMP2}} + \frac{C_1 g_{mFF}}{g_{m1} g_{m2}} \right) s + 1 \right) \left(C_M \left(R_M - \frac{1}{g_{mMP2}} \right) s + 1 \right)}{(g_{m2} R_1 R_2 (C_Y g_{mMP2} R_O + C_Q) s + 1) \left(C_X \left(R_X + \frac{1}{g_{mM3}} \right) s + 1 \right) \left(1 + \left(\frac{C_Q}{g_{mY} g_{mMP2} R_O} + \frac{C_Q}{g_{mB}} \right) s \right) \left(1 + C_M R_M s + \frac{C_1 C_2}{g_{m2} g_{mY} g_{mMP2} R_O} s^2 \right)} \quad (71)$$

The dc gain is the same as (61). There are five zeros and five poles in this case, which are expressed as follows,

$$p_{-3dB} = p_1 = -\frac{1}{g_{m2} R_1 R_2 (C_Y g_{mMP2} R_O + C_Q)} \quad (72)$$

$$z_1 = z_{\text{TDFC}} = -\frac{1}{C_X (R_{\text{on}} + R_X)} \quad (73)$$

$$p_2 = p_{\text{TDFC}} = -\frac{1}{C_X (R_X + 1/g_{\text{mM3}})} \quad (74)$$

$$z_2 = -\frac{g_{\text{mY}}}{C_Y} \quad (75)$$

$$p_3 \approx -\frac{1}{\left(\frac{C_Q}{g_{\text{mY}} g_{\text{mMP2}} R_O} + \frac{C_Q}{g_{\text{mB}}} \right)} \quad (76)$$

$$z_3 = -\frac{g_{\text{mB}}}{C_Q} \quad (77)$$

$$|p_{4,5}| \approx \sqrt{\frac{g_{\text{m2}} g_{\text{mY}} g_{\text{mMP2}} R_O}{C_1 C_2}} \quad (78)$$

$$z_4 = -\frac{1}{\frac{C_2 g_{\text{mMP1}}}{g_{\text{m2}} g_{\text{mMP2}}} + \frac{C_1 g_{\text{mFF}}}{g_{\text{m1}} g_{\text{m2}}}} \quad (79)$$

$$z_5 = -\frac{1}{C_M (R_M - 1/g_{\text{mMP2}})} \quad (80)$$

In case (iii), z_1 and p_2 are out-band. z_1 will partially null the high frequency pole p_2 contributed by the degenerated transistor whereas z_2 and z_3 will partially cancel p_3 . Refer to the second-order term in (71), the complex poles are expressed in (78). Since C_1 and C_2 are parasitic capacitances and g_{mp2} is very large, the complex poles are easily located in high frequency. It is noted that the Q factor can be obtained as

$$Q = \frac{1}{C_M R_M} \sqrt{\frac{g_{\text{m2}} g_{\text{mY}} g_{\text{mMP2}} R_O}{C_1 C_2}} \quad (81)$$

Due to strong Miller effect in the main power transistor and reduction of R_O which is inversely proportional to I_L , this leads to reduction of gain peaking effect through lowering the Q factor. It has shown that R_M and C_M play the role to reduce and control the Q factor, which will mitigate the gain peaking effect.

The respective operating range for calculated poles and zeros are listed in Table 4.1. Figure 4.6 shows the corresponding plot to illustrate the relative location of poles and zeros in the loop gain response at three load current levels. As can be observed, the pole p_2 will be partially cancelled by the zero z_1 at different load currents whereas all the other non-dominant poles and the zero are located above the zero z_1 . Since the proposed work adopts the adaptive frequency compensation scheme, Table 4.2 summarizes the activities of different frequency compensation schemes at different load current levels. In light load current case, the TDFC is embedded to ensure the stability against the second non-dominant pole effect. In moderate load current case, the Q -reduction takes place to control the complex poles. In high load current case, due to increase of g_{mMP2} , the clash of high frequency poles contribute complex poles. Miller-RC compensation is employed to reduce Q factor of the complex poles.

Table 4.1 Poles and zeros location at three load current levels and $C_L = 100$ pF

Load Current Level					
Low		Moderate		High	
Parameter	Range	Parameter	Range	Parameter	Range
p_1	60 Hz-120 Hz	p_1	250 Hz-800 Hz	p_1	2 kHz-3 kHz
p_2	15 kHz-40 kHz	z_1	1.5 MHz-2.5 MHz	z_1	1.7 MHz-2.3 MHz
z_1	150 kHz-250 kHz	p_2	2 MHz-2.8 MHz	p_2	2.4 MHz-2.8 MHz
z_2	200 kHz-250 kHz	z_2	3.1 MHz-3.8 MHz	z_2	3.5 MHz-4.5 MHz
p_3	220 kHz-270 kHz	$ p_{3,4} $	8 MHz-10 MHz	p_3	5 MHz-6 MHz
p_4	320 kHz-350 kHz			$ p_{4,5} $	20 MHz-35 MHz

Figure 4.6 Poles and zeros in the loop gain response at three load current levels

Table 4.2 Summary of frequency compensation techniques at different load current levels

Load Current	Topology	TDFC	Q -reduction	Miller-RC
Low	2-Stage	On	Off	Off
Moderate	2-Stage	Strong	Strong	Weak
High	3-Stage	Strong	Weak	Strong

4.4 Stability Simulation Results

As discussed above, the simulation results are verified in the following.

Figure 4.7 (a) Loop gain and (b) Phase at different load currents

Figure 4.7 shows the loop gain and phase at different load currents. Figure 4.8 shows the Unity Gain Frequency (UGF), Phase Margin (PM) and Gain Margin (GM) against different load currents. It has shown that UGF can reach 2.2 MHz when the load current is increased to 1 mA and above, with a minimum value of 104 kHz at

no-load current condition. The PM has attained a minimum value of 45 degree at worst case of no-load current condition. However, it displays larger than 45 degree when load current conducts. Besides, the GM can achieve more than 6 dB when the load current exceeds 3 mA. This has validated that the system is stable with full load current range.

Figure 4.8 (a) UGF and (b) PM and (c) GM of the loop response for load current range from 0 to 100mA

Of particular noted, the stability of regulator can be maintained for the capacitive load ranging from 0 to 100 pF. Figure 4.9 shows the variation of GM and PM from zero load current to full load current at $CL=0$ pF, 50 pF, and 100 pF. As can be seen, the obtained minimum PM is about 46 degree and the minimum GM is about 6 dB. This satisfies the stability criteria. In addition, the GM and PM at the capacitive load

of 0pF, 50pF and 100 pF have confirmed that the regulator is stable in the C_L operating range from 0 to 100pF. Further corner simulations in a temperature range from -20 °C to 80 °C, the worst-case loop response, which happens at slow NMOS and slow PMOS corner at -20°C, displays PM of about 40 degree and GM of about 6 dB. This has validated that the regulator will be stable for full load current range across process corners and temperature corners. The details of the simulation results at different corners are shown in the Appendix.

Figure 4.9 PM, GM of the proposed regulator at different load currents and three capacitor loads of 0pF, 50pF and 100pF.

Chapter 5 Simulation Results and Discussions

In this chapter, simulation results will be shown and discussed. Table 5.1 summarizes the passive components used in the proposed work.

Table 5.1 Value of capacitive and resistive components

Component	Value	Component	Value
C_Y	2 pF	R_M	2 k Ω
C_X	1.3 pF	R_X	27.5 k Ω
C_Q	0.485 pF	$R_{a1,2}$	254 k Ω
C_M	2 pF	$C_{a1,2}$	0.356 pF

5.1 Steady-State Simulation Results

5.1.1 Load Regulation

Figure 5.1 Simulated output voltage against load current

Figure 5.1 depicts the dc output voltage against load current. For the maximum load current of 100 mA, the load regulation can be calculated as follows:

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_L} = \frac{3.82\text{mV}}{100\text{mA}} = 0.0382 \text{ mV/mA} \quad (82)$$

The calculation result is consistent with the transient simulation result.

5.1.2 Line Regulation

Figure 5.2 depicts the line regulation simulations for both zero-load current and full-load current.

Figure 5.2 Simulated line regulation for (a) $I_L = 0$ A and (b) $I_L = 100$ mA

The line regulation is calculated by dividing the largest dc output voltage variation caused by the change of supply voltage. The largest output variation occurs when the load current attains at its maximum value. Therefore, we have

$$\text{LNR} = \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} = \frac{0.6 \text{ mV}}{0.1 \text{ V}} = 6 \text{ mV/V} \quad (83)$$

5.1.3 Temperature Coefficient

Figure 5.3 Simulated output voltage drift against temperature

The temperature drift can be induced by the reference source or regulator circuit. In this simulation, the reference voltage is assumed as a constant voltage source whereas the circuit temperature drift is conducted on the basis of LDO regulator circuit itself.

When $I_L = 0$ A,

$$\text{T.C.} = \frac{1}{V_{\text{out}}} \times \frac{\Delta V_{\text{OUT}}}{\Delta \text{Temp}} = \frac{1}{1\text{V}} \times \frac{1.91\text{ mV}}{90^\circ\text{C} - (-40^\circ\text{C})} = 14.7\text{ ppm} \quad (84)$$

When $I_L = 100$ mA,

$$\text{T.C.} = \frac{1}{V_{\text{out}}} \times \frac{\Delta V_{\text{OUT}}}{\Delta \text{Temp}} = \frac{1}{1\text{V}} \times \frac{1.12\text{mV}}{90^\circ\text{C} - (-40^\circ\text{C})} = 8.6\text{ ppm} \quad (85)$$

5.1.4 Quiescent Current and Current Efficiency

Figure 5.4 Variation of I_Q against *load* current. According to (5), the current efficiency at full load current is 99.7 %.

Figure 5.4 Variation of I_Q against load current

5.2 Stability Simulations

5.2.1 Composite Transistor Pair Compensation

All the poles and zeros are moving towards lower frequencies at reduced quiescent bias, thus degrading the stability especially at the worst case of no-load current condition. The simulation results have shown that the PM is 39.6 degree / 45.6 degree without/with C_X and R_X in TDFC, respectively. This has validated the PM improvement using the TDFC scheme.

Figure 5.5 Loop gain and phase response at no-load current condition with/without C_X and R_X

5.2.2 Q-Reduction Compensation

During low-to-moderate load current transition, the complex poles will create a peaking effect in loop gain and contribute a sharp drop in loop phase. Therefore, the complex poles will degrade the phase margin in the loop response. It may cause oscillation in the transient response. Q-reduction compensation is therefore added to reduce the Q factor, hence minimizing the peaking effect. The simulation result for moderate load current appears at $I_L=1$ mA as shown in Figure 5.6. Without C_Q , the loop gain peak caused by the complex poles will be more than 0 dB while the corresponding phase is negative, causing negative PM. With the use of C_Q , the peak in loop gain is reduced to less than 0 dB, resulting in a stable loop response.

Figure 5.6 Loop gain and phase response at $I_L=1$ mA with/without Q-reduction C_Q

In order to demonstrate the effect of C_Q , the parametric stability simulation with load current from 0.5 mA to 30 mA is shown in Figure 5.7. It is apparent that without C_Q , the PM and GM are severely degraded in some of moderate load current range. The instability will cause potential oscillation in the circuit response. By adoption of C_Q , the peaking effect caused by the complex poles will be reduced, the adequate value of PM and GM ensure the stable loop response. Furthermore, the frequency of the complex pole will also be pushed to a higher value. Thus, the stability is ensured.

Figure 5.7 Comparison of (a) GM (b) PM (c) DC gain and (d) UGF with/without C_Q

5.2.3 Miller-RC Compensation

The Q-reduction compensation is adopted to control the Q factor during low-to-moderate load current. Pertaining to the high load current case, a Miller capacitor C_M in series with a nulling resistor R_M is added to improve the stability such that it avoids the peaking effect caused by the complex poles related to the parasitic effect from the gate of the auxiliary power transistor and the main power transistor. The simulation result with an example of $I_L = 50$ mA is shown in Figure 5.8. It is apparent that by adding the high-frequency Miller-RC compensation, the peak of the loop gain is suppressed and the phase does not drop sharply.

Figure 5.8 Loop gain and phase response at $I_L = 50$ mA with/without C_M and R_M

In order to demonstrate the effect of C_M and R_M , stability simulations with load current from 30 mA to 100 mA is depicted in Figure 5.9. It is clearly shown that

without C_M and R_M , the PM and GM are severely degraded in some of high load current range. C_M and R_M will help to reduce the peaking effect contributed by complex poles.

Figure 5.9 Comparison of (a) UGF (b) DC gain (c) PM and (d) GM with/without C_M and R_M

5.3 Transient Response Simulations

In transient response, undershoot and overshoot are very important parameters which are caused by sudden change in load current. Besides, overshoot and undershoot are also associated with settling time, which is another important parameter that evaluates the operation speed of the circuit. It refers to how fast the circuit can settle the output within the given error band. In evaluating the settling time in transient response, there are two important transient related parameters. They are the edge time and the step size of current change. The edge time, defined in (86), is the time difference when the load current I_L changes between 10% and 90% of its maximum value. Furthermore, the output variation will increase when edge time is small. The rise time or fall time is defined as follows:

$$t_{\text{rise}} = t_{\text{fall}} = \left| t_{90\%I_{L\text{max}}} - t_{10\%I_{L\text{max}}} \right| \quad (86)$$

where $t_{90\%I_{L\text{max}}}$ and $t_{10\%I_{L\text{max}}}$ denote the time when load current I_L achieves 90% and 10% of $I_{L\text{max}}$ respectively.

The worst case of change is when the load current changes from its zero-load current (0 A) to the maximum full load current $I_{L\text{max}}$ (100 mA). The simulation results of transient response will be evaluated at the edge time of load current of 300 ns. The error accuracy is based on 1%.

5.3.1 Transient Response with 0–100mA step at $C_L=100\text{pF}$

Figure 5.10 Simulated transient response with 0-100 mA load current step at $C_L = 100\text{ pF}$

The worst case transient response, which is based on maximum load current step, is illustrated in Figure 5.10. Both the rising and falling time of the load current are 300 ns. The undershoot and overshoot is 94.2 mV and 29.7 mV, respectively. The output will be settled in 2 μs when the load current changes from maximum to zero. The response time pertaining to undershoot is 340 ns when the regulator starts to regulate from zero to full-load current transition.

5.3.2 Transient response with 1-100mA step at $C_L=100\text{pF}$

Figure 5.11 Simulated transient response with 1-100 mA load current step at

$$C_L=100\text{ pF}$$

Figure 5.11 shows the transient response for the load current step between 1 and 100 mA. The undershoot and overshoot are obtained as 26.6 mV and 17.4 mV, respectively. The reduction in undershoot voltage is caused by the adaptively-biased current that increases the bandwidth of the feedback system.

5.3.3 Transient Response with 10-100mA Step at $C_L=100\text{pF}$

Figure 5.12 Simulated transient response with 10-100 mA load current step at

$$C_L = 100\text{pF}$$

The transient simulation results for the load step of 10-100 mA and 100-10mA are presented in Figure 5.12. The edge time of the load current is 300 ns. The results have shown the regulator is stable and the undershoot and overshoot voltages are obtained as 15.2 mV and 20.9 mV, respectively. The output will be settled within 2 μs .

5.3.4 Transient Response with C_X and R_X in TDFC

Figure 5.13 shows the comparison of load current transient responses with and without C_X and R_X . It can be observed that the overshoot is reduced from 52.68 mV to 29.7 mV due to faster input stage with transconductance boosting. It is mainly caused by the shorting effect of C_X under transient condition. As a result, it reduces the degeneration effect of the triode-biased transistor M_1 to the main input transistor M_3 as depicted in Fig. 3.3.

Figure 5.13 Comparison of transient responses with/without C_X and R_X in TDFC

5.3.5 Transient Response with Distributed Overshoot Reduction Circuit

With the proposed distributed overshoot reduction circuit, the discharge time of overshoot voltage spike can be reduced by 15%.

Figure 5.14 Improvement of transient response of the proposed DOVSR circuit
from the conventional counterpart

5.3.6 Improvement of Transient Response Using Proposed Circuit Techniques

Figure 5.15 shows the improvement of transient responses between the proposed C_X and R_X in TDFC technique incorporating DOVSR and the conventional counterpart using the transistor compensation and the standard overshoot reduction circuit. Figure 5.15 depicts transient responses pertaining to case (i) with OVSF circuit [54] and without C_X and R_X , case (ii) with DOVSR circuit and without C_X and R_X and case (iii) with DOVSR circuit and C_X and R_X . The simulation results have shown an overshoot of 62.43 mV and the settling time of 21.9 μ s with the OVSF circuit only. The proposed DOVSR circuit has enhanced the transient response with an overshoot of 52.6 mV and the settling time of 2.3 μ s. The combined technique of case (iii) has achieved an overshoot of 29.7 mV and 2 μ s settling time. It is evident that the C_X – R_X network provides fast loop bandwidth to reduce the overshoot, and this is correlated to the rapid G_{m1} enhancement as observed in Figure 3.9. Regarding the DOVSR circuit, not only does it provides larger discharge current for fast discharge of large capacitance at the output node, it also reduces the overshoot voltage.

Figure 5.15 Transient improvement by C_x and R_x in TDFC and DOVSR circuit

5.3.7 Transient Response with 0 – 100 mA step at $C_L = 100\text{pF}$ with $V_{DD} = 1.1\text{ V}$ and $V_{OUT} = 0.9\text{ V}$

At lower supply and lower regulator's output voltage as depicted in Figure 5.16. The overshoot voltage and undershoot voltage are increased under lower supply condition. According to the bias current generation as discussed in Chapter 3.3, the input supply voltage and output voltage will govern the headroom of the transistors. Further lowering the output voltage through the reduction of supply voltage, it will stress the bias transistors, hence reducing the bias current at no-load current condition and the slewing current at full-load current condition. Therefore, the voltage spikes appears to increase under lower supply and lower output voltage.

Figure 5.16 Simulated transient response with 0-100 mA load current step at

$$C_L=100\text{ pF}, V_{DD} = 1.1\text{ V and } V_{OUT} = 0.9\text{ V}$$

5.4 Power Supply Rejection (PSR)

Figure 5.17 Simulation results of PSR at different load currents

Figure 5.17 depicts the simulated power supply rejection (PSR) at different load currents at DC, 1 kHz, 10 kHz, and 100 kHz. The results are summarized in Table 5.2. It can be seen that the regulator can offer good PSR for the typical frequency range.

Table 5.2 Simulated PSR at different load currents

Load Current	PSR (dB) @ DC	PSR (dB) @ 1 kHz	PSR (dB) @ 10 kHz	PSR (dB) @ 100 kHz	PSR (dB) @ 1MHz
$I_L = 0 \text{ A}$	-87.89	-71.45	-51.24	-23	-22.18
$I_L = 1 \text{ mA}$	-52.64	-52.63	-52.62	-51.74	-37.58
$I_L = 10 \text{ mA}$	-52.11	-52.11	-52.1	-51.2	-36.98
$I_L = 100 \text{ mA}$	-47	-47	-46.82	-40.2	-22.3

Chapter 6 Measurement Results

6.1 Fabricated Chip and PCB

The proposed LDO regulator is fabricated and verified in AMS 0.18- μm CMOS technology. The microphotograph is shown in Figure 6.1, with all the sub-blocks indicated in the boxes. It has an estimated active area of 0.055 mm^2 . The printed circuit board (PCB) for prototype testing is shown in Figure 6.2

Figure 6.1 Microphotograph of the proposed LDO regulator

Figure 6.2 PCB for prototype testing

6.2 Measured Quiescent Current

The measured variation of quiescent current against different load currents is illustrated in Figure 6.3. Based on the current efficiency $\eta = I_L / (I_L + I_Q)$, the proposed work can attain $\eta = 99.75\%$ at full load current of 100 mA.

Figure 6.3 Measured variation of I_Q against load current

6.3 Measured Load Regulation

The output voltage at different load currents is measured and illustrated in Figure 6.4.

Figure 6.4 Measured output voltage against load current

According to (3), the load regulation can be calculated as follows:

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_L} \approx \frac{7.7 \text{ mV}}{100 \text{ mA}} = 0.077 \text{ mV/mA} \quad (87)$$

The obtained result is expected very good because of the use of multiple gain stage design in the proposed LDO regulator.

6.4 Measured Line Transient Response

The line transient performances are measured at no-load current condition and shown in Figure 6.5. The supply voltage V_{DD} changes at an edge time of $10\ \mu\text{s}$ and the regulator's output voltage is $1\ \text{V}$. As shown in Figure 6.5, when V_{DD} changes between $1.15\ \text{V}$ and $1.25\ \text{V}$, the largest output voltage spike is $787.6\ \mu\text{V}$

Figure 6.5 Measured line transient response with V_{DD} step between $1.15\ \text{V}$ and 1.25

V

6.5 Measured Load Transient Response

Figure 6.6 illustrates the load transient response with a load current step between 0 A and 100 mA. At the edge time of 300 ns, the measured undershoot and overshoot voltages are 117 mV and 35.33 mV, respectively. Based on 1% accuracy, the settling time is 1.56 μ s. It correlates well with the simulation result of 2 μ s as depicted in Figure 5.10. The voltage spike of 117mV undershoot is constrained by the bandwidth of the loop at no load current case. It is reasonable in view of ultra-low bias. The overshoot and settling time are improved by using the adaptively-biased topology, the DOSVR circuit and the TDFC technique.

Figure 6.6 Measured load transient response with 0-100mA load current step

The transient response of load current step between 1 mA to 100 mA is depicted in Figure 6.7. The overshoot and undershoot voltages are 27.88 mV and 18.75 mV, respectively. The improvement is the outcome of increasing bias currents to yield higher transconductance for bandwidth and faster slew rate at the internal and output nodes in the regulator.

Figure 6.7 Measured load transient response with 1-100mA load current step

6.6 Measured Power Supply Rejection

The measured PSR using a network analyzer is shown in Figure 6.8. The obtained PSR is -46.82 dB at 10 kHz and -37.7 dB at 1MHz. The measured results of PSR at different load currents and frequencies are summarized in Table 6.1

Figure 6.8 Measured PSR at $I_L=100$ mA

Table 6.1 Measured PSR at different load currents and frequencies

Load Current	PSR (dB) @ DC	PSR (dB) @ 1 kHz	PSR (dB) @ 10 kHz	PSR (dB) @ 100 kHz	PSR (dB) @ 1MHz
$I_L = 0$ A	-50.93	-53.1	-53.2	-30.68	-31.7
$I_L = 1$ mA	-47.86	-47.5	-48.2	-50.9	-34
$I_L = 10$ mA	-47.3	-47.2	-47.6	-50.5	-34.8
$I_L = 100$ mA	-46.82	-45.7	-45.9	-48.5	-37.8

6.7 Measured Noise

Figure 6.9 shows the measured noise spectrum of the regulator, it displays -121.45 dBm at 100 kHz.

Figure 6.9 Measured output spectral noise density of the proposed regulator

6.8 Comparison with Prior-Art Works

Table 6.2 summarizes the performance comparison of this work with that of the representative OCL-LDO regulators. From Table 6.2 , the proposed LDO regulator can achieve lowest quiescent current, good settling time under ultra-low quiescent bias and the best transient FOMs whilst offering other comparable performance metrics such as undershoot/overshoot, line regulation and load regulation. This has demonstrated the effectiveness of regulator architecture and circuit techniques.

Table 6.2 Performance comparison of the proposed LDO regulator with the reported works

Parameter	JSSC [42]	TCASII [56]	JSSC [30]	TCASII [44]	TCASI [37]	TCASII [22]	TVLSI [57]	JSSC [41]	TPE [58]	TCASII [59]	TPE [27]	This Work
Year	2005	2010	2010	2011	2012	2013	2014	2014	2016	2017	2018	2018
CMOS Technology (μm)	0.09	0.35	0.09	0.13	0.065	0.35	0.065	0.065	0.18	0.18	0.13	0.18
Chip Area (mm^2)	0.008	0.145	0.019	0.03	0.017	0.04	0.0133	0.0133	0.07	0.033	0.008	0.055
V_{DD} (V)	1.2	1.8-4.5	0.75-1.2	0.9	1.2	1.2	0.75-1.2	0.75-1.2	1.4	1.8	1-1.4	1.2
V_{OUT} (V)	0.9	1.6	0.5-1	0.8	1	1	0.5	0.55	1.2	1.6	0.8	1
V_{DO} (V)	0.3	0.2	0.2	0.1	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
$I_{Q(MIN)}$ (μA)	6000	20	8	1.33	0.9	1.2	16.2	15.9	0.61	71	112	0.407 [@]
$I_{L(MIN)}$ (mA)	0	0	3	0	0	0.1	0	0	0.01	0.2	0.12	0
$I_{L(MAX)}$ (mA)	100	100	100	50	100	100	50	50	100	100	25	100
C_T^* (pF)	N.A.	7	7	5 [*]	4.5	9	2	4.1	9	12.7	0.73	6.5
C_L (pF)	600	100	50	10000	100	100	100	470	100	100	25	100
Line Regulation (mV/V)	N.A.	0.0574	3.78	N.A.	4.7	N.A.	0.56	4	0.6	N.A.	2.25	0.283
Load Regulation (mV/mA)	0.9	0.109	0.1	N.A.	0.3	N.A.	6.67	0.18	0.27	N.A.	0.173	0.077
PSR (dB) Frequency (Hz)	N.A.	-40 @ 10k	-44 @ 1k	N.A.	-58 @ 10k	N.A.	-46 @ 1k	-51 @ 1k	-26 @ 1M	-76 @ 1M	-57 @ 1M	-37.7 @ 1M
$T_{\text{settle}}^{\#}$ (μs)	0.00054	9	4 [*]	28	6	2.7	1.2	0.25	7.7 [*]	0.2	0.19	1.56
ΔV_{OUT} (mV)	90	97	114	224.5 [*]	68.8	270	103	113	110	110	284	117
T_{edge} (ns)	0.1	100	100	200	300	N.A.	100	100	1000	100	0.3	300
Edge Time Ratio	1	1000	1000	2000	3000	N.A.	1000	1000	10000	1000	3	3000
FOM ₁ (mV)	5.4	19.4	9.12	11.9	1.8576	N.A.	33.4	35.94	6.71	78.1	3.82	1.42
FOM ₂ (fs)	32400	19.4	4.56	1194.34	0.6192	3.24	66.74	337.78	0.671	78.1	1272.3	0.475

* denotes the total on-chip capacitance. # denotes the settling time of the regulator on the basis of 1% accuracy. ※ denotes the estimated value from the reported works.

Chapter 7 Conclusion and Future Works

This Chapter draws the concluding remarks and describes the future works of this project.

7.1 Conclusion

Literature reviews are conducted on the conventional LDO regulators and the frequency compensation techniques. The design, analysis and implementation of a new CMOS output capacitor-less LDO regulator is presented in this work. By adopting the adaptively-biased on an improved adaptive-stage architecture and the employment of adaptive frequency compensation scheme which includes new transistor degeneration frequency compensation (TDFC), indirect feedback frequency compensation, Q-reduction based compensation and Miller-RC compensation, the regulator can achieve good stability under ultra-low quiescent power even in worse case of zero minimum load current. The proposed TDFC scheme also helps the transient overshoot reduction by g_m boosting in the degenerated input differential pair. Furthermore, a distributed overshoot reduction (DOVSR) circuit is also proposed. This effectively reduces both the overshoot voltage spike and the settling time in comparison to that of the conventional counterpart without the stated circuit. In conjunction with a fast feedforward path established in the architecture to provide dual functions of saving quiescent power in an economical way and enhancing negative feedback response, the regulator can achieve fast response time even biased at ultra-low quiescent condition. The performance comparison with the representative state-of-art works have confirmed the effectiveness of the proposed LDO regulator which has been verified and fabricated using AMS 0.18 μm CMOS technology.

7.2 Future Works

Although the current LDO regulator can achieve stability across all the operation conditions, sustainable loop response with stability needs to be addressed because it is critical to provide a stable transient response. One of the future works is to investigate the method for further improvement of the loop stability, particularly at zero load current condition. The rationale is that especially under variation of ultra-low quiescent current in the design, both the bias currents in the core circuit and the minimum load current at the output node will cause the poles and zeros moving to lower frequency and close to each other to degrade the phase margin. In this aspect, through the improvement method, it guarantees that the stability is enhanced all the time. Another future work is pertaining to the reduction of the undershoot voltage and the settling time, which are limited by the bandwidth and the slew rate at the internal nodes and the regulator's output node. An improved method is therefore needed for further enhancement. In this way, the regulator can provide reliable output voltage with sustainable fast transient response under ultra-low power operation.

List of Publication

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Appendix

A.1 Device Sizes and Parameters

The size of transistors and the value of passive components in the bias circuit are summarized in Table A.0.1.

Table A.0.1 Size of Components in bias circuit

Device	Size
$M_{B1,2}$	4/0.75
$M_{B3,4}$	4/0.18
M_{B5}	12/1.5
M_{B6}	3/1.5
$M_{B7,8}$	0.8/0.18
R_{B1}	706 k Ω
$C_{B1,B2}$	500 fF

The size of transistors in the core circuit are summarized in Table A.0.2.

Table A.0.2 Size of Components in core circuit

Device	Size ($\mu\text{m}/\mu\text{m}$)	Device	Size($\mu\text{m}/\mu\text{m}$)
$M_{1,2}$	10.4/0.5	M_{11}	13/1.2
$M_{3,4}$	19/0.42	M_{12}	62/0.75
$M_{5,6}$	2/0.75	M_{MP1}	60/0.18
M_7	2/0.18	M_{MP2}	5400/0.18
M_8	12/1.5	$M_{FB1,2,3}$	2/0.5
M_9	0.8/1.2	$M_{a1,a2}$	0.8/0.5
M_{10}	5.2/1.2		

The respective transconductance of devices at no-load (0 A), medium load (1 mA) and full-load (100 mA) current is summarized in Table A.0.3.

Table A.0.3 Parameters of the core circuit

Parameter	No-load current	Medium load current	Full-load current
g_{m1}	1.04 ($\mu\text{A/V}$)	17 ($\mu\text{A/V}$)	19 ($\mu\text{A/V}$)
g_{m2}	0	478 ($\mu\text{A/V}$)	487 ($\mu\text{A/V}$)
g_{MP1}	3.37 ($\mu\text{A/V}$)	4.2 (mA/V)	4.2 (mA/V)
g_{MP2}	0	8.6 (mA/V)	357 (mA/V)
g_{mFF}	0	0.7 (mA/V)	0.8 (mA/V)
g_{mB}	0	23.5 ($\mu\text{A/V}$)	25 ($\mu\text{A/V}$)
g_{mY}	2.9 ($\mu\text{A/V}$)	49.5 ($\mu\text{A/V}$)	54.6($\mu\text{A/V}$)

A.2 Corner Simulation Results

Figure A.0.1, Figure A.0.2, Figure A.0.3 and Figure A.0.4 show the stability simulation with the load current of 0 A, 1 mA, and 100 mA across ss and ff corners and temperature of -20 °C and 80 °C

Figure A.0.1 Stability simulation at ss corner and -20 °C

Figure A.0.2 Stability simulation at ss corner and 80 °C

Figure A.0.3 Stability simulation at ff corner and -20 °C

Figure A.0.4 Stability simulation at ff corner and 80 °C