Design and realization of high-performance LED drivers for automotive lighting applications

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2018

Qu, Y. (2018). Design and realization of high-performance LED drivers for automotive lighting applications. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/82740>

<https://doi.org/10.32657/10220/46654>

**Design and Realization of
High-Performance LED Drivers for
Automotive Lighting Applications**

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A thesis submitted to Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2018

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my supervisor, Professor Joseph Chang, who has been my advisor since 2012 when I was a research associate. The success of this Ph.D. research program would not have been possible without him. I am most grateful to him, not only for his scholarly guidance and insightful suggestions pertaining to the technical aspects in this research program, but also for his support throughout these years. Most importantly, I would like to thank him for imparting his knowledge and understanding of the philosophical aspects of life and research, which I believe are the most valuable part that anyone can ever hope for in a research program.

I would like to thank Dr. Shu Wei, who had offered his invaluable guidance as well as his kind support throughout this Ph.D. program. It has been both enjoyable and rewarding working with him.

I would like to thank all my friends. These years would not have been enjoyable and enriching without them.

Last but not least, I would like to thank my parents, who have been supportive of me throughout the years. I am also particularly grateful to my wife, who has always been unconditionally supportive and loving.

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SUMMARY

This Ph.D. program pertains to the design and monolithic realization of Light Emitting Diode (LED) drivers for automotive lighting where the imperative parameters are high power-efficiency and high reliability. The grand objectives thereto are substantial improved specifications over the state-of-the-art, including power-efficiency, reliability, current driving capability, and dimming range. To achieve the said grand objectives, the specific objectives are to decouple, and hence mitigate the following two major design trade-offs that limit the performance of contemporary automotive LED drivers.

The first trade-off is between high reliability and high current driving capability, and applies to both single-phase and multi-phase LED drivers. Specifically, to achieve high current driving capability, the contemporary single-phase LED driver typically suffers from low reliability arising from large current ripples. On the other hand, the multi-phase LED driver is highly advantageous to provide high current driving capability, but suffers from low reliability because of the ensuing subharmonic oscillation. To decouple this limiting trade-off, we propose the design and monolithic realization of a novel Pulse-Width-Modulation (PWM)-based dual-phase LED driver in Global Foundries (GF) 130nm BCDLite process. To achieve high current driving capability, we adopt a dual-phase power stage. To achieve high reliability, we propose an Average Current Control to eliminate the subharmonic oscillation by considering the complete inductor-current profile vis-à-vis peak current adopted/reported elsewhere. To further improve the reliability, we propose an accuracy-enhanced current sensor to ascertain good current balance in the adopted dual-phase power stage. With measurements on our prototype LED driver ICs embodying our aforesaid adoption and

proposed circuits, we demonstrate, to the best of our knowledge, for the first time that the trade-off between high reliability and high current driving capability is decoupled, i.e., an LED driver uniquely featuring high reliability, yet high current driving capability.

The second trade-off is between high power-efficiency and wide dimming range. Specifically, a wide dimming range is derived by means of high switching frequency, hence the ensuing reduced settling time of the LED current. This, however, in turn leads to a degradation of the power-efficiency due to increased switching losses. To decouple this limiting trade-off, we propose the design and monolithic realization of a novel fully soft-switched LED driver in GF 130nm BCDLite process. We achieve wide dimming range by operating at high switching frequencies, but the high switching does not compromise the power-efficiency. Using a fully soft-switching approach, the ensuing switching losses are negligible. This is achieved by a proposed Hysteretic Soft-Switching Controller (HSSC) and proposed circuitries, i.e., a voltage detector, current sensor, and a level shifter. The HSSC enables complete soft-switching, including zero-voltage switching and zero-current switching, by means of turning on/off power switches when their voltage/current is zero. The proposed voltage detector and current sensor, featuring low power, monitor the voltage and current of the power switches. The proposed level shifter, featuring ultra-fast speed, serves to quickly transmit the monitored signal from the said voltage detector and current sensor to the HSSC. With measurements on our prototype LED driver ICs embodying our proposed HSSC and proposed circuits, we demonstrate, to the best of our knowledge, for the first time that the trade-off between high power-efficiency and wide dimming range is decoupled, i.e., an LED driver uniquely featuring wide dimming range, yet high power-efficiency.

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NOMENCLATURE

ACC	Average Current Control
CMOS	Complementary Metal Oxide Semiconductor
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
HSSC	Hysteretic Soft-Switching Controller
GBW	Gain Band Width
LDMOS	Lateral Diffused Metal Oxide Semiconductor
LDNMOS	<i>n</i> -type LDMOS
LDPMOS	<i>p</i> -type LDMOS
LEB	Leading Edge Blanker
LED	Light Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	<i>n</i> -type MOSFET
PCB	Printed Circuit Board
PCC	Peak Current Control
PFM	Pulse Frequency Modulation
PMOS	<i>p</i> -type MOSFET
PWM	Pulse Width Modulation
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1 INTRODUCTION

1.1 MOTIVATION

Light Emitting Diode (LED) lighting is now routinely used over its fluorescent and incandescent counterparts for its luminous efficacy, reliability, and eco-friendliness [1], [2]. These LED lights are ubiquitous in automotive, consumer, and industrial lighting applications [3], [4]. For instance, Figure 1.1 depicts a typical automotive LED lighting system for a myriad of exterior lights such as the stop/tail lights, turn indicators, daytime running lights, headlights, etc. [5], [6]

Figure 1.1 A typical automotive LED lighting system

Unlike the traditional fluorescent and incandescent counterparts [7], which are voltage driven, LED lighting is current driven [8], [9]. This is evident in the LED I_V characteristics depicted in Figure 1.2, where a small 8% forward voltage increase, ΔV_F , leads to a large 110% LED current increase, ΔI_{LED} . The LED is driven by an LED driver.

Figure 1.2 Typical LED IV characteristics

The LED driver may be viewed as a type of dedicated DC-DC converter that functionally serves to convert the energy from a power rail (e.g., battery) to a predetermined and appropriate current for the LED load [10], [11]. Of the various LED lighting systems, it is well recognized that the design and realization of automotive LED drivers are challenging. This is because of their stringent requirements including high power-efficiency, high reliability, high current driving capability, and wide dimming range [8, 12, 13]. The mechanisms of these four requirements will now be delineated.

Power-efficiency is defined by the ratio of the useful power (delivered to the LED load) to the total power (drawn by the LED driver) [14]. A commonality in all LED drivers is the need for high power-efficiency. In general, the automotive is highly resource-constrained, including the often fully loaded battery (and alternator). For automotive lighting, it is imperative that its lighting is power-efficient [15].

The power losses in the LED lighting can be classified into the losses in the LED or in the LED driver. It is well established that the losses in the LED mainly comprise

two parts, photoelectric conversion loss [16] and device impedance loss. On the other hand, the losses in the LED driver include the switching loss, conduction loss, gate driving loss, inductor loss, etc. [17], [18]

Of the losses in the LED driver, the switching loss is typically the largest when the switching frequency is high ($\geq 1\text{MHz}$); we will explain later that high switching frequency is, at this juncture, prevalent due to the need for a wide dimming range. Not unexpectedly, the maximum frequency is limited because the large switching loss increases proportionally to the switching frequency [19]. In some reported cases, the approach adopted [18, 20-22] to improve the power-efficiency of the LED driver is to reduce the large switching loss. This, in our opinion, is an unattractive approach because the reported mitigation of losses is not very efficacious as the loss reduction is not over the entire load range; details will be delineated later.

Reliability is a measure of the consistency of the LED within specified performance limit and without degradation or failure [13]. A general requirement of LED drivers is the need for high reliability, particularly for automotive lighting because safety is always the highest priority in automotive applications.

The reliability of the LED light relies on two parts – the LED device and the LED driver. In the case of the LED device, the two primary parameters that affect its reliability are current ripple and temperature. From a broad perspective, the reliability of the LED device can be enhanced simply by employing an LED driver with a small current ripple and managing the heat, e.g., using a large heat sink to dissipate heat safely [23], [24]. In the case of the LED driver, the reliability issue is often more complex as the driver comprises several components which may be affected by a number of inter-related parameters, including stability, overshoot/undershoot, and component reliability

[13], [25]. For example, if the LED driver suffers from stability, e.g., subharmonic oscillation, the reliability of the LED driver be easily degraded because of the potential current/voltage overstress on the power transistors [26]. Not surprisingly, there is considerable effort within the LED driver design community to address this oscillation problem [27], [28]. Some efforts include the reported slope compensation [29] which mitigates the subharmonic oscillation. Nevertheless, this reported and other reported methods are unable to completely eliminate the subharmonic oscillation. Further, in general, these reported techniques are complex and the ensuing hardware overheads substantially complicate the LED driver design [30].

In general, an LED driver with high current driving capability is desirable as this provides for a wider application space [31]. Typically, the current driving capability of the LED driver depends on the power transistors which may be an on-chip integration or off-chip. In the case of the former, due to current limitation of bonding wires and the practical maximum number of bonding wires, the maximum drivable current of on-chip integrated power transistors is lower than the off-chip counterpart [26], [32]. On the other hand for the latter, as the power transistors are off-chip, there is no limitations associated with bonding wires. The LED driver can subsequently feature much higher current driving capability. Nevertheless, the off-chip power transistors are often bulky and suffer from large parasitic inductance/capacitance. These shortcomings typically compromise the form factor and potentially the power-efficiency [11].

To improve the current driving capability of the LED driver, the well-established multi-phase modality is often adopted over its single-phase counterpart [33]. Another advantage offered by the multi-phase modality is its inherent current ripple cancellation [34]. This feature is very worthy because large current ripples potentially degrade the reliability of LED devices [35].

The dimming range is defined as the brightness tuning range of the LED light [36]. In general, a wide dimming range is desirable to expand the application space. For instance for the automotive applications, the same set of LED lighting system (LED device and LED driver) may be applied for both tail light and brake light by means of operating at different brightness levels — full brightness for braking, and 10% to 25% of the maximum brightness (i.e., dimmed) for the tail light [8], [37]. In this example, the LED driver for the stop/tail light is required to provide a wide dimming range [38, 39].

In view of these four basic requirements and in the perspective of present-day design-art of LED drivers, the design of automotive LED drivers suffers from two trade-offs. First, high reliability and high current driving capability are often a trade-off because of the large current ripple in single-phase modality [40], [41] and the subharmonic oscillation in multi-phase modality [27], [28]. Second, high power-efficiency and wide dimming range are often a trade-off, where a wide dimming range requires a high switching frequency, hence the ensuing high switching losses [5], [16]. Consider now these trade-offs and the inadequacy of heretofore design approaches.

The first trade-off arises largely from the simultaneous need for high reliability and high current driving capability. LED drivers are based on either single-phase modality or multi-phase modality, and the reasons for the said trade-off in these two modalities are different. They will now be delineated.

The reliability of the single-phase LED driver with high current driving capability is often compromised [13, 31, 42, 43] because the ensuing current ripple is typically large (e.g., one-third of the average current) in the inductor. This, in turn, undesirably accelerates the aging of the LEDs where their power-efficiency degrades and their color

shifts [23], [24]. Although the large current ripple can be mitigated by the employment of a larger power inductor, there are undesirable compromises. Specifically, other than the higher associated cost and larger form-factor, the large power inductor with high DC resistance undesirably degrades the power-efficiency of the LED driver [31], [44].

Interestingly, although the well-established multi-phase modality can substantially reduce the current ripple, it is rarely adopted for LED drivers [33, 45-48]. Besides the ensuing higher cost of multiple inductors, this is mainly because state-of-the-art multi-phase LED drivers typically embody peak current control. This is the most widely used control scheme of Pulse Width Modulation (PWM), and suffers from two issues. First, the average output current is imprecise. This is because the peak current control regulates only the peak current of the inductor, whilst the other parameters, such as the inductance, input voltage and output current that could affect the average output current, are not regulated [3], [11]. Second, the peak current control suffers from subharmonic oscillation when the duty cycle is larger than 0.5. This renders the need for slope compensation which substantially complicates the design and reduces the robustness of the LED driver [29], [49]. Put simply, the reliability of the multi-phase LED driver is also often compromised because of the aforesaid two issues.

In short, a monolithic PWM-based single-phase or multi-phase LED driver with high current-accuracy and innate elimination of subharmonic oscillation remains unreported, and we will discuss this later.

The second trade-off is between the attributes of high power-efficiency and wide dimming range. Specifically, the wide dimming range is achieved by shortening the duration of the settling time — the time for the output LED current to settle to the predetermined value (from zero) once the dimming function is triggered [50]. The

common practice [38], [51] of shortening the settling time is to increase switching frequency of the LED driver which in turn leads to power-efficiency degradation due to increased switching losses [52], [53]. For example, Figure 1.3 depicts the switching losses in a typical hard-switching LED driver, where C_X is the capacitor that represents the sum of parasitic capacitors at the switching node V_X . V_{DS} and i_D within the dotted ellipse are the source-to-drain voltage and current of power switch M_P (or M_N), respectively. The switching losses comprise the transition losses on power switches (M_P and M_N) and the losses on C_X . When the switching frequency is increased from 500kHz to 2MHz, the ensuing settling time (that determines the dimming range) is typically two times shorter, but the switching losses increase by four times. This in turn undesirably increases the switching losses over the total power loss from ~10% to ~30%. Put simply, the improved dimming performance is often achieved with a severe compromise to the power-efficiency.

Figure 1.3 Switching losses in a typical hard-switching LED driver

To mitigate this second trade-off, it is imperative to reduce the excessive switching losses. In this respect, soft-switching [22], which involves turning on/off the

power switches only when their voltage/current is zero (depending on the specific circumstances, the current is zero, the voltage is zero, or both the current and voltage are zero), is advantageous over hard-switching [20, 21, 54]. Reported soft-switching techniques include Zero-Current Switching (ZCS) and Zero-Voltage Switching (ZVS) [18].

At this juncture of the LED driver design-art, fully soft-switching – the realization of soft-switching at every turn-on and turn-off of the power switches – cannot be obtained by means of either ZCS or ZVS for two reasons [55], [56]. First, although ZCS can be realized at the turn-on of the high-side switch and the turn-off of the low-side switch, it conversely cannot be realized at the turn-off of the high-side switch and at the turn-on of the low-side switch. This is because of the continuation of the inductor current [3]. Second, although ZVS can be realized at the turn-off of the high-side switch and at both the turn-on and the turn-off of the low-side switch, it conversely cannot be realized at the turn-on of the high-side switch. This is because of the continuation of the capacitor voltage at the switching node.

To enable both ZCS and ZVS, three circuitries, i.e., a current sensor [57], voltage detector [58], and a level shifter [59], are required. The current sensor and voltage detector are required to respectively sense the current and voltage of the power switches when the current/voltage is close to zero. The level shifter, on the other hand, is required to transmit these sensed signals to their respective controllers. For the design of these three circuits, the power consumption and speed are two key parameters [60]. Low power consumption is imperative because it may otherwise defeat the benefit of the elimination of the switching losses offered by the fully soft-switching. High speed, on the other hand, is imperative to provide a means of quickly turning on/off the power switches at the instance when the current/voltage of the power switches become

practically zero. Low speed would otherwise compromise the efficacy of the fully soft-switching [61].

Although a plethora of prior-art current sensors [62], voltage detectors [61] and level shifters [63] have been reported, they remain inadequate for three reasons. First, reported current sensors are often based on off-chip current-sensing by means of an external resistor, and dissipate relatively high power and occupy a relatively large PCB footprint [29], [64]. Second, state-of-the-art voltage detectors typically embody voltage dividers and window comparators, and dissipate relatively large power and suffer from a narrow detecting range [61]. This narrow detecting range undesirably reduces the input voltage range of the LED driver. Third, state-of-the-art level shifters often suffer from low speed due to the large parasitic capacitance of the high-voltage transistors adopted for high-voltage handling capability [65]. Put simply, a current sensor, voltage detector and a level shifter with low power and/or high speed attributes are highly desirable, and are largely unavailable/unreported.

In summary, the aforesaid two trade-offs somewhat severely compromise the performance of the LED driver for automotive lighting applications. Consequently, the stringent requirements – high power-efficiency, high reliability, high current driving capability, and wide dimming range – remain somewhat unsatisfactory, their full mechanisms are in our review, insufficiently well understood, and there are no avant-garde solutions. There are hence strong motivations to comprehensively investigate the switching and control mechanisms of LED drivers.

From a design perspective, there is a real need for innovative techniques/approaches to mitigate or decouple the ensuing above-mentioned design trade-offs that limit the simultaneous high power-efficiency, high reliability, high

current driving capability, and wide dimming range of present-day automotive LED drivers. The process of deriving these innovative techniques/approaches (vis-à-vis empirical approaches) would include analytical investigations to ascertain the mechanisms of the phenomenon/phenomena – that lead to limitations of the pertinent parameter(s) and its relationship with the other parameters within the trade-off of interest. These analytical investigations will also provide an analytical means to optimize the pertinent parameters, particularly in view of the said trade-offs.

1.2 OBJECTIVES

The broad objective of this Ph.D. program is to design and realize automotive LED drivers that simultaneously feature high power-efficiency, high reliability, high current driving capability, and wide dimming range, by means of novel architectures and/or techniques to mitigate or decouple the aforesaid trade-offs delineated in Section 1.1. The said design and realization are on the basis of analytical investigations (into the mechanisms of and the circuit parameters affecting the various specifications of LED drivers) and verified on the basis of measurements of monolithically realized LED driver prototypes embodying the said novel architectures and/or techniques.

The specific objectives are:

- (i) A comprehensive literature review of reported realizations of automotive LED drivers, including a critical appraisal of their merits and limitations/issues;
- (ii) An investigation into reported/prior-art automotive LED driver control methodologies, which is the most prevalent methodologies for the realization of

state-of-the-art LED drivers, with emphasis on their limitations, design trade-offs, and their associated attempts to mitigate these trade-offs;

- (iii) On the basis of (ii), the proposal of novel control methodologies and/or techniques for an LED driver that features mitigated or decoupled trade-off between the reliability (of the LED light) and high current driving capability. The reliability is to be derived by eliminating subharmonic oscillation and reducing current ripples. To obtain high current driving capability, the multi-phase modality approach is adopted. The specifications of the LED driver are tabulated in Table 1.1;

Table 1.1 Specifications of the proposed PWM-based dual-phase LED driver prototype

Parameter	Value
Process	GF 130nm BCDLite
Input Voltage	5-16V
Output Voltage (max)	10V
Output LED Current (max)	2.4A
Output LED Power (max)	24W
Switching Frequency	1MHz
Current Regulation Accuracy: Current Derivation	$\leq 5\%$
Current Ripple Factor	$\leq 10\%$
Peak Power-Efficiency	94%

- (iv) On the basis of (iii), to design and monolithically realize a PWM-based dual-phase LED driver prototype, and verify its performance, including benchmarking against its state-of-the-art counterparts;
- (v) On the basis of (ii), the proposal of novel techniques/topologies and circuitries for an LED driver that features mitigated or decoupled trade-off between high power-

efficiency and wide dimming range. The power-efficiency is to be derived by means of fully soft-switching and the wide dimming range by shortening the settling time. The specific specifications are tabulated in Table 1.2; and

Table 1.2 Specifications of the proposed fully soft-switched LED driver

Parameter	Value
Process	GF 130nm BCDLite
Input Voltage	6-18V
Output Voltage (max)	10V
Output LED Current (max)	1.3A
Output LED Power (max)	12W
Dimming Range at 20kHz Dimming Frequency	0.1-1
Settling Time	2 μ s
Maximum Switching Frequency	2.8MHz
Peak Power-Efficiency	96%

- (vi) On the basis of (v), to design and monolithically realize a fully soft-switched LED driver prototype, and verify its performance, including benchmarking against its state-of-the-art counterparts.

1.3 CONTRIBUTIONS

The contributions made in this Ph.D. research program are congruous to the specific objectives outlined above. Specifically, they are:

- (i) A comprehensive literature review of automotive LED drivers, including a critical appraisal of the imperative performance attributes pertaining to the design and monolithic realization of high-performance LED drivers featuring high power-

efficiency, high reliability, high current driving capability, and wide dimming range.

- (ii) Analytical investigations into the mechanism of control methodologies and design techniques for LED drivers in view of the aforesaid imperative performance attributes. The contributions herein include our mathematical derivation of expressions to provide an analytical means for ascertaining the power losses and the system stability.
- (iii) On the basis of (i) and (ii), an investigation into design trade-offs that compromise the performance of automotive LED drivers. Specifically, for the trade-off between high reliability and high current driving capability, we critically reviewed prior-art control methodologies and their limitations/issues. For the trade-off between high power-efficiency and wide dimming range, we critically reviewed conventional hard-switching mechanisms and their issues in terms of power losses. Prior-art reported attempts to mitigate these issues were also reviewed.

On the basis of (iii), two novel LED drivers – a novel PWM-based dual-phase LED driver and a novel fully soft-switched LED driver – are proposed, monolithically implemented, and physically verified. The pertinent contributions of the two LED drivers are as follows.

For the realization of the first LED driver – our proposed PWM-based dual-phase LED driver – our contributions include:

- (iv) Our proposal of a novel PWM-based dual-phase LED driver that features the decoupling of the trade-off between high reliability and high current driving

capability by means of eliminating the subharmonic oscillation and providing large output current with small current ripples; see Chapter 3 later.

The detailed contributions include the following:

- (a) The design and realization of a proposed novel Average Current Control (ACC) scheme that provides the elimination of the subharmonic oscillation and that features high accuracy of LED current regulation by considering the complete inductor-current profile vis-à-vis peak current adopted elsewhere,
 - (b) The design and realization of proposed novel accuracy-enhanced on-chip current sensors that are monolithically realized with the ACC and power transistors - to the best of our knowledge, the first-ever PWM-based dual-phase LED driver embodying on-chip current sensors. This is highly advantageous to the improvement of component reliability, and
 - (c) The design and monolithic realization of the dual-phase modality that features high reliability and high current driving capability.
- (v) The measurements of the prototype PWM-based dual-phase LED driver ICs realized using the GF 130nm BCDLite process, depicted that the proposed LED driver features an input voltage range of 5-16V, output to drive 1-3 series-connected LEDs, provides a current regulation accuracy of at least 96.2%, dimming frequency up to 20kHz, and features a peak power-efficiency of 94.7%, settling time of 5 μ s, LED current range of 0.4-2.4A and current-ripple factor of 8%. In short, the specifications tabulated in Table 1.1 are satisfied. When benchmarked against the state-of-the-art LED drivers (see Section 3.3 later), our design features the largest current driving capability, yet with the lowest current-

ripple factor. In short, the measurements and benchmark depict the decoupling of the said trade-off between high reliability and high current driving capability.

For the realization of the second LED driver – our proposed fully soft-switched LED driver – our contributions include:

- (vi) Our proposal of a fully soft-switched LED driver that provides the decoupling of trade-off between high power-efficiency and wide dimming range by substantially eliminating the switching losses, i.e., the switching losses are negligible. The said fully soft-switching is achieved by the realization of both Zero-Current Switching (ZCS) and Zero-Voltage Switching (ZVS); see Chapter 4 later.

The detailed contributions include the following:

- (a) The design and realization of a proposed novel Hysteretic Soft-Switching Controller (HSSC) that turns on/off the power switches at zero voltage/current to achieve complete soft-switching,
- (b) The design and realization of a proposed novel current sensor that provides low power and small form factor by employing on-chip current-sensing,
- (c) The design and realization of a proposed novel voltage detector that exhibits low power and wide detecting range by employing the voltage pre-biasing technique, and
- (d) The design and realization of a proposed novel level shifter that offers ultra-fast speed and zero quiescent current by means of leveraging on a floating capacitor that provides high voltage handling capability, and its digital operation mechanism.

- (vii) The measurements of the prototype fully soft-switched LED driver ICs realized using the GF 130nm BCDLite process, depicted that the proposed LED driver features 6-18V input voltage range, output current of 0.5-1.3A, drives 1-3 series-connected LEDs, 12W maximum output power, 2.8MHz maximum switching frequency, 96.1% peak power-efficiency, 1.4 μ s settling time, and 0.08-1 dimming range at 20kHz dimming frequency. In short, the specifications in Table 1.2 are satisfied. When benchmarked against state-of-the-art LED drivers (see Section 4.3 later), our design simultaneously features the widest dimming range, shortest settling time, and requires the smallest inductor. In short, the measurements and benchmark depict the decoupling of the said trade-off between high power-efficiency and wide dimming range.

From an overall perspective, the contributions herein provide useful insight to automotive LED driver designers into the pertinent mechanisms of power-efficiency, reliability, current driving capability, and dimming range. The contributions also provide analytical and practical means to mitigate design trade-offs and to optimize the various pertinent parameters of LED drivers to meet a given set of specifications.

1.4 THESIS ORGANIZATION

The subsequent chapters of this thesis are organized in the following manner.

Chapter 1 presented the introduction of this project, including the motivation, objectives, and contributions.

Chapter 2 presents a comprehensive literature review of various design techniques and control methodologies for automotive LED drivers. The emphasis of the review is a critical review on the limitations/trade-offs of these design techniques and control methodologies, and on the inadequacy of reported state-of-art work to mitigate these limitations/trade-offs.

Chapter 3 presents the design and realization of our proposed PWM-based dual-phase LED driver featuring the decoupling of the trade-offs between high reliability and high current driving capability for automotive lighting. To the best of our knowledge, this is the first-ever monolithically integrated PWM-based LED driver embodying the LED driver and accuracy-enhanced on-chip current sensors. In this chapter, the system architecture is introduced first, followed by the detailed explanation of the proposed Average Current Control (ACC) and the proposed accuracy-enhanced on-chip current sensors. Finally, the measurements and benchmarking are presented, followed by the conclusions.

Chapter 4 presents the design and realization of our proposed fully soft-switched LED driver featuring the high power-efficiency and wide dimming range by decoupling of the trade-off. In this chapter, the system architecture is first introduced, followed by the explanation of proposed Hysteretic Soft-Switching Controller (HSSC) and the critical building blocks including the proposed circuit – current sensor, voltage detector, and level shifter. Finally, the measurements and benchmarking are presented, followed by the conclusions.

Chapter 5 draws the conclusions of this thesis and suggests recommendations for future work.

Chapter 2 LITERATURE REVIEW

This chapter provides a comprehensive and critical review of the LED drivers for automotive lighting applications and it serves as a preamble to our contributions delineated in the following chapters.

This literature review is arranged in the following fashion. In Section 2.1, an overview of automotive LED lights in terms of installation and function is provided. This overview discusses the wide implementation of LEDs in automotive lighting systems. In Section 2.2, an overview of the key design parameters, including power-efficiency, reliability, dimming range, settling time, and Electro-Magnetic Interference (EMI), is presented. This overview explains why these parameters are critical to automotive LED lighting and summarizes the pertinent design approaches. In Section 2.3, an overview of the circuitry blocks – output power stage, dead-time circuit, current sensor, voltage detector and level shifter – is described. In Section 2.4, a comprehensive review of modulation schemes, including Pulse Frequency Modulation (PFM), Pulse Width Modulation (PWM) and digital control, is conducted. Their features and shortcomings are summarized and compared. Section 2.5 presents our derivations of analytical expressions for the stability analysis and small-signal modeling of LED drivers, followed by conclusions in Section 2.6.

2.1 OVERVIEW OF AUTOMOTIVE LED LIGHTS

Automotive LED lights are typically mounted or integrated to the front, lateral, and rear of automobiles to provide lighting/signaling for drivers and pedestrians [8], [12]. Figure 2.1 depicts the LED lights in a typical automotive lighting system, where

the automotive LED lights can be classified into three categories – exterior, interior, and infotainment lights – according to their installation and function [6].

Figure 2.1 LED lights in a typical automotive lighting system

In this section, a review of the exterior, interior and the infotainment lights will be delineated in turn, followed by pertinent design techniques and considerations pertaining to the detailed implementation.

2.1.1 Exterior Lights

As depicted in Figure 2.1, a typical automotive LED lighting system embodies a myriad of exterior lights such as the headlight, daytime running light, stop/tail light, turn

indicator, etc. These exterior lights often employ switched-mode LED drivers shown in Figure 2.2, vis-à-vis linear counterparts, for substantially higher power-efficiency and higher power handling capability [37].

Figure 2.2 Block diagram of a typical switched-mode LED driver

The exterior lights typically employ step-down (i.e., buck topology) for higher power-efficiency, wider dimming range, and robustness, save the high-power headlight (e.g., $\geq 40\text{W}$) that often employs step-up (i.e., boost topology) to achieve relatively low output current (e.g., 1A) for reliability [62], [66].

Besides the electrical and optical performance of the exterior lights, their reliability must be ascertained in consideration of its operation in harsh environments, including climatic and physical factors. Climatic factors, including ambient temperature, air moisture and salt content, greatly impact the reliability of the exterior lights [66]. Physical factors, including vibration, shock and impact stresses, also potentially affect the reliability of the exterior lights [37].

2.1.2 Interior Lights

As depicted in Figure 2.1, a typical automotive LED lighting system also embodies various interior lights, including the dome light and the console light. Because

of their low power rating, the interior lights typically employ linear LED drivers shown in Figure 2.3, vis-à-vis aforesaid switched-mode counterparts, for sake of smaller form factor and lower cost [67].

Figure 2.3 Schematic of a typical linear LED driver

The modus operandi of the linear LED driver is simple. If the LED current, i_{LED} , slightly exceeds a predetermined value, V_{REF}/R_S , the amplifier correspondingly reduces its output voltage and subsequently reduces the current passing through the power transistor, M_N . The amplifier and the power transistor comprise a negative feedback loop which accurately regulates the LED current, $i_{LED} = V_{REF}/R_S$.

The benefits of the linear LED driver include high accuracy, small form factor, and low cost, whilst its main shortcoming is low power-efficiency and low power handling capability.

2.1.3 Infotainment Lights

As depicted in Figure 2.1, a typical automotive LED lighting system also embodies various infotainment lights, including the Liquid Crystal Display (LCD)

backlight and the reading light. The infotainment lights typically employ either the linear LED drivers in Figure 2.3 or the combination of the switched-mode and the linear LED drivers, according to the specific applications [66]. Consider the LED driver for LCD backlight as a case in point.

Figure 2.4 depicts the block diagram of a typical combined LED driver for display backlighting [38]. The switched-mode LED driver serves to boost the input low voltage (e.g., $V_{IN}=12V$) to output high voltage (e.g., $V_O=36V$) and the linear LED driver [66] serves to precisely regulate the LED current, i_{LED} . The dimming function is obtained by means of the dimming clocks for switches S_1 and S_2 . This combined LED driver features high current regulation accuracy and wide dimming range. However, it suffers from low power-efficiency because of the large forward voltage drop across diode D_1 and the overhead voltage drop on the linear LED driver [43].

Figure 2.4 Block diagram of a typical combined LED driver for display backlighting

In summary, an automotive lighting system typically embodies dozens of LED lights in a contemporary automobile. These lights with various functions have stringent requirements for the LED drivers, and we will delineate their key design parameters in the following section.

2.2 OVERVIEW OF DESIGN PARAMETERS

In this section, a review of the critical design parameters for automotive LED drivers will be delineated, followed by detailed reported design techniques and considerations pertaining to these design parameters. In the case of automotive lighting applications, the imperative requirements include high power-efficiency, high reliability, wide dimming range, low EMI, etc. They will now be delineated in turn.

2.2.1 Power-efficiency

Power-efficiency is defined by the ratio of the useful power (delivered to the LED load) to the total power (drawn by the LED driver). Generally, it is desirable for all LED drivers to be highly power-efficient. This power-efficiency is highly imperative in automotive applications as the automotive is highly resource-constraint, including the often fully loaded battery (and alternator) [68-70].

The power losses of the LED lighting can be classified into the losses in the LED or in the LED driver. Consider these in turn.

A. Power Losses in the LED

The power losses in the LED mainly comprise two parts, photoelectric conversion loss [39] and device impedance loss. It is well established that one of the most straightforward methods to reduce the former loss is to employ high-performance LEDs. For the latter loss, it can be desirably reduced by means of providing a driving current with small current ripples.

Figure 2.5(a) depicts the approximate-linear LED model, where D_1 is an ideal diode, V_F the forward voltage drop, and r is the sum of the internal series resistance, bond-wire resistance and connection resistance. Figure 2.5(b) depicts a typical LED current with large current ripple, where the average current is 2A, the peak 3A, and the valley is 1A.

Figure 2.5 (a) approximate-linear LED model, (b) a typical LED current with large current ripples

The LED current with large current ripples, ΔI , causes added power loss, P_X , on r , when compared to a constant current, I_{CON} . We can easily derive P_X over the constant power loss P_{CON} as

$$\frac{\int_0^T [(\frac{I_{PK} - I_{VY}}{T}) \cdot t + I_{VY}]^2 \cdot \gamma dt}{I_{AVG}^2 \cdot \gamma \cdot T} - 1 = \frac{1}{3} \left(\frac{\Delta I}{I_{AVG}} \right)^2 \times 100\% \quad (2.1)$$

where I_{PK} is the peak of the LED current,

I_{VY} the valley of the LED current,

T one switching cycle,

r the internal resistance of the LED device,

I_{AVG} the average of the LED current, and

$$\Delta I = I_{PK} - I_{VY}.$$

Equation 2.1 depicts that an added 33% power loss will be dissipated on r when $\Delta I = I_{AVG}$. For the case where $r = 3\Omega$ and the thermal resistance is 2.5°C/W [23], [71], the added power loss P_X leads to a temperature increase ΔT around 10°C . This ΔT results in severe consequences to the LED reliability – the LED lifetime is typically shortened by $\sim 10\%$. These large current ripples not only degrade the power-efficiency, but also accelerate the LED aging due to the increase in temperature (see Section 2.2.2 later).

B. Power Losses in the LED Driver

The power losses in the LED driver include the switching loss, conduction loss, gate driving loss, inductor loss, etc. [9], where the former three are dissipated in power switches (transistors). Consider now these losses.

Switching loss

Of the losses in the LED driver, the switching loss is typically the largest when the switching frequency is high ($\geq 1\text{MHz}$) [72]. Not unexpectedly, the maximum

frequency is limited because the large switching loss increases proportionally to the switching frequency.

Figure 2.6 depicts the switching loss in the typical hard-switching LED driver, where C_X is the capacitor that represents the sum of parasitic capacitors at the switching node V_X , and V_{MP} and i_{MP} are the source-to-drain voltage and current of power switch M_P , respectively. V_{MN} and i_{MN} are the drain-to-source voltage and current of power switch M_N , respectively. The switching loss consists of two portions: the loss on C_X and the transition loss on M_P and M_N . It is straightforward to approximate the switching loss, P_{SW} , as

$$P_{SW} = 0.5C_X \cdot V_{IN}^2 \cdot f_{SW} + 0.5V_{IN} \cdot I_L \cdot (t_R + t_F) \cdot f_{SW} \quad (2.2)$$

where V_{IN} is the input voltage,

I_L the inductor current,

t_R the rising time during transitions at the switching node V_X , and

t_F is the falling time during transitions at the switching node V_X .

Figure 2.6 Switching loss in the typical hard-switching LED driver

Equation 2.2 depicts that the switching loss is proportional to the switching frequency, f_{sw} . This results in large switching loss in the hard-switching LED drivers, particularly at high switching frequencies ($\geq 1\text{MHz}$).

It is well recognized that transformer-based converters, including the LLC converter [73] and the flyback converter [74], can easily achieve fully soft-switching [75]. However, due to their adoption of bulky transformers, they often suffer from complicated hardware realization and large form-factor [41]. In contrast, the inductor-based buck-type LED driver features small form-factor and low cost.

Conduction Loss

Besides the aforesaid switching loss, the conduction loss in the power switches is also large, and can be easily derived as

$$P_{ON} \approx I_L^2 \cdot [D \cdot R_{ON_P} + (1-D) \cdot R_{ON_N}] \quad (2.3)$$

where I_L is the inductor current,

D the duty cycle of the control signal,

R_{ON_P} the on-resistance of the power switch M_P in output power stage, and

R_{ON_N} is the on-resistance of the power switch M_N in output power stage.

Equation 2.3 depicts that the conduction loss is proportional to the on-resistance of power switches. Consequently, one of the most straightforward approaches to reduce the conduction loss is to employ power switches featuring low on-resistance.

Gate Driving Loss

Another large power loss in the power switches is the gate driving loss, which can be easily derived as

$$P_{GS} \approx (C_{GS_MP} + C_{GS_MN}) \cdot V_{DDL}^2 \cdot f_{SW} \quad (2.4)$$

where C_{GS_MP} is the gate capacitance of the power switch M_P ,

C_{GS_MN} the gate capacitance of the power switch M_N ,

V_{DDL} the gate driving voltage, and

f_{SW} is the switching frequency of the LED driver.

Besides the switching loss and conduction loss, the power switches also suffer from a gate driving loss as expressed in Equation 2.4. Because P_{GS} is proportional to the square of V_{DDL} , some reported design techniques (e.g., adaptive voltage scaling [53, 76, 77]) are proposed to reduce P_{GS} by means of adjusting V_{DDL} . These approaches are efficacious in low-power LED drivers (<10W) but their efficacy diminishes in high-power applications because of the somewhat unexpected increasing conduction loss [78].

Inductor Loss

In some reported cases [17], [19], the power losses in the LED driver may be dominated by the inductor loss. This loss can be easily derived as

$$P_L \approx I_L^2 \cdot DCR + P_M \quad (2.5)$$

where I_L is the inductor current,

DCR the direct current resistance of the inductor, and

P_M is the magnetic-core loss of the inductor.

Equation 2.5 depicts that the inductor loss is a result of the DC Resistance (DCR) of the winding and the magnetic-core loss. Typically, the inductor loss is reduced by increasing the switching frequency, and employing a small inductor. This is because the small inductor requires fewer turns of winding and provides a low DCR.

2.2.2 Reliability

Reliability is a measure of the consistency of the LED with specified performance and without degradation or failure. A general requirement of the LED drivers is the need for high reliability, particularly for automotive lighting, because, as delineated earlier, safety is always the highest priority in automotive applications [13].

The reliability of the LED light relies on two parts – the LED device and the LED driver. They will now be delineated in turn.

A. *LED Device Reliability*

In the case of the LED device, the two primary parameters that affect its reliability are current ripple and temperature. As discussed earlier, the LED load is a current-driven device. The current ripple is a key parameter for the LED reliability in terms of thermal degradation and color shift.

Figure 2.7 depicts the typical dominant wavelength shift with different LED forward currents at room temperature of 25° [71]. It can be seen that the wavelength of the LED light, including blue, green, yellow and red, varies with different forward LED currents. Consequently, the forward current with large current ripples undesirably accelerates the LED color shift by means of shifting its ensuing dominant wavelength.

As discussed in Section 1.1, the multi-phase modality features advantages over the single-phase counterpart because of the reduced current ripple. The input and output current ripples are substantially mitigated due to the current ripple cancellation [79], [80]. Figure 2.8(a) and (b) depict the cancellation of input and output normalized current ripples, respectively, in multi-phase LED drivers [81]. It can be seen that the input and

output normalized current ripples in multi-phase modality, including 2-phase and 4-phase, get substantially reduced, particularly when the duty cycle is approximately 0.5.

Figure 2.7 Typical dominant wavelength shift with different LED forward currents at room temperature of 25°

Figure 2.8 Current ripple cancellation in multi-phase LED drivers: (a) input current, and (b) output current

Besides the above-mentioned current ripples, the temperature is another key parameter that degrades the reliability of LED devices, where color shift becomes increasingly obvious [71]. Figure 2.9 depicts the typical dominant wavelength shift with different case temperatures. When the temperature increases, the dominant wavelength shift becomes more serious. In other words, good thermal dissipation is critical to LED reliability.

Figure 2.9 Typical dominant wavelength shift with different case temperatures

In summary, the reliability of the LED device can be enhanced simply by employing an LED driver with small current ripple and managing the heat, e.g., using a large heat sink to dissipate the heat safely.

B. LED Driver Reliability

In the case of the LED driver, the reliability issue is more complex as the driver comprises several components which may be affected by a number of inter-related parameters, including stability, overshoot/undershoot, and component reliability [42], [82].

In most scenarios, the failure of an LED driver is because of the breakdown of power transistors, which can be classified into three scenarios.

First, if the LED driver suffers from stability issue, e.g., subharmonic oscillation, the reliability of the power transistors would easily get degraded. This is mainly because of the potential current/voltage overstress on power transistors [25].

Second, if the LED driver with multi-phase modality suffers from current imbalance issue, the power transistors would also get easily degraded. This is mainly because of the extra power loss caused by the unbalanced current [83].

Third, the parasitic inductance/capacitance at the switching node may introduce large overshoot and undershoot. Once the overshoot/undershoot voltage is beyond the breakdown voltage of the power transistors, it subsequently results in failure of the power transistors [4]. It is well recognized that monolithic integration shows privileges in parasitic inductance/capacitance minimization [9].

Based on the above discussion, we can draw the conclusion that good stability, good current balance and minimized parasitic inductance/capacitance are beneficial to the reliability of power transistors and subsequently improve the reliability of the LED driver.

2.2.3 Dimming Range

The dimming range is defined as the brightness tuning range of the LED light. In general, a wide dimming range is desirable as this expands the application space [84]. For example, for the automotive application, the same set of LED light (LED device and LED driver) may be applied for both the tail light and the brake light by means of

operating it at different brightness levels – full brightness for braking, and 10% to 25% of the maximum brightness (i.e., dimmed) for the tail light [37].

The topologies of dimmable LED drivers can be generally classified into either off-chip dimming or on-chip inherent dimming [35]. They will now be delineated in turn.

The off-chip dimming topology is prevalent in contemporary backlighting systems for Liquid Crystal Displays due to its ensuing wide dimming range [82]. Figure 2.10 depicts a typical block diagram of the LED driver with off-chip dimming, where power switch M_D is controlled by the dimming signal, DIM . This off-chip dimming topology features high dimming accuracy and wide dimming range [43]. However, it suffers from low power-efficiency and as expected, it is inappropriate for automotive applications. This low power-efficiency is because the LED driver provides a constant voltage output and the output voltage (i.e., V_O) is required to offer a large voltage headroom for the LEDs.

Figure 2.10 A typical block diagram of the LED driver with off-chip dimming

The on-chip inherent dimming is widely adopted by automotive lighting systems largely because of its high power-efficiency, and small form factor because of its monolithic integration [85]. Figure 2.11 depicts the block diagram of the LED driver with on-chip inherent dimming. Unlike the off-chip dimming, the LED driver with on-chip inherent dimming provides a constant current output and subsequently requires a small output capacitor (C_o) [38].

Figure 2.11 Block diagram of the LED driver with on-chip inherent dimming

2.2.4 Settling Time

Settling time is defined as the time for the output LED current to settle to the determined value (from zero) once the dimming function is triggered [50], [86]. Settling time is imperative to the dimming performance of the LED driver because a wide dimming range is often achieved by shortening the settling time. The desirable short settling time of the LED driver can be improved by the following four approaches [87], [88] that are switching frequency, output low-pass filter, control methodology, and multi-phase modality. Consider these in turn.

A. Switching Frequency

One of the most straightforward approaches to reduce the settling time is to increase the switching frequency. This is mainly because of its ensuing higher Gain Band Width (GBW) and larger inductor-current slew rate [31].

B. Output Low-Pass Filter

The bandwidth of output *LC* low-pass filter is critical to the transient response of the LED driver and subsequently the settling time [89]. Specifically, a large output inductor and capacitor provide for a small inductor-current slew rate and a small output voltage change rate, respectively. Because of this, the LED driver featuring fast settling time and wide dimming range often embodies small values of output inductors and capacitors [56].

C. Control Methodology

The control methodology is also critical to the settling time. In terms of control for the settling time, the Pulse Frequency Modulation (PFM) is highly advantageous over the Pulse Width Modulation (PWM). This is because the LED driver with energy-demand PFM control typically settles within one or two switching cycles [68]. Conversely, the LED driver with PWM control often requires at least five switching cycles to settle due to its low crossover frequency that is judiciously selected around one-fifth of the switching frequency [75].

D. Multi-phase Modality

The *N*-phase modality can generally reduce the settling time of the LED driver by *N* times because of the parallel operation [86], [90]. Figure 2.12 depicts the block

diagram of the LED driver with multi-phase modality, where V_{IN} is the input voltage, V_O the output voltage, PWM_1 , PWM_2 , and PWM_N are the control signals for power stage 1, 2, N , respectively. The multi-phase LED driver operates in an interleaving mode with a phase shift of $180^\circ/N$. Subsequently, the effective switching frequency of the LED driver is N times higher and the settling time is shortened up to N times.

Figure 2.12 Block diagram of the LED driver with multi-phase modality

2.2.5 Electro-Magnetic Interference (EMI)

EMI may undesirably disrupt the operation of an electronic device when it is in the vicinity of an electromagnetic field (in the frequency spectrum) generated by another electronic device [13]. Low EMI is imperative because switched-mode LED drivers typically generate severe EMI, which potentially affects the electronics in close proximity.

In theory, EMI is generated either by an instantaneous change in current resulting in a magnetic field or by a differential voltage resulting in an electric field [91]. Figure 2.13 depicts the sensitive current loops in the LED driver including two sensitive current loops and two high di/dt areas. Loop 1 is formed during the on-time of the high-side

power switch (M_P). The current flow originates from the input capacitor, C_{IN} , and finally returns to C_{IN} after passing through M_P , the output inductor (L_1) and the output capacitor (C_O). When M_P is turned off and M_N is turned on, loop 2 is formed, where the energy stored in the inductor flows through C_O and M_N .

Figure 2.13 Sensitive current loops in the LED driver

Area A is formed from the nonoverlapped area of these two loops. It is worthwhile to note that area A is an area with high di/dt because large high-frequency AC currents flow on the boundary traces of area A. These high-frequency currents are the main sources of far-field EMI, while the high-frequency voltage changes are contributing to near-field EMI [72]. Area B is located at the switching node, V_X , where the output inductor, low-side and high-side power switches are connected. Area B creates EMI in two ways. First, the large voltage swings capacitively couples to other traces. Second, the area itself radiates due to the high switching currents [92].

It is well known that the EMI [12] can be classified into two categories, radiated EMI and conducted EMI.

Radiated EMI

Radiated EMI is often challenging for automotive LED drivers because of the stringent requirements of the radiated EMI for automotive applications [91], [93]. There are in general three reported methods [13, 94, 95] to mitigate the radiated EMI. First, radiated EMI can be mitigated by means of minimizing the length/area of aforesaid sensitive current loops (Figure 2.13) and high di/dt areas to reduce the loop antenna effect [96]. This is a classical approach to reduce EMI because the strength of EMI is related to loop area and the proximity of loops. In the case of LED drivers, the output low-pass filter should be laid out as compactly as possible and kept close to the power stage. Hence, a monolithic integration would mitigate radiated EMI [9].

Second, radiated EMI can be mitigated by the adoption of superior control methodology, where for automotive lighting applications, these would be based on either PFM or PWM. Reported PFM offers hardware and design simplicity [97]. However, because of its variable switching frequency, PFM generates wide and unpredictable EMI spectrum. On the other hand, the EMI of PWM is more easily mitigated because arising from its fixed switching frequency, its EMI is predictable, and the spectrum is relatively narrow [36].

Third, thermal case shielding is highly effective to mitigate the radiated EMI by means of blocking the electromagnetic field with barriers of conductive or magnetic materials [93]. The amount of reduction typically depends on the material used, the thickness, and the size of the shielded volume. Practically, EMI shielding is usually a last resort in view of the added expense.

Conducted EMI

Conducted EMI arises from high-frequency noise conducted from the LED driver to the input leads of the power supply [67]. For example, the input capacitor C_{IN} in Figure 2.13 plays a critical role in supplying high-frequency currents to the LED driver. The high-frequency noise that C_{IN} is unable to bypass will be conducted into the input leads of the power supply, resulting in conducted EMI.

Conducted EMI can be classified into either differential mode or common mode. In a typical IC based non-isolated LED driver, only two lines are connected to the input port. Hence, any current going in through one terminal must go out through the other. In this configuration, the common-mode noise of the LED driver is theoretically negligible [8]. In view of this, the focus in this thesis is on the mitigation of differential-mode noise, e.g., input and output current ripples.

2.3 OVERVIEW OF CIRCUITRY BLOCKS

An automotive LED driver typically comprises an output power stage, dead-time circuit, controller, and a current sensor for LED current regulation. Some LED drivers further comprise voltage detectors for adaptive dead-time control, and level shifters for signal transitions from the current sensors (or the voltage detectors) to the controller. We will now review design techniques and considerations pertaining to these circuitry blocks in automotive LED drivers.

2.3.1 Output Power Stage

The output power stage in the LED driver serves to provide sufficient driving capability to drive the LED loads, typically of high-impedance with a desirable constant-current output [14], [98]. It is a critical part of the LED driver because it not only occupies a large silicon area but also consumes a significant portion of the total power loss. For instance, in a reported LED driver [50] that drives a 26W output LED load, the output stage occupies over 60% of the active area and dissipates over 90% of the total power loss.

In principle, the design of the output stage in the LED driver is relatively simple compared to that of controllers. Figure 2.14 depicts the block diagram of a typical output power stage, where V_{PWM} is the control signal, and V_{IN} and V_O are the input and output voltages, respectively. The output stage consists of power transistors (i.e., M_P and M_N) and their corresponding gate drivers. Interestingly, despite the simple schematic design of the output power stage, because of its sheer size and power dissipation, it has appreciable and sometimes subtle effects on the various specifications of LED drivers.

Figure 2.14 Block diagram of a typical output power stage

The output LC_O low-pass filter in the output power stage typically determines the LED current ripple [99-101] and the controller stability (see Section 2.5 later). To qualify the degree of noise of the LED current, I_{LED} , the current ripple factor γ is widely adopted [40]. It is defined as the peak-to-peak LED current (Δi_L) over the average LED current (I_{LED}) and can be derived as

$$\gamma = \frac{\Delta i_L}{I_{LED}} = \frac{(1-D) \cdot V_O}{L \cdot f_{SW} \cdot I_{LED}} \quad (2.6)$$

where V_O is the output voltage,

D the duty cycle of the control signal,

L the inductance of the output inductor, and

f_{SW} is the switching frequency of the LED driver.

Equation 2.6 depicts that γ is inversely proportional to f_{SW} and L . Thus, a large L or high f_{SW} is required for a small Δi_L .

2.3.2 Dead-Time Circuit

The dead-time circuit [59] serves to introduce a small time-interval into the output stage control signal to ensure that the two complementary output power transistors (high side and low side) will not simultaneously be switched on. This is critical because the on-resistance of said power transistors is so small (e.g., typically in the order of $\sim 0.05\Omega$ for a 1A load) that, such that if the output transistors are simultaneously switched on, the ensuing large current will be large. This would not only degrade the power-efficiency, but also potentially damage the output transistors, resulting in an outright device failure [94].

The most robust reported method to introduce the dead-time is probably the non-overlapping logic method [102]. Figure 2.15 depicts the block diagram of the said dead-time circuit. The robustness of this design is due to the feedback mechanism thereof – the feedback control circuit ensures that the high-side (or low-side) output power transistor can only be switched on after the low-side (or high-side) power transistor is switched off.

Figure 2.15 Block diagram of a typical dead-time circuit

2.3.3 Current Sensor

LED drivers require current sensors for LED current regulation. Figure 2.16 depicts the block diagram [60, 103-105] of the resistor-based current-sensing, which is most widely used due to its simple hardware realization. The modulus operandi is very simple – the LED current is linearly converted to a voltage, V_I , by the current-sensing resistor, R_S , and the signal amplifier, A_I . $V_I (= I_{LED} \cdot R_S \cdot A_I)$ is thereafter sent to the controller.

The resistor-based current-sensing features easy implementation and relatively high accuracy but compromises the power-efficiency. This is because the voltage drop on the current-sensing resistor typically consumes a large portion of power loss [90], [106].

Figure 2.16 Block diagram of the resistor-based current-sensing

Figure 2.17 depicts a typical schematic of the state-of-the-art on-chip current sensors [26], where V_X and V_{isen} are the input switching-node voltage and the output current-sensing voltage signal, respectively. Switches S_1 and S_2 serve to sense the inductor current and hold the voltage signal of V_X , respectively. Because of the adoption of the resistors R_1 – R_4 and the amplifier, this current sensor suffers from current-sensing delay and consumes relatively higher power.

Figure 2.17 A typical schematic of reported on-chip current sensors

2.3.4 Voltage Detector

The voltage detector is typically employed for adaptive dead-time control by means of monitoring the voltage at the switching node [61]. Figure 2.18 depicts the schematic of conventional comparator-based voltage detectors, where V_{IN} and V_X are the input and the switching-node voltages, respectively. V_H and V_L are the voltage references for the high-voltage and low-voltage detectors, respectively. V_{XH} and V_{XL} are the outputs of the high-voltage and low-voltage detectors, respectively. It can be seen that high-voltage and low-voltage detectors are combined with the same window comparator. By means of capacitors (i.e., C_1 and C_2), glitches are prevented, and the speed of the comparator-based voltage detectors is limited.

Figure 2.18 Schematic of conventional comparator-based voltage detectors

The voltage detectors comprise three voltage dividers (R_1 and R_2 , R_3 and R_4 , R_5 and R_6), which typically dissipate large power because of the high voltages and small RC time constraints. They further suffer from a narrow detecting range. This narrow detecting range undesirably reduces the input voltage range of the LED driver [107].

2.3.5 Level Shifter

The level shifter serves to transmit the signals with a level shift from the aforesaid current sensors or voltage detectors to the controller [108]. Figure 2.19 depicts the block diagram of a typical latch-based level shifter [109], where V_{IN_L} and V_{O_H} are the input low-voltage and the output high-voltage signals, respectively. The level shifter features fast speed and simple realization. However, it suffers from large power consumption due to the direct conduction from V_{DDH} to GND during transitions, and from low reliability because the voltages at nodes A and B suffer from the risks of being pulled below V_{SSH} .

Figure 2.19 Block diagram of a typical latch-based level shifter

Figure 2.20 Block diagram of a typical clamp-based level shifter

Figure 2.20 depicts the schematic of a typical clamp-based level shifter [64], where V_{IN_L} and V_{O_H} are the input low-voltage and the output high-voltage signals, respectively. This level shifter mitigates the issue of large power consumption that the aforesaid latch-based level shifter suffers from, by means of employing high-voltage transistors M_3 and M_5 . However, the employment of M_3 and M_5 introduces a trade-off between speed and reliability. Specifically, due to the adoption of M_3 and M_5 , the voltages at node C and D are limited to between V_{DDH} and $V_{SSH}-V_{TH}$, where V_{TH} is the threshold voltage of M_3 and M_5 , thereby improving the reliability [110]. However, speed is compromised due to the parasitic capacitance of M_3 and M_5 .

2.4 OVERVIEW OF MODULATION SCHEMES

LED drivers are often categorized into three categories according to their modulation scheme: PFM, PWM, and digital control. In this section, we will now review in turn, with a critical review of their merits and limitations.

2.4.1 PFM Control

PFM control is widely employed in present-day LED drivers due to its hardware and design simplicity [39], [85]. Figure 2.21 depicts the block diagram of a typical floating buck LED driver with constant off-time control [111], where R_S is the current-sensing resistor and V_{REF} is the voltage reference. The modus operandi is simple – if the current in R_S exceeds a predetermined value, V_{REF} / R_S , a peak current signal is generated by the comparator and is sent to the control logic (RS latch), which would turn off the power switch M_N . Thereafter, the inductor current starts to decrease due to the discharging through the diode D_1 . After a predetermined constant off-time (T_{OFF}), M_N is turned on and the inductor current restarts to increase. By this mechanism, a new switching cycle is initiated.

Figure 2.21 Block diagram of a typical floating buck LED driver with constant off-time control

The main shortcoming of this floating buck LED driver [111] is the large power loss in the diode D_1 that serves as an asynchronous rectifier and degrades the power-efficiency of the LED driver by means of due to its relatively large voltage drop ($\sim 0.7\text{V}$).

Unlike the floating buck topology, the synchronous buck topology features high power-efficiency due to the removal of the power-hungry diode [50]. Figure 2.22 depicts the block diagram of a typical synchronous buck LED driver with hysteretic current control. The controller can be realized by two comparators, two voltage references (V_H and V_L), one current-sensing resistor (i.e., R_S), and one RS latch. The LED current (i.e., I_{LED}) is regulated with the reference of $(V_H + V_L) / (2 \cdot R_S)$.

For example, a reported design [111] provides a small LED current variation by the employment of a variable off-time controller. However, it expectedly suffers from low power-efficiency. Another reported design [64] embodies a synchronous rectifier

to replace the power-hungry diode and desirably obtains higher power-efficiency than [111]. Nevertheless, the power-efficiency of the hard-switching design [64] can be further improved by means of soft-switching techniques. This was thoroughly discussed in Section 2.2.1.

In summary, there are several advantages of the PFM control. First, PFM features low hardware because no compensation network is required due to its inherent stability – for the PFM-controlled LED drivers with the in-phase inductor current-sensing approaches [112]. Second, as PFM features self-regulation, the clock generator is not required. Third, the hysteretic current control [1] of the PFM features high current regulation accuracy by means of regulating the peak and the valley of the LED current [3], [113].

Figure 2.22 Block diagram of a typical synchronous buck LED driver with hysteretic current control

Nevertheless, consequent to the aforesaid, the PFM control suffers from the following. First, as delineated earlier, as the PFM control operates at a variable

switching frequency, the generated EMI spectrum is often wide and unpredictable [102]. Consequently, the spectrum is often difficult or expensive to mitigate. Second, the control logic in the PFM control typically requires a large LED current ripple to ascertain the appropriate operation of the control logic. The large LED current ripple deteriorates the LED performance and accelerates the degradation of the LED [13]. Third, the PFM control suffers from the current imbalance issue if it is configured in multi-phase modality.

2.4.2 PWM Control

PWM control is prevalent in automotive lighting applications because arising from its fixed switching frequency, its EMI is predictable, and its frequency can be easily synchronized [89], [114]. Moreover, the PWM control offers compatibility with the multi-phase configuration (see Section 2.4.3 later).

Figure 2.23 depicts the block diagram of an LED driver with peak current control. The peak current control is one of the most widely used PWM control schemes for LED drivers, attributed to its relatively simple hardware and realization [3], [115]. The peak current controller comprises a current-sensing resistor, a comparator, a voltage reference, an *RS* latch, and a clock signal generator. The modus operandi of the LED driver with peak current control is simple. If the LED current exceeds a predetermined value, V_{REF}/R_S , a peak current signal is generated by the comparator and is sent to the control logic. After turning off the pertinent power transistor, the control logic restarts and waits for the next turn-on clock signal.

Figure 2.23 Block diagram of an LED driver with peak current control

As the peak current control features fixed switching frequency, it has a significant advantage over the PFM control for EMI-sensitive applications [6]. In multi-phase configurations, the LED drivers embodying peak current control feature the same peak current. Thus, a relatively good current balance can be achieved when compared to the aforesaid PFM control [28].

Nevertheless, the peak current control suffers from subharmonic oscillation when the duty cycle is greater than 0.5 [29]. Furthermore, the peak current control only regulates the peak of the LED current and does not account for the other LED-current parameters (e.g., full current profile), thereby resulting in imprecise current-regulation. We will now delineate the subharmonic oscillation and imprecise current regulation in turn – issues that are addressed in our work (see Chapter 3).

Figure 2.24 depicts the timing diagram of the LED driver with peak current control, where subharmonic oscillation occurs when the duty cycle (D) is greater than 0.5. T is

one switching cycle time and I_{REF} is the peak current reference. The solid lines, i_L and PWM , are the LED current and the PWM signal at steady state, respectively. The dashed lines i_{LP} and PWM_P are the LED current with a variation, $\Delta I_{t=0}$, caused by a perturbation at $t=0$ and its corresponding PWM signal, respectively. We can easily derive the relationship between the current variations $\Delta I_{t=0}$ and $\Delta I_{t=T}$ as:

$$\frac{\Delta I_{t=0} - \Delta I_{t=T}}{V_{IN}} = \frac{1-2D}{L} \cdot \Delta D \cdot T \quad (2.7)$$

where ΔD is the increment of the duty cycle,

V_{IN} the input voltage, and

L is the inductor value.

Equation 2.7 depicts that ΔI in the peak current control amplifies with time as $\Delta I_{t=0} < \Delta I_{t=T}$, when $D > 0.5$. This hence results in subharmonic oscillation.

Figure 2.24 Current waveforms of the LED driver with peak current control

Figure 2.25 depicts the current waveforms of the peak current controlled LED driver for two inductor values, where the low current regulation accuracy is largely due to the mechanism of the control scheme. The solid line, i_{L1} , and the dashed line, i_{L2} , represent the output LED current of the LED driver with a large inductor L_1 and with a small inductor L_2 , respectively. ΔI_{L1} and ΔI_{L2} represent the average current error (with respect to I_{REF}) of i_{L1} and i_{L2} , respectively. It can be observed that ΔI_{L2} is larger than ΔI_{L1} as the inductance variation impacts the accuracy of current regulation. For example, a 20% inductance variation degrades the current accuracy by 10%. Other variations such as the input voltage, the duty cycle, and the slope compensation (that distorts the peak current reference) further degrade current accuracy.

Figure 2.25 Current waveforms of the peak current controlled LED driver with two inductor values

2.4.3 Digital Control

Digital control is not a commonly-used methodology in automotive lighting applications due to its complicated and power-hungry regulation blocks [26], [116]. Figure 2.26 depicts the block diagram of a typical LED driver with digital control, which embodies complicated blocks including an Analog-to-Digital Converter, a digital

controller with compensator, and a digital control signal generator. These blocks typically dissipate somewhat considerable power. Due to the limitation of the signal sampling rate, the digital control provides nonlinear LED current control and requires a relatively large voltage drop on R_S to ascertain the current regulation accuracy [5], [57].

Figure 2.26 Block diagram of a typical LED driver with digital control

We summarize in Table 2.1 a critical comparisons between PFM, PWM, and digital control schemes [41, 68, 75, 117]. The specific advantageous parameters of the various control schemes are highlighted in bold. In general, the PFM control features small quiescent current, no compensation network for stability, fast transient response, and medium current regulation accuracy (low for constant off-time control and high for hysteretic current control). On the other hand, the PWM control features fixed switching frequency, inherent compatibility with multiphase configuration, and high output power rating. As the PWM control offers the advantages, it is expectedly the control methodology of choice for automotive applications. The digital control is prevalent in present-day consumer backlighting applications because of its compatibility with the

digital signals from the central controller, e.g., Graphic Processing Unit. However, it is inappropriate for automotive lighting applications because the hardware is complicated, dissipates relatively high power, and the reliability is potentially compromised.

Table 2.1 Comparisons between PFM, PWM and digital control schemes

Parameters	Pulse Frequency Modulation (PFM)	Pulse Width Modulation (PWM)	Digital Control
Quiescent Current	Small	Medium	Large
Compensation Network for Stability	No	Yes	Yes
Transient Response	Fast	Slow	Slow
Current Regulation Accuracy	Low/High	Low	Medium
Switching Frequency	Variable	Fixed	N.A.
Inherent Compatibility with Multiphase Configuration	No	Yes	N.A.
Output Power Rating	Low	High	Medium

2.5 STABILITY ANALYSIS AND SMALL-SIGNAL MODELING

Following the last section, the PWM control is of specific interest in this Ph.D. program; nevertheless, one of our designs adopt the PFM control because its EMI performance is much better than conventional counterparts. In this section, a review of type II compensation and type III compensation for PWM control will be delineated, followed by our mathematical derivations of the small-signal modeling for the LED drivers.

State-of-the-art PWM-based LED drivers employ either type II or type III compensation networks for stability. Typically, the type II compensation network is required when the conjugate poles (arising from the output LC low-pass filter) are beyond the crossover frequency (typically 1/6 of the switching frequency). The type III compensation network, on the other hand, is required when the crossover frequency is beyond the conjugate poles [30], [41].

2.5.1 Type II Compensation

Figure 2.27 depicts the schematic of the type II compensation network [30], where i_E is the input current signal, V_C the output voltage signal, and R_1 is the output impedance of the transconductor g_m . We easily derive the transfer function $G_C(s)$ of the type II compensation network as

$$G_C(s) = k \cdot \frac{1 + \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_{P1}}\right) \cdot \left(1 + \frac{s}{\omega_{P2}}\right)} = R_1 \cdot \frac{sR_2C_2 + 1}{(sR_1C_2 + 1)(sR_2C_1 + 1)} \quad (2.8)$$

Equation 2.8 depicts that the type II compensation network embodies two poles, $\omega_{P1} = 1/(R_1C_2)$ and $\omega_{P2} = 1/(R_2C_1)$, and one zero, $\omega_Z = 1/(R_2C_2)$, and this leads to the appropriate design of the ensuing compensator.

Figure 2.27 Schematic of the type II compensation network

Figure 2.28 depicts the block diagram of an LED driver with the type II compensation network, where the peak current control is employed. We easily derive the loop gain $LG(s)$ of the LED driver as

$$LG(s) = H(s) \cdot G_C(s) \cdot G_M(s) \cdot G_{ID}(s) \cdot G_{LC}(s) \cdot G_{LED}(s) \quad (2.9)$$

where $H(s)$ is the current-sensing ratio,

$G_C(s)$ the transfer function of the compensation network,

$G_M(s)$ the transfer function of the PWM modulator,

$G_{ID}(s)$ the transfer function of the dead-time circuit,

$G_{LC}(s)$ the transfer function of the output power stage, and

$G_{LED}(s)$ is the transfer function of the LED load.

Figure 2.28 Block diagram of an LED driver with the type II compensation network

Based on Equation 2.9, we draw the bode plot of the LED driver with the type II compensation network in Figure 2.29. It can be seen that a 90° phase is boosted by the type II compensation network and the crossover frequency (f_c) can be desirably predetermined. By this means, we are able to obtain good stability for the LED driver, where the LC conjugate poles are beyond the crossover frequency.

Figure 2.29 Bode plot of the LED driver with the type II compensation network

2.5.2 Type III Compensation

Figure 2.30 depicts the schematic of the type III compensation network [118], where V_I is the input signal, and V_C is the output signal. We easily derive the transfer function $G_C(s)$ of the type III compensation network as

$$G_C(s) = \frac{\omega_1}{s} \cdot \frac{(1 + \frac{s}{\omega_{Z1}}) \cdot (1 + \frac{s}{\omega_{Z2}})}{(1 + \frac{s}{\omega_{P1}}) \cdot (1 + \frac{s}{\omega_{P2}})} = \frac{R_1 + R_3}{R_1 \cdot R_2 \cdot C_1} \cdot \frac{(s + \frac{1}{R_2 \cdot C_2}) \cdot [s + \frac{1}{(R_1 + R_3)C_3}]}{s \cdot (s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}) \cdot (s + \frac{1}{R_3 \cdot C_3})} \quad (2.10)$$

As $R_3 \ll R_1$ and $C_1 \ll C_2$, Equation 2.10 can be simplified to

$$G_C(s) = \frac{\omega_1}{s} \cdot \frac{(1 + \frac{s}{\omega_{Z1}}) \cdot (1 + \frac{s}{\omega_{Z2}})}{(1 + \frac{s}{\omega_{P1}}) \cdot (1 + \frac{s}{\omega_{P2}})} \approx \frac{1}{R_3 \cdot C_1} \cdot \frac{(s + \frac{1}{R_1 \cdot C_3}) \cdot (s + \frac{1}{R_2 \cdot C_2})}{s \cdot (s + \frac{1}{R_2 \cdot C_1}) \cdot (s + \frac{1}{R_3 \cdot C_3})} \quad (2.11)$$

Equation 2.11 depicts the type III compensation network embodies three poles and two zeros, $\omega_{P1} = 1/(R_3 C_1)$, $\omega_{P2} = 1/(R_2 C_1)$, $\omega_{P3} = 1/(R_3 C_3)$, $\omega_{Z1} = 1/(R_1 C_3)$, and $\omega_{Z2} = 1/(R_2 C_2)$.

Figure 2.30 Schematic of the type III compensation network

Figure 2.31 Bode plot of the LED driver with the type III compensation network

Based on Equation 2.11, we draw the bode plot of the LED driver with the type III compensation network as shown in Figure 2.31. It can be seen that a 180° phase is boosted by the type III compensation network and the crossover frequency (f_c) can be desirably predetermined. By this means, we are able to obtain good stability for the LED driver, where the crossover frequency is beyond the LC conjugate poles.

2.5.3 Small-Signal Modeling

To theoretically analyze the operation of LED drivers, we will now delineate the small-signal modeling for the LED drivers.

Figure 2.32 depicts the small-signal equivalent circuit of the LED driver with the type II compensation network, where $H(s)$, $G_C(s)$, and $G_M(s)$ are the transfer functions of the current sensors, compensation network, and PWM modulator, respectively. $H(s)=1/\alpha$, $G_M(s)=1/V_M$, where α is the current sensing ratio, and V_M is the amplitude of the ramp signal.

Figure 2.32 Small-signal equivalent circuit of the LED driver with type II compensation network

Figure 2.33 depicts the control diagram of the LED driver with type II compensation network, where G_{ID} and G_{LC} are the transfer functions of the dead-time circuit and the output power stage, respectively. We easily derive the loop gain $LG(s)$ of the LED driver as

$$LG(s) = \frac{1}{\alpha} \cdot \frac{R_1}{r} \cdot \frac{V_{IN}}{V_M} \cdot \frac{sR_2 \cdot C_1 + 1}{(sR_1 \cdot C_1 + 1) \cdot (sR_2 \cdot C_2 + 1)} \cdot \frac{sR \cdot C_o + 1}{s^2 \cdot LC_o + s \cdot \frac{L}{R} + 1} \quad (2.12)$$

where r is the LED load impedance, and

V_M is the amplitude of the ramp signal in the PWM modulator.

Figure 2.33 Control diagram of the LED driver with type II compensation network

Equation 2.12 depicts that the LED driver with type II compensation network has four poles ($P_1 \approx 1/R_1C_2$, $P_2 \approx 1/R_2C_1$, $P_3 = P_4 \approx 1/\sqrt{LC_o}$) and two zeros ($Z_1 \approx 1/R_2C_2$, $Z_2 \approx 1/RC_o$). For the loop gain design, the crossover frequency is set at $f_c \approx f_{sw}/7$ by appropriately setting the first zero (Z_1) and the second pole (P_2) to introduce the crossover frequency, and placing the second zero (Z_2) around the conjugate poles (P_3 and P_4) arising from the output LC_o low-pass filter [14, 30, 86, 119]. By this means, we are able to obtain good stability for the LED driver.

2.6 CONCLUSIONS

We have critically reviewed automotive LED drivers, including the delineation of the imperative performance attributes. In view of design parameters, including power-efficiency, reliability, current driving capability, and dimming range, the emphases of our review are the prevalent PWM-based and Soft-Switched realizations, including a critical review of the design trade-offs and state-of-the-art attempts to mitigate these trade-offs. Consequent to our critical review, for the PWM-based realization, we argue that a dual-phase LED driver with the proposed Average Current Control (ACC) could potentially decouple the trade-off between reliability and high current driving capability by means of featuring small current ripples, elimination of the subharmonic oscillation, enhanced current regulation accuracy, and excellent current balance. For the soft-switched realization, we argue that a fully soft-switched LED driver could potentially circumvent the yet unsolved trade-off for the design and realization of high power-efficiency and wide dimming range LED drivers.

In view of the critical review of automotive LED drivers and the imperative design trade-offs, we will now in turn describe a proposed PWM-based dual-phase LED driver design and a proposed fully soft-switched LED driver design in Chapters 3 and 4, respectively.

Chapter 3 DESIGN OF A PWM-BASED DUAL-PHASE LED DRIVER

3.1 INTRODUCTION

This chapter delineates the design, monolithic realization, and measurements (and benchmarking) of our proposed PWM-based dual-phase LED driver. A large portion of this chapter has been accepted for publication in the IEEE Journal of Emerging and Selected Topics in Power Electronics.

As earlier delineated in Chapter 1, the performance of contemporary LED drivers for automotive lighting applications is often compromised because of the design trade-off between high reliability and high current driving capability.

In this chapter, we propose a PWM-based dual-phase LED driver that features the decoupling of the said trade-off by means of eliminating the subharmonic oscillation and providing large output current with small current ripples. These attributes are obtained by employing our proposed Average Current Control (ACC), proposed accuracy-enhanced on-chip current sensors, and a dual-phase power stage. Specifically, to achieve high current driving capability, we adopt a dual-phase power stage. To achieve high reliability, we propose an Average Current Control to eliminate the subharmonic oscillation by considering the complete inductor-current profile vis-à-vis peak current adopted/reported elsewhere. To further improve the reliability, we propose an accuracy-enhanced current sensor to ascertain good current balance in the adopted dual-phase power stage.

The prototype LED driver embodying the aforesaid, realized in a 130nm BCDLite process, has an input voltage range of 5-16V, drives 1-3 series connected LEDs with the current of 0.4-2.4A, and dimming frequency up to 20kHz with the dimming ratio range of 0.2-1. The proposed design features a minimum current regulation accuracy of 96.2%, settling time of 5 μ s, current-ripple factor of 8%, and a peak power-efficiency of 94.7%. Overall, on the basis of benchmarking against the state-of-the-art (see Section 3.3 later), we demonstrate, to the best of our knowledge, for the first time that the trade-off between high reliability and high current driving capability is decoupled, i.e., an LED driver uniquely featuring high reliability, yet high current driving capability.

The organization of this chapter is as follows. The system-level design and circuit realization of the proposed LED driver are delineated in Section 3.2. Measurements and benchmarking are presented in Section 3.3, and finally, the conclusions in Section 3.4.

3.2 PROPOSED DESIGNS AND CIRCUITRY IMPLEMENTATIONS

In this section, we will first delineate the system architecture of our proposed PWM-based dual-phase LED driver. Thereafter, we will delineate the design of our proposed ACC, our approaches to eliminate subharmonic oscillation and to obtain high current regulation accuracy, and our proposed accuracy-enhanced on-chip current sensors.

Figure 3.1(a) depicts the system architecture of our proposed PWM-based dual-phase LED driver. All blocks are realized by low-voltage MOS transistors, save the power switches (M_{H1} , M_{H2} , M_{L1} , and M_{L2}) which are realized by high-voltage Lateral Diffused MOS (LDMOS) transistors [25] for low on-resistance and high switching reliability. The two phases (Phase 1 and Phase 2) operate in an interleaved fashion with

180° phase shift, rendering inherent current ripple cancellation [120]. Consequently, a large output current (i_{LED}) is obtained with small current ripple.

Figure 3.1 Proposed PWM-based dual-phase LED driver: (a) system architecture, and (b) current waveforms when the duty cycle is 0.5

Figure 3.1(b) depicts its current waveforms when the duty cycle is 0.5, where T is one period, and PWM_1 and PWM_2 are the control signals of phase 1 and phase 2, respectively. The input is the sum of the two phases currents, i.e., $i_{IN} = i_{IN1} + i_{IN2}$, where i_{IN1} and i_{IN2} are the input currents in Phase 1 and Phase 2, respectively. The output is the sum of the two phase currents, i.e., $i_{LED} = i_{L1} + i_{L2}$, where i_{L1} and i_{L2} are the inductor currents in the Phase 1 and Phase 2, respectively. It can be seen that consequent to the dual-phase modality, the current ripples in the large input and output currents are small.

The proposed design features enhanced reliability by means of small input/output current ripples and embodying monolithic integration of controllers, current sensors, and power transistors [67].

3.2.1 Proposed Average Current Control (ACC)

Figure 3.2 depicts the block diagram of the proposed ACC controller, comprising a current reference, Leading Edge Blanker (LEB), compensation network, and a PWM modulator. The objective herein is to process the complete inductor-current profile (vis-à-vis peak current) to precisely regulate the inductor current to the LED load and to eliminate the subharmonic oscillation.

The modus operandi is as follows. i_{LDP} and i_{LDN} sensed by the LDPMOS and LDNMOS current sensors are the scaled (1000x lower) replica of the currents (i_{LDPMOS} and i_{LDNMOS}) in power transistors, M_H and M_L , respectively. These scaled currents are summed at node A, and compared against the current reference (I_{REF}) to obtain the error current (i_E), i.e., $i_E = i_{LDP} + i_{LDN} - I_{REF}$. As $i_L = i_{LDPMOS} + i_{LDNMOS}$, i_E is a representative of the current discrepancy between i_L and I_{REF} , and should be small. To minimize i_E , the LEB eliminates the switching-induced inaccurate portion of i_E and the LEB outputs the

reduced error current, i_{E_B} , to the compensation network, where i_{E_B} is amplified and converted to a voltage, v_C . The PWM modulator thereafter generates a corresponding PWM signal. By this mechanism, the ACC provides an on-chip negative current feedback loop that processes the complete inductor-current profile based on its average. In short, the ACC provides two key features – elimination of the subharmonic oscillation and high accurate current regulation. These will now be delineated in turn.

Figure 3.2 Block diagram of the proposed ACC controller

A. Elimination of Subharmonic Oscillation

Figure 3.3 depicts the timing diagram of the LED driver with the proposed ACC, where the solid lines i_L , v_C , and PWM are steady-state waveforms, and the dashed lines i_{LA} , v_{CA} , and PWM_A are transient waveforms with a current variation $\Delta I_{t=0}$ caused by a perturbation at $t=0$. D is the duty cycle of the PWM signal, and in this example, $D>0.5$. The variation $\Delta I_{t=0}$ causes v_{CA} to be slightly smaller than v_C . Consequent to this, PWM_A has a slightly larger duty cycle than PWM , which in turn results in the current variation $\Delta I_{t=T}$. The relationship between $\Delta I_{t=0}$ and $\Delta I_{t=T}$ can be easily derived as:

$$\Delta I_{t=0} - \Delta I_{t=T} = \frac{V_{IN}}{L} \cdot (\Delta D_{t=0} + \Delta D_{t=T}) \cdot T \quad (3.1)$$

where $\Delta I_{t=0}$ is the current variation at $t=0$,

$\Delta I_{t=T}$ the current variation at $t=T$,

V_{IN} the input voltage,

L the inductance of the output inductor,

$\Delta D_{t=0}$ the current variation at $t=0$,

$\Delta D_{t=T}$ the current variation at $t=T$, and

T is one switching cycle.

Equation 3.1 depicts that ΔI in the ACC reduces with time as $\Delta I_{t=0} > \Delta I_{t=T}$, and finally leading to the elimination of the subharmonic oscillation.

Figure 3.3 Timing diagram of the LED driver with the proposed ACC

B. Highly-Accurate of Current Regulation

Figure 3.4 depicts the current waveforms of the ACC-based LED driver with two inductor values, where the solid line i_{L_L1} and the dashed line i_{L_L2} are the inductor current for a large and small inductor, respectively. T_{ON} and T_{OFF} are respectively the turn-on and turn-off times within one period, T . i_{L_L1} and i_{L_L2} have two cross points, P and Q , at $t_1=0.5T_{ON}$ and at $t_3=T-0.5T_{OFF}$, respectively. As both points are located on the current reference line (I_{REF}), the average current derived by the integration of i_{L_L1} and of i_{L_L2} from $t=0$ to $t=T$ over time equals to I_{REF} . Put simply, a current regulation that is highly accurate and that is tolerant to inductance variations is achieved.

Figure 3.4 Current waveforms of the ACC-based LED driver with two inductor values

C. Comparison between PCC and ACC

Table 3.1 tabulates the comparison of the pertinent characteristics between the PCC and the proposed ACC. As discussed in Section 2.4.2, the PCC adopts slope compensation to address the issue of subharmonic oscillation [29]. The design of the slope compensation heavily depends on output inductor value and input/output voltage

because the slope of compensation ramp must be larger than half of the slope of inductor current [26]. Put simply, the slope compensation complicates the design.

Table 3.1 Comparison of the pertinent characteristics between the PCC and the proposed ACC

	Peak Current Control (PCC)	Proposed Average Current Control (ACC)
Slope compensation	Yes	No
LED current regulation accuracy	Low	High
Current Limit	Cycle-by-cycle	Soft starter

In this aspect, the ACC is particularly advantageous as the subharmonic oscillation is innately absent. This is because slope compensation is not required, thereby resulting in design simplicity.

Table 3.1 also depicts that PCC suffers from low accuracy of LED current regulation because it regulates only the peak current of the inductor. Further, the other parameters, such as the inductance, input voltage and output current that could affect the average output current, are not regulated. Conversely, ACC features high accuracy of LED current regulation by considering the complete inductor-current profile.

Moreover, unlike the cycle-by-cycle approach in PCC, the proposed ACC achieves current limit by embodying a soft starter to ensure that the LED current reaches the steady-state current without an overcurrent during current transitions. No current limit is required for the steady-state operation of LED driving.

D. ACC Circuit Design and Stability Analysis

Figure 3.5 depicts the circuit schematic of the proposed ACC controller whose block diagram was earlier depicted in Figure 3.2. The ACC controller embodies a soft starter to, upon startup ($EN=0$), momentarily introduce a high-voltage for v_C . This is to ensure that the LED current reaches the steady-state current without a large current overshoot which could otherwise compromise reliability.

Figure 3.5 Circuit schematic of the proposed ACC controller

The current reference, $I_{REF} = V_{REF}/R_{IL}$ can be adjusted by the off-chip resistor R_{IL} , [14], [119]. The cascode current mirror provides a wide output voltage swing at node B , thereby providing a wide PWM duty-cycle range.

Consider now the system stability where we will first derive the transfer function of the compensation network and the ensuing loop gain of the system. Thereafter, we will ascertain the phase margin and the gain attenuation.

Figure 3.6 depicts the small-signal equivalent circuit of the synchronous buck LED driver, where $H(s)$, $G_C(s)$, and $G_M(s)$ are the transfer functions of the current sensors, compensation network, and PWM modulator, respectively. $H(s)=1/N$, $G_M(s)=1/V_M$, where N ($=1000$) is the current sensing ratio, and V_M the amplitude of the ramp signal.

Figure 3.6 Small-signal equivalent circuit of the synchronous buck LED driver

As there is only one current feedback loop and an error amplifier is not required in the proposed ACC controller, the Type II compensation network [29], [30] is adopted for stability. The transfer function of the Type II compensation network herein can be derived as

$$G_C(s) = \frac{V_C(s)}{i_{E_B}(s)} \approx R_1 \cdot \frac{sR_2 \cdot C_2 + 1}{(sR_1 \cdot C_2 + 1) \cdot (sR_2 \cdot C_1 + 1)} \quad (3.2)$$

where $G_C(s)$ is the compensation network,

$V_C(s)$ the output voltage of the compensation network,

$i_{E_B}(s)$ the input current of the compensation network, and

$C_1 \ll C_2$ and $R_1 \gg R_2$.

Equation 3.2 shows that the type II compensation network has two poles and one zero, and that the gain at low frequencies is dominated by R_1 . Following this equation and Figure 3.6, the loop gain $LG(s)$ of the system, embodying the power stage $G_{id}(s)$, output LC_O low-pass filter $G_{LC}(s)$ and the ACC controller, can be derived as

$$LG(s) = \frac{1}{N} \cdot \frac{R_1}{R} \cdot \frac{V_{IN}}{V_M} \cdot \frac{sR_2 \cdot C_2 + 1}{(sR_1 \cdot C_2 + 1) \cdot (sR_2 \cdot C_1 + 1)} \cdot \frac{sR \cdot C_O + 1}{s^2 LC_O + s \frac{L}{R} + 1} \quad (3.3)$$

where $LG(s)$ is the loop gain of the system,

N the current-sensing ratio,

V_{IN} the input voltage of the LED driver,

V_M the voltage of the PWM modulator, and

R is the LED load resistance.

Equation 3.3 shows that the system has four poles ($P_1 \approx 1/R_1 C_2$, $P_2 \approx 1/R_2 C_1$, $P_3 = P_4 \approx 1/(LC_O)^{1/2}$) and two zeros ($Z_1 \approx 1/R_2 C_2$, $Z_2 \approx 1/RC_O$). From this equation, we plot in Figure 3.7 the loop gain and phase frequency responses of the proposed LED driver. The design of the crossover frequency (f_C) involves a trade-off between the transient response and the high-frequency noise filtering [30], and on this basis, we set the crossover frequency to 150kHz ($f_C \approx f_{sw}/7$). On the other hand, an 18dB attenuation at $0.5f_{sw}$ and a 57° phase margin (PM) are judiciously selected to ascertain stability. These attributes are achieved by appropriately setting the first zero (Z_1) and the second pole (P_2) to introduce the crossover frequency, and placing the second zero (Z_2) around the conjugate poles (P_3 and P_4) arising from the output LC_O low-pass filter. In this design, the conjugate poles are conveniently located beyond the crossover frequency because only a small output capacitor ($C_O = 6.8\text{nF}$) is needed due to the small output current ripple (quantified in Table 3.2 later).

Figure 3.7 Loop gain and phase frequency responses of the proposed PWM-based dual-phase LED driver

E. Transient Performance

As automotive battery voltage may vary sharply due to its harsh environment including load dump and cold cranking, simulations of load-dump and cold-cranking are conducted to better illustrate the transient performance of the proposed LED driver. The duration of voltage rise-up (or drop-down) caused by the load dump (or cold cranking) is $\sim 5\text{ms}$ [121]. To adequately illustrate the rapid transient response of our design, the transition time of $50\mu\text{s}$ is used. As this is $50\mu\text{s} - 100\times$ faster than that required, the simulations should be comprehensive.

Figure 3.8 shows the emulated load-dump transient performance of the proposed LED driver when the input voltage V_{IN} rises from 7V to 16V within $50\mu\text{s}$, where V_{X1} is the voltage at the Phase 1 switching node, V_{X2} is the voltage at the Phase 2 switching

node, i_{L1} the Phase 1 inductor current, i_{L2} the Phase 2 inductor current, i_{LED} the output LED current, and V_O the output voltage. Despite that the input voltage V_{IN} varying quickly, no overshoot/undershoot current (and voltage) is observed, and the output LED current remains constant. These simulations unambiguously depict that the proposed LED driver exhibits a sufficiently fast transient response to cope with the voltage rise-up caused by the load dump.

Figure 3.8 Emulated load-dump transient performance of the proposed LED driver when the input voltage rises from 7V to 16V within 50μs

Figure 3.9 shows the emulated cold-cranking transient performance of the proposed LED driver when the input voltage HV_{DD} (i.e., V_{IN}) rises from 16V to 7V within 50μs. It can be observed that there is no overshoot/undershoot current (and voltage), and that the output LED current remains constant. Similarly, these simulations unambiguously depict that the proposed LED driver exhibits a sufficiently fast transient response to cope with the voltage drop-down caused by the cold cranking.

Figure 3.9 Emulated cold-cranking transient performance of the proposed LED driver when the input voltage drops from 16V to 7V within 50 μ s

3.2.2 Proposed On-Chip Current Sensors

To enable the ACC, on-chip current sensors (LDPMOS and LDNMOS current sensors in Figure 3.2) are realized to sense the inductor current for the ACC. As delineated earlier, the accuracy of these current sensors directly ascertains the accuracy of the LED current regulation. To this end, the spikes and valleys of the sensed currents [64], [50], due to current switching in the power transistors are removed by the proposed LEB (in section 3.2.3).

Figure 3.10(a) and (b), respectively, show the schematic of the proposed LDPMOS and LDNMOS current sensors, in Phase 1 of the proposed LED driver system discussed earlier in Figure 3.1(a). For the sake of brevity, the LDPMOS current sensor in Figure 3.10(a) will only be described. GP is the gate-driving PWM signal, M_{H1} the high-side power transistor, and M_{HS} the current-sensing LDPMOS. By generating a

replica current (i_{LDP+I_b}) in proportion to the current (i_{LDPMOS}) passing through M_{H1} , M_{HS} is a 1/1000 current replica of M_{H1} . As the gate and the source terminals of M_{HS} and M_{H1} are directly connected, the accuracy of the replica current is obtained by biasing the drain voltage of M_{HS} at node E to be equal to the drain voltage of M_{H1} at node V_{X1} . This involves making the voltage at node E follow the voltage at node F by means of the negative feedback loop consisting of $M_3 \sim M_5$. Consequently, the voltage discrepancy between node V_{X1} and node F is a negligible $<0.1\text{mV}$, particularly when compared against the $\sim 80\text{mV}$ source-drain voltage drop of M_{H1} .

The proposed LDPMOS current sensor suffers from a shortcoming due to transition delays arising from the parasitic capacitance at node G , settling of voltage transitions at nodes E and F , etc. This reduces the accuracy of current sensing. To circumvent this shortcoming, we propose two design techniques. First, $M_3 \sim M_5$ are realized by low-voltage PMOS (with symmetrical layout) instead of high-voltage LDMOS (with asymmetrical layout) to minimize the parasitic capacitance at node G . M_{LD2} is realized by high-voltage LDMOS to ascertain reliability. Second, to obtain smooth voltage transitions at nodes E and F , we provide bias to obtain a voltage drop ($\sim 80\text{mV}$) across R_1 (and R_2) when M_{H1} is turned off. This is because the source-to-drain voltage drop of M_{H1} is $\sim 80\text{mV}$ when M_{H1} is turned on.

Figure 3.10 Schematic of the proposed current sensors: (a) LDPMOS, and (b) LDNMOS (Phase 1)

In short, the sensed current ($i_{LDP}=i_{LDPMOS}/1000-I_b$) of the LDPMOS current sensor is 1000 times lower (see Figure 3.13 later for the simulated accuracy) than the current (i_{LDPMOS}) passing through the power transistor (M_{H1}), where the bias current ($I_b=5\mu A$) is negligible compared to the sensed current i_{LDP} (0.2mA~1.2mA).

Figure 3.11 depicts the layout of the power transistor M_H and the current-sensing transistor M_{HS} , where the drain 1 and drain 2 are the drain terminals of M_H and M_{HS} , respectively. Because M_H occupies a large silicon area, thousands of small groups of transistors are required to prevent the possible issue of latch-up. To improve the layout matching, common centroid technique [25] is employed for the current-sensing transistor M_{HS} . The inter-digitation technique [122] is employed for the transistor group to further improve the layout matching.

Figure 3.11 Layout of the power transistor M_H and the current-sensing transistor M_{HS}

3.2.3 Proposed Leading Edge Blanker (LEB)

Figure 3.12(a) shows the circuit schematic of the proposed Leading Edge Blanker (LEB) that serves to enhance the accuracy of the aforesaid current sensors. Specifically,

after each PWM signal transition, a time interval Δt is generated to block the flowing of the error current (i_E) from node B to the compensation network (also shown in Figure 3.5) by turning off the transmission gate (comprising M_1 and M_2).

Figure 3.12(b) illustrates the operational waveforms of the proposed LEB, where for sake of illustration, the dotted line i_L is the inductor current drawn on a scale of 1:1000 with respect to i_{LDPB} and i_{LDNB} . The solid lines i_{LDP} and i_{LDN} are the sensed currents from the LDPMOS and LDNMOS current sensors, respectively. Due to the current switching in the power transistors and the transition delays of the current sensors, there are peaks and valleys in $i_E (=i_{LDP}+i_{LDN}-I_{REF})$ that undesirably compromise the current-sensing accuracy. To circumvent this, the proposed LEB generates a time interval Δt in each PWM signal transition to ‘shield’ against the said peaks and valleys in i_E , i.e., the said peaks and valleys do not influence the accuracy of the current-sensing. After LEB modification, i_{LDP} , i_{LDN} , I_{REF} and i_E become i_{LDPB} , i_{LDNB} , I_{REF_B} and i_{E_B} , respectively. Particularly, there are no spikes and valleys in the modified sensed currents (i_{LDPB} and i_{LDNB}). Consequently, the average of i_{E_B} within each period is approximately equal to zero, and highly-accurate current-sensing is obtained.

The accuracy of the proposed current sensors with LEB modification can be derived as

$$\left| \frac{I_{AVG_S_LEB}}{I_{REF}} \right| = 1 - \left| \frac{(\Delta t)^2}{T} \cdot \frac{1-2D}{D-D^2} \cdot \frac{1}{T-2 \cdot \Delta t} \right| \quad (3.4)$$

where $I_{AVG_S_LEB}(s)$ is the average of the modified sensing currents,

I_{REF} the average current reference,

Δt the time interval of the proposed LEB,

T one switching cycle time, and

D is the duty cycle.

Equation 3.4 shows that the current-sensing accuracy may be improved by minimizing the time interval (Δt). Furthermore, the duty cycle (D) influences the current-sensing accuracy and the influence becomes infinitely small when $D=0.5$.

(a)

Figure 3.12 The proposed LEB: (a) circuit schematic, and (b) operational waveforms

To illustrate the efficiency of the proposed LEB, Figure 3.13 shows the simulated accuracy of the on-chip current sensors with and without the LEB modification for $\Delta t = 40\text{ns}$ and $T = 1\mu\text{s}$. The peak accuracy of the on-chip current sensors with and without LEB modification is 98.9% and 93.6%, respectively – an improved accuracy of at least 5.4%. In short, the accuracy of the proposed on-chip current sensors is now at least 97.5%.

Figure 3.13 Simulated accuracy of the on-chip current sensors with and without LEB modification

In summary, by means of our proposed ACC and proposed accuracy-enhanced on-chip current sensors, the proposed PWM-based dual-phase LED driver features no subharmonic oscillation, highly-accurate current regulation, and a large output current with small current ripple.

3.3 MEASUREMENTS AND BENCHMARKING

Figure 3.14(a) demonstrates the microphotograph of the proposed PWM-based dual-phase LED driver fabricated in a 130nm BCDLite process. The prototype occupies an area of $2.5 \times 2.5 \text{ mm}^2$ (the active area is $\sim 2.0 \times 2.0 \text{ mm}^2$), with 60% being the power transistors LDPMOS and LDNMOS.

Figure 3.14(b) depicts the block diagram of the measurement setup for the proposed PWM-based dual-phase LED driver, where C_{IN} and C_O are the input and output capacitors, respectively. L_1 and L_2 are the inductors in phases 1 and 2, respectively.

(a)

(b)

Figure 3.14 The proposed PWM-based dual-phase LED driver: (a) microphotograph of the proposed LED driver IC, and (b) the measurement setup

Figure 3.15(a), 3.14(b), and 3.15(c) show the measured voltage and current waveforms of the proposed LED driver for a duty cycle of ~ 0.5 , with $V_{IN}=5V$ driving 1 LED, $V_{IN}=12V$ driving 2 LEDs, and $V_{IN}=16V$ driving 3 LEDs, respectively. The respective voltage and current waveforms of Phase 1 and Phase 2, are v_{X1} and v_{X2} at the

switching node, and i_{L1} and i_{L2} in the inductor; see Figure 3.1(a). Note that the current per grid for Figure 3.15(a), (b) and (c) is 0.2A, 0.2A, and 0.5A, respectively. As designed, the switching frequency (PWM) is a constant 1MHz.

It can be seen that the ACC is highly efficacious in reducing the subharmonic oscillation – there is no observable subharmonic oscillation for all cases, including when the duty cycle in Figure 3.15(a) and 3.15(c) is larger than 0.5; see Equation 3.1 earlier. In Figure 3.15(a), the unbalanced current ($\Delta I_{L1_AVG} - \Delta I_{L2_AVG}$) between i_{L1} and i_{L2} is $\sim 2.5\text{mA}$, and the current imbalance (unbalanced current over the average current) is a very small 0.6%. In Figure 3.15(b), the unbalanced current and the current imbalance are similarly small, $\sim 2.5\text{mA}$ and 0.6%, respectively. In Figure 3.15(c), the worst-case current imbalance remains low, $\sim 3.1\%$ – this is 3x lower than the competing state-of-the-art multiphase design (e.g., 10.5% in [120]).

(a)

(b)

(c)

Figure 3.15 Measured voltage and current waveforms of the proposed PWM-based dual-phase LED driver for a duty cycle of ~ 0.5 and with (a) $V_{IN}=5\text{V}$ driving 1 LED, (b) $V_{IN}=12\text{V}$ driving 2 LEDs, and (c) $V_{IN}=16\text{V}$ driving 3 LEDs (note the expanded current scale compared to (a) and (b))

For sake of brevity, we will only illustrate the current ripple waveforms of $i_{L1}+i_{L2}$ for the scenario in Figure 3.15(b) (of the three scenarios in Figure 3.15(a)-(c)). This is depicted in the bottom trace in Figure 3.16. As the current ripple of $i_{L1}+i_{L2}$ is a very small 0.1A, the current-ripple factor ($\gamma = \Delta i_L / I_{L_AVG}$) is similarly low – 8%. It can also be seen that the voltage overshoot, undershoot and ringing of v_{X1} and v_{X2} during switching transitions are desirably low.

Figure 3.16 Measured current ripple waveforms of $i_{L1}+i_{L2}$ for the scenario in Figure 3.15(b)

Figure 3.17(a) and 3.16(b) show the measured waveforms of phase 1 with 20kHz dimming frequency, with a dimming ratio of 0.2 and 0.8, respectively. i_{LED} ($=i_{L1}+i_{L2}$) is the output LED current. The proposed LED driver supports high dimming frequency up to 20kHz, and a wide dimming ratio range of 0.2-1 is obtained by means of a dimming clock at the input pin DIM in Figure 3.1(a). After triggering the dimming function, the

output LED current features a fast-transient response — settling within $5\mu\text{s}$ from zero to the predetermined value. Moreover, the overshoot of the inductor current is very small during the startup. This is attributed to the soft starter embodied in the proposed LED driver.

(a)

(b)

Figure 3.17 Measured waveforms of phase 1 in the proposed LED driver with 20kHz dimming frequency, with (a) dimming ratio of 0.2, and (b) dimming ratio of 0.8

Figure 3.18 plots the measured power-efficiency with different series-connected LEDs over different input voltages. As depicted, for the same input voltage, the configuration with a higher number of series-connected LEDs generally exhibits higher power-efficiency. This is as expected because of the higher duty cycle and the larger output power. With fixed PWM switching frequency of 1MHz and 1.2A output current, the proposed LED driver achieves a high peak power-efficiency of 94.7% under 11V input voltage and 3 series-connected LEDs.

Figure 3.18 Measured power-efficiency with different series-connected LEDs over different input voltages

Figure 3.19 plots the measured average LED current for different series-connected LEDs over different input voltages. The dotted line is the average current reference (I_{REF}) in the ACC. The worst-case current discrepancies for 1, 2, and 3 LEDs against I_{REF} are small – 3.5%, 2.5%, and 3.8%, respectively. The worst-case 3.8% current discrepancy is for high duty cycle ($D \approx 0.9$) when the input voltage is 10V and the output is 3 series-connected LEDs.

Figure 3.19 Measured average LED current with different series-connected LEDs over different input voltages

Table 3.2 summarizes the key parameters of several state-of-the-art LED drivers. Of the three PWM-based LED drivers for automotive applications, our design is the only design that considers the complete inductor-current profile **and** on-chip current sensing. Consequent to this and despite its PWM modality, our chip features no subharmonic oscillation, while the PWM-based designs suffer from subharmonic oscillation; subharmonic oscillation is not disclosed in design [5]. As expected the PFM-based designs feature no-subharmonic oscillation – nevertheless, PFM-based designs are avoided in LED drivers for automotive lighting applications for their challenging EMI.

In the perspective of form-factor, our design requires the smallest passive components. Specifically, the inductance of the power inductor and the capacitance of the output capacitor are the smallest. In the perspective of the PWM-based controllers, we achieve these low passive values largely because of the highest switching frequency.

In the perspective of the LED current output, our design features not only the widest current range but also the highest current output. A wide current range is advantageous as this provides for an LED driver with a wider application space. Further, our design features the shortest settling time, and this shortest settling is advantageous in terms of the ‘reaction time’ of the LED driver.

In terms of reliability, it is imperative that the LED driver features low current-ripple factor and good LED current regulation qualified as current discrepancy. In terms of current ripple, the PWM-based LED drivers are, as expected, highly advantageous over their PFM counterparts in Table 3.2. This advantage is at least a factor of 3x. Of the PWM-based LED drivers, our design features the lowest current-ripple factor. In terms of LED current regulation for all LED drivers, our design arguably features the best regulation, i.e., the lowest current discrepancy.

Finally, in terms of peak power-efficiency, our design features the highest peak power-efficiency. In summary, our LED driver design is arguably the most competitive design of all PWM-based LED drivers for automotive applications. In the context of both PWM-based designs for automotive applications and PFM-based LED designs for general purpose applications, our LED driver is also, arguably, the most competitive design.

Table 3.2 Performance comparisons of different state-of-the-art LED drivers with similar specifications

	This Work	LT3474 [123]	TPS92602- Q1 [37]	TPE 2014 [5]	JSSC 2014 [111]	TPE 2014 [10]
Application	Automotive Lighting				General Lighting	
Fabrication Process	0.13μm BCDLite	N.A.			0.5μm CMOS	0.18μm CMOS
Power Transistor	Integrated	Integrated	Discrete	Discrete	Discrete	Integrated
Current-Sensing Technique	On-Chip	Off-Chip Resistor			Off-Chip Resistor	N.A.
Control Methodology	PWM				PFM	
	Average Current Control	Peak Current Control	Peak Current Control	Digital Control	Variable Off-Time Control	Automatic Mode Switching
Slope Compensation	No	Yes	Yes	N.A.	No	
Switching Frequency (MHz)	Fixed				Variable	
	1	0.5	0.6	0.5	≤0.2	≤2.5
No. of Phases	2	1	2	1	1	1
Input Voltage (V)	5-16	4-36	6-16	8-18	11-20	2.7-5.5
Output Voltage ^{DIM} (V)	6	6	13.2	15	12	2-5
Output Power ^{DIM} (W)	7.2	6	13.2	15	1.2	N.A.
Settling Time (μs)	5.0	N.A.	N.A.	~20	165	40
Power Inductor (μH)	4.7-8.2	10	22	22	100-1000	1
Output Capacitor (nF)	6.8	2200	16200	100	100	33000
LED Current (A)	0.4-2.4	0.035-1	≤2.0	1.0	0.1	2
Current-Ripple Factor*	~8%	N.A.	~20%	~10%	~70%	~40%
LED Current Regulation: Current Discrepancy	±3.8%	N.A.	4%	4.3%	±10%	N.A.
Peak Power- Efficiency	94.7%	89%	92.5%	89.7%	91%	91%

^{DIM} The dimming scenario that the settling time refers to

* The current-ripple factor (γ) is defined as the peak-to-peak current ripple over the average current ($\gamma = \Delta i_L / I_{L_AVG}$) [40]

3.4 CONCLUSIONS

We have proposed a PWM-based dual-phase LED driver featuring both high reliability and high current driving capability by means of circumventing the trade-off between them. The design embodied our proposed ACC that considered the complete inductor-current profile (vis-à-vis peak current elsewhere) and our proposed accuracy-enhanced on-chip current sensors. A dual-phase modality has been adopted. Collectively, our proposed LED driver featured zero subharmonic oscillation, good current balance, and small current ripple. A prototype was fabricated, and its measured parameters depicted that our design is the most competitive LED driver when benchmarked against all PWM-based LED drivers, and is arguably the most competitive design when benchmarked against PWM-based and PFM-based LED drivers (for general purpose applications).

Chapter 4 DESIGN OF A FULLY SOFT-SWITCHED LED DRIVER

4.1 INTRODUCTION

This chapter delineates the design, monolithic realization, and measurements (and verification) of our proposed fully soft-switched LED driver. A large portion of this chapter has been published in the IEEE Transactions on Power Electronics.

As earlier delineated in Chapter 1, the performance of contemporary LED drivers for automotive lighting applications is often compromised because of the design trade-off between high power-efficiency and wide dimming range.

In this chapter, we propose a fully soft-switched LED driver that features the decoupling of the said trade-off by means of operating at high switching frequencies, but the high switching does not compromise the power-efficiency. These attributes are achieved by our realization of fully soft-switching, where the ensuing switching losses are negligible. We achieve the said fully soft-switching by our proposed Hysteretic Soft-Switching Controller (HSSC) and proposed circuits – voltage detector, current sensor, and level shifter. The HSSC enables the fully soft-switching, including zero-voltage switching and zero-current switching, by means of turning on/off power switches when their voltage/current is zero. The proposed voltage detector and current sensor, featuring low power, monitor the voltage and current of the power switches. The proposed level shifter, featuring ultra-fast speed, serves to quickly transmit the monitored signal from the said voltage detector and current sensor to the HSSC.

The prototype LED driver embodying the aforesaid, realized in a 130nm BCDLite process, features 6-18V input voltage range, output current of 0.5-1.3A, drives 1-3 series-connected LEDs, 12W maximum output power, 2.8MHz maximum switching frequency, 96.1% peak power-efficiency, 1.4 μ s settling time, and 0.08-1 dimming range at 20kHz dimming frequency. When benchmarked against state-of-the-art LED drivers, our design simultaneously features the highest peak power-efficiency, widest dimming range, shortest settling time, highest switching frequency, and requires the smallest inductor. The measurements and benchmark demonstrate the decoupling of the said trade-off between wide dimming range and high power-efficiency.

This chapter is organized as follows. The system-level design and circuit realization of the proposed LED driver are delineated in Section 4.2. Measurements and benchmarking are presented in Section 4.3, and finally, the conclusions are drawn in Section 4.4.

4.2 PROPOSED DESIGNS AND CIRCUITRY IMPLEMENTATIONS

In this section, we will first delineate the system architecture of our proposed fully soft-switched LED driver. Thereafter, we will delineate the design of our proposed HSSC and proposed circuits – low-power current sensor, low-power voltage detector, and ultra-fast level shifter – followed by a power loss analysis of our proposed fully soft-switched LED driver. This analysis serves to qualify and quantify the power-efficiency improvement of our proposed design over the state-of-the-art.

Figure 4.1(a) shows the system architecture of our proposed fully soft-switched LED driver embodying a synchronous buck topology. The circuit blocks and circuit elements within the shaded box are monolithically realized in an IC, while the circuit

elements outside the box are external to the LED driver IC. Fully soft-switching, including both ZCS and ZVS, is achieved by our proposed HSSC and proposed circuits. The dimming function is controlled by means of the dimming clock at the input pin, DIM . C_X is the capacitor that represents the sum of parasitic capacitors at the switching node V_X . All circuit blocks are realized by low-voltage MOS transistors, save the power switches (M_P and M_N) which are realized by high-voltage Lateral Diffused MOS (LDMOS) transistors for their low on-resistance attributes.

Figure 4.1(b) depicts the operational waveforms of the proposed LED driver, where T is one clock period, and GP and GN are the gate driving signals of M_P and M_N , respectively. The solid line V_{MP} and the dashed line i_{MP} are the source-to-drain voltage and current of M_P , respectively. The solid line V_X and the dashed line i_{MN} are the drain-to-source voltage (where the drain is the switching node) and current of M_N , respectively. i_L is the inductor current. The average inductor current (or the average LED current) is approximately equal to $(I_{PK}-\Delta I)/2$, where I_{PK} and ΔI are the magnitudes of the maximum and minimum inductor currents, respectively. Both power switches M_N and M_P achieve fully soft-switching. As their operations are similar, the steady-state operation of M_N will be only described herein for sake of brevity.

ZVS to turn on M_N is realized as follows. At $t = t_1$, M_P is turned off and V_X commences to decrease because i_L continues to flow and C_X discharges. When V_X drops to zero at $t=t_2$, a low-voltage signal ($V_{XL}=0$) is generated by the proposed low-voltage detector in Figure 4.1(a) and is sent to the HSSC which subsequently turns on M_N by setting $GN=1$.

(a)

(b)

Figure 4.1 Proposed fully soft-switched LED driver: (a) system architecture, and (b) operational waveforms

ZCS and ZVS to turn off M_N are realized as follows. After M_N turns on, the stored energy in the inductor discharges to the LED load and i_{MN} commences to decrease. When i_{MN} is zero at $t=t_3$, $V_X=0$. At this instance, the proposed zero-current sensor in Figure 4.1(a) generates a zero-current signal ($V_{ZC}=0$) that is output to HSSC. This subsequently turns off M_N by setting $GN=0$. The fully soft-switching for M_N is hence realized.

Consequent to the fully soft-switching, the proposed LED driver features three worthy benefits. First, because of the realization of fully soft-switching for both M_N and M_P , the switching losses are eliminated, thereby enhancing the power-efficiency. Second, because of ZVS, the rate of voltage change, dv_X/dt , at the switching node is substantially reduced. This in turn mitigates Electro-Magnetic Interference (EMI) [14], [98]. Third, because of ZCS, the overshoot at the switching node is largely mitigated. This in turn enhances the reliability of the power switches [13], [119].

4.2.1 Proposed Hysteretic Soft-Switching Controller (HSSC)

The fully soft-switching described above by means of regulating turn-on and turn-off of the power switches is enabled by the proposed HSSC. Figure 4.2 depicts the flowchart of the modus operandi of the proposed HSSC, where V_{PK} and V_{ZC} are the voltage signals from the proposed peak-current and zero-current sensors in Figure 4.1 (a), respectively. V_{XL} and V_{XH} are the signals from the proposed low-voltage and high-voltage detectors in Figure 4.1(a), respectively

Figure 4.2 Flowchart of the modus operandi of the proposed HSSC

The modus operandi of the HSSC is as follows. When the proposed LED driver is first turned on at $t=0$ in Figure 4.1(b), both M_P and M_N in Figure 4.1(a) are initially turned off. If the HSSC is enabled ($EN=1$) and the dimming function is disabled ($DIM=1$), M_P is turned on and the inductor current, i_L , increases from zero. When i_L reaches the predetermined maximum magnitude I_{PK} in Figure 4.1(b), the peak-current sensor in Figure 4.1(a) outputs high, $V_{PK}=1$, and the HSSC subsequently turns off M_P at $t=t_1$ in Figure 4.1(b). The low-voltage detector in Figure 4.1(a) thereafter outputs low, $V_{XL}=0$, indicating that V_X is low, the HSSC turns on M_N , and i_L commences to decrease at $t=t_2$ in Figure 4.1(b). As long as i_L drops near to zero and the zero-current sensor outputs low, $V_{ZC}=0$, at $t=t_3$ in Figure 4.1(b), M_N is turned off and V_X commences to increase due to the charging of C_X . When the high-voltage detector in Figure 4.1(a) outputs high, $V_{XH}=1$, at $t=T$, the HSSC ends this switching cycle and initiates a new cycle by means of turning on M_P .

4.2.2 Proposed Low-Power Current Sensors

The proposed low-power current sensors serve to provide current-sensing for the HSSC to realize ZCS and to regulate the output LED current. Figure 4.3(a) and 4.3(b) show the schematic of the proposed low-power zero-current and proposed low-power peak-current sensors for the LED driver, respectively. I_b is the bias current, V_{REF} the voltage reference, and GP and GN are the gate-driving signals for the power switches M_P and M_N , respectively. The operation of the zero-current and peak-current sensors is similar. For sake of brevity, only the operation of the zero-current sensor in Figure 4.3(a) will be described herein; Figure 4.3(b) will not be described.

(a)

(b)

Figure 4.3 Schematic of two proposed low-power circuits for the LED driver: (a) zero-current sensor, and (b) peak-current sensor

The primary design consideration of the proposed zero-current sensor is to realize ZCS whilst dissipating low power consumption. Specifically, to mitigate the power overhead in the current sensor, the proposed zero-current sensor in Figure 4.3(a) features current limitation by means of R_{SN} , where $i_{MNS} \leq V_{DDL}/R_{SN}$. In our design with $V_{DDL}=5V$ and $R_{SN}=25k\Omega$, $i_{MNS} \leq 0.2mA$ (waveforms within the dotted ellipse in Figure 4.3(a)), the current sensor is designed to track i_{MN} only when $i_{MN} \leq 0.1A$. By this means, the maximum current of the zero-current sensor is capped at 0.2mA, i.e., the power overhead is limited to $\sim 0.5mW$. This power overhead is $\sim 20\times$ lower than conventional designs [5], [29].

The modus operandi of the proposed zero-current sensor is as follows. In Figure 4.3(a), when a low i_{MN} ($\leq 0.1A$) flows in M_N , the 1/500 replica current (i_{MNS}) flows in M_{NS} . This 1/500 ratio is obtained by designing the aspect ratio, W/L , of M_{NS} to 1/500 of that of M_N . It is worthwhile to note that when GN is high and as the drain and gate terminals of M_{NS} and M_N are directly connected, the highly accurate 1/500 replica current is obtained by biasing the source voltage of M_{NS} to be equal to the source voltage of M_N at GND . This involves forcing the voltage at node F to follow the voltage at node E by means of the negative feedback loop comprising M_7 - M_9 . Consequently, the voltage discrepancy between node E and GND is a negligible $< 0.1mV$, particularly when compared against the $\sim 10mV$ source-drain voltage drop of M_N .

ZCS is ascertained as follows. In Figure 4.3(a), when i_{MNS} is less than the predetermined low value of $80\mu A$ ($i_{MNS} = (V_{DDL} - V_{REF})/R_{SN}$) and $i_{MN} = 40mA$ ($500 \times 80\mu A$), a zero-current voltage signal, $V_{ZC}=0$, is generated by the comparator and is sent to the HSSC in Figure 4.1(a). The HSSC subsequently turns off power switch M_N with a delay of $\sim 0.3ns$ by means of the low-side gate driver. Put simply, by means of the zero-current sensor, M_N is turned off when its current is practically close to zero, hence ZCS.

For completeness, note that the proposed zero-current sensor inserts a time delay ($\sim 20\text{ns}$) for GP in Figure 4.1(a) and Figure 4.3(a). This serves to eliminate the possibility of shoot-through or false triggering between power switches M_P and M_N in Figure 4.3(a) during transitions. This is because, before M_N is turned on, $V_{SN} > V_{REF}$ in Figure 4.3(a).

4.2.3 Proposed Low-Power Voltage Detectors

The proposed low-power high-voltage and low-voltage detectors, depicted in Figure 4.4, serve to provide voltage-detection for the HSSC to achieve ZVS. I_b is the bias current, and V_{XL} and V_{XH} are the outputs of the low-voltage and high-voltage detectors, respectively. All transistors are realized by low-voltage MOS for high speed, save M_{HV} and M_{LV} that are realized by high-voltage LDMOS for reliability. The operation of the low-voltage and high-voltage detectors is similar and for sake of brevity, only the former will be described herein.

The primary design consideration of the proposed low-voltage detector is to realize ZVS whilst dissipating low power consumption. Specifically, to mitigate the power overhead in the voltage detector, the proposed low-voltage detector in Figure 4.4 features a maximum current of $2I_b$ ($=12\mu\text{A}$), thereby, limiting the power overhead to $\sim 70\mu\text{W}$. This power overhead is $\sim 20\times$ lower than conventional designs [59], [107].

Figure 4.4 Schematic of the proposed low-power low-voltage and proposed high-voltage detectors

To mitigate the power overheads from the voltage detector, the proposed low-voltage detector features a maximum current of $2I_b$ ($=12\mu\text{A}$), hence, limiting the power overheads to $\sim 50\mu\text{W}$.

The proposed low-voltage detector ascertains ZVS for the turn-on of M_N at $t=t_2$ in Figure 4.1(b) as follows. When V_X is above $(V_{DDL}-V_{TH})$, the voltage at node P is pre-biased at $(V_{DDL}-V_{TH}) \approx 4.2\text{V}$. Once V_X drops from the V_{IN} voltage (e.g., 15V) to the threshold of the inverter I_{N1} (i.e., 1.2V), V_{XL} toggles from V_{DDL} to GND , indicating that V_X has become low. With the HSSC and the low-side gate driver having a delay of $\sim 0.3\text{ns}$, M_N is turned on when V_X is practically close to zero, hence ZVS is attained.

4.2.4 Proposed Ultra-Fast Level Shifters

The proposed level shifters serve to transmit signals from the aforesaid zero-current sensor (Figure 4.3) and voltage detectors (Figure 4.4) to the HSSC. To ascertain the efficacy of fully soft-switching, these level shifters need to feature stringent requirements, including ultra-fast speed (typically $<150\text{ps}$ transition delay [22], [59]) and low power consumption (typically $<10\mu\text{A}$ [63]).

Figure 4.5(a) and 4.5(b) depict the schematic of the proposed ultra-fast down-level and up-level shifters, respectively. Both level shifters feature zero quiescent current, ultra-fast speed, and high-voltage handling capability without the adoption of high-voltage transistors – all transistors are realized by low-voltage MOS for their substantially higher speed and smaller size attributes. The operation of the down-level and up-level shifters is similar. For sake of brevity, only the operation of the down-level shifter (Figure 4.5(a)) in the proposed low-voltage detector (Figure 4.4) will be described herein.

The primary design consideration of the proposed down-level shifter is the transmission of signals from the aforesaid current sensors and voltage detectors to the HSSC with short transition delays whilst dissipating low power. The modus operandi of the proposed down-level shifter is as follows. When the input signal GP changes from the V_{IN} voltage to V_{SSH} (waveforms within the dotted ellipse in Figure 4.5(a)), V_A changes from V_{SSH} to V_{IN} . Because of the charge balance ($V_{SSH}-GND$) in the floating capacitor C_{DOWN} , V_B follows V_A to change from GND to V_{DDL} virtually without delay. Thereafter, the output signal V_{O_L} changes from V_{DDL} to GND . By this means, the down-level shifter features ultra-fast signal transition from high-voltage V_{IN} to low-voltage

V_{DDL} with only two inverter propagation delays (i.e., $\leq 66\text{ps}$). Moreover, the down-level shifter dissipates zero quiescent current because of its digital operation.

Figure 4.5 Schematic of two proposed ultra-fast (a) down-level, and (b) up-level shifters

To enable the high-voltage handling capability with low-voltage transistors, the proposed down-level shifter embodies three design techniques. First, the down-level shifter embodies a pre-set to, upon startup, momentarily introduce a high signal (V_{DDL}) for V_{O_L} . This is because the initial state of GP is high (V_{IN}) during the startup period. Second, the inverter comprising M_7 and M_8 is employed to prevent signal glitches by means of biasing V_B to either V_{DDL} or GND . Note that the aspect ratios of M_7 and M_8 are much smaller than that of M_1 and M_2 to ascertain smooth toggling of V_B . Third, the diodes (D_1 and D_2) are integrated to provide protection for the low-voltage transistors in high-voltage n-well (HVNWELL). This protection is obtained by means of limiting V_A within the safe operating region, from $V_{SSH}-0.7V$ to $V_{IN}+0.7V$, during the startup period. Similarly, the diodes (D_3 and D_4) are integrated to limit V_B within the safe operating region, from $-0.7V$ to $V_{DDL}+0.7V$.

To demonstrate the speed of our proposed ultra-fast down-level shifter, we perform a 100-run Monto-Carlo simulation for the voltage transition from 30V to 5V. Figure 4.6 depicts these simulation results where GP and V_{O_L} are the input high-voltage signal and the output low-voltage signal, respectively. It can be seen that the down-level shifter features a worst-case transition delay of 66ps. This is at least $5\times$ shorter than the state-of-the-art [124]. It is worthwhile to note that the down-slope and up-slope transition delay of the proposed down-level shifter varies from 47ps to 66ps. This is much shorter than the required 150ps [22].

Figure 4.6 100-run Monto-Carlo simulation results of the proposed ultra-fast down-level shifter

4.2.5 Power Loss Analysis

To qualify and quantify the power-efficiency improvement of our proposed design over the conventional hard-switching counterpart, Figure 4.7(a) and 4.7(b), respectively, demonstrate the power loss breakdown of our proposed fully soft-switching and conventional hard-switching LED drivers; other comparisons are tabulated in Table 4.1 (see later). For sake of readability, the size of the pie indicates the magnitude of the power dissipation. In this typical example, the switching frequency is 2MHz and the output LED power is 6W.

Total Power Loss =277mW

(a)

Total Power Loss =540mW

(b)

Figure 4.7 Power loss breakdown of LED drivers with (a) proposed fully soft-switching, and (b) conventional hard-switching. The size of the pie indicates the magnitude of the power dissipation.

The total power loss, 277mW, in Figure 4.7 is obtained on the basis of physical measurement of our proposed LED driver. The calculated total power loss, 250mW, is slightly lower than the measured one because of the variations of the different parameters including the parasitic resistance of PCB trace and connection wires in practical applications.

On the basis of Figure 4.7(a) and 4.7(b), we have noted the following. Consequent to our proposed LED driver embodying fully soft-switching, the conventional hard-switching counterpart dissipates a very significant, $\sim 2\times$ higher power, i.e., 277mW vis-à-vis 540mW. This significant reduction in power losses can be explained as follows. First, the loss due to the controller is reduced from 72mW to 12mW by means of the

low-power circuits embodied in our LED driver including the proposed HSSC and proposed circuits – current sensors, voltage detectors, and level shifters. Nevertheless, the conduction loss in our proposed design is slightly compromised from 66mW to 72mW due to the relatively larger peak-to-peak inductor current. Second, the inductor loss is reduced from 157mW to 109mW because a much smaller inductor is now required (see Table 4.1 later). From a practical perspective, not only is the loss significantly reduced, a smaller inductor results in a desired smaller form-factor and cost. Third and most significantly, in terms of the mechanism of the largest power loss, i.e., switching loss, our proposed design dissipates practically zero switching loss due to fully soft-switching. By comparison, the conventional hard-switching dissipates 163mW switching loss.

4.3 MEASUREMENTS AND BENCHMARKING

Figure 4.8(a) depicts the microphotograph of the proposed fully soft-switched LED driver fabricated in a 130nm BCDLite process. The prototype is $2.5 \times 1.3 \text{mm}^2$ with 50% of the area occupied by power switches M_P and M_N . The external passives, LC (L and C_O in Figure 4.1(a)), used are surface-mounted $0.82\mu\text{H}$ output inductor and $1\mu\text{F}$ ceramic capacitor. The specifications of the proposed fully soft-switched LED driver are tabulated in Table 4.1 (see later). For sake of brevity, we will now delineate the performance of the proposed LED driver for an input voltage of 15V and the output comprising 2 series-connected LEDs.

Figure 4.8(b) depicts the block diagram of the measurement setup for the proposed fully soft-switched LED driver, where C_{IN} is the input capacitor, L the output inductor, and C_O is the output capacitor.

(a)

(b)

Figure 4.8 The proposed fully soft-switched LED driver: (a) microphotograph of the proposed LED driver IC, and (b) the measurement setup

Figure 4.9(a) and 4.9(b) depict the measured voltage and current waveforms of the proposed LED driver with the output current at the minimum $I_{LED}=0.5A$ and at the maximum $I_{LED}=1.3A$, respectively. It can be seen that the highest switching frequency (i.e., 2.8MHz) is achieved when $I_{LED}=0.5A$ and the peak-to-peak current ripple of i_{LED} is a low 0.1A. This low current ripple is highly desirable as it enhances the reliability of the LED driver.

Figure 4.10 depicts the measured waveforms of the proposed LED driver, where it can be seen that fully soft-switching is practically realized; as earlier denoted, M_P and M_N are the power switches in Figure 4.1(a). ZVS is demonstrated as M_P is turned off and turned on when its voltage is (practically) close to zero, $\Delta V_1=0.1V$ and $\Delta V_4=0.6V$; and M_N is turned on when its voltage is also close to zero, $\Delta V_2=0.1V$. ZCS is demonstrated as M_N is turned off when its current is (practically) close to zero, $\Delta I_L=0.01A$, and subsequently, its voltage is also (practically) close to zero, $\Delta V_3=0.1V$.

(a)

(b)

Figure 4.9 Measured voltage and current waveforms of the proposed LED driver with the output current at the (a) minimum $I_{LED} = 0.5A$, and (b) maximum $I_{LED} = 1.3A$

Figure 4.10 Measured waveforms of the proposed LED driver

Figure 4.11(a), 4.11(b) and 4.11(c) show the measured waveforms of the proposed LED driver with 20kHz dimming frequency and with dimming ratios of 0.08, 0.4 and 0.92, respectively. As mentioned earlier, the dimming function is activated by means of the dimming clock at the input pin *DIM* in Figure 4.1(a). It can be seen that the proposed LED driver supports a high dimming frequency up to 20kHz – this is desirable as it is subsequently inaudible. Because of the short settling times of i_L and i_{LED} , the proposed LED driver also features a wide dimming range of 0.08-1. Specifically, upon triggering the dimming function, the inductor current i_L features settling within one switching cycle (0.5 μ s), and the output LED current i_{LED} features settling within 1.4 μ s from zero to the predetermined value.

(a)

(b)

(c)

Figure 4.11 Measured waveforms of the proposed LED driver with 20kHz dimming frequency and with a dimming ratio of (a) 0.08, (b) 0.4, and (c) 0.92

Figure 4.12 depicts the measured power-efficiency with different series-connected LEDs over different input voltages. We note two observations. First, it can be seen that for the same input voltage, the configuration with a higher number of series-connected LEDs desirably exhibits higher power-efficiency. This is as expected because the operational power (losses due to gate driving, controller, etc.) is generally constant while the output power is increased. Second, for the same series-connected LEDs, the operation with a lower input voltage offers higher power-efficiency. This is also as expected because of the relatively lower switching frequency with reduced voltage, and subsequently smaller gate driving loss. Further to the said first and second observations, the proposed LED driver with 0.7A output current achieves a peak power-efficiency of 96.1% at 11V input voltage and with 3 series-connected LEDs.

Figure 4.12 Measured power-efficiency with different series-connected LEDs over different input voltages

Table 4.1 summarizes the benchmarking of the key parameters of several state-of-the-art LED drivers against the proposed LED driver. Of particular pertinence, our

proposed design is the only design that features fully soft-switching, including both ZVS and ZCS. Consequently, as expected, our proposed design is the most power-efficient design. The next most-competitive design [55] embodies only ZVS, and does not feature ZCS. Consequently and as expected, its power-efficiency is lower than our proposed design but is higher than the hard-switching counterparts [5, 64, 111, 125].

In terms of the dimming performance qualified by the dimming range at 20kHz dimming frequency, our design is, as expected, highly advantageous over the state-of-the-art. Specifically, our design features the widest dimming range where its smallest dimming ratio (0.08) is a very significant $5\times$ smaller than the next-best design (0.4 in [64]); $7.5\times$ and $11.25\times$ smaller than [5] and [125], respectively. This is the consequence of the short settling time in our proposed design (see later). The designs [55] and [111] cannot offer dimming capability at 20kHz dimming frequency due to their low maximum switching frequencies.

In the perspective of settling time defined as the time for the output LED current to settle from zero to the predetermined value (see Section 2.2.4), our design desirably features the shortest settling time of $1.4\mu\text{s}$. The next most-competitive design [64] is a significant $\sim 6\times$ slower than our design. This is largely because our design features the highest switching frequency.

In the perspective of output inductor, our design desirably requires a significant $10\times$ smaller inductance than the next most-competitive design [125]. This is also largely because our design features the highest switching frequency. In the practical LED driver applications, a small valued inductor is highly desirable in terms of (smaller) form-factor and (lower) cost.

In summary, by means of fully soft-switching that substantially eliminates the switching losses, our proposed LED driver design features high power-efficiency, yet wide dimming range – effectively circumventing the trade-off between the said two parameters. Put simply, because of this trade-off decoupling, our proposed design simultaneously features the highest power-efficiency, widest dimming range, shortest settling time, highest switching frequency, and requires the smallest output inductor – our design is the most competitive design when benchmarked against state-of-the-art LED drivers.

Table 4.1 Measured performance of different state-of-the-art LED drivers

	This Work	TPE 2017 [55]	TPE 2014 [5]	JSSC 2014 [64]	JSSC 2014 [111]	LM3405 2016 [125]
Fabrication Process	0.13μm BCDLite	N.A.	N.A.	0.35 μ m CMOS	0.5 μ m CMOS	N.A.
Control Scheme	Hysteretic Soft-Switching Control	Variable Inductor Control	Digital Control	Digital Control	Variable Off-Time Control	Peak Current Control
Fully Soft-Switching	Yes	No	No	No	No	No
Soft-Switching Techniques	ZVS and ZCS	ZVS	None	None	None	None
Input Voltage (V)	6-18	48	8-18	10-40	11-20	3-15
LED Current (A)	0.5-1.3	0.1-0.35	1	0.345	0.1	0.2-1
Max. Output Power (W)	12	22	40	10	1.2	15
Power Inductor (μ H)	0.68-1	40-150	22	10-39	100-1000	6.8-22
Max. Switching Frequency (MHz)	2.8	0.1	0.5	1	0.2	1.6
Input Voltage ^{DIM} (V)	15	48	15	40	18	15
LED Current ^{DIM} (A)	0.7	0.35	1	0.345	0.1	1
Output Power ^{DIM} (W)	4.4	22	15	10	1.2	9
Settling Time (μ s)	1.4	>30	20	8.5	165	30
Dimming Range at 20kHz Dimming Frequency	0.08-1	1	0.6-1	0.4-1	1	0.9-1
Peak Power-Efficiency	96.1%	94%	89.7%	92.5%	91%	91%

^{DIM} The results are measured under the dimming scenario of the given input voltage and LED current of the various LED drivers

4.4 CONCLUSIONS

We have proposed a fully soft-switched LED driver featuring both high power-efficiency and wide dimming range by means of circumventing the trade-off between them. The proposed design embodied our proposed HSSC and proposed other circuits that collectively enabled fully soft-switching, including ZCS and ZVS. Consequently, the switching losses – the mechanism of the major power loss – were shown to be practically eliminated. The prototype LED driver embodying the proposed HSSC and proposed other circuits featured 96.1% peak power-efficiency, 0.08-1 wide dimming range at 20kHz dimming frequency, 1.4 μ s settling time, and 2.8MHz maximum switching frequency. It was shown to be the most competitive design when benchmarked against the state-of-the-art, and demonstrated the decoupling of the said trade-off between high power-efficiency and wide dimming range.

Chapter 5 CONCLUSIONS AND RECOMMENDATIONS

This chapter draws the conclusions of the work reported in this Ph.D. research program and delineates the recommendations for future work.

5.1 CONCLUSIONS

The primary objective of this Ph.D. program pertained to the design, monolithic realization and measurements (and verification) of our two proposed automotive LED drivers. The conclusions of the research work are as follows.

In Chapter 1, we have presented the motivation, objectives, and contributions of our Ph.D. program delineated in this thesis.

In Chapter 2, we have critically and comprehensively reviewed automotive LED drivers, including an overview of the automotive lighting systems and their design parameters. Our review included an in-depth analysis of the critical issues and the limitations of reported modulation schemes and circuitry blocks, and our analytical derivations for stability analysis and small-signal modeling involved in LED driver designs. Because of the stringent requirements of the LED driver for automotive lighting applications, the emphases of this review were the limitations/trade-offs of reported state-of-the-art design techniques and control methodologies, and on the inadequacy of these reported work to mitigate these limitations/trade-offs.

In Chapter 3, we have presented the design, monolithic realization, and measurements (and verification) of our (first) proposed PWM-based dual-phase LED driver. The proposed LED driver has been shown to simultaneously feature high

reliability (attributed to the elimination of subharmonic oscillation, small current ripple, and good current balance) and high current driving capability (because of the adoption of the dual-phase modality) by means of decoupling the trade-off thereto. Of particular note, we have proposed a novel PWM control scheme, i.e., the ACC, to completely resolve the issues reported peak current control suffers from, including the “problematic” subharmonic oscillation and the imprecise current regulation.

The prototype LED driver has been fabricated in a 130nm BCDLite process. Its primary attributes included 5-16V input voltage range, 0.4-2.4A LED current range, 94.7% peak power-efficiency, 5 μ s settling time, and 8% current-ripple factor. When benchmarked against state-of-the-art LED drivers, our design simultaneously featured the largest current driving capability, yet with the lowest current-ripple factor. With measurements on our prototype LED driver ICs embodying our aforesaid adoption and proposed circuits, we have demonstrated, to the best of our knowledge, for the first time that the trade-off between high reliability and high current driving capability was decoupled, i.e., an LED driver uniquely featuring high reliability, yet high current driving capability.

In Chapter 4, we have presented the design, monolithic realization, and measurements (and verification) of our (second) proposed fully soft-switched LED driver. The proposed LED driver has been shown to simultaneously feature high power-efficiency (attributed to the realization of fully soft-switching) and wide dimming range (because of the high switching frequencies and its ensuing short settling time) by means of decoupling the trade-off thereto. Of particular note, we have proposed a novel control scheme, i.e., the HSSC, to enable the fully soft-switching, including zero-voltage switching and zero-current switching, by means of turning on/off power switches when their voltage/current was zero. We have also proposed several novel circuits – voltage

detector, current sensor, and level shifter – to improve the efficacy of the fully soft-switching by means of low power and/or high speed.

The prototype LED driver, realized in a 130nm BCDLite process. It featured 6-18V input voltage range, output current of 0.5-1.3A, drives 1-3 series-connected LEDs, 12W maximum output power, 2.8MHz maximum switching frequency, 96.1% peak power-efficiency, 1.4 μ s settling time, and 0.08-1 dimming range at 20kHz dimming frequency. When benchmarked against state-of-the-art LED drivers, our design simultaneously featured the highest peak power-efficiency, widest dimming range, shortest settling time, highest switching frequency, and required the smallest inductor. The measurements and benchmark depicted the decoupling of the said trade-off between high power-efficiency and wide dimming range.

As an overall conclusion, the work delineated in this thesis is a worthy contribution to the automotive LED driver literature. Specifically, the work herein provides useful insight to automotive LED driver designers on the imperative attributes of the design parameters, including high power-efficiency, high reliability, high current driving capability, and wide dimming range, by means of decoupling the trade-offs thereto.

5.2 RECOMMENDATIONS FOR FUTURE WORK

On the basis of the literature review and the research work in this research program, the following future work is recommended:

- (i) We suggest an investigation into the design of automotive LED drivers embodying Gallium Nitride (GaN) or other III/V-semiconductor power switches

on the basis of SMART-LEES (III/V-on-CMOS) process, including a critical appraisal of their merits and limitations, particularly in view of power-efficiency, switching frequency, and high voltage handling capability.

As described in Chapter 2, power switches are critical to the automotive LED drivers as they largely determine two imperative parameters – power-efficiency and reliability. Present-day power switches are typically realized by silicon MOSFET mainly for sake of monolithic integration, but the penalty is sometimes severe. Specifically, the losses (including switching losses, conduction losses, and gate driving losses) in the power switches may be large, particularly in the case of high switching frequencies. Although our proposed fully soft-switching can substantially mitigate the switching losses, the conduction losses and the gate driving losses cannot be reduced. Moreover, silicon MOSFETs are inferior in terms of switching frequency and voltage handling capability.

In view of these limitations, there are unambiguous advantages to realize the power switches on the basis of a III/V process that intrinsically embodies higher electron mobility, wider bandgap, and smaller gate capacitance. These attributes are beneficial to largely reduce the conduction losses and the gate driving losses, and substantially increase the switching frequency and voltage handling capability.

- (ii) Following (i), in view of the attractive merits of the GaN or other III/V semiconductor power switches, there is a good possibility that a hybrid monolithic integration of a GaN power switch and a CMOS controller would offer substantial advantages of higher power-efficiency, higher switching

frequency, and higher voltage handling capability over the state-of-the-art CMOS realizations. In view of these unique advantages, we recommend an investigation into the design and realization of a hybrid GaN-CMOS automotive LED driver, with substantially enhanced power-efficiency, improved switching frequency, and widened input voltage range over the conventional CMOS-only counterparts.

- (iii) Finally, we suggest an application of the GaN-based LED driver for automotive matrix headlights based on the emerging SMART-LEES process. It would be interesting to analytically investigate the mechanisms of and the circuit parameters affecting the power-efficiency and dimming accuracy of the LED matrix. Further, on the basis of the said investigation, to provide insights into the optimization of matrix headlights in terms of power-efficiency and dimming accuracy.

AUTHOR'S PUBLICATIONS

Patent Publications (Related Work)

- [1] J. Chang, W. Shu, **Y. Qu**, E. Fitzgerald, L. Zhang, K. Lee, S. Chua, and S. Chiah

“Subpixel Circuit, and Display System and Electronic Device Having the Same”

US Provisional Patent 62/458, 775, 2017

- [2] L. Zhang, K. Lee, S. Chua, E. Fitzgerald, S. Chiah, J. Chang, **Y. Qu**, W. Shu, K. Lee, and B. Wang

“A Method of Forming a Multilayer Structure for a Pixelated Display and a Multilayer Structure for a Pixelated Display”

US Provisional Patent 62/445, 877, 2017

Journal Publications (Related Work)

- [3] **Y. Qu**, W. Shu, and J. Chang

“A Low-EMI High-Reliability PWM-Based Dual-Phase LED Driver for Automotive Lighting”

IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1179-1189, Sep. 2018.

- [4] **Y. Qu**, W. Shu, and J. Chang

“A 2.8MHz 96.1%-Peak-Efficiency 1.4 μ s-Settling-Time Fully Soft-Switched LED Driver with 0.08-1 Dimming Range”

IEEE Transactions on Power Electronics, Conditionally Accepted for Publication.

Conference Publications

- [5] Y. Qu, W. Shu, and J. Chang

“An Air-Core Coupled-Inductor Based Dual-phase Output Stage for Point-of-Load Converters”

IEEE International Symposium on Circuits and Systems (ISCAS), 2018, Florence, Italy.

- [6] J. Jiang, W. Shu, Y. Qu, K. Chong, and J. Chang

“Design and Test of a RHBD CMOS-Only Voltage Reference”

IEEE Nuclear and Space Radiation Effects Conference (NSREC), 2018, Hawaii, US.

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