Design of low-power PVT-aware circuits for power management applications

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**NANYANG
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**DESIGN OF LOW-POWER PVT-AWARE CIRCUITS
FOR POWER MANAGEMENT APPLICATIONS**

**WANG DONG
SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING
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DESIGN OF LOW-POWER PVT-AWARE CIRCUITS FOR POWER MANAGEMENT APPLICATIONS

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ABSTRACT

In recent electronics industry, power management plays a significant role to extend the battery life of battery-powered portable electronic devices. Due to the push for low-power CMOS circuits, the power-aware design agenda will be addressed in the power management circuits. Besides, turning to sub-90nm CMOS technologies in System-on-Chip (SoC) environment, the performances are often significantly influenced by process, supply voltage and temperature (PVT) variations. These two key issues impose design challenges to circuits that are able to sustain the targeted specifications and to provide good fabrication yield. To tackle the stated problems, this work aims to explore the research, design, analysis and implementation of low-power PVT-aware circuits for power management applications in advanced nanometer CMOS technologies.

In an exemplary application of a smart power system that the supply voltage can be a function of device's threshold voltage (V_{TH}) to counteract the process variation, a threshold voltage reference circuit is often needed in the design. This thesis will present the MOSFET V_{TH} reference circuit that employs a dual-segment nonlinear temperature compensation method to provide thermal stability. Besides, the supply insensitivity is another key design parameter to be addressed in this work. The measured results have indicated that the V_{TH} reference circuit yields a $T.C.$ of 28.7 ppm/ $^{\circ}C$, power supply rejection (PSR) of -43.5 dB at 10 MHz and line sensitivity of 70.8 ppm/V. The performance metrics are better than those of reported works.

In another circuit of the above power system, it requires a stable current source. This work presents a new current source architecture which is the embodiment of a process-tolerant bias current circuit and a scaled process-tracking bias voltage source

for the dedicated temperature-compensated voltage-to-current (VI) conversion. The measurement results have shown that the current source consumes a quiescent power of $7.18\ \mu\text{W}$ whilst achieving a sensitivity figure-of-merit (FOM) of 2.34% in terms of total PVT variation. Such the low-power low-sensitive features are better than most of the reported works and comparable with the state of art.

On top of that, there exists another challenge from the non-ideal CMOS stress effect that causes the performance degradation in the PVT-aware circuits. In this work, a new electrical model is proposed to predict the stress effect that impacts on the electrical performance of reference circuits. It has validated that there is a reasonable correlation between the model prediction results and the measurement results of the above stated voltage and current reference circuits. Of particular noted, this is the first electrical model that addresses the impact of stress effect on the reference circuit designs in the field.

In the low-dropout (LDO) regulator dedicated to power management applications where low power, low voltage, low transient spike and sustainability of transient metrics are concerned, the circuit techniques are the major focus of this work. First, a new low-voltage transient-assisted embedded driving stage (TAEDS) with low-output impedance is presented. This aims to enhance the slew rate at the gate of power transistor whilst allowing low quiescent current under low supply design. Second, the transient-assisted technique together with the multiple feedback circuit topology, process-temperature (PT) aware power transistor biasing network and the aforementioned constant current source architecture are then applied to realize a low-power PT-aware LDO regulator in 40nm CMOS technology. This results in the performance-aware regulator which can sustain low undershoot/overshoot effect, reduce speed degradation, maintain good stability and eliminate the circuit trimming in

the context of total process and temperature variation under low-quiescent power constraint. The measurement results have confirmed the circuit operation for a full load current of 100 mA at a parasitic capacitive load of 100 pF under a 0.75 V supply. Based on the measured results from 12 samples, the regulator consumes an average quiescent power of 19.5 μ W whilst an average settling time of 414 ns during full load current step transitions at room temperature. The average load transient voltage variation is 23.9 mV and the regulator achieves an average transient FOM value of 12.6 mV, which is better or comparable than most of the published output capacitor-less (OCL) LDO counterparts. The process corner simulations as well as the measurement results under temperature corners have validated the regulator's sustainable transient performance metrics under process and temperature variations.

DEDICATION

I dedicate this work to my family and friends, who offered unconditional love and support and have always been there for me. Thank you so much.

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ACRONYMS

BGR	Bandgap Reference
BJT	Bipolar Junction Transistors
CMOS	Complementary metal-oxide semiconductor
CTAT	Complementary-to-Absolute Temperature
DC	Direct Current
GPS	Global Positioning System
IC	Integrated Circuit
LCD	Liquid-crystal-display
LDO	Low-dropout
LSI	Large-scale Integration
LTS	Lower Temperature Segment ($T < T_r$)
MIC	Microphone
MOSFET	Metal–oxide–semiconductor Field-effect Transistor
NCTAT	Nonlinear Complementary-to-Absolute Temperature
NPTAT	Nonlinear Proportional-to-Absolute Temperature
Op-amp	Operational amplifier
PCB	Printed Circuit Board
PLL	Phase-locked Loop
PMU	Power Management Unit
PSR	Power Supply Rejection
PTAT	Proportional-to-Absolute Temperature
PVT	Process, Voltage, and Temperature
RAM	Random-access Memory
RF	Radio Frequency
RTC	Real Time Clock
SCE	Short-channel Effect
SoC	System-on-Chip
T.C.	Temperature Coefficient
UTS	Upper Temperature Segment ($T > T_r$)
WPE	Well-proximity Effects

SYMBOLS

T_r	Reference Room (Nominal) Temperature
T_1	Reference Temperature at UTS
T_2	Reference Temperature at LTS
V_{REF}	Voltage Reference
V_{TH}	Threshold Voltage
V_{TH0}	Threshold Voltage at zero Kelvin (K)
V_{GS}	Gate-to-Source Voltage of MOSFET
V_{NPTAT}	NPTAT Voltage
V_{NCTAT}	NCTAT Voltage
V_{REF_SEG}	UTS Compensated Reference Voltage
V_{R_Comp}	Reference Compensation Voltage
V_{Aux_Comp}	Auxiliary Compensation Voltage
V_{PTrack}	Process-Tracking Bias Voltage
I_{REF}	Reference Current
I_{PTAT}	PTAT Current
I_{CTAT}	CTAT Current
I_{PTol}	Process-Tolerant Bias Current
I_B	Bias Current
K_i	Aspect ratio of the corresponding MOSFET device
C_{ox}	Gate Oxide Capacitance per unit area
α_μ	Carrier Mobility temperature exponent in MOSFET
η	Subthreshold slope factor
k_B	Boltzmann constant
q	Elementary charge

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Chapter One

Introduction

This Chapter introduces the background information and motivations of this research project. Besides, the project objectives as well as the achievements will be presented

1.1 Motivations

In recent years, the electronics market of mobile and battery-powered portable devices such as cell-phone, tablets, video camera, music players, GPS as well as handheld home health monitors like glucometer and blood pressure meter is growing rapidly to facilitate consumers' demand [1], [2]. However, the limited life of the batteries used to provide supply for these devices raises significant concerns to this industry and becomes one critical issue that needs to be considered. Therefore, the research field of performance-aware power management which provides an important solution for extending the battery life has received great attention from the integrated circuit (IC) designers. Moreover, with the continual development of the device scaling, the focus of modern power management IC designs is shifting to the fully integrated System-on-Chip (SoC) system. This implies that the circuits should have the advantages of high-accuracy, fast-speed, area and power-efficiency, as well as less or without off-chip components. As a consequence, the circuits can be easily suitable for applications in the portable electronic devices. As an essential unit in the SoC system, the power management unit (PMU) or power management IC (PMIC) plays a significant role in saving the battery life by providing the power supply dedicated to different internal parts of the portable devices. Fig. 1.1 illustrates the basic block

Fig. 1.1 Simplified block diagram of a typical power management unit integration for battery powered devices [3]

diagram of a typical PMU integration implemented in a portable device. According to [3], a PMU mainly consists of the voltage regulators such as switching DC/DC converters, linear low-dropout (LDO) regulators for processors or peripherals, battery management management part and additional functional blocks dedicated to lighting, audio codecs, USB connectivity as well as other control logic, drivers, and data converters. Refer to [4], switching DC/DC converters have higher power efficiency than LDO regulators, making it more suitable to step down the input voltage to the desired one for the systems such as the laptop or microprocessors in which high power efficiency is of great concern. Considering internal functional blocks of the electronic devices such as sensors, RF circuits, precision analog circuits, oscillators, memory cell and digital core in the processors or peripherals as shown in Fig. 1.1, they are sensitive to noise. It is of importance to provide them with clean supplies having different voltage ranges as well as different driving current levels. As a result, to optimize the power efficiency and reduce the cross-talk between internal blocks, several dedicated LDO regulators are utilized after the DC/DC converters to meet the requirements of voltage supply and current for each internal part. The coexistence of the DC/DC and

LDO regulators help to achieve low-noise power supply whilst maintaining high power efficiency. The increasing demand on the LDO regulators for the portable devices gives rise to one of the motivations on the design of performance-aware LDO regulators.

Besides, the low-supply digital large-scale integration (LSIs) circuits are in great demand for the portable mobile devices under low power constraint. However, as the supply drops to close to the threshold voltage (V_{TH}) of the transistors, the performance of LSIs will degrade due to the variations of V_{TH} , depending on the Process, Voltage, and Temperature (PVT) [5]. Therefore, it is of paramount importance to investigate the novel PVT compensation techniques so as to devise the PVT-aware circuits for the power management IC dedicated to low power applications. From the literature, many works on the compensation techniques such as body bias control [6] and supply voltage control [7], [8] have been reported to realize the PVT compensation system for the digital LSIs. However, those works add complexity of the circuit, leading to higher power consumption. Fig. 1.2 shows an exemplary PVT-compensated structure [9] for low-voltage digital LSIs. It consists of a current reference (I_{REF}) circuit, a process tracking circuit and a buffer circuit using DC/DC converters. The current reference circuit comprises a threshold voltage reference circuit which can track the process information. However, the V_{TH} reference circuit faces challenges to maintain stability against process variations in the advanced nanometer CMOS technology. In addition, the switching DC/DC converters will limit the response speed of the digital LSIs and may cause the other circuits to suffer from noise issues, especially for those noise-sensitive applications. As such, good power supply rejection (PSR) of the reference circuit is another design requirement.

As shown in Fig. 1.2, threshold voltage reference circuit plays a key role in PVT compensation systems for digital LSIs in power management applications. It can be used to generate the process information that facilitates the design of a process insensitive current reference [10]. Besides, it also serves as a CMOS voltage reference building block for on-chip system applications. Despite the bandgap reference (BGR) circuits, that incorporate the bipolar transistors (BJTs), are popular on the basis of their low temperature coefficient ($T.C.$) performance and high power supply rejection (PSR) [11], [12], they usually require a higher supply voltage and power consumption to drive the BJT devices. However, the growing interest in low-power aware applications like battery-powered portable mobile devices has significantly pushed the need of low-power voltage references. As a consequence, the CMOS voltage references [13]–[27] without BJTs have drawn much attention because of their low power property.

Similar to the voltage reference circuits, the current reference is also another essential building block for the analog and mixed-signal circuits systems such as operational amplifier (op-amp), buffers, oscillators, phase-locked loops (PLLs), data

Fig. 1.2 Exemplary PVT-Compensated Supply System [9].

converters, and so on. To provide a reliable operation for such circuits and systems, the current reference must have good stability against wide temperature operating range as well as a high tolerance for process variations. In addition, it should consume low power as stated. Although many works [10], [28]–[45] pertaining to the compensation techniques for temperature and process variations have been reported, other limitations like poor line sensitivity [31], relatively high $T.C.$ [33] and high sensitivity to process variations [32], are needed to be tackled for the robust current reference design.

It is of particularly noted that as aggressive technology scaling to sub-90nm technology, the process variation arising from lithographic variation [46] and many other non-lithographic factors such as dopant variation [47], well-proximity effects (WPE) [48], [49], and layout-dependent stress variation [50] have imposed challenges for robust circuit performance in terms of a model-to-hardware correlation [51]. Besides, the temperature fluctuation induced variation on the carrier mobility significantly becomes much higher for MOSFET devices in the 65nm CMOS technology than that of 180nm CMOS technology [52]. The short-channel effect (SCE) also contributes another key factor that limits the circuit performance using advanced nanometer technology [53]. Furthermore, the MOS transistors suffer from high current leakage level as well as reduced output resistance [54]. As mentioned above, these non-ideal effects increase the difficulty in the design of precision analog circuits like voltage or current reference with PVT-aware performance metrics in the context of aggressively scaled nanometer technology.

Therefore, to address the aforementioned problems, further research on new techniques for the design of PVT-aware blocks is another motivation for power management IC applications in nanometer CMOS technology. Unfortunately, the non-ideal CMOS stress effect can cause the performance degradation in the PVT-aware

circuits imposes another challenge for the analog reference design. For this reason, a new electrical model is needed to predict the stress effect on the electrical performance of the reference circuits.

As noted, LDO regulators can be used to provide clean supplies with small transient voltage variations dedicated to different noise sensitive circuit blocks of the portable devices and serve as the drivers for the LSIs in the supply system illustrated in Fig. 1.2. With the increasing demand of on-chip integration, the conventional LDO regulators [55]–[59], which rely on a μF range off-chip capacitor to achieve stability, turn out to be unsuitable for realization. Therefore, the output capacitorless LDO (OCL-LDO) regulator becomes more prominent for fully on-chip designs [60]–[85]. However, without the off-chip capacitor to absorb the transient currents, the OCL-LDO regulator typically displays large undershoot/overshoot voltages during the load current step transitions from no load to full load. Attaining small transient voltage variations in absence of the large output capacitor always comes along with the significant tradeoff of high quiescent current or non-zero minimum load current.

To address these limitations, many circuit techniques, such as increasing the loop bandwidth or the slew rate at the gate of power transistor, have been utilized on the basis of the foundation investigations from [55]. However, the prior-art works still have difficulty to address the limitations such as large quiescent current [72], high value on minimum load current I_L [70], restricted to small load current specification [65] and so forth. Moreover, some digital circuits like memory banks, microprocessors and digital signal processing (DSP) cores exhibit large parasitic capacitance at the supply line (few pF to few nF) [86],[87] under the SoC requirement. However, most prior reported works can support a C_L up to 100 pF [66] or 1 nF [67]. Especially, when it is pushed towards sub-1V supply in context of the trend of low-voltage SoC

environment, the LDO regulator will suffer from the performance degradation in terms of speed and stability due to the substantial increase in the power transistor's size. This raises another motivation for the investigation and design of an improved low-voltage LDO regulator with fast transient response whilst the feature of driving wide capacitive load range is included.

Furthermore, under low quiescent design, the OCL-LDO regulators tend to suffer from the poor transient sustainability under process and temperature variations, leading to a significant yield problem in production. As reported in [88] due to the unpredictable working environment of the LDO regulators in the various SoC packages, the intellectual property (IP) vendors face great challenges to design a robust LDO regulator that still operate stably in spite of different electrical environment or operating temperatures. More importantly, the stability or speed will also be degraded due to the increased process variation when using the sub-90nm technology [53].

Consequently, turning to the low-dropout regulator dedicated to power management applications where low power, low voltage, low transient spike and sustainability of transient metrics are of key concern, the circuit techniques become the major focus of this work.

1.2 Project Objectives

The main objectives of this research project are to explore the research, design and implementation of PVT-aware Circuits dedicated to power management IC applications in advanced nanometer CMOS technology. They are given as follows:

- (i). to investigate, design, analyse and implement new performance-aware MOSFET threshold voltage reference circuit so as to provide the information of process variation,
- (ii). to investigate, design, analyse and implement low-power CMOS constant current source with reduced PVT variation,
- (iii). to investigate and propose a new electrical model for stress effect on the electrical performance of analog reference circuits,
- (iv). to investigate, design and analyse the new circuit technique for fast transient LDO regulator with heavy capacitive load,
- (v). to design, analyse and implement a low-voltage low-quiescent 40nm CMOS process-temperature-aware (PT-aware) output-capacitorless LDO regulator through employing the transient-assisted technique of part (iv) together with the multiple feedback topology, the proposed PT-aware power transistor biasing network and the related constant current source architecture of part (ii).

These contributions will be presented in details in the subsequent Chapters.

1.3 Report Organization

This report comprises seven Chapters. The details are summarized as follows:

- (i). Chapter one gives an introduction of background about the power management circuits in electronics and the motivation of PVT-aware circuits for power management IC applications.
- (ii). Chapter two reviews recently published literatures on the low-power CMOS threshold voltage reference designs. It also describes the working principle

and circuit implementation of the proposed V_{TH} reference circuit in 65nm CMOS technology. The measurement results will be discussed.

- (iii). Chapter three describes the prior-art research works on the constant current reference circuit in nanometer CMOS technology. Besides, a low power CMOS constant current course with reduced PVT variations is proposed, analyzed and discussed.
- (iv). Chapter four describes the realistic design problem arising from the non-ideal CMOS devices' stress effect on the electrical performance of analog references circuits. A new model pertaining to the stated effect for realistic BSIM4 Monte Carlo simulation is presented. The simulation results correlating to the measurement results of part (ii) and (iii) are discussed.
- (v). Chapter five reviews the LDO regulators. It also introduces a transient-assisted driving stage circuit design technique for achieving fast transient regulator design.
- (vi). Chapter six presents the low-voltage low-quiescent, process-temperature aware OCL-LDO regulator with low transient spike and transient sustainability. The measurement results are discussed.
- (vii). Chapter seven gives the conclusions and recommendations for future works.

Chapter Two

Threshold Voltage Reference Circuits

This Chapter briefs the fundamental information of the threshold voltage (V_{TH}) reference circuits and review different studies and related circuit techniques realized in the recently-published works. Finally, a new V_{TH} reference circuit is proposed and the measurement results are discussed.

2.1 Introduction

Threshold voltage (V_{TH}) reference circuit can generate the extrapolated V_{TH} of a single MOSFET at absolute 0 K (V_{TH0}), which is stabilized over temperature and supply voltage. Due to the process dependence characteristic of V_{TH0} , the V_{TH} reference circuit is able to sense the intrinsic V_{TH} parameter to yield the process information [25]. Of particularly noted, since most V_{TH} reference circuits [15], [16], [19], [20] are fabricated in long-channel CMOS process technologies, this turns out that their $T.C.$ performance may be greatly influenced in the context of PVT variations in advanced nanometer technologies.

As mentioned above, these non-ideal effects in the aggressively scaled technology increase the difficulty in the design of a V_{TH} reference circuit with performance metrics having strong immunity against PVT variations in the context of aggressively scaled nanometer technology. For examples, several threshold-related voltage references [17], [18], and [23] realized in advanced technologies can be observed with common characteristics of either consuming relatively large power or suffering from relatively high $T.C.$, high line sensitivities and possibly low PSR in majority. Of another

important issue, they cannot generate V_{TH0} owing to different voltage generation principles, thus causing the difficulty to provide the process information on the basis of the given circuit topologies. A 65nm V_{TH} reference circuit [24] has been recently reported. However, the improvement of $T.C.$ performance metric is restricted by its temperature compensation method whilst the circuit architecture also suffers from the issues of finite high-frequency PSR and line sensitivity.

Therefore, a new low-power performance-aware V_{TH} reference circuit that features high PSR, small $T.C.$ as well as low line sensitivity in nanometer CMOS technology is proposed and discussed.

2.2 Review of V_{TH} Reference Circuit

This section will review different studies and related circuit techniques realized in the recently-published works.

2.2.1. Temperature Effect of $V_{GS}(T)$ for Subthreshold MOFET

For a sub-threshold biased MOSFET with the assumption of long channel length/width and uniform substrate doping concentration, the relationship between its gate-source voltage $V_{GS}(T)$ and the temperature can be expressed as

$$V_{GS}(T) = V_{TH0} \left(1 - \frac{T}{T_r} \right) + V_{GS}(T_r) \left(\frac{T}{T_r} \right) + (\alpha_\mu - 1) \frac{\eta k_B T}{q} \ln \left(\frac{T}{T_r} \right) \quad (1)$$

where α_μ is the mobility temperature exponent (1.5~2) , η is the subthreshold slope factor, k_B is the Boltzmann constant, q is the elementary charge, T is the operating temperature in Kelvin (K) and T_r is the reference room temperature. V_{TH0} is the threshold voltage at absolute zero [15], [24], [89]. Considering the first-order temperature dependence in (1), $V_{GS}(T)$ appears to be a CTAT voltage since

$V_{GS}(T_r) < V_{TH0}$ in the weak inversion region. Hence, in a conventional Brokaw V_{TH} reference circuit, the first-order temperature compensated output voltage (V_{REF_1st}) can be generated utilizing a PTAT voltage to compensate the first-order temperature effect in $V_{GS}(T)$.

$$V_{REF_1st} = V_{GS}(T) + kV_{PTAT}(T) \quad (2)$$

where k is the coefficient of the PTAT voltage. The general compensation principle of V_{TH} reference circuit is depicted in Fig. 2.1.

Fig. 2.1 Compensation principle of V_{TH} reference circuit.

From Fig. 2.1, the V_{REF_1st} can be easily achieved by optimizing the coefficient k in (2). However, the $T \ln(T/T_r)$ term in (1) contributes to the nonlinearity of $V_{GS}(T)$ with respect to T . Thus, even the optimal first-order compensation is achieved; the reference output voltage has exhibited some temperature dependence terms. Therefore, the $T.C.$ of V_{REF_1st} will be limited by the nonlinear temperature effect in $V_{GS}(T)$, leading to the requirement of high-order temperature compensation.

Many research works pertaining to the threshold voltage reference circuit have been reported and several representative ones will be reviewed in the following subsection.

2.2.2. Linear Resistor Based V_{TH} Reference Circuit.

A low-voltage low-power CMOS V_{TH} reference circuit using linear resistor is proposed by Ferreira et al.[15]. It is implemented by relying on a PTAT voltage generated by a single resistor to compensate the temperature effect of $V_{GS}(T)$ of transistors operating in subthreshold region. The simplified schematic circuit is illustrated in Fig. 2.2. Q_4 operates in subthreshold region such that $V_{GS4}(T)$ will show the characteristic as described in (1). The PTAT current is obtained as

$$I_B(T) = \frac{V_{DSR1}}{R_1(T)} = \frac{V_{SG1} - V_{SG3}}{R_1(T)} = \frac{\eta_p V_T}{R_1(T)} \ln \left(\frac{K_2 K_3}{K_4 K_1} \right) \quad (3)$$

where η_p represents the subthreshold slope factor for PMOS Transistors and K_i denotes the aspect ratio for the corresponding devices.

Thus, the output voltage can be generated by

$$V_{OUT}(T) = R_2(T)I_B(T) + V_{GS4}(T) \quad (4)$$

For same type of resistors that have the same $T.C.$, the resistor ratio will be approximately independent on the temperature. Assuming the higher-order $T.C.$ is too small to be negligible, it is described as

$$\frac{R_2(T)}{R_1(T)} = \frac{R_2(T_r) \left[1 + \alpha(T - T_r) + \beta(T - T_r)^2 \right]}{R_1(T_r) \left[1 + \alpha(T - T_r) + \beta(T - T_r)^2 \right]} \approx \frac{R_2(T_r)}{R_1(T_r)} \quad (5)$$

in which, α is the first-order $T.C.$ of the resistor and β is the second-order $T.C.$ of the resistor. T_r is the room temperature.

Fig. 2.2 Schematic of Ferreira's V_{TH} reference circuit [15].

Substituting (1) and (3) to (4), the output voltage is expressed as

$$V_{OUT}(T) = \begin{cases} \left[V_{GS}(T_r) - V_{TH0} \right] \left(\frac{T}{T_r} \right) + \frac{R_2(T_r)}{R_1(T_r)} \eta_p V_T \ln \left(\frac{K_2 K_3}{K_4 K_1} \right) \\ + V_{TH0} + (\alpha_\mu - 1) \frac{\eta_n k_B T}{q} \ln \left(\frac{T}{T_r} \right) \end{cases} \quad (6)$$

Similarly, η_n represents the subthreshold slope factor for NMOS Transistors. According to (6), the first term decreases linearly with temperature while the second term increases with temperature. Neglecting the nonlinear logarithmic term introduced by $V_{GS4}(T)$, $V_{OUT}(T)$ can be optimized by changing the resistor ratio and transistors' dimensions to compensate its temperature effect. Therefore, a compensated output voltage reference can be approximated as

$$V_{OUT}(T) \approx V_{TH0} \quad (7)$$

Although a good solution for the threshold voltage reference is reported using the weak inversion transistors and linear resistors other than the bipolar transistors, the $T.C.$ is limited by the nonlinear temperature effect existing in $V_{GS}(T)$. In addition, due to the simple current source structure, the line sensitivity or PSR performance is relatively poor which constrains its capability for applications requiring a good immunity against the fluctuation of supply voltage [90], [91].

2.2.3. Subthreshold Region Transistors Based V_{TH} Reference Circuit

A CMOS V_{TH} reference circuit without resistors is presented by Ueno et al. [19]. Fig. 2.3 shows the core circuit schematic. It makes use of MOSFET devices biased in subthreshold region so as to avoid the use of passive resistors. Stacked transistors are used to generate several thermal voltages with positive $T.C.$ to compensate the negative $T.C.$ of a MOSFET's threshold voltage. As such, a V_{TH} reference of zero $T.C.$ can be achieved.

From Fig. 2.3, all transistors are operating in subthreshold region except M_{R1} that works in triode region. The active resistance can be expressed as

$$R_{M_{R1}} = \frac{1}{K_{R1} \mu C_{OX} (V_{REF} - V_{TH})} \quad (8)$$

where K_{R1} is the aspect ratio of M_{R1} , μ represents the carrier mobility; and C_{OX} denotes the gate-oxide capacitance.

Thus the PTAT current I_P can be derived as

$$I_P = \frac{V_{DSR1}}{R_{M_{R1}}} = \frac{V_{GS1} - V_{GS2}}{R_{M_{R1}}} = K_{R1} \mu C_{OX} (V_{REF} - V_{TH}) \eta V_T \ln(K_2/K_1) \quad (9)$$

where K_1 and K_2 denotes the aspect ratio of M_1 and M_2 , respectively.

Fig. 2.3 Schematic of Ueno's V_{TH} reference circuit [19]

Injecting I_P to M_3 - M_7 , the output reference voltage will be

$$V_{REF} = V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} \quad (10)$$

For MOSFET operating in subthreshold region, the drain current [92] is

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (11)$$

where $I_0 = \mu C_{OX} (\eta - 1) V_T^2$ and assuming $V_{DS} > 0.1$ V.

Since M_3 - M_7 operate in subthreshold region, by substituting (11) to (10), (10) can be simplified as

$$V_{REF} = V_{GS4} + \eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right) = V_{TH} + \eta V_T \ln\left(\frac{3I_P}{K_4I_0}\right) + \eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right) \quad (12)$$

The V_{TH} of the transistor is assumed [93] to depends on the temperature and can be expressed as

$$V_{TH}(T) = V_{TH}(T_r) - \theta(T - T_r) = V_{TH0} - \theta T \quad (13)$$

where θ is the slope magnitude of V_{TH} with respect to temperature.

Refer to (12) and (13), by properly choosing the aspect ratios of transistors to change the coefficients of the two thermal voltage terms in (12) so as to compensate that in V_{TH} with negative $T.C.$, a temperature compensated reference voltage can be achieved

$$V_{REF}(T) \approx V_{TH0} \quad (14)$$

This V_{TH} reference circuit can provide good $T.C.$ and consumes low power. However, the threshold voltage mismatch of the stack transistors (M_3 & M_4) and (M_5 & M_6) raises the sensitivity to the process variations. The growing SCE and V_{TH} variations have imposed more challenges for the robust circuit implementation when aggressive technology scaling to sub-90nm CMOS process technology. Thus, this issue needs to be addressed.

2.2.4. Saturation Region Transistors Based V_{TH} Reference Circuit

Another CMOS V_{TH} reference circuit, which is based on a saturation region MOSFET is reported by Lee et al. [20]. The proposed circuit schematic is shown in Fig. 2.4. A saturation region operated transistor M_1 is utilized to generate the reference output voltage along with an active resistor M_2 that operates in triode region. The working theory is described as follows:

Fig. 2.4 Schematic of Lee's V_{TH} reference circuit [20]

As M_3 and M_4 operates in subthreshold region while M_2 is biased in triode region, the branch current I_R will be

$$I_R = \frac{V_{DS2}}{R_{M_2}} = \frac{V_{GS4} - V_{GS3}}{R_{M_2}} = K_2 \mu_2 C_{OX} (V_{OUT} - V_{TH2}) \eta V_T \ln(K_3/K_4) \quad (15)$$

where each parameter has its usual meaning.

When M_1 is kept in saturation region, the drain current can be derived as

$$I_R = \frac{1}{2} K_1 \mu_1 C_{OX} (V_{GS1} - V_{TH1})^2 = \frac{1}{2} K_1 \mu_1 C_{OX} (V_{OUT} - V_{TH1})^2 \quad (16)$$

Combining (16) and (15), assuming the threshold voltage of M_1 matches to the one of M_2 ($V_{TH1} \approx V_{TH2}$), the output voltage can be simplified as

$$V_{OUT} = V_{TH0} - \theta T + \frac{2K_2}{K_1} \frac{\mu_2 \eta \ln(K_3/K_4)}{\mu_1} V_T \quad (17)$$

Obviously, the coefficient of the thermal voltage can be properly designed by adjusting the aspect ratio for M_1 - M_4 such that it can cancel the temperature effect in $V_{TH}(T)$ which is of opposite $T.C.$. Therefore, a temperature compensated threshold output voltage can be obtained, which is approximated as V_{TH0} according to (19).

Owing to the simple circuit structure, this V_{TH} reference circuit can achieve low $T.C.$ performance. However, the V_{TH} mismatch between M_3 and M_4 , as well as M_1 and M_2 makes the $T.C.$ performance becomes more prone to the process variation, especially for the advanced sub-90nm CMOS technology in which the SCE contributes another key factor that limits the circuit performance [53].

2.2.5. Second-order Temperature Compensated V_{TH} Reference Circuit

A 65nm V_{TH} reference circuit [24] with the implementation of second-order temperature compensation has been recently reported by Tan et al.. It relies on the use of different temperature properties of two types of resistors (P+ diffusion and poly resistors). As such, the induced second-order temperature effect can be used to compensate that of $V_{GS}(T)$ in the Brokaw V_{TH} circuit. The proposed circuit schematic is shown in Fig. 2.5.

Refer to the Brokaw circuit in Fig. 2.5, the output voltage is generated as

$$\begin{aligned} V_{OUT}(T) &= V_R + V_{GS1}(T) = [2I_1(T) + I_2(T)] R_2(T) + V_{GS1}(T) \\ &= 2\eta \frac{k_B}{q} \ln\left(\frac{K_2}{K}\right) \frac{R_2(T)}{R_1(T)} T + N\eta \frac{k_B}{q} \ln\left(\frac{K_4}{K_3}\right) \frac{R_2(T)}{R_5(T)} T + V_{GS1}(T) \end{aligned} \quad (18)$$

Fig. 2.5 Schematic of Tan's V_{TH} reference circuit.

Assume that the first-order $T.C.$ of R_2 and R_1 (high resistive poly resistor), and R_5 (P+ diffusion resistor) is α and β , then applying the Taylor series, the temperature dependence of $[R_2(T)/R_5(T)]T$ can be expressed as

$$\frac{R_2(T)}{R_5(T)}T \approx \frac{R_2(T_r)}{R_5(T_r)} \left\{ [2(\alpha - \beta)T_r + 1]T + (\alpha - \beta)T^2 + (\alpha - \beta)T_r^2 \right\} \quad (19)$$

Substituting (19) and (1) to (18), V_{OUT} can be optimized to be approximately equal to V_{TH0} of zero $T.C.$ by choosing the appropriate values for the resistors and aspect ratios.

Unfortunately, the improvement of $T.C.$ performance metric is restricted by its temperature compensation method whilst the circuit architecture also suffers from the issues of finite high-frequency PSR and line sensitivity. Furthermore, using the Taylor series, the $T \ln(T/T_r)$ term from (1) can be expanded as

$$T \ln\left(\frac{T}{T_r}\right) \approx (T - T_r) + \frac{(T - T_r)^2}{2T_r} - \frac{(T - T_r)^3}{6T_r^2} \quad (20)$$

From (20) it can be seen that the second-order temperature effect is symmetrical to the reference temperature, whereas the third-order term suffers from unsymmetrical property. When $T \leq T_r$, $V_{GS}(T)$ curve will exhibit a larger thermal drift, contributing to

stronger nonlinear effect at the lower temperature segment (LTS) ($T \leq T_r$) than that at the upper temperature segment (UTS) ($T > T_r$). Furthermore, for the slope of $V_{GS}(T)$ as $dV_{GS}(T)/dT$, its changing rate can be further obtained via the second-order derivative of $V_{GS}(T)$ to yield

$$\frac{\partial^2 V_{GS}(T)}{\partial T^2} = (\alpha_\mu - 1) \frac{\eta k_B}{q} \frac{1}{T} \quad (21)$$

From (21), it is apparent that a lower T will lead to a larger value of $\partial^2 V_{GS}(T)/\partial T^2$. For this reason, the rate of change of the slope pertaining to $V_{GS}(T)$ increases faster at the LTS than that of the upper counterpart. The results suggest that stronger nonlinear effect appears at the LTS with respect to the UTS. From this perspective, a new dual-segment nonlinear temperature compensation method is proposed in this nanometer based V_{TH} reference circuit, with the goal of improved $T.C.$ for meeting one of performance-aware objectives.

2.3 Proposed 65nm CMOS Threshold Voltage Reference circuit

The working principle, circuit implementation as well as the measurement results discussion will be presented in this Section. The acronyms and nomenclature which are adopted are listed in the Acronyms and Symbols page.

2.3.1. Operation Principle of Proposed V_{TH} Reference Circuit

Fig. 2.6 illustrates the conceptual synthesis of the dual-segment temperature-compensated voltage reference from five process design steps. $I_{PTAT1}(T)$ and $I_{PTAT2}(T)$ are denoted as the proportional to absolute temperature (PTAT) currents while $I_{NCTAT}(T)$ denoted as the non-linear complementary to absolute temperature (NCTAT) current. They are converted to the corresponding voltage, $V_{NPTAT}(T)$ and $V_{NCTAT}(T)$, through the I - V_{NPTAT} and I - V_{NCTAT} converters. This arrangement will provide the segment compensation for the above mentioned nonlinear temperature characteristic in $V_{GS}(T)$ to yield a low $T.C.$ V_{TH} reference circuit.

The UTS compensation is based on a 0K Brokaw V_{TH} reference circuit comprising both first-order and second-order compensation. Using the I - V_{NPTAT} converter, a $V_{NPTAT}(T)$ is synthesized. It includes the sum of the PTAT and NPTAT voltages generated by means of different temperature properties from two types of resistor [94]. Its temperature characteristic is denoted in Fig. 2.6(b). When the $V_{GS}(T)$ is summed with the $V_{NPTAT}(T)$ for the first-level compensation, the minute second-order effect of $V_{GS}(T)$ at high temperature can be effectively compensated by the second-order

Fig. 2.6 Operation principle of the proposed V_{TH} reference circuit.

compensation.

On the other hand, the dominant first-order compensation at LTS is not adequate to compensate the strong nonlinear $V_{GS}(T)$ at low temperatures as implied in (3). This yields a partial temperature compensated voltage, with the temperature characteristic depicted in Fig. 2.6(c). Such the generated voltage is called the upper segment compensated reference voltage $V_{REF_SEG}(T)$.

In order to further improve the compensation in LTS, a $V_{NCTAT}(T)$ is needed to counteract the relatively large nonlinear $V_{GS}(T)$ at this segment. Since the $V_{NCTAT}(T)$ is designed to be dominant in the LTS, its value tends to be very small or considered to be negligible in the UTS as shown in Fig. 2.6(d). It is noted that the $V_{NCTAT}(T)$ is subsequently subtracted from the $V_{REF_SEG}(T)$ for the second-level compensation dedicated to the LTS.

In brief, the nonlinear terms of $V_{GS}(T)$ at both segments can be effectively compensated. As a consequence, the target output voltage V_{REF} will be made temperature independent over the operating temperature range as illustrated in Fig. 2.6(e).

2.3.2.CMOS Implementation of Proposed V_{TH} Reference Circuit

The V_{TH} reference circuit in Fig. 2.7 consists of a pre-regulator, a 0 K Brokaw V_{TH} core circuit with a NPTAT voltage generator and a segment NCTAT voltage generator. The pre-regulator loop [95] is used to enhance the PSR of V_{TH} reference circuit for meeting another performance-aware objective. All the resistor values are listed in Table 2-I. As seen in Fig. 2.7, the operational transconductance amplifier (OTA) in the core circuit is employed to equalize the voltages at nodes A and B such that the

Fig. 2.7 Schematic of the proposed MOSFET V_{TH} reference circuit.

TABLE 2-I RESISTOR VALUES FOR THE RESISTORS IN FIG.2.7.

Devices	Values (Ω)	Devices	Values (Ω)	Devices	Values (Ω)
R_1	398k	R_5, R_6	860k	R_{11}	2.58M
R_2	1.4M	R_7, R_8	258k	R_{12}	25.9k
R_3	208k	R_9	600k	R_C	17.18k
R_4	159k	R_{10}	172k		

corresponding current flowing through M_1 and M_2 as well as the resistive load ($R_5 = R_6$, $R_7 = R_8$) are identical. The Miller capacitor C_3 is used to ensure the loop stability. Moreover, a simple output source follower, composed of M_{11} and M_{12} , is added at the output of OTA to permit the current sinking capability. The core circuit, with the aid of the $V_{\text{NPTAT}}(T)$ generator, provides $V_{\text{REF_SEG}}(T)$ at the node G_1 . This resulting nodal potential behaves negative $T.C.$ at the LTS whilst remaining constant at the upper counterpart.

To realize the temperature compensation at the LTS, $V_{\text{NCTAT}}(T)$ is established by injecting $I_{\text{NCTAT}}(T)$ from the NCTAT current generator into R_C , as illustrated in Fig. 2.7. It is then able to compensate the nonlinear negative $T.C.$ arising from $V_{\text{REF_SEG}}(T)$.

Consequently, the overall combination of two compensated segments will offer an improved $T.C.$ over the operating temperature range. Following the operation principle as graphically illustrated from design step (a) to design step (e) in Fig. 2.6, the analysis of nonlinear compensation is as follows:

(I). Gate-Source Voltage Generation

The gate-source voltage is provided by M_1 in the core circuit as shown in Fig. 2.7. To reduce the variation due to SCE, M_1 and M_2 are implemented using long channel length (3 μm in this design). Meanwhile, they are biased in the subthreshold region. Of particularly noted, the temperature characteristic of $V_{\text{GS1}}(T)$, which is corresponding to the design step (a) of Fig. 2.6, is described by (1) in Section 2.2.1.

(II). NPTAT Voltage Generation

Referring to Fig. 2.7, it realizes the design step (b) of Fig. 2.6 which comprises both linear and nonlinear PTAT segments. The core circuit provides a PTAT current $I_{\text{PTAT1}}(T)$ through a high resistive poly resistor (R_1). Another PTAT current $I_{\text{PTAT2}}(T)$ is

concurrently generated through a P+ diffusion resistor (R_3). These currents are then combined and converted to a voltage by R_2 (high resistive poly resistor) which functions as a I - V_{NPTAT} converter as shown in Fig. 2.6. This gives $V_{\text{NPTAT}}(T)$ at node S_1 having a PTAT² voltage characteristic because of different temperature properties between R_2 and R_3 . As such, it will compensate the moderate nonlinear $V_{\text{GS1}}(T)$ at the UTS.

To demonstrate the compensation at UTS, the reference temperature point is shifted to a higher temperature T_1 other than room temperature T_r . Therefore, the first-order derivative of $V_{\text{REF_SEG}}(T)$ can be designed to be zero at T_1 as shown in Fig. 2.6(c). T_1 is approximately the middle point between T_r and maximum temperature (T_H), leading to $T_1 \approx (T_r + T_H) / 2$. In this way, the temperature compensation can be established for the UTS.

In the core circuit, M_1 and M_2 operate in the weak inversion region. $I_{\text{PTAT1}}(T)$ can be expressed in the form of $I_{\text{PTAT1}}(T) = [V_{\text{GS1}}(T) - V_{\text{GS2}}(T)] / R_1(T) \approx \eta V_T \ln(K_2/K_1) / R_1(T)$, which assumes that M_1 and M_2 have the identical V_{TH} and drain current (I_D). K_1 and K_2 represent the respective aspect ratio and V_T is the thermal voltage. Similarly, we can obtain $I_{\text{PTAT2}}(T) \approx \eta V_T \ln(K_4/K_3) / R_3(T)$. For the given approximation that $R(T) \approx R(T_1)[1 + \alpha(T - T_1)]$ and α is the first-order $T.C.$ of resistor, $V_{\text{NPTAT}}(T)$ can be obtained as

$$\begin{aligned}
 V_{\text{NPTAT}}(T) &= [2I_{\text{PTAT1}}(T) + I_{\text{PTAT2}}(T)] R_2(T) \\
 &= 2\eta \frac{k_B}{q} \ln\left(\frac{K_2}{K_1}\right) \frac{R_2(T)}{R_1(T)} T + \eta \frac{k_B}{q} \ln\left(\frac{K_4}{K_3}\right) \frac{R_2(T)}{R_3(T)} T \\
 &\approx 2\eta \frac{k_B}{q} \ln\left(\frac{K_2}{K_1}\right) \frac{R_2(T_1)}{R_1(T_1)} T + \eta \frac{k_B}{q} \ln\left(\frac{K_4}{K_3}\right) \frac{R_2(T_1)}{R_3(T_1)} [T + (\alpha_1 - \alpha_2)(T - T_1)^2]
 \end{aligned} \tag{22}$$

where α_1 is the first-order $T.C.$ of R_2 and α_2 is the first-order $T.C.$ of R_3 . Since R_1 and R_2 are the same resistor type, $R_2(T)/R_1(T)$ will be temperature independent to the first

order. As suggested in (22), the first term is regarded as the first-order compensation T term for $V_{GS1}(T)$. Turning to the second term, since $\alpha_1 < 0$ and $\alpha_2 > 0$, a negative nonlinear T^2 term is contributed by $T[R_2(T)/R_3(T)]$. This aims to reduce the second-order thermal drift in $V_{GS1}(T)$ at high temperatures. Of particularly noted, the third-order term in the Taylor series expansion of $T[R_2(T)/R_3(T)]$ is quite small so that its contribution is negligible in the upper segment.

(III). Voltage Reference Generation with Upper Temperature

Segment Compensation

This is referred to the core circuit which is embedded with NPTAT voltage generator in Fig. 2.7. The combining effect of the design step (a) and the design step (b) yields the design step (c) in Fig. 2.6. As a result, the $V_{REF_SEG}(T)$ is obtained as $V_{REF_SEG}(T) = V_{NPTAT}(T) + V_{GS1}(T)$. Based on (1) and (2), by expanding $T \ln(T/T_1)$ term in $V_{GS1}(T)$ using Taylor Series at T_1 instead of T_r and assuming higher-order T terms are negligible, $V_{REF_SEG}(T)$ can be approximated as

$$V_{REF_SEG}(T) \approx V_{TH0} + a_1 T + a_2 (T - T_1)^2 - a_3 (T - T_1)^3 \quad (23)$$

where a_1 , a_2 and a_3 are the temperature independent coefficients.

By properly choosing the aspect ratios of transistors ($M_1 - M_4$) and the resistors to equalize the temperature coefficient a_1 to be zero, a compensated voltage [$V_{REF_SEG}(T)$] with an optimal point being approximately relocated at T_1 can be generated. This can be generalized as follows:

$$V_{REF_SEG}(T) \approx V_{TH0} + a_2 (T - T_1)^2 - a_3 (T - T_1)^3 \quad (24)$$

In (24), at the UTS, the third-order term is relatively small and negligible. Although a_2 tends to be zero after this first-level compensation in principle, it remains small due to

imperfect compensation in practice. In the practical design guideline, the typical value for this residual second-order term should be controlled to less than 2 mV (about 0.4% deviation from the targeted nominal V_{TH0} value). This is assumed as follows:

$$\Delta V \approx a_2 (T_H - T_l)^2 \approx a_2 \left(\frac{T_H - T_r}{2} \right)^2 \leq 2 \text{ mV} \quad (25)$$

Using the typical process and design parameters for the V_{TH} reference circuit, the simulated $V_{REF_SEG}(T)$ and its first-order derivative with respect to temperature are demonstrated in Fig. 2.8(a) and (b), respectively. It can be seen that the dominant DC average value of $V_{REF_SEG}(T)$ is V_{TH0} which is around 500 mV for a low threshold NMOS device in this 65nm CMOS process. Moreover, it has confirmed the almost flat temperature response starting from T_r in the UTS whilst the deviation of V_{TH0} at T_r is much less than 1 mV. Compared to this dominant DC term V_{TH0} , the second term remains insignificant. Thus, it meets the design guideline in (25). Therefore, the upper segment compensated voltage can be achieved through the first-level compensation. On the contrary, the residual thermal drift at the LTS can rise to few mV in the exemplary design.

Fig. 2.8 (a) Simulated $V_{REF_SEG}(T)$ with respect to temperature. (b)

Simulated slope of $V_{REF_SEG}(T)$ with respect to temperature.

(IV). NCTAT Voltage Generation

For the design step (d) of Fig. 2.6, it is realized by the NCTAT voltage generator in Fig. 2.7. The NCTAT current generator comprises a CTAT voltage generator formed by transistors $M_{16} - M_{19}$ and resistors $R_9 - R_{11}$ in conjunction with a nonlinear current generator including transistors $M_{13} - M_{15}$ and resistor R_{12} . It is noted that M_{17} is implemented by a native transistor to reduce the high drain voltage of M_{16} .

Consider the transistor M_{15} , it is biased by a CTAT voltage, $V_{GS16}(T)$. At UTS, M_{15} works in the sub-threshold region, yielding considerably small and linear $I_{12}(T)$. When the temperature decreases from the reference point T_r at the LTS, the transistor M_{15} starts moving to the saturation region due to reduction of threshold voltage through the increase of body bias from the tap-point voltage of the resistor chain $R_{10} - R_{11}$ with CTAT effect. Therefore, $I_{12}(T)$ has larger magnitude whilst having nonlinear and temperature segment characteristic.

In order to generate $I_{NCTAT}(T)$, a nonlinear current mirror (M_{13} , M_{14} and R_{12}), with R_{12} serving as the source degeneration resistor, is employed. As such, a stronger nonlinear effect appears in $I_{NCTAT}(T)$, allowing $V_{NCTAT}(T)$ to compensate the residual temperature effect at the LTS.

Similar to the treatment at UTS, it assumes that the reference temperature for the LTS is located at T_2 which is approximately the middle point between minimum temperature (T_L) and T_r , namely $T_2 \approx (T_L + T_r) / 2$, as depicted in Fig. 2.6(c). For simplicity, the temperature effect of resistors in the following analysis will be ignored due to their relatively small $T.C.$ with respect to that of $I_{NCTAT}(T)$.

a) Generation of NCTAT Current

The threshold voltage of M_{15} with a forward body bias voltage, denoted as $V_{TH15_B}(T)$, can be obtained following [92] as

$$V_{TH15_B}(T) \approx V_{TH15}(T) + \gamma \left[\sqrt{2\phi_F(T) - V_{BS15}(T)} - \sqrt{2\phi_F(T)} \right] \quad (26)$$

where γ is the body-effect constant, $\phi_F(T) = (k_B T / q) \ln(N_A / n_i)$ is the Fermi potential in which N_A is the channel doping concentration and n_i is the intrinsic carrier concentration. $V_{BS15}(T)$ represents the body bias voltage of M_{15} . It is defined as

$$V_{BS15}(T) \approx V_{GS16}(T) \frac{1}{1 + R_{10}(T_r)/R_{11}(T_r)} \quad (27)$$

As can be seen from (26), the higher the $V_{BS15}(T)$, the smaller the $V_{TH15_B}(T)$ will be. Refer to (27), through the resistor ratio of R_{10}/R_{11} to define $V_{BS15}(T)$, the threshold temperature point at which M_{15} changes its operation from sub-threshold region to saturation region can be designed. $V_{BS15}(T)$ follows $V_{GS16}(T)$ with scaled CTAT characteristic. The analysis of this operation principle is described as follows:

In general, for identical type of MOS device without forward body bias, the threshold voltages for M_{16} [$V_{TH16}(T)$] and M_{15} [$V_{TH15}(T)$] tend to track each other in terms of temperature effect. However, due to the CTAT nature of added forward bias $V_{BS15}(T)$ as described in (27), the thermal changing rate of $V_{TH15_B}(T)$ turns out to be less than that of M_{16} counterpart according to (26). As a result, [$V_{GS16}(T) - V_{TH15_B}(T)$] will exhibit a negative $T.C.$.

Substituting (27) into (26) and setting that the gate-source voltage of M_{15} equals to its threshold voltage expressed in (26), a resistor ratio R_{10}/R_{11} of 1/15 is then obtained using the typical process and design parameters. This is based on that the center reference temperature T_r between the two segments is at room temperature. Pertaining to the negative $T.C.$ of [$V_{GS16}(T) - V_{TH15_B}(T)$], the analysis of $I_{NCTAT}(T)$ generation can be divided into two cases:

i) At Upper Temperature Segment: In this case, due to small body bias voltage $V_{BS15}(T)$, the reduction of $V_{TH15_B}(T)$ is insignificant. M_{15} operates in the sub-threshold region. While $V_{DS15} > 3V_T$, the current $I_{12}(T)$ is derived as [92]

$$I_{12}(T) = K_{15} I_{D0} \exp \left[\frac{V_{GS16}(T) - V_{TH15_B}(T)}{\eta V_T} \right] \quad (28)$$

where K_{15} is the aspect ratio of M_{15} and I_{D0} implies the characteristic current [92]. Due to the negative $T.C.$ characteristic of $\left[V_{GS16}(T) - V_{TH15_B}(T)\right]/(\eta V_T)$, using the Taylor series expansion at the reference temperature T_2 , (28) can be simplified and modeled as

$$I_{12}(T) \approx K_{15} A_0 \exp\left[-A_1 (T - T_2)\right] \quad (29)$$

where A_0 and A_1 are constants. As indicated in (29), $I_{12}(T)$ is an exponential function with respect to T . When $T > T_r$ and $T_r > T_2$, the current magnitude at UTS is considerably small. It does not have significant effect in the upper segment temperature compensation.

ii) *At Lower Temperature Segment:* When $V_{BS15}(T)$ increases under forward biasing condition, $V_{TH15_B}(T)$ decreases to the extent that the gate-overdrive voltage of M_{15} becomes larger than zero. Hence, the transistor is gradually driven towards the saturation region and the current $I_{12}(T)$ is defined as

$$I_{12}(T) = \frac{1}{2} \mu_n(T) C_{ox} K_{15} \left[V_{GS16}(T) - V_{TH15_B}(T)\right]^2 \quad (30)$$

where $\mu_n(T)$ is the electron mobility of NMOS transistors with the model expression of $\mu_n(T) = \mu_n(T_r) (T/T_r)^{-2}$ [93]. C_{ox} is the gate oxide capacitance per unit area. It is apparent from (30) that a NCTAT current $I_{12}(T)$ is generated at this LTS.

Refer to the current mirror transistor pair, M_{13} and M_{14} , which operate in the sub-threshold region, $I_{NCTAT}(T)$ can be expressed as

$$\begin{aligned} I_{NCTAT}(T) &= \frac{K_{13}}{K_{14}} I_{12}(T) \exp\left\{\left[V_{SG13}(T) - V_{SG14}(T)\right]/(\eta V_T)\right\} \\ &= \frac{K_{13}}{K_{14}} I_{12}(T) \exp\left\{\left[I_{12}(T) R_{12}(T)\right]/(\eta V_T)\right\} \end{aligned} \quad (31)$$

Based on the NCTAT characteristic of $I_{12}(T)$, (31) can be generalized as follows:

$$I_{NCTAT}(T) \propto I_{NCTAT0} I_{12}(T) \exp[-B_1 K_{15} R_{12}(T_r)(T - T_2)] \quad (32)$$

where $I_{NCTAT0} = (K_{13}/K_{14}) \exp[B_0 K_{15} R_{12}(T_r)]$ is a small constant current term which depends on the process and design parameters. B_0 and B_1 are also the constants. As revealed by (32), the nonlinear effect will be enhanced at this LTS owing to the exponential term. This provides temperature compensation for strong nonlinear effect in $V_{REF_SEG}(T)$ as suggested in (24).

b) Generation of NCTAT Voltage

When the segment $I_{NCTAT}(T)$ is injected to R_C , a $V_{NCTAT}(T)$ is developed as $V_{NCTAT}(T) = R_C(T) I_{NCTAT}(T)$. Based on the exponential function (32) with temperature in $I_{NCTAT}(T)$, it can be approximated as the sum of a positive $(T - T_2)^2$ term and a negative $(T - T_2)^3$ term through the Taylor's Series expansion. This nonlinear generation voltage enables the compensation of similar thermal behavior arising from the residual thermal drift as encountered in $V_{REF_SEG}(T)$ at the LTS.

In this work, the value of R_C at room temperature (25°C) is 17.18 kΩ while the design current of I_{NCTAT} is 113.9 nA. As a result, $V_{NCTAT}(T)$ can have a small voltage magnitude at UTS such that the effect arising from the LTS compensation on UTS of $V_{REF_SEG}(T)$ can be negligible. The simulated $V_{NCTAT}(T)$ and its first-order derivative against temperature under typical process and design parameters is illustrated in Fig. 2.9(a) and (b), respectively. As interpreted from Fig. 2.9(a), the thermal drift ΔV at the UTS is only few mVs which can be negligible with respect to the DC average output voltage of about 500 mV in this design.

On the other hand, it offers comparable voltage level with reference to that of the nonlinear segment voltage level in $V_{REF_SEG}(T)$ at the LTS shown in Fig. 2.8(a).

Fig. 2.9 (a) Simulated $V_{NCTAT}(T)$ with respect to temperature. (b) Simulated slope of $V_{NCTAT}(T)$ with respect to temperature.

Turning to the slope of $V_{NCTAT}(T)$ in Fig. 2.9(b), it reveals that the thermal effect of $V_{NCTAT}(T)$ is similar as that of $V_{REF_SEG}(T)$ depicted in Fig. 2.8(b). This confirms the effectiveness of the segment NCTAT voltage for the LTS compensation.

The Monte-Carlo simulation results of $V_{NCTAT}(T)$ with respect to temperature and its voltage drift (ΔV_{NCTAT}) at LTS under a sample size of 300 with 3σ coverage are depicted in Fig. 2.10(a) and (b), respectively. From Fig. 2.10(a), it shows that the variation of curvature shape of $V_{NCTAT}(T)$ illustrated in Fig. 2.9(a) is due to the process variations on I_{NCTAT} and R_C in this 65nm CMOS technology. Based on the Monte

Fig. 2.10 (a) Monte-Carlo simulation results of $V_{NCTAT}(T)$ with respect to temperature.(b) Monte-Carlo simulation results of V_{NCTAT} voltage drift (ΔV_{NCTAT}) at LTS.

Carlo simulation results from Fig. 2.10(b), ΔV_{NCTAT} exhibits a mean value of 4.79 mV and a standard deviation of 0.91 mV at LTS. This variation will cause the imperfect compensation on the LTS. To address this issue, the temperature calibration is applied and discussed in Section 2.3.3. According to Fig. 2.10(a), in spite of the process variation, $V_{NCTAT}(T)$ still exhibits a similar thermal behavior when compared to the residual thermal effect at LTS in $V_{REF_SEG}(T)$ in Fig. 2.8(a). This leads to the successful nonlinearity compensation.

(V). Final Voltage Generation with Added Lower Temperature

Segment Compensation

By summing $V_{REF_SEG}(T)$ and $V_{NCTAT}(T)$ in the final design step (e) of Fig. 2.6, the output voltage of V_{TH} reference circuit is as follows:

$$V_{REF}(T) = V_{REF_SEG}(T) - V_{NCTAT}(T) \approx \begin{cases} V_{TH0} + m_0 + m_1T + m_2T^2 + m_3T^3, & T \leq T_r \\ V_{TH0}, & T > T_r \end{cases} \quad (33)$$

where m_0 , m_1 , m_2 and m_3 are constants which are functions of I_{NCTAT0} [as generalized in (32)] and the resistor R_C . By equalizing m_0 to zero for compensating the residual thermal drift whilst relating the temperature coefficients for first-order term m_1 and high-order T terms m_2 and m_3 in (33), the final output voltage V_{REF} over the whole temperature range can be approximated as

$$V_{REF}(T) \approx V_{TH0} \quad (34)$$

It can be seen from (34), with the proposed segment temperature compensation, an output voltage with improved $T.C.$ can be achieved.

Fig. 2.11 shows the simulated V_{REF} with respect to temperature. It has revealed that the thermal drift at LTS is kept within 1 mV, leading to successful second-level compensation at this segment. Comparing with Fig. 2.8(a), it can be seen that a small voltage drift exists at UTS. This is due to the minute sub-threshold current at UTS shown in Fig. 2.9(a), whereas it is insignificant to the overall output voltage. According to Fig. 2.11, the voltage drift arising from $V_{NCTAT}(T)$ at the UTS becomes less than 1.5 mV, which is negligible in comparison to the DC average voltage V_{TH0} . These results have confirmed that the dual-segment compensation permits low $T.C.$ performance.

Fig. 2.11 Simulated V_{REF} with respect to temperature.

(VI). PSR Enhancement

A pre-regulator loop [95] (enclosed in the left dashed box in Fig. 2.7) is added to enhance the PSR of this V_{TH} reference circuit. M_{R1} in conjunction with the current source I_{BR} form the inverting gain stage for the establishment of feedback loop in the pre-regulator. I_{BR} is a PTAT current from the conventional constant-gm current source [96]. M_{R2} and M_{R3} form the source follower. They are implemented with native transistors with almost zero threshold voltage to improve the operation headroom under minimum 1.1 V supply. C_1 and C_2 are compensation capacitors with capacitance of 2 pF. They are realized with native transistors to save chip area. With the aid of the feedback control loop, it can significantly shield V_{REF} from the ac fluctuations in the main supply line, leading to a good PSR performance metric.

2.3.3. Results and Discussions

The segment-compensated V_{TH} reference circuit is designed and fabricated in UMC 65-nm CMOS process. The chip micrograph of the V_{TH} reference circuit is shown in Fig. 2.12. It occupies an active area of 0.0769 mm^2 .

Fig. 2.12 Microphotograph of the proposed V_{TH} reference circuit.

In order to address the major issues using this advanced nanometer CMOS technology, several circuit design techniques have been employed in this work. High- V_{TH} MOSFET devices (or IO devices in 65nm CMOS technology) are used to reduce the leakage current. Besides, the on-chip internal pre-regulator loop, which has been discussed in Section 2.3.2-(VI), is used to provide adequate immunity against the supply fluctuation. Meanwhile, a distance larger than $2\ \mu\text{m}$ from the transistor gate to adjacent well edge is applied in the matching layout for critical transistor pairs so as to mitigate the WPE effect. Similarly, the long channel length/width transistors are employed to reduce the short-channel effect and to enhance the device matching characteristic.

To compensate the $T.C.$ deviation of V_{REF} arising from the process variation, a two-step calibration is applied. The first step is to minimize the temperature dependency at UTS by a 4-bit calibration of R_2 . The trimming range of R_2 is around about $-21\%\sim+18.5\%$. After that, the LTS compensation is then carried out through a 3-bit calibration of R_C .

(I). Sensitivity of T.C. on Process Variations

It is noted that the process variations may influence the $T.C.$ performance of this V_{TH} reference circuit. In this section, the effects due to variations are discussed as follows.

Within-die (WID) variation and die-to-die (D2D) variation are two important categories of process variations [97], [98]. The WID variation will cause mismatch between transistors and resistors on the same die, influencing the output characteristics. It can be reduced with the careful layout techniques [98]. In this work, large-sized transistors and same resistor unit are used to minimize the mismatch. Regarding the D2D variation, it may cause the deviation of $T.C.$ because of the variation of resistors and resistor ratios used for the temperature compensation.

In order to examine these characteristics, Monte-Carlo (MC) simulations are conducted with a sample size of 300 with 3σ coverage. Fig. 2.13(a) presents the MC simulation results of the $T.C.$ with respect to the WID variation. It has revealed that the V_{TH} reference circuit exhibits a small sensitivity in view of WID variations. Fig. 2.13(b) shows the MC simulation results of the $T.C.$ with D2D variation. The $T.C.$ deviation is subject to increase with the effect of D2D variation. To achieve small $T.C.$ performance-aware objective, the temperature calibration is introduced for the resistors R_2 and R_C in NPTAT and NCTAT voltage generator circuit in Fig. 2.7, respectively. TABLE 2-II summarizes the simulated $T.C.$ performance at different process corners with and without calibration. It has confirmed that the temperature calibration yields low $T.C.$ in context of D2D process variation.

Fig. 2.13 (a) Monte-Carlo simulation results of $T.C.$ with WID variation. (b) Monte-Carlo simulation results of $T.C.$ with D2D variation.

TABLE 2-II SIMULATED TEMPERATURE DEPENDENCE PERFORMANCE AT PROCESS CORNERS WITH AND WITHOUT CALIBRATION.

Parameters	TT	SS	SF	FS	FF
T.C.(ppm/°C)	18.6	16.8/45.79*	25.4/68.37*	11.1/85.92*	24.8/75.71*
V_{OUT}(mV)	502	515/524.6*	511/520.5*	491/483*	478/481.6*
Temp. Range (°C)	-30-80	-30-80	-30-80	-30-80	-30-80
VDD (V)	1.1	1.1	1.1	1.1	1.1
Power (μW)	2.06	1.87	2.17	1.94	2.49

TT = Typical; SS = Slow NMOS/Slow PMOS; SF = Slow NMOS/Fast PMOS; FS = Fast NMOS/Slow PMOS; FF = Fast NMOS/Fast PMOS. *Results without Calibration

(II). Measurement Results

The temperature dependence of V_{TH} reference circuit is measured with a temperature range from $-30\text{ }^{\circ}\text{C}$ to $80\text{ }^{\circ}\text{C}$ at a supply voltage of 1.1V . All the measurement results are obtained after calibration. The power consumption measured at room temperature is $2.64\text{ }\mu\text{W}$. In this work, 15 samples were measured. Fig. 2.14(a) depicts the measured V_{REF} as a function of temperature. It can be seen that V_{REF} is very stable across temperature variation for each sample. Fig. 2.14(b) shows the measured V_{REF} as a function of temperature at various supply voltages. It has demonstrated that this V_{TH} reference circuit can work well at different voltage supplies. It is noted that the final output voltage of this V_{TH} reference circuit shows slight concaveness. It is due to the process variation that causes imperfect LTS compensation at one end. Pertaining to UTS compensation at another end, the process variation gradually builds up V_{DS} stress on transistors in the core circuit at high temperature under the approximate 0.75V pre-regulator supply, V_{PREG} . Fig. 2.15(a) shows the measured V_{REF} at room temperature as a function of power supply and it reveals the V_{TH} reference circuit operates well when the supply is higher than 1.1 V . The circuit has achieved a line sensitivity of 70.8 ppm/V in a supply range of 1.1 to 1.4 V . Fig. 2.15(b) shows the measured PSR of the V_{TH} reference circuit with pre-regulator loop (bottom curve) and without pre-regulator loop (top curve). Owing to the pre-regulator loop, this circuit offers a PSR of -54.5 dB at 100 Hz and -43.5 dB at 10 MHz without any filtering capacitor at the output node. In comparison to the design without pre-regulator loop, the proposed design improves about 20 dB in low frequency range, 30 dB in mid frequency range and 10 dB in high frequency range. Therefore, the proposed circuit with pre-regulator will increase the immunity against the supply variation from dc to high frequencies.

Fig. 2.14 (a) Measured output voltage V_{REF} as a function of temperature for 15 samples at 1.1 V supply voltage. (b) Measured output voltage V_{REF} as a function of temperature for different supply voltages.

Fig. 2.15 (a) Measured V_{REF} at room temperature as a function of V_{DD} . (b) Measured PSR with pre-regulator loop (bottom curve) and without pre-regulator loop (top curve) at room temperature and 1.1 V supply.

Fig. 2.16(a) illustrates the distribution of V_{REF} at room temperature. The measured mean output voltage is 470.3 mV with a standard deviation of 15.1 mV. Fig. 2.16(b) shows the measured $T.C.$ distribution. Based on the temperature compensation technique, the V_{TH} reference circuit achieves a minimum $T.C.$ of 18.8 ppm/ $^{\circ}$ C and

(a)

(b)

Fig. 2.16 (a) Distribution of V_{REF} for 15 samples at room temperature. (b) Distribution of the $T.C.$ performance metric for 15 samples.

a maximum $T.C.$ of 34.9 ppm/°C. The average $T.C.$ is 28.7 ppm/°C with a standard deviation of 5.1 ppm/°C. This has validated that the V_{TH} reference circuit is insensitive to temperature and supply voltage.

Table 2-III depicts the performance comparison with the reported voltage reference

TABLE 2-III PERFORMANCE COMPARISON OF THE PROPOSED V_{TH} REFERENCE CIRCUIT WITH REPORTED VOLTAGE REFERENCES

Parameters	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[23]	[24]	[26]	[27]	This Work	
Year	2007	2007	2008	2009	2009	2011	2011	2012	2014	2014	2015	2015	
Process (μm)	0.35	0.35	0.090	0.032	0.35	0.13	0.18	0.065	0.065	0.18	0.18	0.065	
Temp. Range(°C)	-20-80	0-80	5-100	0-125	-20-80	-50-130	0-125	-20-80	-40-90	0-120	-40-125	-30-80	
V _{DD} (V)	0.95-3	0.9-4	0.55-1	0.9-1.4	1.4-3	0.7-1.8	0.45-1.8	0.5-2.5	0.75-1.2	0.15-1.8	0.45-1.8	1.1-1.4 0.75-1.2*	
V _{REF} (mV)	741	670	243	540	745	501	263.5	330.1	474	17.69	118.46	470.3	
Power (nW)	390	36	547000	12600	300	210	2.6	0.24	290	0.0261	14.6	2640	
Min. T.C. (ppm/°C)	38.8	N/A	N/A	N/A	7	23.8	N/A	N/A	24	N/A	N/A	18.8	
Max. T.C. (ppm/°C)	40.1	N/A	N/A	N/A	45	41.1	N/A	N/A	50.4	N/A	N/A	34.9	
Mean T.C. (ppm/°C)	39	10	160	962	15	29.3	165	89.1	40	1426.4	63.6	28.7	
Chip Area (mm ²)	0.0759	0.045	0.07	0.016	0.055	0.023	0.043	0.0009	0.0198	0.0012	0.012	0.0769	
Samples	3	20	16	N/A	17	12	40	17	15	60	55	15	
High-order Compensation(Y/N)	N	N	N	N	N	N	N	N	Y	N	N	Y	
No. of Trimming Bits	4+4	0	0	0	0	0	0	0	4	0	5	4+3	
Pre-reg. based (Y/N)	N	N	N	N	N	N	N	N	N	N	N	Y	
Line Sens. (ppm/V)	32524	2700	123457	N/A	20	337	4400	3300	2423	20300	1200	70.8	
PSR (dB) @100 Hz	-23.4	-47	N/A	N/A	-45	N/A	-40	-40	-40	-64(sim.)	-44.2	-54.5	-31.5*
PSR (dB) @10 MHz	@1kHz	-40	N/A	N/A	N/A	N/A	-12	N/A	N/A	-124(sim.)	N/A	-43.5	-29*

* Measurement results without pre-regulator.

circuits implemented in both standard and advanced CMOS technologies. Although the reported works from CMOS 90nm [17], CMOS 32nm [18] and CMOS 65nm [23] are useful for low voltage operation, their *T.C.* performance will be relatively poor with respect to that of other works using larger channel-length process. This is mainly due to the fact that their intrinsic transistor's process parameters display relatively poor immunity against the process and temperature variations. On the contrary, the proposed V_{TH} reference circuit, which is implemented in the aggressively scaled 65nm CMOS technology, it can achieve comparable *T.C.* with respect to that of [15], [19], and [20] or even better *T.C.* than that of [21], [26], and [27].

Besides, this work achieves the best performance in terms of high-frequency PSR and line sensitivity in comparison to other works except for [19] in which the higher line sensitivity may rely on high supply architecture. Nevertheless, the tradeoff in this work is that it requires relative larger area occupation and slightly higher minimum supply voltage due to the added pre-regulator loop and the additional compensation circuit for LTS. This may not be the major issues in the high-performance multiple-supply integrated systems whilst the silicon overhead is exchanged with improved performance.

In order to realize the dual-segment temperature compensation technique, several functional circuit blocks are employed in this V_{TH} reference circuit. Despite it consumes relatively high power consumption except for [9]-[10], these disadvantages are counteracted by the fact that [26] and [27] cannot provide the process information. It is because their outputs only reflect the scaled V_{TH} difference and V_{GS} difference, respectively. The same goes for the cases of [17], [18], and [23]. They face the same difficulty to track the process information. On the contrary, this V_{TH} reference circuit generates V_{TH} of a single NMOS at absolute zero temperature (V_{TH0}). Not only does it

serve as the voltage reference having both temperature and supply independent characteristics, it can be used in a PVT compensation system [9] which requires the process-tracking voltage reference circuit.

Of particular interest, when compared to the recent published counterpart [24] using as V_{TH} reference circuit under identical channel-length technology (65 nm), this work offers better performance in terms of $T.C.$, dc to high-frequency PSR and line sensitivity owing to the new temperature compensation method in conjunction with the improved circuit architecture. These have demonstrated its key technical merits for use in performance-aware nanometer applications using aggressively scaled nanometer CMOS technology.

2.4 Summary

Several techniques for achieving good temperature stability in V_{TH} reference circuits have been reviewed. Besides, a performance-aware MOSFET threshold reference circuit in 65-nm CMOS is proposed. By utilizing both NPTAT and NCTAT segment compensation, a temperature compensated V_{TH} reference circuit with lower $T.C.$ over the operating temperature range is achieved. With the embedded pre-regulator, it is able to achieve a good PSR performance even at high frequency, which makes it less sensitive to the variations of supply voltages. The design performance is validated in a UMC 65-nm CMOS process. Furthermore, the proposed V_{TH} reference circuit obtains better $T.C.$ than those reported counterparts with nanometer technology whilst comparable to those using long-channel CMOS process technologies. This V_{TH} reference circuit is useful for applications that require good temperature stability and good immunity against the fluctuation of supply voltage.

Chapter Three

CMOS Current Reference Circuits

A current reference (I_{REF}) circuit is of paramount importance to the analog, digital, and mixed-signal circuit systems as a fundamental bias source. This Chapter reviews different techniques to implement a constant current reference which is insensitive to temperature and process variations in recently-reported literatures. This is then followed by a novel constant current source proposed in 65nm CMOS Technology.

3.1 Introduction

Various current reference designs have been reported in the literature [10], [28]–[45]. These works are generally classified into three categories. They are the V_{TH} -based current reference [10], [29]–[35], the summing current reference using a proportional-to-absolute-temperature (PTAT) current and a complementary-to-absolute-temperature (CTAT) current [36]–[38] and the VI convertor using a compensation voltage across a resistor [13]–[14]. Among the three techniques, the V_{TH} -based current references are implemented using tracking self-biasing topology [29]–[32], [35] or separately-biasing topology [10], [33], [34]. The key advantage is that of the reduction of process dependence. This is mainly due to the process tracking property of a V_{TH} -based voltage driving transistor, which allows it to bias a similar type of counterpart that defines the current generation. Therefore, the process-tolerant V_{TH} -based design will be one of the focuses of this paper.

Oguey presented a self-biased topology [30] by means of biasing a triode-biased nMOS transistor through a saturation-biased transistor in a circuit feedback loop for

current generation. However, it has difficulty cancelling the temperature effect arising from the matching between the mobility temperature exponent and the mobility degradation factor [93], [99]. Besides, the V_{TH} mismatch issue between the tracking device pair will degrade the current accuracy. Due to the topology, the current reference suffers from poor line sensitivity (10%/V). All of these non-ideal effects cause the accuracy of the reference current to deviate significantly from the process variations ($\sim\pm 30\%$). Alternatively, a low-voltage, low-power MOSFET-only self-biased current source was reported in [31]. The temperature dependence could reach as high as 2500 ppm/ $^{\circ}\text{C}$ over the operating range of -20 to 70 $^{\circ}\text{C}$. To improve the temperature coefficient (T.C.), the prior work suggested second-order temperature compensation [32]. Since both the reference current and its T.C. are process-sensitive, unavoidable trimming is required to preserve the accuracy. Later, Bendali showed a reference circuit utilizing the zero T.C. point of the transistor to generate a constant output current [33]. This relies on the temperature compensation concept using mutual temperature compensation between the carrier mobility and the threshold voltage [93]. Following a similar technique, Ueno realized the current reference with an improved T.C. of 46 ppm/ $^{\circ}\text{C}$ [10]. Although low line sensitivity is achieved, it may not be adequate if the circuit is designed using nanometer technology. At this juncture, the output current, which is obtained from the saturation-based transistor to serve as a VI converter, is sensitive to the offset of the driving op-amp, thus increasing the process sensitivity. In another design [35], a current reference was generated by means of a constant overdrive voltage. However, the line sensitivity becomes a major concern because the supply voltage needs to be well controlled. Turning to the current summing design technique [36]–[38], the power consumption is generally high because of the circuit's complexity. Although the floating-gate transistor based current

reference [39] offers a precise current, it is expensive in the trimming method. The same is true for the low T.C. current reference [40] which depends upon a low T.C precision-trimmed voltage reference at the expense of drawing extra power. It is of particular note that these reported designs are implemented using 0.18 μm CMOS technology or above. As the technology is further scaled down to sub-100nm [100], the performance of current references will be degraded by the process-voltage-temperature (PVT) variations. This stems from the fact that the process variations arising from the lithography imperfections and uncontrollable factors such as random dopant fluctuations, the well-proximity effect (WPE) [48], and layout-dependent stress variation [50] impose challenges for robust circuit designs [51], [53]. In addition, the MOS transistors suffer from a high current leakage level [54]. The temperature fluctuation induced variation in the carrier mobility becomes significantly higher for MOSFET devices in the exemplary 65 nm CMOS technology than in 0.18 μm technology [52]. Finally, the short-channel effect (SCE) contributes another factor that limits the circuit performance in advanced nanometer technology [46]. In brief, the lower the channel-length in a technology, the more difficult it is to achieve a stable reference design because of the relatively poor output characteristic of long channel transistors compared to those with higher channel-lengths in technologies. As a consequence, the design in a 65nm process turns out to be more challenging than that in other processes ($> 65\text{nm}$) even when transistors with larger than the minimum size are used.

Therefore, these problems have increased the motivation for the design of a low-power constant current reference with reduced PVT variation in the context of aggressively scaled nanometer technology.

However, the details of the proposed current source will be presented in next

Chapter. In the following subsections, the popular techniques in the prior-art works are described. This is then followed by the proposed current source.

3.2 Review of CMOS Current Reference

This section reviews different techniques to achieve good temperature stability in the reported works.

3.2.1. Current Summing Based I_{REF} Circuit

The most common technique for generating a constant current reference which is insensitive to temperature variations is to summing a positive $T.C.$ current with a negative $T.C.$ one. The conventional circuit theory and simplified schematic [37] is shown in Fig. 3.1. Based on this current summing concept, Liu et al. has reported one resistor-free temperature compensated I_{REF} [38]. Fig. 3.2 depicts the circuit schematic consisting of the positive $T.C.$ current (I_{PTC}) generator and the negative $T.C.$ current (I_{NTC}) generator.

By combining this two current having opposite $T.C.$, an output current can be obtained as

$$I_{out}(T) = I_{PTC}(T) + I_{NTC}(T) \quad (35)$$

A temperature compensated I_{out} is thus achieved once the $T.C.$ of $I_{NTC}(T)$ is cancelled by that of $I_{PTC}(T)$.

Although it avoids the use of passive resistors and achieves a reasonable $T.C.$ performance, however, it will increase the demand of a high supply voltage in order to drive the bipolar transistors (Q_1 and Q_2). Besides, high power consumption will become a concern since several blocks are required for the current summation.

Fig. 3.1 Conventional (a) circuit theory and (b) simplified schematic for current reference.[37]

Fig. 3.2 Circuit schematic of Liu's current reference [38].

Moreover, the $T.C.$ will be sensitive to the process variations since the coefficients of $I_{PTC}(T)$ and $I_{NTC}(T)$ are process dependent.

3.2.2. Zero-Temperature-Coefficient (ZTC) Bias Points Based I_{REF} Circuit

Besides the current summation, another popular method that many researchers had explored is to operate the transistors at zero temperature coefficient (ZTC) bias point [10], [33]. It makes use of an output MOSFET transistor while relying on the mutual compensation of the MOSFET carrier mobility and threshold voltage temperature effect [93]. In general, the drain current of a NMOSFET output transistor in saturation region is given by [101]

$$I_{OUT} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (36)$$

where the carrier mobility is a function of temperature as

$$\mu_n(T) = \mu(T_0) (T_0 / T)^{\alpha_\mu} \quad (37)$$

in which, α_μ is the mobility temperature exponent and T_0 is the reference temperature; whereas V_{TH} can be expressed with respect to temperature as

$$V_{TH}(T) = V_{TH}(T_0) - \alpha_{VT}(T - T_0) \quad (38)$$

In (38), the α_{VT} is the magnitude of temperature coefficient of V_{TH} .

Following [93], substituting (37) and (38) to (36) and assuming α_μ is 2, there will be a bias voltage independent of temperature. Thus, it yields

$$V_{GS} = V_{ZTC} = V_{TH}(T_0) + \alpha_{VT}T_0 = V_{TH0} \quad (39)$$

and the temperature independent output current is obtained as

$$I_{ZTC} = I_{OUT} = \frac{1}{2} \mu_n(T_0) C_{ox} \frac{W}{L} (\alpha_{VT}T_0)^2 \quad (40)$$

Fig. 3.3 plots the simulation results of transconductance characteristics of an output NMOSFET at different temperatures. It reveals that when V_{GS} is around 0.6 V, the transistor will generate a temperature independent current of $I_d = 140\mu A$, exhibiting the ZTC operation region. Bendali et al. [33] presents a 1-V CMOS current reference on the basis of this ZTC bias technique. However, a complicated bias voltage generator is implemented, which relies on the bandgap reference (BGR) core with a transimpedance amplifier. The $T.C.$ achieved is also restricted by the deviation of the generated reference bias voltage from the exact ZTC bias voltage.

To address this issue, Ueno et al. [10] has reported a ZTC bias point based current reference using a scaled voltage reference as the ZTC bias voltage of the output transistor. It achieves a better $T.C.$ in comparison to [33]. However, the V_{REF} generator [19] is still complicated which may suffer from large process variation especially

Fig. 3.3 Simulation of ZTC point of the output transistor [33].

under nano-meter CMOS process. In addition, an op-amp is utilized to scale V_{REF} . Its output is then applied as the driving voltage of output transistor working in saturation. As a result, the output current will be very sensitive to the offset of the amplifier.

On the other hand, a triode region NMOSFET can likewise exhibit the characteristics of ZTC operation region between the gate driving voltage and drain current. Oguey et al. has presented a simple resistor-less CMOS current reference using a single nMOS transistor in the linear region [30]. Fig. 3.4 shows the schematic of Oguey's I_{REF} circuit. N4 is biased in linear region by the gate voltage of N3 which operates in saturation region. It is based on the mutual temperature compensation of mobility and thermal voltage. The current generated is proportional to the $\beta(V_T)^2$, where β is the gain factor showing the same temperature effect as mobility and V_T is the thermal voltage. The relationship between the output current and temperature is thus expressed as

$$i_1 = \varphi_0 \left(\frac{T}{T_0} \right)^{2-m} \quad (41)$$

Fig. 3.4 Schematic of Oguey's I_{REF} Circuit [30]

where ψ_0 is the temperature independent parameters defined in room temperature T_0 and m shows the mobility temperature exponent.

Based on (41), since the exponent $(2-m)$ is a small value, thus the temperature dependency of current can be reduced. When m is closer to 2, it yields better suppression on the current sensitivity. It may have the difficulty to have m exactly equal to 2 in practical process technology. Furthermore, in this design, N_3 is implemented with the different channel length from N_4 , as $L_{N_3}=(2/3)L_{N_4}$. This causes a V_{TH} mismatch issue, which makes the current still sensitive to the process variations (around $\pm 30\%$). It turns out to be even worse in the aggressively scaled technology due to reverse short-channel length effect [102], [103]. Moreover, this design suffers from poor line sensitivity because of the low PSR (10%/V).

3.2.3. On-Chip Resistors Based I_{REF}

Many researchers have made use of the temperature effect of on-chip resistors to realize a temperature independent current [32], [35], [40]. Fiori et al. has proposed a constant I_{REF} circuit with second-order temperature compensation which relies on the use of resistors [32]. Fig. 3.5 illustrates the core schematic of their I_{REF} circuit. Due to the nonlinear current mirror comprising M_3 , M_4 and R_2 , the second-order temperature compensation is realized in the generated current, leading to the low $T.C.$. However, the $T.C.$ is very prone to vary due to process variations, resulting in limited $T.C.$ in the context of process variations.

In addition, Lee et al. has reported an I_{REF} circuit on the basis of a super transistor V-to-I converter using a MOSFET, an op-amp and a passive resistor. The core schematic of their I_{REF} circuit is shown in Fig. 3.6. A compensation voltage is generated such that the $T.C.$ of resistor is cancelled, thus a low $T.C.$ can be achieved.

Fig. 3.5 Schematic of Fiori's I_{REF} Circuit [32]

Fig. 3.6 Schematic of Lee's I_{REF} Circuit [40]

The output current can be expressed as

$$I_{ref} = \frac{V_{comp}}{R} = \frac{V_{comp0}(1 + \alpha_{comp}\Delta T)}{R_0(1 + \alpha_R\Delta T)} \quad (42)$$

where α_{comp} and α_R is the *T.C.* of V_{comp} and resistor R , respectively. Assume that α_{comp} and α_R match each other, and then I_{REF} can be obtained as

$$I_{\text{ref}} \approx \frac{V_{\text{comp}0}}{R_0} \quad (43)$$

where $V_{\text{comp}0}$ and R_0 represent the voltage and resistance at the reference temperature T_0 . From (43), as long as the *T.C.* of R is cancelled by that of V_{comp} , a low *T.C.* I_{REF} can be achieved.

However, in this design, V_{Comp} is generated from the power supply which means that I_{REF} suffers from poor line sensitivity. In order to maintain stable operation against supply voltage, an additional very stable bandage reference (BGR) is required to provide the supply voltage, resulting in circuit complexity and thus higher power consumption and additional trimming on the voltage reference for meeting precision issue.

Another I_{REF} circuit based on the on-chip resistor is reported by Kayahan et al. and shown in Fig. 3.7 [35]. It depends on a constant overdrive voltage for M_3 such that the current I_{out} is insensitive to the process variations. For the temperature effect, a resistor R is used to compensate temperature effect of mobility. However, the *T.C.* of this design is limited by the *T.C.* of the resistor and it requires proper selection of the resistor. Moreover, the temperature range is still restricted and the poor PSR also presents an issue that needs to be addressed.

In brief, the above mentioned techniques have been confirmed to be useful for the constant I_{REF} design. However, none of the reported current reference designs is implemented in advanced nano-meter technology. In view of that, a low *T.C.* current reference with PVT insensitivity and wide temperature range in 65-nm CMOS technology is proposed. The stated issues in previous deigns are to be addressed. The

Fig. 3.7 Schematic of Kayahan's I_{REF} Circuit [35].

proposed current reference with its temperature compensation principle is discussed in the following section.

3.3 Proposed CMOS Constant Current Source with Reduced PVT Variation

This section presents a new nanometer-based low-power constant current reference that attains a small value in the total process-voltage-temperature (PVT) variation. The circuit architecture is based on the embodiment of a process-tolerant bias current circuit and a scaled process-tracking bias voltage source for the dedicated temperature-compensated voltage-to-current (VI) conversion in a pre-regulator loop. Fabricated in a UMC 65-nm CMOS process, this work offers a better sensitivity figure-of-merit (FOM) with respect to the reported representative counterparts.

3.3.1. Operation Principle of Proposed Constant Current Reference

The constant current generation is devised from a process-tolerant temperature-compensated VI converter. It aims at establishing a constant V_{TH0} reference compensation voltage having a first-order T.C. with reduced process sensitivity in series with another auxiliary compensation voltage having a second-order T.C. with low process sensitivity. The combined temperature characteristic will match the corresponding linear T.C. and non-linear T.C. of the integrated resistor in the VI converter. The outcome leads to a constant current reference with reduced PVT variation. The operation principle of this proposed circuit is illustrated in Fig. 3.8.

A process-tolerant bias current (I_{PTol}) and a process-tracking voltage (V_{PTrack}) are generated through the I_{PTol} and V_{PTrack} bias circuits in self-biasing topology. When a scaled I_{PTol} is injected into a MOSFET transistor, it will generate a gate-source voltage,

Fig. 3.8 Operation principle of the proposed I_{REF} circuit with the temperature characteristic of (a) $V_{GS}(T)$, (b) $V_{Aux_Comp}(T)$, (c) $V_{R_Comp}(T)$, (d) $R_O(T)$, and (e) I_{REF} .

$V_{GS}(T)$ with a first-order negative T.C. as shown in Fig. 3.8(a). Fig. 3.8(c) depicts the target reference compensation voltage $V_{R_Comp}(T)$ that is formed by summing the nonlinear auxiliary compensation voltage $V_{Aux_Comp}(T)$ in Fig. 3.8(b) with the gate-source voltage $V_{GS}(T)$. On the other hand, $V_{Aux_Comp}(T)$ is synthesized from the IV conversion in which the scaled I_{PTol} is passed to an active resistor. The resistor realization is based on a scaled V_{PTrack} to bias the gate of the triode transistor. Since $V_{R_Comp}(T)$ exhibits a similar T.C. to the sense resistor $R_O(T)$ with the temperature characteristic shown in Fig. 3.8(d), the final output current I_{REF} can be made temperature independent over the operating temperature range as illustrated in Fig. 3.8(e).

3.3.2. Implementation of Proposed Current Reference

The current reference depicted in Fig. 3.9 consists of a pre-regulator, a process-tolerant current bias circuit with an embedded process-tracking voltage bias circuit, and a temperature-compensated VI converter. For simplicity, the capacitive start-up circuit [95] and the biasing circuit are not shown. The pre-regulator loop, which has been reported in a nanometer-based MOSFET V_{TH} reference circuit [104], is used to provide good line sensitivity. Referring to Fig. 3.9, when the op-amp is employed in the bias current circuit, the drain voltages at nodes N_1 and N_2 are close to each other. This establishes identical currents flowing through M_1 and M_2 , which are biased in the sub-threshold region. On the other hand, M_{R1} operates in the triode region as an active resistor. It is self-biased by V_{PTrack} which is generated from M_8 in the saturation region. This turns out to be a process-tolerant active resistor R_{MR1} . As such, the current I_{PTol} flowing through M_1 or M_2 becomes process-tolerant.

Referring to Fig. 3.8, with the scaled I_{PTol} , the $V_{R_Comp}(T)$ is established by summing

Fig. 3.9 Schematic of the proposed constant current reference circuit.

$V_{GS}(T)$ and $V_{Aux_Comp}(T)$. $V_{GS}(T)$ comes from M_{01} operating in the saturation region, whereas $V_{Aux_Comp}(T)$ comes from $V_{DS}(T)$ of M_{R2} operating in the triode region. Similarly to M_{R1} , M_{R2} is biased by another scaled process-tracking voltage ($V_{1_PTTrack}$) such that the required process-tolerant resistance is created. Moreover, an appropriate on-chip high-resistance poly resistor R_O having low process variation and negative T.C. is chosen as the sense resistor in the temperature-compensated VI converter.

Consequently, the transistor aspect ratios can be made to permit the T.C. of $V_{R_Comp}(T)$ to be close to that of $R_O(T)$. This will yield a constant reference current with a low process-tolerant T.C. over a wide operating temperature range.

Referring to the operation principle, which is graphically illustrated from design step (a) to design step (e) in Fig. 3.8, the temperature compensation analysis is presented as follows:

(I). Thermal Effect of Output Sense Resistor and Bias Generation for VI Converter

The temperature effect of the output sense resistor $R_O(T)$ and the dedicated circuit bias I_{PTol} and $V_{PTTrack}$ for the proposed VI converter are described as follows:

1). Temperature Characteristic of Output Sense Resistor

As shown in Fig. 3.9, a high-resistance poly resistor R_O having negative T.C. serves as the sense resistor in the VI converter. Unlike those designs [39], [40] that deal with the first-order temperature effect from the on-chip resistors, the proposed circuit takes into account the second-order temperature effect. The temperature characteristic of the resistor, depicted in Fig. 3.8(d), is given as

$$R_O(T) = R_O(T_r) \left[1 + a_1(T - T_r) + a_2(T - T_r)^2 \right] \quad (44)$$

where a_1 and a_2 represent the first- and second-order T.C.s of the sense resistor at T_r , respectively. From (44), the T.C. of $R_O(T)$ is obtained as $TC_{RO}(T) = [1/R_O(T_r)] \times [\delta R_O(T) / \delta T] = a_1 + 2a_2(T - T_r)$, which is a temperature function having the slope $[\delta TC_{RO}(T) / \delta T]$ denoted as $2a_2$. Of particular note, the T.C. values for a_1 and a_2 are usually independent of process variations despite the variations of the resistor values [105].

The temperature dependence of the sense resistor is characterized in the UMC 65nm CMOS process. Fig. 3.10(a) and (b) depict the simulated $R_O(T)$ and its first-order T.C. against temperature under typical process, respectively. It can be seen from Fig. 3.10(a) that $R_O(T)$ of 69.11 k Ω at room temperature (25 °C) is implemented and it exhibits a negative first-order T.C.. Besides, the increasing T.C. with respect to temperature implies a contribution from a positive second-order T.C.. Monte-Carlo (MC) simulations pertaining to the T.C. characteristics are conducted on the basis of a sample size of 500 with 3 σ coverage. The MC simulation results of the magnitude of the first-order T.C. ($|a_1|$) and the slope of the first-order T.C., ($2a_2$), at nominal room temperature (T_r) are shown in Fig. 3.11(a) and (b), respectively. The mean value of a_1 is -374.91 ppm/°C, whereas that of a_2 is about 0.825 ppm/°C². The obtained process sensitivity (σ/μ) for $|a_1|$ and $2a_2$ are 0.6% and 4.6%, respectively. From the statistical results, $|a_1|$ is regarded as a fairly constant T.C. due to its process sensitivity of 0.6% and a_2 remains a fairly constant T.C. in view of the finite value of 0.825 ppm/°C² from the mean T.C. result. This validates that both the first- and second-order T.C.s of $R_O(T)$ are insensitive to process variations. Finally, the sense resistor process variation can be quantified by running the MC simulation since it will affect the variation of output current. In this process, the one sigma resistor variation is about 4.5%, as shown in Fig. 3.11(c).

(a)

(b)

Fig. 3.10 (a) Simulated $R_O(T)$ with respect to temperature. (b) Simulated first-order T.C. of $R_O(T)$ with respect to temperature.

(a)

(b)

(c)

Fig. 3.11 (a) Monte-Carlo simulation results of the first-order T.C. magnitude ($|a_1|$) of $R_O(T)$ at room temperature. (b) Monte-Carlo simulation results of the slope of first-order T.C. ($2a_2$) of $R_O(T)$ at room temperature. (c) Monte-Carlo simulation results of the magnitude of R_O at room temperature.

2). Bias Generation for VI Converter

In order to generate I_{PTol} and V_{PTrack} described Fig. 3.8, the process-tolerant bias current circuit and the process-tracking voltage bias circuit are designed using the self-biasing technique as shown in Fig. 3.9. To reduce the variation due to SCE, M_1 and M_2 are implemented using the long channel length (10 μm in this design). A detailed analysis of V_{PTrack} and I_{PTol} is given as follows:

(i). Process-tracking Bias Voltage Generation

In the proposed current reference topology, V_{PTrack} is generated by M_8 . Besides, an additional source follower stage (M_7 , R_1 and R_2) is employed to scale V_{PTrack} to V_{1_PTrack} so that the optimal bias for controlling the second-order temperature coefficient can be obtained to drive the triode transistor M_{R2} . The temperature dependency of $V_{PTrack}(T)$ is analyzed as follows.

Referring to Fig. 3.9, M_1 and M_2 work in the subthreshold region. From [92], the subthreshold drain current (I_D) in each M_1 and M_2 can generally be expressed as

$$I_D \approx K \mu C_{OX} (\eta - 1) V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) = K I_S \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (45)$$

assuming that the drain-source voltage, $V_{DS} > 75 \text{ mV}$, where I_S refers to the characteristic current and is defined as $I_S = \mu C_{OX} (\eta - 1) (V_T)^2$, in which μ is the carrier mobility and C_{OX} is the gate-oxide capacitance. V_{GS} is the gate-source voltage and V_{TH} is the threshold voltage of the transistor. $K (= W/L)$ is the aspect ratio of the transistor, $V_T (= k_B T/q$, where k_B is the Boltzmann constant, q is the elementary charge, and T represents the temperature in Kelvin) is the thermal voltage, and η is the subthreshold slope factor. Considering the temperature characteristics of V_{TH} and μ , they are given by

$$V_{TH}(T) = V_{TH0} - \kappa T \quad (46)$$

$$\mu(T) = \mu(T_r)(T_r/T)^m \quad (47)$$

where V_{TH0} is the threshold voltage at 0 K, κ is the slope magnitude of the threshold voltage with respect to temperature [106], $\mu(T_r)$ is the carrier mobility at nominal room temperature T_r , and m is the temperature exponent of the mobility (1.5~2) [93], [107]. Since M_1 and M_2 are the same type of transistor, it is assumed that $V_{TH1} = V_{TH2}$ for a negligible body effect and $I_{S1} = I_{S2}$. With $I_{D1} = I_{D2}$, the difference in V_{GS} between M_1 and M_2 is derived as

$$V_{MR1} = \Delta V_{GS} = V_{GS1} - V_{GS2} = \eta(k_B T/q) \ln(N) \quad (48)$$

where $N = K_2/K_1$. This suggests that the drive voltage (V_{MR1}) of M_{R1} displays a PTAT characteristic.

Since M_{R1} works in the linear region and serves as an active resistor, the drain current I_D can be obtained from (48) as

$$I_D \approx V_{MR1}/R_{MR1} = \beta_{MR1}(V_{PTrack} - V_{TH_MR1})\eta(k_B T/q) \ln(N) \quad (49)$$

where R_{MR1} is the equivalent resistance of M_{R1} and β_{MR1} is the current gain factor which is proportional to $[\mu C_{OX}(W/L)_{MR1}]$ [92]. As for the long channel saturation-based transistor M_8 , the bias voltage can be expressed as

$$V_{PTrack} = V_{GS8} \approx \sqrt{MI_D/\beta_{M8}} + V_{TH_M8} \quad (50)$$

where M is the current mirror ratio, $M = K_{11}/K_6$, for M_{11} and M_6 , [92]. Rearranging (50) gives

$$(V_{PTrack} - V_{TH_M8})^2 \approx M \frac{I_D}{\beta_{M8}} \quad (51)$$

Since M_8 and M_{R1} are implemented using the same type of device with identical channel length, it can be assumed that $V_{TH_M8} \approx V_{TH_MR1}$. When substituting (46) and (49) into (51), V_{PTrack} can be approximated as

$$V_{PTrack} \approx V_{TH0_M8} + 2M\eta \frac{K_{MR1}}{K_8} \frac{k_B T}{q} \ln(N) - \kappa T \approx V_{TH0_M8} \quad (52)$$

where V_{TH0_M8} is defined as the threshold reference voltage of M_8 at 0 K, and assuming $\beta_{MR1}/\beta_8 \approx 2K_{MR1}/K_8$.

From (52), by setting the aspect ratios for M , K_{MR1}/K_8 , and N , the V_{PTrack} can be optimized to yield a zero T.C. whilst maintaining an average voltage approximated as V_{TH0} of M_8 . This confirms that the generated voltage bias is a thermally stable voltage with the capability to track the process variations.

(ii). Process-tolerant Bias Current Generation

Referring to (49) and (52), the generated bias current I_D in Fig. 3.9 can be expressed as

$$I_{PTol} = I_D \approx \beta_{MR1} \eta (\kappa T) (k_B T / q) \ln(N) \quad (53)$$

assuming that the V_{TH0} of M_8 is identical to that of M_{R1} . Obviously, this reveals that the bias current is insensitive to any V_{TH} variations. Thus, it is denoted as the process-tolerant bias current. With the application of this bias current, the compensation voltage will be generated, as discussed in Section B.

(II). Reference Compensation Voltage

Combining the design steps (a) and (b) yields the design step (c), as depicted in Fig. 3.8. Referring to Fig. 3.9 for detailed illustration, the synthesis of $V_{R_Comp}(T)$ is described as follows:

1). Gate-Source Voltage Generation

The gate-source voltage is provided by M_{01} in the core circuit shown in Fig. 3.9. Since it is biased in the saturation region with a scaled bias current $I_{2_PTol} = P \times I_{PTol}$ and neglecting the body effect, the gate-source voltage becomes

$$V_{GS01} = \sqrt{PI_{PTol}/\beta_{M01}} + V_{TH_M01} \quad (54)$$

where $P = K_{12}/K_6$. Using (46) and (53), the temperature dependence of $V_{GS01}(T)$, as shown in Fig. 3.8(a), is described as

$$V_{GS01}(T) = V_{TH0_M01} + (\varphi - \kappa)T \quad (55)$$

where $\varphi = \sqrt{2P(K_{MR1}/K_{01})(k_B/q)\eta\kappa\ln(N)}$.

According to (55), the first-order T.C. of the gate-source voltage can be controlled by the aspect ratios (P , K_{MR1}/K_{01} , and N) in φ . The coefficient $(\varphi - \kappa)$ will cancel the first-order T.C. from the output sense resistor in accordance with a_1 in (44).

2). Auxiliary Compensation Voltage Generation

The design step (b) in Fig. 3.8 is realized by the auxiliary compensation voltage generator in Fig. 3.9. This is simply obtained through the V_{DS} of M_{R2} , which operates in the triode region under the bias voltage of $V_{1_PTrack} = S_1 \times V_{PTrack}$ in which S_1 is the scaling ratio defined by $S_1 = R_2/(R_1 + R_2)$. Assuming that $V_{TH0_M8} = V_{TH0_MR1} = V_{TH0_MR2}$, the temperature dependence of $V_{Aux_Comp}(T)$ can be obtained as

$$V_{Aux_Comp}(T) = I_{2_PTol}R_{MR2} \approx \psi T^2/(T - A) \quad (56)$$

where $A = V_{PTrack}(1 - S_1)/\kappa$, and $\psi = P(K_{MR1}/K_{MR2})(k_B/q)\eta\ln(N)$. Obviously, the coefficient ψ is a temperature independent constant. It is also independent of process variations since the mobility variations can be cancelled by the ratio of the gain factors based on

the relationship $\beta_{MR1}/\beta_{MR2}=K_{MR1}/K_{MR2}$. Using the Taylor series expansion at T_r , the $V_{Aux_Comp}(T)$ in (56) can be simplified to

$$V_{Aux_Comp}(T) \approx b_0 + b_1(T - T_r) + b_2(T - T_r)^2 \quad (57)$$

in which the third-order term is small and can be ignored. The coefficients b_0 , b_1 , and b_2 are constants, where

$$b_0 = \frac{\psi T_r^2}{T_r - A}, b_1 = \frac{\psi T_r (T_r - 2A)}{(T_r - A)^2} \text{ and } b_2 \approx \frac{\psi A^2}{(T_r - A)^3}$$

From (56) and (57), the second-order nonlinear temperature effect is introduced with the inclusion of the scaling factor S_1 for the bias voltage of M_{R2} . Controlling S_1 and hence the coefficient b_2 in (57) permits the second-order T.C. of $V_{Aux_Comp}(T)$ to compensate that of the output sense resistor in accordance with a_2 in (44).

In this work, the second-order T.C. of $R_O(T)$ shown in Fig. 3.11(b) is positive at room temperature (25°C). Therefore, this suggests that a positive b_2 ($b_2 > 0$) is desired for the second-order temperature compensation in the VI conversion. It is necessary that $0 < A < T_r$ from (57). This yields the practical design guideline for S_1 to fulfill the design condition that $[V_{TH_M8}(T_r)/V_{PTTrack}] < S_1 < 1$. After extracting the design parameters from the simulation setup, it can be found that $0.7 < S_1 < 1$. Thus, the value of S_1 is designed to be around 0.8 to achieve the biasing condition. This results in a negative b_1 with $2A > T_r$. However, it is not of concern since it can be combined with the first-order temperature term in $V_{GS01}(T)$. This will be illustrated in the next subsection.

The simulated $V_{Aux_Comp}(T)$ and its first-order derivative against temperature under typical process and design parameters is illustrated in Fig. 3.12(a) and (b), respectively. From Fig. 3.12 (a), it exhibits a negative first-order T.C. characteristic, which

(a)

(b)

Fig. 3.12 (a) Simulated $V_{\text{Aux_Comp}}(T)$ with respect to temperature. (b) Simulated slope of $V_{\text{Aux_Comp}}(T)$ with respect to temperature.

is consistent with a negative b_1 in (57). More importantly, Fig. 3.12(b) reveals that $V_{\text{Aux_Comp}}(T)$ can offer a positive second-order T.C. (i.e. $b_2 > 0$), thus allowing to cancel the nonlinear temperature effect in the output sense resistor. The simulation results have confirmed the correlation with the theory.

3). Reference Compensation Voltage Generation

Based on $V_{\text{GS01}}(T)$ and $V_{\text{Aux_Comp}}(T)$, the $V_{\text{R_Comp}}(T)$ can be represented as

$$\begin{aligned}
V_{R_Comp}(T) &= V_{GS01}(T) + V_{Aux_Comp}(T) \\
&\approx V_{TH0_M01} + (\varphi - \kappa + b_1)(T - T_r) + b_2(T - T_r)^2
\end{aligned} \tag{58}$$

assuming V_{TH0_M01} is the dominant voltage magnitude. In (58), φ and κ are defined in (55) and (46), respectively, while b_1 and b_2 are given by the coefficients in (57). From (58), $V_{R_Comp}(T)$ can be rewritten in the final form of

$$V_{R_Comp}(T) = V_{R_Comp}(T_r) \left[1 + m_1(T - T_r) + m_2(T - T_r)^2 \right] \tag{59}$$

where m_1 and m_2 are constants. This indicates that the circuit can generate a compensation voltage having $V_{R_Comp}(T_r)$ as the magnitude at T_r , m_1 as the first-order T.C. and m_2 as the second-order T.C.. It can be found from (58) that by setting the aspect ratios in b_2 and φ , the compensation voltage can be made to have a T.C. identical to that of the output sense resistor.

Using the typical process and design parameters for the proposed current reference, the simulated $V_{R_Comp}(T)$ and its first-order T.C. with respect to temperature are demonstrated in Fig. 3.13(a) and (b), respectively. The dominant DC average value of $V_{R_Comp}(T)$ is V_{TH0} , which is around 687.4 mV for a regular threshold NMOS device in this 65nm CMOS process at room temperature. In addition, $V_{R_Comp}(T)$ has displayed almost the same thermal behaviour of the first-order T.C. as that of the sense resistor $R_O(T)$ given in Fig. 3.10(b). Furthermore, the MC simulation results on the basis of a sample size of 500 with 3σ coverage of the first-order T.C. magnitude ($|m_1|$) and the slope of the first-order T.C. ($2m_2$) at T_r are shown in Fig. 3.14(a) and (b), respectively. The variations for $|m_1|$ and $2m_2$ are 3.5% and 9.8%, respectively. The mean value of m_1 is -372.82 ppm/ $^{\circ}\text{C}$ while that of m_2 is 0.805 ppm/ $^{\circ}\text{C}^2$. Table 3-I summarizes the simulated T.C. of $R_O(T)$ and $V_{R_Comp}(T)$. It is evident that these results suggest a good match between the temperature effect of $V_{R_Comp}(T)$ and that of the sense resistor.

(a)

(b)

Fig. 3.13 (a) Simulated $V_{R_Comp}(T)$ with respect to temperature. (b) Simulated first-order T.C. of $V_{R_Comp}(T)$ with respect to temperature.

Therefore, the proposed circuit will offer improved temperature compensation for the output reference current in comparison to the counterparts employing only first-order T.C. compensation.

To verify the design theory with numerical values, the design parameters calculated from the design equations are compared with the key design parameters extracted from

(a)

(b)

Fig. 3.14 (a) Monte-Carlo simulation results of the first-order T.C. magnitude ($|m_1|$) of $V_{R_Comp}(T)$ at room temperature. (b) Monte-Carlo simulation results of the slope of first-order T.C. ($2m_2$) of $V_{R_Comp}(T)$ at room temperature.

the simulation setup. Table 3-II shows the design parameters and verification of the important T.C. using the simulation results and the calculated theoretical results with extracted process parameters. It can be seen that they are consistent with each other. The deviations are due to the non-ideal effects arising from the sophisticated models in advanced CMOS process.

TABLE 3-I SIMULATED T.C. OF THE OUTPUT SENSE RESISTOR AND REFERENCE COMPENSATION VOLTAGE

Parameter	$R_O(T)$		$V_{R_Comp}(T)$	
T.C.	a_1 (ppm/ $^{\circ}$ C)	a_2 (ppm/ $^{\circ}$ C ²)	m_1 (ppm/ $^{\circ}$ C)	m_2 (ppm/ $^{\circ}$ C ²)
Mean Value (μ)	-374.91	0.825	-372.82	0.805
Proc. Sens. (σ/μ) (%)	0.6	4.6	3.5	9.8

TABLE 3-II DESIGN PARAMETERS AND VERIFICATION OF IMPORTANT T.C. USING THEORETICAL RESULTS AND SIMULATION RESULTS.

Parameters	Design Parameters		
	Equation	Theory	Simulation
N	K_2/K_1	24	24
M	K_{11}/K_6	2	2
P	K_{12}/K_6	1	1
$\beta_{MR1}/\beta_8[2(K_{MR1}/K_8)]$	(8)	2*0.35	2*0.75
$\beta_{MR1}/\beta_{01}[2(K_{MR1}/K_{01})]$	(11)&(14)	2*0.7	2*0.816
$\beta_{MR1}/\beta_{MR2}(K_{MR1}/K_{MR2})$	(13)&(12)	0.1	0.136
$S_1[R_2/(R_1+R_2)]$	(13)&(12)	0.7~1	0.78
Verification			
	Equation	Theory	Simulation
T.C. of V_{PTrack} (ppm/ $^{\circ}$ C)	(8)	0	15
m_1 (ppm/ $^{\circ}$ C)	(15)	-374.91	-372.82
m_2 (ppm/ $^{\circ}$ C ²)	(15)	0.825	0.805

It is of particular note that in the technology with a positive TC resistor, the polarity of T.C. in the compensation voltage can be changed and adjusted accordingly by changing the corresponding transistor (M_{01}) aspect ratios and the current mirror ratio (P) in the parameter φ of (55) and the resistor ratio (S_1) in the coefficient b_2 of (57).

(III). Output Reference Current

By combining $V_{R_Comp}(T)$ and $R_O(T)$, the output reference current can be obtained as

$$I_{REF} = \frac{V_{R_Comp}(T)}{R_O(T)} \approx \frac{V_{R_Comp}(T_r) \left[1 + m_1(T - T_r) + m_2(T - T_r)^2 \right]}{R_O(T_r) \left[1 + a_1(T - T_r) + a_2(T - T_r)^2 \right]} \quad (60)$$

Based on (60), the T.C. of I_{REF} can be expressed by

$$TC_{I_{REF}} = \frac{1}{I_{REF}(T_r)} \frac{dI_{REF}(T)}{dT} = TC_{V_{R_Comp}} - TC_{R_o} \quad (61)$$

This reveals that as long as the T.C. of $V_{R_Comp}(T)$ is designed to match that of $R_O(T)$ (i.e. $TC_{I_{REF}} \approx 0$), a temperature insensitive I_{REF} can then be produced. According to (60), it is concluded that when m_2 is equalized to a_2 and m_1 to a_1 , optimal temperature compensation including the first- and second-order T terms will be realized.

The final output current I_{REF} over the whole temperature range can be approximated as $I_{REF} \approx V_{R_Comp}(T_r)/R_O(T_r)$ from (60). This shows that the output current has good temperature stability using the proposed temperature compensation method. Fig. 3.15 shows the simulated I_{REF} as a function of temperature. The thermal drift over the

Fig. 3.15 Simulated I_{REF} with respect to temperature.

temperature range is quite small and within 5 nA, demonstrating that the proposed temperature compensation method permits a low T.C. performance metric.

It is of particular interest that the direct generation of I_{REF} , by mirroring bias current I_{PTol} in the self-biasing topology, is easily subject to process variations due to the offset induced by the device mismatch [3]. On the contrary, the I_{PTol} in this work is firstly converted to the target compensation voltage through the saturation-based transistor M_{01} . The variation of the compensation voltage can be reduced because of the effect of the square root on I_{PTol} in the IV conversion, as revealed in (54) of Section 3.3.2. At the same time, the voltage error introduced by $V_{\text{DS_MR2}}$ through the error of I_{2_PTol} is considered small because the magnitude of $V_{\text{DS_MR2}}$ occupies only a few percent of the dominant $V_{\text{GS01}}(T)$ term. Furthermore, the removal of the op-amp in this VI converter gives another level of reduced process sensitivity. To this end, a thermally stable reference current I_{REF} with reasonably good accuracy is produced by the temperature-compensated VI converter.

(IV). Line Sensitivity

To obtain good stability against the variations of the supply voltage, a pre-regulator loop [95] (enclosed by the left dashed box in Fig. 3.9) is embedded in this current reference. M_{PR1} and M_{PR2} , in conjunction with the current source I_{BR} , form the inverting gain stage for the establishment of the feedback loop in the pre-regulator. M_{PR3} and M_{PR4} form the source follower. They are implemented using native transistors with almost zero threshold voltage to improve the operation headroom under a supply of a minimum of 1.4 V. C_1 and C_2 are compensation capacitors that are realized using native transistors to save chip area. With the aid of the feedback control loop, $V_{\text{R_Comp}}$ can significantly be shielded from the supply noise. The same is true for I_{REF} , leading to good line sensitivity performance in nanometer technology.

3.3.3. Results and Discussions

The proposed current reference is designed and fabricated in the UMC 65-nm CMOS process. The chip micrograph of the proposed circuit, with an active area of 0.089 mm^2 , is shown in Fig. 3.16.

(I). Sensitivity of IREF and Its T.C. to Process Variations

The variations arising from the process mainly consist of within-die (WID) variation and die-to-die (D2D) variation [97]. The WID variation will cause mismatches in the transistors and the resistors under the same die, influencing the output characteristics. They can be reduced by careful layout techniques [98]. In this work, long-channel large-sized transistors and the same resistor unit are used to minimize the channel-length modulation effect and mismatch as one of the design strategies. On the other hand, the D2D variations may cause the deviation of I_{REF} and its T.C. because of the variation of threshold voltage, resistors, and resistor ratios used for the temperature

Fig. 3.16 Microphotograph of the proposed current reference

compensation. However, owing to the proposed process-tolerant compensation method, together with the usage of the sense resistor type with low variation, the effect of D2D variations tends to be considerably weak.

In order to evaluate the process sensitivity of the T.C., Fig. 3.17(a) and (b) present the MC simulation results of the corresponding T.C. for the WID variation and D2D variation. It has been validated that the T.C. of the I_{REF} circuit exhibits a small sensitivity in view of both the WID and D2D variations due to the small sensitivity of the T.C. in the sense resistor and the compensation voltage.

Considering the output current, MC simulation is also conducted and the results of I_{REF} with respect to the WID variation and D2D variation are illustrated in Fig. 3.18(a) and (b), respectively. It can be seen that the output current is less sensitive to the WID variation. One important reason is that the proposed circuit does not require an op-amp in the VI converter design. This is in contrast with the designs from [10] and [40], which suffer from the offset issues induced by the op-amp. In view of D2D variation, the obtained process sensitivity is 5% because it comes from the combined accuracy of the compensation voltage and the sense resistor. Nevertheless, it is still considerably small and is acceptable for many applications.

Fig. 3.17 (a) Monte-Carlo simulation results of T.C. with WID variation. (b) Monte-Carlo simulation results of T.C. with D2D variation.

(a)

(b)

Fig. 3.18 (a) Monte-Carlo simulation results of I_{REF} with WID variation.

(b) Monte-Carlo simulation results of I_{REF} with D2D variation.

Table 3-III summarizes the simulated T.C. performance at different process corners and the simulated output current at room temperature for the corresponding corners. It has been confirmed that the circuit yields a low T.C. in the context of D2D process variation even without calibration, leading to stable operation with low sensitivity to the process corners and temperature. It is of particular note that the performance of this

TABLE 3-III SIMULATED TEMPERATURE DEPENDENCE PERFORMANCE AND I_{REF} AT DIFFERENT PROCESS CORNERS

Parameter	TT	SS	SF	FS	FF
I_{REF} @ 25 °C (μA)	9.947	9.08	10.23	9.66	11.08
T.C.(ppm/°C)	4.18	6.13	4.78	5.60	21.77
Temp. Range (°C)	-30-90	-30-90	-30-90	-30-90	-30-90
V_{DD} (V)	1.4	1.4	1.4	1.4	1.4
Power (μW)	8.2	7.58	8.11	8.36	8.99

* TT = Typical; SS = Slow NMOS/Slow PMOS; SF = Slow NMOS/Fast PMOS; FS = Fast NMOS/Slow PMOS; FF = Fast NMOS/Fast PMOS.

work can be improved through calibration. The output resistor can be trimmed to calibrate the output current deviations arising from the process variation. Alternatively, the T.C. of I_{REF} can also be trimmed through the forward body bias voltage of transistor M_{01} .

(II). Measurement Results

The temperature dependence of the I_{REF} circuit is measured in a temperature range from -30 to 90 °C at a supply voltage of 1.4V. All the measurement results are obtained without calibration. The power consumption measured at room temperature is 7.18 μW. In this work, 12 samples were measured. Fig. 3.19(a) depicts the measured output current I_{REF} as a function of temperature. It has confirmed that I_{REF} is very stable under temperature variation for each sample. Fig. 3.19(b) shows the measured I_{REF} as a function of temperature at various supply voltages. The current reference circuit can work well at different voltage supplies. Fig. 3.20(a) shows the measured output current I_{REF} at room temperature as a function of power supply. It reveals that the constant I_{REF} circuit operates well when the supply is higher than 1.3 V. The circuit achieves a line sensitivity of 180 ppm/V in a supply range of 1.3 to 2.5 V. Fig. 3.20(b) shows the measured output current I_{REF} at room temperature as a function of output voltage. It exhibits a good load sensitivity of 755 ppm/V. Fig. 3.21(a) illustrates the distribution of measured I_{REF} at room temperature. The measured mean output

(a)

(b)

Fig. 3.19 (a) Measured output current I_{REF} as a function of temperature for 12 samples at 1.4 V supply voltage. (b) Measured output current I_{REF} as a function of temperature for different supply voltages.

(a)

(b)

Fig. 3.20 (a) Measured I_{REF} at room temperature as a function of V_{DD} . (b) Measured I_{REF} at room temperature as a function of V_{OUT} .

current is 9.422 μA with a standard deviation of 0.066 μA . Fig. 3.21(b) shows the measured T.C. distribution. Based on the temperature compensation technique, the constant I_{REF} circuit achieves a minimum T.C. of 85.8 ppm/ $^{\circ}C$ and a maximum T.C. of 149.8 ppm/ $^{\circ}C$. The average T.C. is 119 ppm/ $^{\circ}C$ with a standard deviation of 20.1 ppm/ $^{\circ}C$. It is noted that there is a drift of the measured T.C. in comparison to the

Fig. 3.21 (a) Distribution of I_{REF} for 12 samples at room temperature. (b) Distribution of the T.C. performance for 12 samples.

simulated result. The main cause of this is the additional offset effect introduced to the matching device pairs. This arises from the internal mechanical stress induced by the shallow trench isolation (STI) in the MOSFET devices. It has been reported that the stress induced in a packaged die can result in device parameter shifts of 5-10%, leading

to variation of the drain current [108], [109]. This effect is not predictable and thus results in the discrepancy between the measurement results and the simulation results. Nevertheless, despite the drift of the T.C. from the simulation results, this work can still offer stable operation against the temperature variations. This validates that a constant I_{REF} circuit can be obtained with a low sensitivity to process, temperature, and supply voltage.

Table 3-IV summarizes the circuit performance of the proposed constant current reference in comparison to the prior-art works being implemented in standard CMOS technologies. In particular, all the works are based on relatively long-channel CMOS process technologies which are above 100 nm. The process parameters of their intrinsic transistors display relatively better immunity to process and temperature variations than advanced nanometer technology. On the contrary, the proposed I_{REF} circuit is realized using 65nm CMOS technology. It can offer a lower T.C. than most of the works [29]–[31], [33]–[39] along with a T.C. that is acceptably higher than those of [32], [10], and [40].

Besides, this work achieves the best performance in terms of line sensitivity in comparison to other works except for [29], in which it benefits from a high supply voltage architecture. It is of particular note that with a smaller operating supply than [29], this work will be subject to smaller current variation under 10% V_{DD} variation. Nevertheless, the tradeoff in this work is that it requires the occupation of a relatively larger area and a slightly higher minimum supply voltage due to the added pre-regulator. However, the minimum supply voltage is still better than that in most of the works in Table V. Furthermore, the line sensitivity without the pre-regulator is still better than that in most works. In particular, it has a lower power consumption except for [30]–[31] and [34], which focus on very low-power circuit design at the expense of

TABLE 3-IV PERFORMANCE COMPARISON OF THE PROPOSED I_{REF} CIRCUIT WITH REPORTED CURRENT REFERENCES

Parameter	[29]	[30]	[31]	[32]*	[33]	[10]	[34]	[35]	[36]	[37]	[38]*	[39]	[40]	This Work
Year	1988	1997	2005	2005	2007	2008	2010	2013	2007	2009	2010	2008	2012	2016
Process (μm)	3	2	1.5	0.35	0.18	0.35	0.35	0.35	0.25	0.35	0.18	0.5	0.18	0.065
V_{DD} (V)	3.5	1.2	1.1	2.5	1	1.4	1.8	5	1.1	2	2	2.3	1/1.2	1.4/1.2 ^{††}
Power (μW)	10@5V	0.0012	0.002	N/A	83	N/A	1	57	77	38	80	21	1.4/32.7 ⁺	7.18/
I_{REF} (μA)	0.774	0.1	0.00041	13.65	144	18.4	0.096	0.025	10.45	16.6	10	16	7.81	9.422
Temp. Range	0~80	-60~80	-20~70	-30~100	0~100	-20~80	0~80	0~80	0~120	-20~100	-20~120	0~80	0~100	-30~90
T.C.(ppm/ $^{\circ}\text{C}$)	375	1333.3 [#]	2500	28	185	46	520	250	720	280	170	130	24.9	119
Proc. Var. Acc. ⁱ (%)	7.5	30	10	15	7	13.2*	19.67 [#]	3.66	N/A	0.42	12.78	0.02	4.5	1.15
Line Sens. (%/V)	0.014	10	6	0.4	N/A	1.5	0.2	150	0.17	N/A	3	1	0.94/0.13 ⁺	0.018/0.1 ^{††}
T.C. Trim	No	No	No	Multi-T	Multi-T	No	No	No	No	Multi-T	No	Multi-T	No [†]	No
I_{REF} Trim	No	No	No	Yes	No	Yes	No	No	No	Yes	No	Yes	No [†]	No
Topology (Based)	V_{TH}	V_{TH}	V_{TH}	V_{TH}	V_{TH} (BGR)	V_{TH} (V_{TH} bias)	V_{TH}	V_{TH}	I -Sum	I -Sum (BJT)	I -Sum	V -to- I	V -to- I	V -to- I
Self-Bias (Y/N)	Y	Y	Y	Y	N	N	N	Y	Y	Y	Y	N	N	N
Samples	90	N/A	5	1	19	N/A	4	90	N/A	1	N/A	5	10	12
Area(mm^2)	0.2	0.06	0.045	0.0042	N/A	N/A	0.015	0.0058	0.002	0.058	N/A	0.06	0.023/ 0.123 ⁺	0.089
Temp. Var. Acc. over 100 $^{\circ}\text{C}$ (%)	3.75	13.333	25	0.28	1.85	0.46	5.2	2.5	7.2	2.8	1.7	1.3	0.249	1.19
Supply Var. Acc. over 10% V_{DD} (%)	0.0049	1.2	0.66	0.1	N/A	0.21	0.036	75	0.0187	N/A	0.6	0.23	0.0156	0.00252
FOM (%)	11.255	44.533	35.66	15.38	N/A	22.87	24.906	81.16	N/A	N/A	15.08	1.55	4.765	2.343/2.35 ^{††}

[#]obtained from measured data; *Simulation results; ⁺Results with BGR; [†]Yes for BGR; ^{††}No Pre-regulator; ⁱAbsolute value of the maximum process variation from the samples.

a higher T.C. performance metric.

On the basis of [100], the final assessment entails comparing the relative accuracy performance among the current references with respect to the total PVT variation. To quantify the performance metric, a sensitivity figure-of-merit (FOM) is adopted by taking into account the absolute maximum process variation accuracy (%) used in [40], the temperature variation accuracy over 100°C span and supply variation accuracy over 10% of supply voltage. The sensitivity FOM is defined as follows:

$$\text{FOM (\%)} = \begin{cases} |\text{Process variation accuracy}| \\ + \text{Temp. variation accuracy over } 100^\circ\text{C span} \\ + \text{Supply variation accuracy over } 10\% V_{\text{DD}} \end{cases} \quad (62)$$

It is noted that the term “|process variation accuracy|” refers to the absolute value of the maximum process variation in percentage (%) from the samples. It involves both D2D and WID variations. This is based on the variation induced by the manufacture of the same devices at different dies and at different locations of the same die, respectively. It can be seen from Table V that the proposed work has achieved one of the lowest values of the sensitivity FOM when compared to most of the published works. Although the value of the FOM in [39] is slightly lower than that in this work, the circuit topology [39] requires a trimming circuit together with a charge pump at the expense of increased cost and test time. On the contrary, this work does not require additional calibration whilst providing a constant output current with low PVT variation. This demonstrates its key technical merits for use in performance-aware applications using nanometer CMOS technology.

Fig. 3.22(a) shows a performance comparison of this work with respect to other reported works in terms of the total sensitivity FOM versus the process used. It can be seen that the sensitivity FOM is generally small when the long-channel process is used.

Fig. 3.22 Performance comparison of this work with respect to other reported works in terms of (a) total sensitivity FOM vs process used and (b).total sensitivity FOM vs Power consumption (*Simulation results; ⁺Results with BGR).

Several circuits have been realized with nano-scaled processes, among which the sensitivity FOM may vary a lot due to the aforementioned non-ideal effects. It has been confirmed that in spite of using the 65nm CMOS technology, this work can still provide a low value of the sensitivity FOM, thus offering a good solution for the constant current reference with reduced PVT variation. Turning to the power consumption issue, it is often regarded as the performance trade-off parameter. In order to fairly compare the performance of this work with other reported works, the relationship between the sensitivity FOM and the power consumption is illustrated in Fig. 3.22(b). It is revealed that the ultra-low power designs tend to have a big trade-off of higher performance at the expense of high sensitivity in the FOM values. As such, they may not be suitable if the total sensitivity is of concern in specific applications. On the other hand, this work can offer good FOM values whilst providing a good balance in the performance metrics like low power consumption and reduced PVT variation. This demonstrates its promising features.

3.4 Summary

This Chapter describes several widely used techniques to realize a good current reference circuit. Moreover, a low-power constant current reference in 65-nm CMOS is proposed. By matching the temperature characteristic of the dedicated reference compensation voltage with that of the output sense resistor in the op-amp-less VI converter, a constant current reference with lower T.C. over the operating temperature range and relatively lower sensitivity to the total PVT is achieved. With the embedded pre-regulator, the current reference gives good line sensitivity. The current reference offers one of the lowest values of the sensitivity FOM with respect to reported counterparts.

Chapter Four

Non-Ideal Stress Effect in Nanometer CMOS Analog Reference Circuits.

This Chapter describes further design challenges arising from the non-ideal CMOS stress on the analog references circuit design. It has drawn great attentions due to the fact that it can cause the performance degradation in the PVT-aware circuits. The mismatch models and stress effects are firstly reviewed. Then, a new electrical model is proposed to predict the stress impact on the electrical performance of reference circuits.

4.1 Introduction

The analog reference circuits with nanometer CMOS technology play a significant role in the modern integrated circuits, especially for System-on-Chip (SoC) applications. However, when technology is aggressively scaled to sub-90nm, the yield of these reference circuits, which aim at offering good precision and process-voltage-temperature (PVT) aware performance, will be subject to sensitivity to the local device mismatch and the physical stress in the circuit implementations [50], [98], [108]–[132]. For this reason, this demands substantial design efforts, performance parameters tradeoff and extensive statistical simulations. The ultimate goal is to provide good prediction in the context of many non-ideal factors that impact on these analog circuits after fabrications.

Local mismatch, which is considered as the with-in-die (WID) variation, defines the random variation on the identically designed devices and components under the same die. It is caused by the random variation of the substrate dopant atoms, implantations, mobility in the front-end-of-line (FEOL) and fixed oxide charge in the fabrication process [98], [110]. Many efforts have been made to investigate the mismatch effect of MOS transistors and develop the mismatch models [98], [111]–[123]. The variations in the MOS transistors are analyzed in [110]. They depend on the dimensions or area of the devices. However, the demonstration is only conducted using NMOS devices with a large geometry. Besides, the physical causes behind the mismatch in all MOSFET devices are elaborated with statistical models in [111]. Later, an alternative mismatch model [98] is thoroughly derived over device's geometry, distance and different orientations. Further analysis of the mismatch has been extended to the deep submicron technologies [113], [115], [120], [121]. On top of that, the design tradeoffs for analog circuits in the context of local mismatch are also reported in details [122]. Besides, the stress impact on the performance of MOSFET devices have been studied by many literatures [50], [108], [109], [124]–[132] which emphasize on the device aspect. However, the other challenge coming from CMOS physical stress is seldom mentioned in the aspect of design and simulation of analog circuits. Therefore, it is considered another important non-ideal effect that will cause significant performance degradation in the PVT-aware circuits, particularly in nanometer CMOS technologies.

The stress, which comprises tensile and compressive stress components, can affect the carrier mobility and modify the drain current or transconductance of the transistors [124], [133]–[136]. Of particular noted, the shallow trench isolation (STI) region in silicon contributes to the dominant compressive mechanical stress, influencing greatly on the device's electrical performance [50], [125], [127], [128], [131]. The mismatch

induced by the physical stress has been analyzed in [109] and [126]. The results have shown that it can contribute a wide variation of device parameter values, ranging from 5% up to 18% in the die.

Regarding the widely used BSIM4 model [137], although it permits the random variation in device parameters, it may not be accurate due to the stress effect is not fully taken into account. This may explain why extra deviations occur between the simulation results and the measurement results from the reported analog reference circuits [31], [36], [138]–[140]. Even though some physical models [129], [131], [132], [141] have been explored, they turn out to be complicated. More importantly, these models may not be compatible to the same simulation platform from the process design kit (PDK) in integrated design and simulation environment. As a result, this gives the motivation to derive an electrical model for the nanometer CMOS device stress effect. Therefore, it is amenable for the design and simulation of analog reference circuits.

In this work, a new electrical model is proposed to predict the stress effect on the electrical performance of reference circuits. It introduces a statistical stress-induced offset voltage on the basis of the random stress to the circuit simulation. This allows an improved prediction on the measurement results using the exemplary voltage and current reference circuits.

The mismatch models from the previous works and stress effect will be reviewed in the next section.

4.2 Review of Mismatch Models and Stress Effect on MOS transistors

In this Section, the mismatch models from the previous works and stress effect will be reviewed.

4.2.1. Mismatch Models for MOS transistors

The investigations [98], [110], [111] pertaining to the matching of identically designed MOSFET devices have reported that the random variations of both the threshold voltage (V_{TH}) and current factor (β) can be modeled as a normal distribution. They have zero mean and the standard deviations are defined as

$$\sigma(\Delta V_{TH}) = \frac{A_{VTH}}{\sqrt{W \times L}} \quad (63)$$

$$\frac{\sigma(\Delta \beta)}{\beta} = \frac{A_{\beta}}{\sqrt{W \times L}} \quad (64)$$

where $\beta = \mu C_{OX}(W/L)$, in which μ represents the carrier mobility, C_{OX} is the gate oxide capacitance, W means the channel width and L is the channel length. A_{VTH} and A_{β} are process dependent constants. It can be observed that these random mismatches are inversely proportional to the square root of the device areas.

Based on the model, the variance of the relative current variation [111] for the saturation based MOSFET device under same bias condition can be obtained as

$$\left(\frac{\sigma(\Delta I)}{I} \right)^2 = \left(\frac{\sigma(\Delta \beta)}{\beta} \right)^2 + \frac{4 \times \sigma^2(\Delta V_{TH})}{(V_{GS} - V_{TH})^2} \quad (65)$$

Similarly, the variance of the V_{GS} variation induced by the device mismatch [114] in a matching pair with identical drain currents can be expressed as

$$\sigma^2(\Delta V_{GS}) = \sigma^2(\Delta V_{TH}) + \frac{(V_{GS} - V_{TH})^2}{4} \times \left(\frac{\sigma(\Delta\beta)}{\beta} \right)^2 \quad (66)$$

From (65) and (66), the matching accuracy depends on the biasing condition. It can be seen that a large overdrive voltage ($V_{GS} - V_{TH}$) can reduce the current variance and increase V_{GS} variance.

In order to meet low power constraint, the weak inversion based designs have been drawn great attention [142]. As such, (65) and (66) are then modified by [114], [143] to cater for both weak and strong inversion based devices. They are given as follows:

$$\left(\frac{\sigma(\Delta I)}{I} \right)^2 = \left(\frac{\sigma(\Delta\beta)}{\beta} \right)^2 + \left(\frac{g_m}{I} \right)^2 \sigma^2(\Delta V_{TH}) \quad (67)$$

$$\sigma^2(\Delta V_{GS}) = \sigma^2(\Delta V_{TH}) + \frac{1}{(g_m/I)^2} \times \left(\frac{\sigma(\Delta\beta)}{\beta} \right)^2 \quad (68)$$

where the derivations of (5) and (6) are based on the operation model of transistor which is valid for all regions [144], [145].

From [92], the subthreshold drain current can generally be expressed as

$$I_D \approx \left(\frac{W}{L} \right) I_S \exp \left(\frac{V_{GS} - V_{TH}}{\eta V_T} \right) \quad (69)$$

with the assumption that the drain-source voltage, $V_{DS} > 75$ mV and the characteristic current is defined as $I_S = \mu C_{OX}(\eta-1)(V_T)^2$, where V_T represents the thermal voltage and η stands for the subthreshold slope factor. From (69), the ratio of g_m/I_D can thus be obtained as follows:

$$\frac{g_m}{I_D} = \frac{\delta I_D}{\delta V_{GS}} \frac{1}{I_D} = \frac{1}{\eta V_T} \quad (70)$$

Comparing (5)-(6) with respect to (3)-(4), it has revealed [146] that the mismatch

between the devices operating in the subthreshold region exhibit less sensitive to the overdrive voltage than that in the saturation region. It is noted that these models are limited to long and wide transistors without taken into account of stress effect.

4.2.2. Stress Effect on MOS transistors

The stress on the device depends on the direction of stress with respect to the device channel. As illustrated in Fig. 4.1 [124], the STI induced compressive stress can be categorized into (i) a transverse stress (ε_T) across or perpendicular to the channel or (ii) a longitudinal stress (ε_L) along the channel. The stress influence on the mobility in MOS transistors is summarized in Table 4-I. As reported in [50], when the MOS transistors are surrounded by STI regions, the mobility variation of the NMOS and PMOS transistor in 40nm CMOS can reach -27 % and 3%, respectively. This is due to the degradation effect of STI stress on NMOS device in both directions, whereas the enhancement effect dominates along the channel for PMOS transistor to yield the slight increase of mobility. In the usual layout practice, the devices' layout is arranged in a dense environment for compactness and device matching. Unfortunately, the transverse stress (ε_T) across the channel will dominate such that both NMOS and PMOS mobility variation reach at about 18% and 14%, respectively, as stated in Table 4-II. This case becomes the focus of this work because it often happens when the matching layout techniques such as common-centroid distribution are employed.

The investigation has reported that the length of diffusion (LOD) and distance of gate to STI are the factors that lead to the unintentional stress [125], [127]. These factors have been considered in the commonly used BSIM model [127], [137]. However, it is not

Fig. 4.1 Cross-sectional view of stress components of MOSFETs.

TABLE 4-I STRESS EFFECT ON MOBILITY OF MOSFETs

Stress Type	Impact on mobility of nanometer MOSFETs [124]			
	NMOS		PMOS	
	Trans. (ϵ_T)	Longit. (ϵ_L)	Trans. (ϵ_T)	Longit. (ϵ_L)
Compressive	Degrade	Degrade	Degrade	Enhance

TABLE 4-II MOBILITY VARIATION OF MOSFETs IN DENSE LAYOUT

Stress Type	3σ mobility variation in nanometer MOSFETs [50]	
	NMOS	PMOS
Compressive	-18%	-14%

adequate to account for other complex layout environment. Several works [129], [131], [132] have reported that, apart from the LOD and gate to STI distance, the gate space as well as the width of STI region contributes to extra sources of stress effect. As reported in [132], the drain current variation can reach 10% due to the width of STI region. Besides, a comprehensive analysis flow targeting for the stress effect on circuit performance is presented in [141].

At this juncture, the stress effect is not thoroughly addressed in the nanometer CMOS process technology using BSIM model as an example, an electrical model which addresses the stress on circuit performance becomes useful for the circuit designers.

4.3 Proposed Electrical Based Stress Model

Fig. 4.2 illustrates the exemplary distributions of temperature coefficient (T.C.) performance metric under process variation in typical analog reference circuits. The total variation can be obtained by the Monte-Carlo (MC) simulation using BSIM4 model. It is common to observe that the actual measurement results, arising from a particular process corner case and limited samples as one example, may fall outside the spread of the total variation from these statistical simulations. This discrepancy is mainly due to the lack of the model dedicated to the devices' stress effect because only the process corner and local mismatch effects are included in BSIM4 model. If a statistical electrical stress model is added for the MC simulation, the total variation can provide an improved occurrence prediction for the measurement results. This is mainly because the random stress will usually induce wider variation of electrical performance parameter in practical scenario.

Fig. 4.2 Distribution of temperature coefficient under process variation at different scenarios.

4.3.1. Electrical Based Stress Model

The threshold voltage variation versus mechanical stress has been found negligible while mobility dependence on stress is considered the most significant effect [109], [128], [134]. For this reason, in this electrical model, the current factor variation caused by the mobility variation is of prime focus.

Referring to the basic mismatch model and the stress impact on the device's carrier mobility, the expression of the drain current variation can be modified in a form as

$$\left(\frac{\sigma(\Delta I)}{I}\right)^2 \approx \left(\frac{g_m}{I_D}\right)^2 \sigma^2(\Delta V_T) + \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + (\alpha_{STR})^2 \quad (71)$$

in which

$$\alpha_{STR} \approx \left(\frac{\sigma(\Delta\mu_{OS})}{\mu_{OS}}\right)_{STR} \quad (72)$$

where α_{STR} denotes the deviation of the relative mobility variation because of physical stress. The 3σ variation ($3\sigma/\mu$) range can be estimated according to the typical estimation in Table II. Finally, the new variance of ΔV_{GS} can be obtained as

$$\sigma_n^2(\Delta V_{GS}) = \sigma_o^2(\Delta V_{GS}) + \frac{1}{(g_m/I)^2} \times (\alpha_{STR})^2 \quad (73)$$

As suggested from (73), the CMOS stress-induced mobility variation will impose additional variation on the variance of ΔV_{GS} . This translates to an additional random offset voltage to model this silicon stress-induced variation for the matching device pairs.

The schematic of stress-induced offset model for the NMOS pair and PMOS pair are depicted in Fig. 4.3(a) and Fig. 4.3(b), respectively. The model consists of two unity-gain voltage control voltage sources (VCVS) which serve as the input and output port

Fig. 4.3 Schematic of stress-induced offset model for (a) NMOS and (b) PMOS transistor pairs.

of the offset voltage (V_{OS}) source. They aim to provide the impedance isolation so that the loading effect of the random generator to the circuit can be avoided. The offset voltage, V_{OSN} , in Fig. 4.3(a) is modeled by the difference between the voltage across a non-ideal high-resistance poly resistor (R_{OS}) and an ideal constant voltage source. It can be represented as

$$V_{OSN} = V_{osni} - V_{osno} = V_A - V_B = V_{NR} - V_{NRm} \quad (74)$$

where $V_{NR} = I_{BN} \times R_{OS}$ and I_{BN} is an ideal current source (CS). V_{NRm} is the mean value of V_{NR} at typical condition. By setting $V_{OSN} = 0$ V, the random offset voltage can have a normal distribution with a mean value, $\mu(V_{OSN})$, of 0 V and a standard deviation determined by $\sigma(V_{OSN}) = I_{BN} \times \sigma(R_{OS})$. Meanwhile, to eliminate the temperature factor of

the poly resistor on the generated V_{OS} , the same T.C. is thus applied to the ideal voltage source, V_{NRm} . The corresponding T.C. is extracted from the used resistors using the characterization method in [140]. Similarly, the offset model, V_{OSP} , in Fig. 4.3(b) can be obtained as

$$V_{OSP} = V_{ospi} - V_{ospo} = V_A - V_B = V_{PRm} - V_{PR} \quad (75)$$

where the symbols have the usual meanings as those in (74). It also exhibits a normal distribution with $\mu(V_{OSP}) = 0$ V and $\sigma(V_{OSP}) = -I_{BP} \times \sigma(R_{OS})$.

It has revealed from (74) and (75) that the two models have different polarities. This is because different polarities of gate-source voltage, V_{GS} , corresponding to the NMOS and PMOS transistor pairs.

Fig. 4.4(a) and Fig. 4.4(b) depict the MC simulation results of the R_{OS} and the obtained offset voltage, V_{OSN} , corresponding to the stress model shown in Fig. 4.3(a). The MC simulation is conducted for 500 runs with 3σ coverage. Besides, I_{BN} and R_{OS} is set to be 10 μ A and 10 k Ω , respectively. According to Fig. 4.4(a), the process variation (σ/μ) of the high-resistance poly resistor R_{OS} is around 4.65%. Accordingly, the model V_{OSN} has a mean value of only 0.083 mV which is relatively small with respect to the standard derivation and can be negligible. Of particular interest, the standard deviation of V_{OSN} is $\sigma(V_{OSN}) = I_{BN} \times \sigma(R_{OS}) \approx 4.65$ mV. In this way, the Gaussian distribution of the IR product generator is translated to that of the approximated V_{OS} model. This has confirmed the random properties of the stress-induced mismatch model.

More importantly, R_{OS} and I_{BN} can be scaled for application of the derived model. The proper constant ratios of K_{RN} and K_{IN} can be applied to R_{OS} and I_{BN} , respectively. Finally, $\sigma(V_{OSN})$ can be approximated as

(a)

(b)

Fig. 4.4 Monte-Carlo simulation of the poly resistor (R_{OS}) and the obtained offset (V_{OSN}) based the stress model shown in Fig 3(a).

$$\sigma(V_{OSN}) \approx K_{IN} I_{BN} \times K_{RN} R_{OS} (4.65\%) = 4.65 K_{IN} K_{RN} \quad (76)$$

In the same way, $\sigma(V_{OSP})$ can also be obtained with the design ratios, K_{IP} and K_{RP} . As a result, the models in Fig. 4.3 can be applied to different scenarios where different variations induced by the physical stress in the silicon are considered.

4.3.2. Implementation of the Stress Model

Referring to the model in Fig. 4.3, each terminal of the model can be connected to any high impedance node such as the gate terminal of the matching pairs. Fig. 4.5 illustrates the exemplary implementation of the proposed models in various types of transistor matching pair. As indicated, V_{OSN} will be added in a form of stress-induced offset on the NMOS matching devices such as the current mirror (M_{N1} and M_{N2}), the differential input pair (M_{D1} and M_{D2}) as well as the current source pair (M_{B1} and M_{B2}). Similarly, V_{OSP} will be responsible for the stress offset model for the PMOS matching transistor pairs. This is placed in the PMOS current mirror (M_{P1} and M_{P2}) example as shown in Fig. 4.5.

To estimate the magnitude of respective V_{OS} , a design procedure is summarized as follows:

- i Identify the critical transistor matching pairs which are highly-sensitive to stress in the circuit.
- ii Referring to the stress-induced 3σ variation range of relative mobility variation in nanometer MOSFETs in Table II, α_{STR} described in (72) can be estimated for NMOS (α_{STRN}) and PMOS (α_{STRP}) accordingly.
- iii Based on (73), the standard deviation of stress-induced offset voltage can be estimated by $\sigma(V_{OSN}) = (I \times \alpha_{STRN}) / g_m$.
- iv Substituting the calculated $\sigma(V_{OSN})$ to (76) and assuming $K_{RN}=1$, the required K_{IN} can be obtained.
- v Based on (74), set $V_{NRm}=V_{NR}=K_{IN} \times I_{BN} \times R_{OS} \times K_{RN}$ that leads to $\mu(V_{OSN})=0$ V. As such, V_{OSN} for NMOS matching pair can be generated. The same goes for V_{OSP} for PMOS matching pair by following the steps from (i) to (v).

Fig. 4.5 Exemplary schematics of transistor matching pairs with stress-induced offset model.

- vi Apply V_{OSN} and V_{OSP} to the selected critical NMOS and PMOS transistor matching pairs, respectively, and run the MC simulation to evaluate the circuit performance.

4.3.3. Results and Discussions

To demonstrate the proposed model, the simulations and analysis are carried out for the constant current source [140] and the threshold reference circuit [139]. Both works were designed using the UMC 65-nm CMOS technology. The stress-induced offset model is inserted in the mismatch sensitive transistor pairs in the corresponding current source and V_{TH} reference circuit, as shown in Fig. 4.6(a) and Fig. 4.6(b), respectively.

Fig. 4.6 (a) Stress-induced offset implementation in critical matching pairs of the current reference circuit [140] (b) Stress-induced offset implementation in the critical matching transistor pairs of the V_{TH} reference circuit [139].

(I). Verification of Stress Effect on I_{REF}

The 500 runs on MC simulation are conducted for the T.C. of current source in [140] and the results are depicted in Fig. 4.7(a). It has revealed that a mean T.C. of 11.78 ppm/ $^{\circ}$ C can be achieved with a standard deviation of 6.84 ppm/ $^{\circ}$ C. As expected, the measurement results (12 samples) shown in Fig. 4.7(b) have indicated that there is a drift of T.C. when compared to that of the simulation results. Since the MC simulation relies on the process and mismatch variation in BSIM4 model. Indeed, the stress caused by the STI region induces extra mismatch in the MOSFET devices. This degrades the circuit operation in a form of temperature stability, leading to the T.C. of measured samples fall outside the prediction from the 500 runs on MC simulation.

In order to verify the proposed work, the electrical stress models, V_{OSP} and V_{OSN} , is then applied to the critical PMOS and NMOS transistor matching pairs, respectively, in the core circuit of [140] according to Fig. 4.6(a). The percentage of the stress effect is set according to Section II-D. Including the statistical stress model, the MC

Fig. 4.7 (a) Monte-Carlo simulation result of T.C. with total process variations (process and mismatch) (b) Distribution of the untrimmed T.C. performance for measured 12 samples. (c). Monte-Carlo simulation result of T.C. with total process variations and statistical stress-induced offset voltages (500 runs) (d). Monte-Carlo simulation result of T.C. with total process variations and statistical stress-induced offset voltages (12 runs). (e). Scatter plot of stress-induced offsets for V_{OSN} and V_{OSP} versus T.C. with total process variations under MC simulation (12 runs). (f). Monte-Carlo simulation result of T.C. with total process variations and extracted stress-induced offset voltages (12 runs).

simulation results of the T.C. on the basis of 500 and 12 samples are shown in Fig. 4.7(c) and Fig. 4.7(d), respectively. Of particularly noted, the MC simulation with 12 runs is to model the variation under small sample size which is similar to the measured sample size. Obviously, the variation of the T.C. is increased when incorporating the stress model. The measurement results fall within the spread of the T.C. distribution,

thus confirming an improved prediction on the performance variation. To further verify the correctness of the proposed model, Fig. 4.7(e) depicts the scatter plot of stress-induced offset of V_{OSN} and V_{OSP} versus T.C. with the total process variation under 12 runs on MC simulation. At this juncture, based on the measurement data, the stress-induced offsets can be extracted. In this scenario case, V_{OSP} and V_{OSN} are about 3.29 mV and 3.15 mV. These offset voltages correspond to about 6% and 8% in mobility variations for the PMOS and NMOS transistor matching pairs, respectively. They are calculated using the value of parameters from the devices M_3 and M_2 in Fig. 4.6(a) and the step (iii) equation in Section 4.3.2. Then, another 12 runs on MC simulation are conducted. As indicated in Fig. 4.7(f), the mean T.C. is close to that of the measurement results. It has validated that there is a reasonable correlation between the predicted results and the measured results using the proposed electrical stress model.

(II). Verification of Stress Effect on V_{TH} Reference Circuit

Similarly, the 500 runs on MC simulation are conducted to obtain the T.C. of the V_{TH} reference circuit in [139] and the results are displayed in Fig. 4.8(a). A mean T.C. of 34.44 ppm/°C can be achieved with a standard deviation of 18.98 ppm/°C. On the contrary, referring to Fig. 4.8(b), the T.C. based on the untrimmed measurement results for 15 samples is degraded. The MC simulation setup is the same as that used for the I_{REF} verification. As expected, the stress on the MOSFET devices reduces the thermal stability.

As shown in Fig. 4.6(b), the same demonstration method is applied through inserting the respective stress-induced offset models (V_{OSP} , V_{OSN1} and V_{OSN2}) to the critical PMOS and NMOS transistor matching pairs in the core circuit of [139]. Fig. 4.8(c) and Fig. 4.8(d) depict the MC simulation results of the T.C. with total process variation

Fig. 4.8 (a) Monte-Carlo simulation result of T.C. with total process variations (process and mismatch) (b) Distribution of the untrimmed T.C. performance for measured 15 samples. (c). Monte-Carlo simulation result of T.C. with total process variations and statistical stress-induced offset voltages (500 runs) (d). Monte-Carlo simulation result of T.C. with total process variations and statistical stress-induced offset voltages (15 runs). (e). Scatter plot of stress-induced offsets for V_{OSN1} , V_{OSN2} and V_{OSP} versus T.C. with total process variations under MC simulation (15 runs). (f). Monte-Carlo simulation result of T.C. with total process variations and extracted stress-induced offset voltages (15 runs).

and statistical stress-induced offset voltage based on 500 and 15 runs, respectively. It is noted that the 15 runs on MC simulation are to model the variation corresponding to the measured sample size. Unsurprisingly, the T.C. is degraded when incorporating the stress effect. The spread of the simulated T.C. distribution can cover the measured T.C. distribution, implying an improved prediction on the performance variation. Fig. 4.8(e)

TABLE 4-III VALUE OF PARAMETERS FOR THE SELECTED DEVICE IN CRITICAL MATCHING PAIRS.

Parameter	Devices in Fig. 4.6(a)		Devices in Fig. 4.6(b)		
Device	M2	M5	M2	M4	M7
Drain Current (nA)	997	997	98.8	53.6	53.6
g_m (μS)	24.6	16.6	3.1	1.6	1.3

shows the scatter plot of stress-induced offsets for V_{OSN} and V_{OSP} versus T.C. with total process variations under the 15 runs on MC simulation. The stress-induced offset voltages can then be extracted on the basis of the result close to the measured mean T.C.. The extracted offset voltages, V_{OSN1} and V_{OSN2} , are close to 1 mV, which imply about 3% in mobility variation for NMOS matching pairs. This is calculated by using the value of parameters from the devices M_2 , M_4 and M_7 in Table 4-III and the step (iii) equation in Section 4.3.2. Similarly, the offset voltage V_{OSP} , is obtained about 2% in mobility variation for the PMOS matching pairs. These specific offsets are included for another 15 runs on MC simulation. The T.C. distribution is illustrated in Fig. 4.8(f). As predicted, the stress-induced offset voltages will degrade the T.C. of output voltage. The mean T.C. is similar to that of the measured mean value, confirming the reasonable correlation between the model prediction result and the measurement result.

(III). Stress Reduction using Simplified DEM Design Method

Regarding the stress-induced mismatch effect, it mainly depends on the surrounding STI regions. To mitigate the effect, the dynamic element matching (DEM) method [147]–[155] can be employed because the mismatch errors, which are caused by the random local mismatch, are averaged out. As a result, it offers better accuracy at the expense of increasing the circuit complexity through adding switches and a clock control signal. The exemplary implementation in the matching pairs of current mirrors

Fig. 4.9 Schematic of exemplary current source with DEM implementation.

is depicted in Fig. 4.9. It is based on the basic circuit of Fig. 4.5 where the current mirror pairs have the corresponding ratio of N and P , the offset effect will be multiplied due to the current gain. For DEM implementation in Fig. 4.9, unit transistors are employed. The switch set being connected to each unit transistor serves as a multiplexer which allows the current to flow via either input node (N_1) or output node (N_2) depending on the DEM control logic. To maintain the correct operation, this DEM control is designed with successive clock cycles to switch each unit current alternately. In this way, the mismatch errors can then be averaged out.

Based on this method, the DEM is applied to the selected PMOS and NMOS matching pairs with a current gain larger than one in the constant current source [140]. The rationale is to simplify the switching design by focusing on critical transistor matching pairs which are sensitive to stress. The schematic with simplified DEM implementation is depicted in Fig. 4.10. Fig. 4.11(a) illustrates the comparative simulation results for the output current T.C. of the current reference circuit [140] under three cases. They are pertaining to (i) the circuit without stress-induced offsets, (ii) the circuit with stress-induced offsets and (iii) the circuit with stress-induced

Fig. 4.10 Schematic of DEM implementation for the selected critical transistor matching pairs in the current source circuit [140].

Fig. 4.11 (a) BSIM4 comparative simulation results for the output current T.C. of current reference circuit under three cases (b) the circuit without stress-induced offset, (c) the circuit with stress-induced offsets (See section IV-A), and (d) the circuit with stress-induced offsets and simplified DEM.

offsets and simplified DEM circuit implementation.

Fig. 4.11(b) shows that the reference circuit can provide a constant current with good temperature stability of 7.14 ppm/°C under typical BSIM4 simulation without stress

taken into account. Once the stress-induced offsets are added, the TC is degraded to about 78.73ppm/ $^{\circ}$ C as shown in Fig. 4.11(c). Nevertheless, if the simplified DEM design approach is applied, it can be seen from Fig. 4.11(d) that the circuit can maintain a reasonably small T.C. of 16.92 ppm/ $^{\circ}$ C regardless of the existence of stress. This has confirmed that the stress effect can be effectively reduced through the implementation of the simplified DEM dedicated to the critical matching transistor pairs having the ratio larger than one.

4.4 Summary

The design challenges like mismatch and stress effect are studied and reviewed. In addition, a new electrical model dedicated to stress effect on nanometer CMOS devices is presented. Based on the current-resistance (IR) product random generator, a statistical stress-induced offset voltage can be included for matched devices in MC circuit simulation. It has shown that there is a reasonable correlation between the prediction results and the measurement results using both 65-nm CMOS voltage and current reference circuits. Validated by the proposed model, a simplified DEM design approach is given to demonstrate the reference circuit with significant less sensitivity to stress effect. The proposed model is useful for providing an improved statistical prediction in the design and simulation of analog circuits.

Chapter Five

Low Dropout Voltage Regulators

This Chapter reviews the reported LDO regulators and proposes an improved method for achieving fast transient response under low power constraint.

5.1 Introduction

As aforementioned, the LDO regulators play a significant role in the power management IC. For instance, as an essential building block of the ultra-low-power microcontroller (MCU) systems for battery-powered applications in portable electronics, LDO regulators are popularly utilized to supply the embedded digital core [87], [156] with moderate to high capacitive load. The OCL-LDO regulator draws great attention for the SoC system. To tackle the transient limitations with absence of the large output capacitor, many circuit techniques have been reported.

Consider an adaptive biasing technique in [61], [68], it is a fast circuit technique which extends the regulator's loop bandwidth when I_L increases. In design concern, [61], [68] may suffer from stability issue which stems from the positive feedback control inside the feedback loop. Turning to the low-power slew-rate enhancement stage [66], it permits fast charging/discharging rate at the gate of pass transistor. Its drawback is that it cannot support low-voltage operation. In [71], a simple quiescent current booster is presented to improve the slew-rate of error amplifier in the regulator. The price paid for that is to support a minimum I_L of 1 mA. In addition, it is subject to the supply variations. Refer to the push-pull topologies in [64], [74], a push–pull output error amplifier [64] offers high slew rate but its limited transconductance restricts the

bandwidth. Despite the assistant push-pull output stage [74] meets both the ultra-low power and fast transient objectives, the price paid for that is in exchange of circuit complexity. Consider the flipped-voltage-follower (FVF) LDO regulator architectural solutions [60], [67], [70], they have been explored in great details. An ultra-fast transient response is reported in [60] but having significantly high quiescent current of 6 mA. [67] and [70] suggest an economical voltage spike detection circuit that generates the momentary current to increase the charging/discharging rate at the power transistor's gate without significantly increasing the static power dissipation. It is regarded as an economical and efficient technique. Unfortunately, their circuit topologies are limited to drive small C_L range and require high minimum loading current I_L . In order to relax the stated problems, the LDO regulators [75], [77], with simple and cost-effective circuit architecture realized in 65nm CMOS technology, has recently been reported. They can provide several good figure-of-merits (FOMs) as well as wide C_L range using Dual Summed Miller Frequency Compensation (DSMFC) at low quiescent current. On the other hand, in order to preserve the battery life of portable electronic devices, it is of paramount importance to reduce the supply voltage so as to meet the low power constraint. A lot of integrated circuits or systems have been reported to operate under a supply voltage down to 0.5 V [157]–[160]. To permit a stable power line of these circuits, a low-voltage LDO regulator providing a 0.5 V output voltage is of great demand. However, when it is pushed towards sub-1V supply in the context of the trend of low-voltage and low-power SoC environment, the LDO regulator will suffer from the performance degradation in terms of speed and stability due to the substantial increase in the power transistor's size to maintain a high current driving capability. This raises the motivation for the investigation and design of an improved low-voltage FVF LDO regulator using the foundation circuits in [75], [77] to

achieve fast transient response under low power constraint. The details of the proposed improved regulator will be presented in the following sections.

5.2 Review of LDO Regulators

This section reviews the major parameters and specifications on the LDO regulator as well as the challenges in OCL-LDO regulator design.

5.2.1.LDO regulator and main specifications

The schematic of a typical LDO regulator with PMOS power transistor and NMOS power transistor are depicted in Fig. 5.1(a) and Fig. 5.1(b). As shown in Fig. 5.1(a), the regulator consists of a power transistor (M_P), a resistive feedback network formed by R_{F1} and R_{F2} , and an error amplifier. They form a negative feedback control loop to regulate the output voltage (V_{OUT}). The error amplifier is utilized to compare the difference between the feedback signal and a reference voltage and control the power transistor to deliver the different load current whilst providing a constant V_{OUT} . Besides, C_L is the output capacitor, which normally has an equivalent series resistance (ESR), R_{ESR} , whereas R_L represents the output resistive load. Prior to the discussion of the proposed LDO regulator, the key terminologies will be described as follows:

(I). Dropout Voltage

Dropout voltage ($V_{DropOut}$) is the voltage difference between the output and input where the regulation fails. It is noted that the PMOS power MOS will behave like a pass element with an on-resistance, R_{ON} , shown in Fig. 5.1(a), such that

$$V_{DropOut} = I_L \times R_{ON} \quad (77)$$

Fig. 5.1 Schematic of conventional LDO regulator with (a) PMOS power transistor and (b) NMOS power transistor [55].

where I_L represents the load current. Of particular noted, R_{ON} may include the equivalent path resistance arising from the interconnect metal, IO pads and packaging bond wires. However, in the case of NMOS power transistor shown in Fig. 5.1(b), the dropout voltage will be as high as $V_{DropOut} = V_{GS} + V_{DSAT}$, implying a much higher supply voltage than that with a PMOS power transistor. To meet the low-voltage and low-power constraint, the PMOS power transistor based regulator will be the focus of this research work.

(II). Quiescent Current

Quiescent current (I_Q) is a main parameter which is of significance to the low-power circuit design. It denotes the current required to supply the internal circuit blocks, such as error amplifier, output sense resistor network, voltage reference and so forth in the presence of the particular minimum load current or no-load current (0 A) condition [161]. The operating conditions like supply voltage and temperature are also needed to be specified, such that

$$I_Q = I_{IN} \Big|_{I_L=0A} \quad (78)$$

It is noted that due to the voltage driven properties of the MOS power transistor, the LDO regulator which is based on MOS transistor tend to have small I_Q . It turns out that MOS transistor based regulator becomes more suitable for the applications with low power constraint.

(III). Load Regulation

Load regulation (LDR) defines the capability of the LDO regulator to sustain the designed output voltage (V_{OUT}) against the load current variations. It can be expressed as [162]

$$\text{LDR} = \frac{\Delta V_{OUT}}{\Delta I_L} \approx \frac{R_{OL}}{1 + A_{OL}\beta} + R_{Par} \quad (79)$$

where R_{OL} is the open-loop output resistance, A_{OL} is the DC open-loop gain, and β is the feedback factor. R_{Par} stands for the parasitic resistance on the PCB during measurement. As interpreted from (79), the load regulation can benefit from a higher DC loop gain.

(IV).Line Regulation

Similar to the LDR, line regulation (LNR) measures the ability of the LDO regulator to maintain the constant V_{OUT} in spite of DC input voltage variations. It is given by

$$\text{LNR} = \left. \frac{\Delta V_{OUT}}{\Delta V_{IN}} \right|_{f=0\text{Hz}} \quad (80)$$

(V). Power Supply Rejection

Power supply rejection (PSR) defines the feature of the LDO regulator to suppress the V_{OUT} variations arising from the input noise and ripples including the entire frequency spectrum. It is given as

$$\text{PSR} = 20 \log \left(\frac{1}{\Delta V_{OUT} / \Delta V_{IN}} \right) \quad (81)$$

From (81), it is noted that the PSR at DC condition is related to the LNR defined in (80).

(VI). Load Transient Response

Load transient response is an important feature of the LDO regulator which specifies the regulator's ability to maintain the targeted V_{OUT} for sudden load current transitions. The V_{OUT} variations (ΔV_{OUT}) induced by these fast load current transitions become a key technical metric to demonstrate the fast transient response. It is noted that the maximum variation occurs when the load current is suddenly switched from zero (no load) to its maximum rated value (full load, $I_{L(\text{Max})}$). ΔV_{OUT} can be modelled by

$$\Delta V_{OUT} \approx \frac{I_{L(\text{Max})}}{C_L} \times \Delta t_r \quad (82)$$

where $I_{L(\text{Max})}$ is the maximum load current and Δt_r denotes the response time of the regulator. Of particular noted, Δt_r depends on the closed-loop bandwidth (BW_{CL}) and the slewing conditions at the gate of the power transistor. It can be expressed as [162]

$$\Delta t_r \approx \frac{0.37}{BW_{CL}} + C_P \times \frac{\Delta V_P}{I_{SR}} \quad (83)$$

where C_P and ΔV_P represent the parasitic capacitance and voltage variation at the gate of power transistor, respectively. I_{SR} is the bias current which limits the slew rate at the gate of the power transistor. When increasing the BW or slew rate at the gate of power transistor, it can reduce the response time, leading to fast transient response with small voltage variations.

(VII). Efficiency

The efficiency of the LDO regulator can be derived as

$$\eta = \frac{V_{OUT} \times I_L}{V_{IN} \times (I_Q + I_L)} \approx \frac{V_{OUT}}{V_{IN}} \quad (84)$$

As indicated from (84), minimizing the quiescent current and dropout voltage can result in high efficiency. If I_L is made much larger than I_Q , the efficiency will be limited by the dropout voltage.

5.2.2.Challenges in Output Capacitor-Less LDO Regulator

The conventional LDO regulator shown in Fig. 5.1 relies on a large output capacitor with R_{ESR} to achieve circuit stability. However, the recent trends are moving towards to remove the large output capacitor for the SoC systems. It is common to observe that the absence of large output capacitor will contribute large transient variation in the OCL-LDO regulator. Therefore, one main purpose of this work is to devise the fast transient techniques to tackle the transient limitations. Another important problem to be addressed is that of the stability issue that usually happens in the OCL-LDO regulator without the large output capacitor under no load condition, with the output pole being located in low frequency. Furthermore, the continuous technology scaling also imposes another challenge for the OCL-LDO design to sustain the stability and transient variation under process and temperature variations.

Starting with the simple FVF LDO regulator, one transient-assisted technique is then proposed and demonstrated in the following section.

5.3 Proposed Wide Capacitive Load Based FVF LDO Regulator using Transient-Assisted Embedded Driving Stage

In this Section, a low-voltage transient-assisted FVF based OCL-LDO regulator in 65nm CMOS technology is presented. It can drive a wide range of capacitive load with the employment of the DSMFC technique. A new low-output impedance transient-assisted embedded driving stage (TAEDS) is devised to enhance the slew rate at the gate of power transistor during load current transitions whilst allowing low quiescent current. This is particularly effective when using large size power transistor to deliver high load current under low supply voltage. The TAEDS is proposed and analyzed, which is then followed by the circuit stability analysis. The tradeoff between the minimum load current and output resistance of the embedded driving stage is discussed. The transient behavior of the TAEDS LDO is also investigated.

5.3.1. Proposed Transient-Assisted Embedded Driving Stage

(I). Review of Embedded Driving Stages

Low power consumption is the crucial requirement to extend the battery life of portable devices. Consequently, low-voltage and low quiescent current based LDO regulators are of great interest in low power electronics. However, reducing the supply and quiescent current will result in poor loop-gain which degrades the load and line regulation. In order to enhance the loop-gain of the LDO regulator, a non-inverting gain stage is usually added between the error amplifier and the power transistor. The conventional embedded driving stage (CEDS) is shown in Fig. 5.2(a) which has been

Fig. 5.2 (a) Conventional embedded driving stage [63]. (b) Class-A embedded driving stage [69]. (c) Push-pull embedded driving stage [76].

widely used in [63], [70], [77]. It is apparent that the CEDS has high output impedance ($R_3 \approx r_{b2} \parallel r_{ds3}$, where r_{b2} is the output impedance of current source I_{b2} and r_{ds3} is the drain-source resistance of M_3). Due to the large parasitic capacitance (C_p) at the gate of the power transistor, a low frequency parasitic pole is then formed at node N_3 , resulting in the possibility to jeopardize the stability of LDO regulator. To reduce R_3 , a Class-A embedded driving stage [69] is reported and shown in Fig. 5.2(b). It can provide a reasonable gain with reference to that of the CEDS. More importantly, it provides lower output impedance. Therefore, the parasitic pole associated with the gate of power transistor can be pushed to a higher frequency. The stability of regulator can be easily maintained, but the tradeoff is that the discharging rate for V_3 in Fig. 5.2(b) is limited by the static current source I_{b2} . This causes a large undershoot during the I_L switching. To increase the discharging current for V_3 , a push-pull embedded driving stage [76] is shown in Fig. 5.2(c). With improved sinking design and low output

impedance property, the undershoot can be reduced with respect to that of [69]. However, under limited quiescent biasing condition, due to the simple current-mirror sinking source, the discharging current at the gate of power transistor M_P is still limited. This gives the motivation to find a solution to enhance the sinking action.

(II). Transient-Assisted Embedded Driving Stage

A TAEDS with low output impedance is proposed in Fig. 5.3(a). It comprises a single-ended VI converter formed by the transistor M_2 , the current source I_{b1} and the transimpedance amplifier. This amplifier consists of the transistor M_3 , the super current sink network and the shunt feedback resistor R_Z . The super current sink network consists of the components M_4 , M_5 , R_{X2} , R_{B1} , and C_{X1} . It aims to boost the sinking current to increase the discharging rate for V_3 at the gate of the power transistor. Refer to the current sink network, M_4 and R_{X2} function as an inverting gain stage with a gain of $-g_{m4}R_{X2}$ (g_{m4} is the transconductance of M_4). It amplifies the voltage change (ΔV_1) appearing at node N_1 . C_{X1} performs as a floating battery and couples the amplified

Fig. 5.3 (a) Transient-assisted embedded driving stage. (b) Simplified ac small-signal model of the TAEDS driving stage.

signal from N_4 to N_5 . Meanwhile, a large R_{B1} keeps C_{X1} from being discharged immediately such that a large voltage spike can be generated at the gate of M_5 during the I_L transitions. Through the amplification effect of ΔV_1 from the added gain-enhancement stage (M_4 and R_{X2}), a large momentary current in M_5 is generated. At steady state, V_5 is settled to the bias voltage V_{B1} , which defines the dc bias current of M_5 .

To examine the frequency response of the TAEDS, the ac small-signal model presented in Fig. 5.3(b) is investigated. Assuming $C_{X1} \gg C_{gs5}$, using nodal analysis, the voltage gain for V_4 with respect to V_1 is approximated as

$$K(s) = \frac{v_4}{v_1} \approx \frac{-g_{m4}R_{X2}(1 + C_{X1}R_{B1}s)}{1 + C_{X1}(R_{X2} + R_{B1})s} \quad (85)$$

where R_{X2} serves the dual functions in the form of a bias resistor and a passive load. From (85), there are one left-half-plane (LHP) pole $\{p = 1/[C_{X1}(R_{X2} + R_{B1})]\}$ and one LHP zero $[z = 1/(C_{X1}R_{B1})]$. A small R_{X2} will ensure that they are closely located in this design and tend to cancel each other. Thus, (85) can be simplified as $-g_{m4}R_{X2}$. The resulting coupled signal V_5 will become $v_5 \approx -(g_{m4}R_{X2})v_1$. Turning to the equivalent output impedance of the TAEDS, it can be approximated as follows:

$$R_3(s) \approx \frac{1}{g_{m3}} \left(1 + \frac{R_Z}{R_2} \right) \frac{1 + [C_2 R_2 R_Z / (R_2 + R_Z)]s}{1 + (C_2 / g_{m3})s} \quad (86)$$

where g_{m3} is the transconductance of M_3 . C_2 and R_2 are the output parasitic capacitance and resistance at node N_2 , respectively. Since C_2 is small, the zero and pole in (86) will be located at high frequencies. Therefore, the equivalent low-frequency output impedance can be approximated as $2/g_{m3}$, as R_Z is close to R_2 in this design using 65 nm CMOS technology. As such, a small time-constant ($R_3 C_p$), denoted as τ_p , at the gate of power transistor is established to permit high speed operation.

Based on the assumption of $C_{X1} \gg C_{gs5}$, the gain of TAEDS can be approximated as follows:

$$G(s) \approx \frac{A_{TAEDS} \left(1 + \left[C_2 (g_{m4} R_{X2} g_{m5}) / (g_{m3} g_{m2}) \right] s \right)}{\left(1 + C_p \left(\frac{R_2 + R_Z}{g_{m3} R_2} \right) s \right) \left(1 + \frac{C_2 R_2 R_Z}{R_2 + R_Z} s \right)} \quad (87)$$

where $A_{TAEDS} = (g_{m2} R_Z + g_{m5} g_{m4} R_{X2} / g_{m3})$ is the dc gain of TAEDS. From (87), one LHP zero and two LHP poles exist. The respective pole and zero associated with small C_2 will be located at high frequencies. The other LHP pole due to small τ_p is also located at high frequency. As a result, (87) can be simplified as A_{TAEDS} . In brief, not only does TAEDS support the gain function and low output impedance, it significantly boosts the pull-down current in comparison to that of simple current mirror topology. As a result, the regulator's transient response can be largely improved in a cost-effective solution.

5.3.2. Implementation of the Proposed LDO Regulator

The simplified circuit of TAEDS based OCL-LDO regulator is presented in Fig. 5.4(a). It consists of a FVF based first gain stage, a TAEDS and a power transistor (M_P). Owing to low output impedance and substantial transient pull-down current of the TAEDS, the regulator can work under low supply without severely degrading both the transient and frequency performance metrics. As [75] and [77] have demonstrated the effectiveness of DSMFC for driving wide load capacitance, the DSMFC stage in [77] with the components M_D , C_{m1} , C_{m2} and R_{X1} have been employed in this design.

Despite the TAEDS can significantly reduce the undershoot, the effect on overshoot reduction is small. To tackle the issue, an overshoot reduction block (M_6 , R_{B2} and C_{X2}) has been implemented.

Fig. 5.4 (a) Simplified circuit schematic of the TAEDS LDO regulator, (b) Ac small-signal model of the TAEDS LDO regulator.

(I). Stability Analysis

The stability of feedback loop in the TAEDS based LDO regulator is analyzed using the small-signal model depicted in Fig. 5.4(b). It is obtained by breaking the loop at the output branch of circuit, as shown in Fig. 5.4(a). The loop-gain transfer function is derived as

$$A(s) = \frac{A_{dc} (1 + s/z_1)(1 - s/z_2)}{(1 + s/p_{-3dB})(1 + s/p_2)(1 + as + bs^2)} \quad (88)$$

where

$$A_{dc} = -g_{m1}g_{mp}A_{TAEDS}R_1R_o \quad (89)$$

$$z_1 = -1/(C_{m2}R_d) \text{ and } z_2 = +A_{TAEDS}g_{mp}/C_{m1} \quad (90)$$

$$p_{-3dB} = -\frac{1}{C_{m1}A_{TAEDS}g_{mp}R_1R_o + C_{m2}g_{md}R_1R_d + C_LR_o} \quad (91)$$

$$p_2 = -\frac{C_{m1}A_{TAEDS}g_{mp}R_1R_o + C_{m2}g_{md}R_1R_d + C_LR_o}{C_{m1}C_{m2}A_{TAEDS}g_{mp}R_1R_oR_d + C_{m2}C_Lg_{md}R_1R_oR_d} \quad (92)$$

$$a = C_{m1}C_L / (C_{m1}A_{TAEDS}g_{mp} + C_Lg_{md}) \quad (93)$$

$$b = \left(\frac{C_{m1}C_L}{C_{m1}A_{TAEDS}g_{mp} + C_Lg_{md}} \right) \frac{C_p(R_2 + R_Z)}{g_{m3}R_2} \quad (94)$$

in which R_o is the effective output impedance including the load resistance R_L . C_{m1} is the standard Miller compensation capacitor whereas C_{m2} is the second Miller capacitor for dual-summed function. The deviation is based on the following assumptions: 1) $g_{m1}R_i \gg 1$, $g_{m2}R_Z \gg 1$, $g_{md}R_d \gg 1$; 2) C_L , C_{m1} , C_{m2} and $C_p \gg C_1$, C_2 and C_d .

From (88), there are one LHP zero (z_1), one RHP zero (z_2), two LHP real poles (p_{-3dB} , p_2) and two other real or complex poles, depending on the loading conditions. Since z_2 in (90) will be located at high frequency through the gain enhancement factor A_{TAEDS} , it is negligible in the subsequent analysis. According to different loading conditions, the stability of the regulator is discussed in four cases. Table 5-I lists the corresponding locations of poles and zeros for each case. They are classified as follows:

TABLE 5-1 POLES AND ZERO LOCATIONS IN FOUR CASES

Condition	z_1	p_{-3dB}	p_2	p_3^*	p_4^*
(Case 1) High C_L ; Low I_L	$\frac{-1}{C_{m2}R_d}$	$\frac{-1}{C_L R_o}$	$\frac{-1}{C_{m2}g_{md}R_dR_1}$	$-\left(\frac{A_{TAEDS}g_{mp}}{C_L} + \frac{g_{md}}{C_{m1}}\right)$	$-\frac{g_{m3}R_2}{C_p(R_2 + R_z)}$
(Case 2) High C_L ; High I_L	$\frac{-1}{C_{m2}R_d}$	$\frac{-1}{C_{m1}g_{mp}A_{TAEDS}R_1R_o + C_{m2}g_{md}R_dR_1}$	$-\left(\frac{1}{C_{m2}R_d} + \frac{g_{md}}{C_{m1}A_{TAEDS}g_{mp}R_o}\right)$	$\sqrt{\left(\frac{A_{TAEDS}g_{mp}}{C_L} + \frac{g_{md}}{C_{m1}}\right)\frac{g_{m3}R_2}{C_p(R_2 + R_z)}}$	
(Case 3) Low C_L ; Low I_L	$\frac{-1}{C_{m2}R_d}$	$\frac{-1}{C_{m1}g_{mp}A_{TAEDS}R_1R_o + C_{m2}g_{md}R_dR_1}$	$-\left(\frac{1}{C_{m2}R_d} + \frac{g_{md}}{C_{m1}A_{TAEDS}g_{mp}R_o}\right)$	$\sqrt{\left(\frac{A_{TAEDS}g_{mp}}{C_L} + \frac{g_{md}}{C_{m1}}\right)\frac{g_{m3}R_2}{C_p(R_2 + R_z)}}$	
(Case 4) Low C_L ; High I_L	$\frac{-1}{C_{m2}R_d}$	$\frac{-1}{C_{m1}g_{mp}A_{TAEDS}R_1R_o + C_{m2}g_{md}R_dR_1}$	$-\left(\frac{1}{C_{m2}R_d} + \frac{g_{md}}{C_{m1}A_{TAEDS}g_{mp}R_o}\right)$	$\sqrt{\left(\frac{A_{TAEDS}g_{mp}}{C_L}\right)\left(\frac{g_{m3}R_2}{C_p(R_2 + R_z)}\right)}$	

Case 1: High C_L with Low I_L

Under this condition, the transconductance of M_P (g_{mp}) is small and $R_o \approx 1/g_{m1}$. The transfer function displays a system with four real poles. As indicated in Table 5-I, p_2 is located at a lower frequency than that of z_1 . This contributes partial pole-zero cancellation effect. p_3 will be pushed to a high frequency because of A_{TAEDS} and g_{md} . Finally, the small R_3 in TAEDS stage permits p_4 to be located at high frequency, thus ensuring the stability.

Case 2: High C_L with High I_L

In this case, g_{mp} is very large whilst R_o becomes very small. z_1 tends to cancel p_2 . The complex poles ($|p_{3,4}|$) occur. As a result of small R_3 , high A_{TAEDS} together with an added term (g_{md}/C_{m1}) which is contributed by the DSMFC stage, $|p_{3,4}|$ can be easily shifted beyond the unity gain frequency (ω_{UGF}) to guarantee the stability.

Case 3: Low C_L with Low I_L

p_2 is again nulled by z_1 . With small C_L and R_3 , the complex poles $|p_{3,4}|$ are located at a high frequency. As such, the circuit maintains stable.

Case 4: Low C_L with High I_L

The pole-zero cancellation occurs between z_1 and p_2 . Due to a large g_{mp} and a small C_L , $|p_{3,4}|$ will be located at high frequency, yielding a stable system.

In brief, it can be confirmed from the above discussion that the regulator is able to operate for a wide C_L range whilst simultaneously supporting different levels of I_L .

(II). Dependence of Minimum I_L on Output Resistance of Embedded**Driving Stage (EDS)**

In order to drive a large I_L under low supply, the size or area of power transistor M_P needs to be increased. Consequently, it introduces a large parasitic capacitance (C_p) at the gate of M_P since C_p is proportional to the area of M_P . This turns out that the frequency of parasitic pole (p_4 or $|p_{3,4}|$ shown in Table I) at the gate of M_P is significantly reduced. This may cause the stability issue in the LDO regulator, especially under low power constraint. For Case 1 in Table 5-I, when C_L is very large, ω_{UGF} will be C_L dependent and small. This allows the parasitic poles to be easily located beyond ω_{UGF} without the stability concern. Based on this reason, only the other three cases having complex poles $|p_{3,4}|$ are considered in the subsequent analysis.

Assuming the loop-gain transfer function for the regulator with an EDS can be derived as $A(s)$ in (88). Consider case 2 to case 4 as given in Table 5-I, they are four-pole systems. The location of the complex poles $|p_{3,4}|$ is approximated as

$$|p_{3,4}| \approx \sqrt{\left(A_{EDS}g_{mp}/C_L + g_{md}/C_{m1}\right)\left(1/C_p R_3\right)} \quad (95)$$

where A_{EDS} is the dc gain of the embedded driving stage and R_3 is the output resistance of EDS.

It has revealed from (95) that $|p_{3,4}|$ can be shifted to high frequency by either increasing g_{mp} or reducing R_3 . This implies that a minimum I_L ($I_{L(\min)}$) is required (as reported in [67], [70]). Alternatively, a driving stage with certain small R_3 can be employed for ensuring stability. Therefore, a tradeoff exists between $I_{L(\min)}$ and R_3 .

If it were assumed the second pole (p_2) and the zero (z_1) in the feedback system given in Table 5-I can cancel each other, the phase margin (PM) for the feedback loop in the regulator can be expressed as

$$PM \approx 90^\circ - \tan^{-1} \left[\frac{2\zeta(\omega_{UGF}/|p_{3,4}|)}{1 - (\omega_{UGF}/|p_{3,4}|)^2} \right] \quad (96)$$

where ζ is the damping factor in the second-order system [163].

From (96), to achieve a minimum PM of 45° at $\zeta = 1/\sqrt{2}$ without frequency peak [164], the following condition that $|p_{3,4}| \geq 2\omega_{UGF}$ should be satisfied. Substituting the design condition of $|p_{3,4}|$ in (95), it can be rewritten in the form

$$\sqrt{\left(A_{EDS}g_{mp}/C_L + g_{md}/C_{m1}\right)\left(1/C_p R_3\right)} \geq 2\omega_{UGF} \quad (97)$$

As described in Section 5.3.2-(I), in Case 2 and Case 4 with high I_L in Table 5-I, g_{mp} is large and the complex poles are easily located at high frequencies. On the contrary, g_{mp} is small and the complex poles are located at low frequencies in Case 3. To increase g_{mp} , it implies that $I_{L(\min)}$ is required under this condition. Consider the case 3, the power transistor operates in the sub-threshold region and its transconductance is approximated as

$$\begin{aligned} g_{mp} &\approx I_{M_p} / nV_T \\ &= \left(I_{L(\min)} + I_{QP}\right) / nV_T \end{aligned} \quad (98)$$

where V_T is the thermal voltage, n is the subthreshold slope factor (~ 1.5) [92] and I_{QP} defines the quiescent bias current for M_p . Through (97) and (98), the required $I_{L(\min)}$ for the LDO regulator can be derived as follows:

$$I_{L(\min)} \approx nV_T \left[\left(2\omega_{UGF}\right)^2 C_p R_3 - \frac{g_{md}}{C_{m1}} \right] \frac{C_L}{A_{EDS}} - I_{QP} \quad (99)$$

It can be seen from (99) that a large R_3 will result in a high value of $I_{L(\min)}$ as far as A_{EDS} and other parameters are kept constant. For the TAEDS with a small R_3 ($2/g_{m2}$, as shown in (86)) and a gain parameter $A_{TAEDS} \approx g_{m2}R_Z$, the $I_{L(\min)TAEDS}$ obtained from (99) can be small. Regarding the large R_3 of the CEDS and comparable gain parameter $A_{CEDS} \approx g_{m2}R_3$, the $I_{L(\min)CEDS}$ is relatively high according to (99). Assume $A_{CEDS} \approx$

A_{TAEDS} together with identical ω_{UGF} and quiescent bias for both regulators, the $I_{\text{L(min)}}$ difference between $I_{\text{L(min)TAEDS}}$ and $I_{\text{L(min)CEDS}}$ can be obtained as

$$\begin{aligned}\Delta I_{\text{L(min)}} &= I_{\text{L(min)CEDS}} - I_{\text{L(min)TAEDS}} \\ &\approx nV_T (2\omega_{\text{UGF}})^2 (C_L/A_{\text{EDS}}) C_p (r_{b2} \parallel r_{ds3} - 2/g_{m3})\end{aligned}\quad (100)$$

From (100), it is obvious that the value of $I_{\text{L(min)CEDS}}$ is larger than that of $I_{\text{L(min)TAEDS}}$ due to significantly larger R_3 value.

To compare the required $I_{\text{L(min)}}$ with respect to R_3 between the CEDS LDO regulator and the TAEDS LDO regulator using numerical examples, the circuit analysis and the simulations of R_3 as well as complex poles at node N_3 are conducted. The results are summarized in Table 5-II. With identical ω_{UGF} and I_Q , the approximated $|p_{3,4}|$ locations, the theoretical value of R_3 and $I_{\text{L(min)}}$ for both designs are calculated for $C_L=100$ pF. They are obtained by using the model parameters extracted from the simulation setup. As indicated in Table 5-II, the frequency of the complex poles of TAEDS regulator without $I_{\text{L(min)}}$ is around three times larger than that in CEDS regulator. The simulation results of $I_{\text{L(min)}}$ for both CEDS and TAEDS LDO regulators to achieve a PM of 45° at $C_L = 100$ pF are $120 \mu\text{A}$ and $0 \mu\text{A}$, respectively. This turns out to be almost consistent with the theoretical results ($119 \mu\text{A}$ and $3.5 \mu\text{A}$, respectively). It has confirmed that TAEDS regulator will demand less $I_{\text{L(min)}}$ based on relatively small value of R_3 . This demonstrates that the TAEDS LDO will offer more power-efficient performance. This is regarded as the key technical merit of the TAEDS LDO regulator.

TABLE 5-II COMPARISON OF MINIMAL I_L AND THE RELATED PARAMETERS IN TERMS OF DESIGN EXPRESSION, CALCULATED THEORETICAL RESULTS AND SIMULATION RESULTS BETWEEN THE CONVENTIONAL AND PROPOSED REGULATORS.

Parameter	CEDS LDO			TAEDS LDO		
	Eqn.	Theor.	Sim.	Eqn.	Theor.	Sim.
$ p_{3,4} $ (MHz) at $I_{L(\min)}=0$	(11)	1.4	1.6	(11)	4.3	4.9
A_{EDS} (dB)	$g_{m2}R_3$	18	17.5	$g_{m2}R_Z$	17.9	16
R_3 (k Ω)	$r_{b2} r_{ds3}$	111	109.6	$2/g_{m3}$	10.8	10
$I_{L(\min)}$ (μ A)	(15)	119	120	(15)	3.5	0

(III). Transient Signal Behavior of TAEDS LDO Regulator

The transient signal responses of the TAEDS LDO regulator are illustrated in Fig. 5.5. Refer to Fig. 5.5(a), V_{out} rapidly drops when the I_L increases suddenly. The voltage drop (ΔV_{out}) is sensed and amplified by the embedded driving stage formed by M_2 , M_{b2} , M_3 , M_5 and R_Z . For the combined response at V_3 (ΔV_3), it is a result of two paths propagated from V_1 (ΔV_1). First, ΔV_1 goes through the driving stage for V_3 . Second, ΔV_1 is amplified by the M_4 and R_{X2} . It is then coupled to V_5 , causing the rapid increase in the V_{GS} of M_5 to yield a large transient discharging current (I_d) for V_3 . As a result, V_3 is quickly reduced to enable large I_L through the power transistor stage. At the same time, rapid reduction of V_3 is sensed by the overshoot reduction network and turn off the discharging current through M_6 . Similarly, it is vice versa for the overshoot case as indicated in Fig. 5.5(b). In this case, the rapid increase of V_3 will drive large discharging current through M_6 and reduce the overshoot and settling time.

In order to achieve large current boosting effect without affecting the stability of LDO regulator, the design strategy for the proposed super current sink network in the TAEDS is investigated. This includes the proper sizing of R_{X2} , C_{X1} and R_{B1} . R_{X2} is designed to be small such that M_4 can always operate in the saturation region during I_L

Fig. 5.5 Transient response illustration of the proposed LDO regulator (a) Undershoot (b) Overshoot.

switching. However, R_{X2} needs to be made larger than $1/g_{m5}$ in order to provide voltage gain. The current design employs a R_{X2} of 80 k Ω . From Fig. 5.3, C_{X1} serves as a voltage divider with respect to the parasitic gate capacitance (C_{gs5}) of M_5 . The voltage at the gate of M_5 is approximated as

$$V_5 \approx V_4 \left[C_{X1} / (C_{X1} + C_{gs5}) \right] \quad (101)$$

For efficient coupling, C_{X1} should be made larger than C_{gs5} . On the other hand, as shown in (85), R_{B1} is designed to be larger than R_{X2} so as to achieve a good stability in the TAEDS regulator. Besides, as proved by [67], the corner frequency determined by $1/(C_{X1}R_{B1})$ is designed to meet the necessary condition that

$$0 < 1/(C_{X1}R_{B1}) < \omega_{UGF} \quad (102)$$

Large $C_{X1}R_{B1}$ will lead to longer settling time and better stability whilst small $C_{X1}R_{B1}$ will reduce the ac coupling efficiency and reduce the settling time. Therefore, a tradeoff exists for the choice of C_{X1} and R_{B1} .

In order to ensure that these parameters are designed properly, the simulation is conducted under the condition of $R_{X2}=80 \text{ k}\Omega$ and $C_L=100 \text{ pF}$. Fig. 5.6(a) and (b) depict the simulated results for the phase margin (PM) and gain margin (GM) of feedback loop in the TAEDS LDO regulator, the settling time (t_s) and the undershoot voltage (V_{US}) versus C_{X1} at $R_{B1}=350 \text{ k}\Omega$ and versus R_{B1} at $C_{X1}=700 \text{ fF}$, respectively. It has shown that increasing C_{B1} and R_{B1} reduces V_{US} , however, it leads to a longer t_s . Therefore, C_{X1} and R_{B1} are optimally chosen to be 700 fF and $350 \text{ k}\Omega$. Moreover, the simulation results have confirmed that good PM and GM are achieved under the stated condition. Similarly, C_{X2} and R_{B2} in the overshoot reduction block are designed to be 700 fF and $600 \text{ k}\Omega$, respectively.

5.3.3.Simulation Results and Discussions

The proposed regulator is implemented and simulated using a UMC 65nm CMOS process. Both compensation capacitors C_{m1} and C_{m2} are 4 pF . Powered by a minimum supply voltage of 0.75 V , the output voltage is designed to be 0.5 V . In typical process and at room temperature, it can deliver a maximum I_L of 100 mA with a quiescent current of $24.6 \text{ }\mu\text{A}$. Owing to the DSMFC technique, it is stable with a wide range of C_L ($10 \text{ pF} \sim 10 \text{ nF}$). Fig. 5.7(a), Fig. 5.7(b) and Fig. 5.7(c) show the loop gain and phase responses at $I_L=0, 5 \text{ mA}, 50 \text{ mA}$, and 100 mA for $C_L=10 \text{ pF}, 200\text{pF}$ and 10 nF , respectively. It has validated that the regulator is able to maintain stability for both $C_L=10 \text{ pF}$ and 10 nF at different I_L . The PM and GM over the whole C_L range under

Fig. 5.6 Simulated phase margin, gain margin, settling time and undershoot voltage V_{US} with variation of (a) C_{X1} (b) R_{B1} at $C_L=100pF$.

different I_L at the typical process corner and room temperature is presented in

Fig. 5.8. It has revealed that a minimum PM of 45° and a minimum GM of 6 dB are attained. Fig. 5.9 shows the simulated PSR of the regulator at different loading current at $C_L=100$ pF. It has shown that the regulator achieves a minimum PSR of 40 dB at full load condition.

Fig. 5.7 Simulated loop gain and phase responses at different I_L for (a) $C_L = 10$ pF, (b) $C_L = 200$ pF, and (c) $C_L = 10$ nF.

Fig. 5.8 Simulated PM and GM vs. C_L at different I_L .

Fig. 5.9 Simulated PSR of the regulator at different loading current at $C_L = 100$ pF

Consider the promising applications for ultra-low-power biomedical devices, such as medical sensors or SoC systems which usually require low clock frequencies less than 1 MHz [165]–[167] for digital processing of the low-frequency biomedical signals [159], a 100 ns edge time of load current transition utilized for evaluation of the transient response in this regulator is adequate. The transient responses of regulator are shown in Fig. 5.10(a) and the zoom in plot of the undershoot cases and overshoot cases are shown in Fig. 5.10(b) and Fig. 5.10(c), respectively. When the I_L is switched between 0 and 100 mA in 100 ns, the regulator can settle within 1.35 μ s with 1% accuracy across the whole C_L range. The simulated undershoot and overshoot are 40.4 mV and 28 mV, respectively, when C_L is 100 pF. For other C_L values, the undershoot and overshoot voltages are also small as indicated in Fig. 5.10. Besides, it displays a line regulation and load regulation of 10 mV/V and 27 μ V/mA, respectively.

The performance is further compared with the previously-reported OCL-LDO regulators in Table 5-III. The transient figure-of-merit (FOM) [70], taken into account of edge time of the load current transition, is adopted. It is given by

$$FOM = K \left(\Delta V_{out} \times I_Q \right) / \Delta I_{LOAD} \quad (103)$$

where K is the edge time ratio and given by

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among designs for comparison}} \quad (104)$$

Refer to Table 5-III, the TAEDS regulator with low supply and quiescent current consumption achieves the best transient FOM except for [60] and [70]. However, the designs in [60] and [70] require a high quiescent current and large minimum load current I_L , respectively, which are not favourable to low power applications. In

Fig. 5.10 Transient responses of (a) the proposed LDO regulator at different C_L , (b) the undershoot case at different C_L , and (c) the overshoot cases at different C_L .

particular, the transient FOM improves its counterpart [77] based on simulation results by almost 50% under similar circuit topology and comparable quiescent current. Another key technical merit is that it offers high load capacitance to total on-chip capacitance ratio ($C_{L(max)}/C_T$). This indicates that the additional capacitors, used for sensing transients, do not significantly increase the silicon area whilst yet not deteriorating the settling time. Finally, it displays good results which are comparable or better than the reported designs in terms of load regulation and line regulation.

TABLE 5-III PERFORMANCE COMPARISON WITH REPORTED OCL-LDO REGULATORS

Parameters	[60]	[62]	[65]	[67]	[70]	[72]	[73]	[75] [†]	[76]	[77] [†]		This Work [†]	
Year	2005	2006	2008	2010	2010	2012	2012	2013	2014	2014		2015	
Technology(μm)	0.09	0.18	0.35	0.35	0.09	0.09	0.35	0.065	0.065	0.065		0.065	
V _{IN} (V)	1.2	0.65 -0.95	0.9 -2	0.95 -1.4	0.75 -1.2	1.2	1.2	1.2	0.75 -1.2	1.2		0.75-1	
V _{OUT} (V)	0.9	0.5	0.5	0.7	0.5	1	1	1.0	0.5	1.0		0.5	
I _Q (μA)	6000	12.72	0.103	43	8	408	28	13.2	16.2	23.7		24.6 [#]	
I _{L(min)} (μA)	0	0	0	1000	3000	0	0	0	0	0		0	
I _{L_MAX} (mA)	100	50	50	100	100	100	100	50	50	50		100	
C _T (pF) ¹	600p	N/A	0	6	7	1.6	9	10	2	8		9.4	
C _L (F)	600p	0	0	100p	0-50p	0-1n	0-100p	10p-10n	0-100p	10p-10n		10p-10n	
Settling Time (μs)	N/A	10	400	3	5	N/A	N/A	0.925	1.2	1.65		1.35	
Line Reg. (mV/V)	N/A	3.63	21.76	N/A	3.78	4.3	0.39	217	6.67	8.89		10	
Load Reg. (μV/mA)	1800	376.3	324	N/A	100	3	78.2	133	560	34		27	
ΔI _{LOAD} (mA)	100	50	50	99	97	100	100	50	50	50	49*	100	99*
ΔV _{OUT} (mV)	90	300	320	70	114	35	105	341.6	103	40	25.7*	40.4	28*
Edge Time (μs)	0.0001	4	80	1	0.1	0.01	1	0.5	0.1	0.1	0.1*	0.1	0.1*
Edge Time Ratio K	1	40k	800k	10k	1k	100	10k	5k	1k	1k	1k*	1k	1k*
FOM(mV)	5.4	3053	527.4	67.5	9.4	14	294	450	33.4	19	12*	9.9	6.9*
C _{L(max)} /C _T	1	N/A	N/A	16.7	7.14	625	11.11	1000	50	1250		1064	

[#] The I_{Q} includes the current consumption of the biasing circuit and the OTA control voltage generator [77].

*Transient performance for I_{L} switching between 1 mA and 100 mA.

¹ Total On-chip Capacitance. [†] Simulation Results

5.4 Summary

A low-voltage FVF OCL-LDO regulator with a transient-assisted embedded driving stage is presented. Owing to the proposed super current sink network in the TAEDS LDO regulator, it permits the generation of a large momentary discharge current and provides transient-enhanced slew rate at the gate of the power transistor. The analytical expression relating to the minimum I_L and the output resistance of TAEDS is derived for giving the design insight as well as the tradeoff. The extensive simulation results have demonstrated the reduced undershoot and improved transient FOM when compared with those of counterparts under the constraint of larger load current at low supply. At this juncture, this work is not fabricated. However, the proposed transient-assisted circuit technique will be applied in the regulator with silicon result described in Chapter 6. By employing both DSMFC and transient-assisted circuit techniques, this regulator attains very high $C_{L(\max)}/C_T$ ratio whilst without causing a significant increase of the area. Therefore, the regulator is suitable for low-supply, high-current-drive on-chip applications with a wide C_L range.

Chapter Six

LDO Regulator with Process-Temperature Aware Transient Response

The LDO regulator is dedicated to power management applications where low power, low voltage, low transient spike and sustainability of transient metrics are concerned. To achieve the goal, the aforementioned transient-assisted circuit techniques in conjunction with the multiple feedback circuit topology, the PT-aware power transistor biasing network and the stated constant current source architecture is applied to realize a low-power capacitorless LDO regulator with process-temperature aware transient response in 40nm CMOS technology. Using these combined techniques, a low-voltage performance-aware regulator, which can sustain low undershoot/overshoot voltage, reduce speed degradation, maintain good stability and eliminate the circuit trimming in the context of process-temperature variation and low-quiescent power constraint, is obtained.

6.1 Architecture and Operation Principle of the Proposed PT-aware LDO Regulator

The conceptual block diagram of the proposed PT-aware OCL LDO regulator is shown in Fig. 6.1. It consists of multiple gain stages (g_{m1} , g_{m2} , and g_{m3}) to obtain a relatively high gain for maintaining good DC regulation accuracy. It also includes multiple feedback loops (main feedback loop, transient-assisted feedback loop and auxiliary bulk control loop) to enhance the transient response. In addition, the

Fig. 6.1 Simplified block diagram of the proposed PT-aware OCL LDO regulator.

feedforward path as well as a transient-assisted current sink having dynamic impedance is employed to produce the push-pull characteristics, leading to fast large-signal response. When the auxiliary bulk control and the transient-assisted current sink circuit techniques are applied to the power transistor M_P , this enables the power transistor stage with enhanced transconductance. Regarding the auxiliary bulk control, it is based on the simplification of the reported work [83]. These circuit techniques will be discussed in the subsequent sections.

Of particular interest, it is common to observe that the gate voltage of M_P , V_3 , will vary a lot when coming to the extreme temperature and process corners. Therefore, huge transistor size is employed when aiming to drive large load current. This creates a drawback to the LDO regulator circuit. To tackle the issue, a process-temperature aware bias current (I_{BPT}) is utilized to overcome potential large bandwidth variation of the main feedback loop under the process and temperature variation. This will ensure the loop stability of the feedback system.

At the extreme process corner of slow NMOS, slow PMOS (SS) and low corner temperature (T_L), the V_{TH} magnitude of M_P will increase to yield a small V_3 . It will force the discharging transistor of the third stage to operate in the triode region, thus degrading the loop gain. In view of this fact, the auxiliary bulk control is used to reduce the V_{TH} of M_P which allows more headroom for proper operating condition. Besides, the decrease of transconductance M_P (g_{mP}) and the increase of output resistance increases due to the reduced sink current of M_P will jeopardize the stability at no load condition. Therefore, a compensation current source, I_{BSL} , is added to obtain high g_{mP} and low output impedance for maintaining good stability.

Regarding the case of the extreme process corner of fast NMOS and fast PMOS (FF) and high corner temperature (T_H), the V_{TH} magnitude of M_P will reduce such that

V_3 appears to be very high because of the small V_{SG} induced by the large aspect ratio at no load condition. This will stress the charging network of the third stage by forcing the driving transistor in the triode region, thus creating the possibility of failing the control loop regulation. This drawback can be overcome with the embedded current sensing network and the additional compensation current source, (I_{BFH}), which aim to increase V_{SG} of M_P to counteract this effect.

In summary, through the use of transient-assisted circuit technique together with the multiple feedback circuit topologies that comprises the feedforward path and multiple feedback paths, the PT-aware power transistor biasing network and the stated current source with reduced sensitivity, a low-voltage low-power performance-aware OCL-LDO regulator with transient sustainability under process and temperature variation is achieved.

6.2 Implementation of the Proposed Circuit

The simplified schematic of the regulator is depicted in Fig. 6.2. It comprises a first gain stage with PT-aware transconductance, the second and third stage with transient-assisted feedback and feedforward stage, and a power transistor (M_P) with transient-assisted current sink and PT-aware bias. The load capacitor C_L and the resistor R_L are used to model the parasitic capacitive load from the power line of the subsequent circuit (~ 100 pF) and the output resistive load, respectively. As seen in Fig. 6.2, a relatively small resistor R_{p2} is integrated to serve as a current sensing element for the V_{SG} variation of M_P . Not only does the small resistor aim to generate I_{BFH} as mentioned above, it also helps to push the parasitic pole at node N_3 to high frequency, hence improving the stability of regulator. Due to this sensing resistor, the transconductance of power transistor's driving stage at the full load condition can be enhanced, resulting

Fig. 6.2 Simplified schematic of the proposed PT-aware OCL LDO regulator.

in good regulation. In addition, the load capacitor and the load resistor are used to model the output parasitic capacitive load and the resistive load, respectively.

The main circuit blocks are described and analysed in details in the following subsections.

6.2.1. Process-Temperature Aware Current Source

Fig. 6.3 depicts the simplified schematic of the process-temperature aware current source. Similar to the core circuit of constant current source reported in [140], it relies on a triode based transistor to generate the process-temperature aware current. The current source consists of a core circuit, a process-tracking voltage ($V_{PTTrack}$) bias and an output stage. It is noted that there are two differences from the core in [140]. In this PT-aware current source, a self-biased op-amp is employed to maintain the same voltage at the drain terminal (N_1 and N_2) of the transistor pairs, M_{B1} and M_{B2} in the core circuit. This eliminates the extra bias for the op-amp, allowing low power

Fig. 6.3 Simplified schematic of the process-temperature aware current source.

consumption. Besides, a scaled voltage V_{PTrack} , which is named as $V_{\text{S_PTrack}}$ in Fig. 6.3, is generated through an embedded resistive voltage scaler. This scaling factor, $S=R_1/(R_1+R_2)$, will define the temperature coefficient of the generated current. The analysis is described as follows:

(I). PT-aware Current Source

Refer to [140], assuming the scaling factor $S \approx 1$ to simplify the analysis, the process tracking voltage can be designed to be a temperature independent threshold voltage. It is derived as

$$V_{\text{PTrack}} \approx V_{\text{TH0_MB8}} + 2M\eta \frac{K_{\text{MR1}}}{K_{\text{MB8}}} \frac{k_B T}{q} \ln(N) - \kappa T \approx V_{\text{TH0_MB8}} \quad (105)$$

where $V_{\text{TH0_MB8}}$ is defined as the threshold voltage of M_{B8} at 0 K. As noted, the V_{PTrack} can track the process information. The $T.C.$ can be adjusted by changing the current mirror ratio, M and the ratio of aspect ratio, $K_{\text{MR1}}/K_{\text{MB8}}$.

Refer to Fig. 6.3, since M_{R1} is biased in the triode region, based on the Alpha law MOSFET model [168], the current can be expressed as

$$\begin{aligned} I_0 &\approx \beta_{\text{MR1}} (V_{\text{GS_MR1}} - V_{\text{TH_MR1}})^{\alpha/2} V_{\text{DS_MR1}} = V_{\text{DS_MR1}} / R_{\text{MR1}} \\ &\approx \beta_{\text{MR1}} \eta (V_{\text{S_PTrack}} - V_{\text{TH_MR1}})^{\alpha/2} \frac{k_B T}{q} \ln\left(\frac{K_2}{K_1}\right) \end{aligned} \quad (106)$$

where β_{MR1} is the current factor of M_{R1} and proportional to $(K_{\text{R}}\mu C_{\text{OX}})$. α is the mobility degradation factor. As $V_{\text{S_PTrack}} = S V_{\text{PTrack}}$ (shown in Fig. 6.3), I_0 will exhibit the process aware characteristic.

It has been described in [140] that both V_{TH} and μ are a function of temperature. They are given as

$$V_{\text{TH}}(T) = V_{\text{TH0}} - \lambda T, \text{ and } \mu(T) = \mu(T_r)(T_r/T)^m \quad (107)$$

where V_{TH0} represents the V_{TH} at 0 K, λ denotes the magnitude of coefficient for the temperature term in $V_{TH}(T)$, $\mu(T_r)$ stands for the carrier mobility at room temperature T_r , and m is the temperature exponent of μ .

Therefore, assuming $V_{TH0_MR1} \approx V_{TH0_MB8}$, the $T.C.$ of I_0 in (106) can be obtained as

$$\begin{aligned} TC_{I_0} &= \frac{1}{I_0(T_r)} \frac{\delta I_0}{\delta T} \\ &\approx \frac{1-m}{T} + \frac{(\alpha/2)\lambda}{[(S-1)V_{TH0_MB8} + \lambda T]} \end{aligned} \quad (108)$$

Obviously, it can be seen from (108) that with the aid of the scaling factor, S , the $T.C.$ of generated current can be adjusted to the target value. Similar to the current reference in [169], the $T.C.$ can even be designed to be close to zero in the context of the recent technologies having α approximately equal to 2 but m is less than 2 [96]. The PT-aware bias for the first stage, I_{BPT} , can thus be obtained by copying I_0 using the current mirrors.

(II). PT-aware g_m of the Input Stage

The PT-aware current is applied to bias the first stage of the regulator. To meet low quiescent current demand in the regulator design, the differential input pair in the first gain stage, as shown in Fig. 6.2, will be biased in the subthreshold region. In this biasing condition, the transconductance of input device (M_1), g_{m1} , can be expressed as

$$g_{m1} = \frac{\delta I_{DM1}}{\delta V_{GS}} = \frac{I_{DM1}}{\eta V_T} \quad (109)$$

where I_{DM1} is the drain current of M_1 and V_T is the thermal voltage. Obviously, a PT-aware I_{DM1} can result in a PT-aware g_{m1} . The $T.C.$ of g_{m1} can be derived as

$$g_{m1} = \frac{I_{DM1}}{\eta V_T} = \frac{I_{DM1}(T_r) [1 + \alpha_{ID}(T - T_r)]}{\eta V_T(T_r) [1 + \alpha_{VT}(T - T_r)]} \quad (110)$$

where α_{ID} is the $T.C.$ of I_{DM1} which is equal to that of I_0 . α_{VT} is the $T.C.$ of V_T and it is equal to $(1/T_r)$.

By designing $\alpha_{ID} = \alpha_{VT}$ at room temperature using (108), we have

$$\frac{1}{T_r} = \frac{1-m}{T_r} + \frac{(\alpha/2)\lambda}{[(S-1)V_{TH0_MB8} + \lambda T_r]} \quad (111)$$

Thus, the scaling factor should satisfy the condition as follows:

$$(S-1) = \frac{[(\alpha/2)-m]\lambda T_r}{mV_{TH0}} \quad (112)$$

Therefore, the g_{m1} can be simplified as

$$g_{m1} \approx \frac{I_{DM1}(T_r)}{\eta V_T(T_r)} \quad (113)$$

It can be concluded that with the aid of the PT-aware current bias, the transconductance of the first gain stage can attain good temperature stability whilst providing immunity against the process variation, leading to stable bandwidth for the feedback loop in the LDO regulator.

Fig. 6.4 illustrates the Monte-Carlo simulation results of (a) the DC value of I_{BPT} at room temperature, (b) the $T.C.$ value of I_{BPT} at room temperature, (c) the DC value of g_{m1} under I_{BPT} at room temperature and (d) the plots of g_{m1} as a function of temperature at different process corners under I_{BPT} . The MC simulations are based on 300 runs with 3σ coverage. It can be seen that the I_{BPT} in this work is designed to be $2.3\mu A$ with a small standard variation (σ/μ) of 6%. It has a mean $T.C.$ of 2.8 kppm/ $^{\circ}C$ which is close to that (α_{VT}) of the thermal voltage which is about 3 kppm/ $^{\circ}C$. As noted from Fig. 6.4(c), the obtained g_{m1} under the bias of I_{BPT} is 30.55 μS with a small variation of 5.5%. It is of particularly noted from Fig. 6.4(d) that g_{m1} also achieves

good temperature stability at typical process corner as well as all extreme process corners including fast-fast (FF), and slow-slow (SS) process.

To compare the advantage of this process-temperature aware bias, the performance of the same parameters discussed in Fig. 6.4 under a conventional PTAT bias, I_B [139] are depicted in Fig. 6.5. It can be noted that both the DC variation and the T.C. of I_B turn out to be two times larger in comparison to those of I_{BPT} . This results in a higher variation of g_{m1} around 14.1%, as depicted in Fig. 6.5(c) and a large temperature variation according to Fig. 6.5(d) at different process corners.

Therefore, the simulation results have confirmed the effectiveness of this proposed process-temperature aware bias to sustain the stable bandwidth across the process and temperature corners.

Fig. 6.4 (a) Monte-Carlo simulation results of the DC value of I_{BPT} at room temperature, (b) Monte-Carlo simulation results of the $T.C.$ value of I_{BPT} at room temperature, (c) Monte-Carlo simulation results of the DC value of g_{m1} under I_{BPT} at room temperature, (d) the plots of g_{m1} as a function of temperature at different process corners under I_{BPT} .

Fig. 6.5 (a) Monte-Carlo simulation results of the DC value of I_B at room temperature, (b) Monte-Carlo simulation results of the $T.C.$ of I_B at room temperature, (c) Monte-Carlo simulation results of the DC value of g_{m1} under conventional I_B at room temperature, (d) the plots of g_{m1} as a function of temperature at different process corners under conventional I_B .

6.2.2. Process-Temperature Compensation Current Generator

As indicated in Fig. 6.2, the internal circuit schematic of compensation current sources I_{BFH} and I_{BSL} are depicted in the dotted box of Fig. 6.6(a) and Fig. 6.6(b), respectively. Both the compensation current sources are targeted for stable operation at no load condition. They are analysed in two worse case scenarios as follows:

(I). At FF Process Corner and High Temperature.

In this extreme case, the decreasing in V_{SG} of M_P results in an increase of the nodal voltage V_3 , leading to a reduction of the sensing current I_{p2} . The current is then mirrored by M_{FN1} and the discharging current through M_{FP1} and M_{FN1} reduces in magnitude. The nodal voltage V_{FN1} will then increase to turn on the transistor M_{FN2} so as to generate the compensation current, I_{BFH} . The added I_{BFH} will increase V_{SG} of M_P and reduce V_3 to maintain the proper operation.

As shown in Fig. 6.6(a), the overdrive voltage (V_{OD}) of M_{FN2} can be obtained as

Fig. 6.6 (a) FF process corner and high temperature compensation bias current (I_{BFH}) loop for V_{GSP} compensation. (b) SS process corner and low temperature-compensation bias current (I_{BSL}) generator for output impedance reduction.

$$\begin{aligned}
V_{OD} &= V_{GS_FN2} - V_{TH_FN2} = (V_{IN} - V_{SGFP1}) - V_{TH_FN2} \\
&\approx V_{IN} - \sqrt{\frac{2N_F I_{p2}}{\beta_{FP1}}} - |V_{TH_FP1}| - V_{TH_FN2}
\end{aligned} \tag{114}$$

where β_{MFP1} is the current factor of M_{FP1} and proportional to $(K_{MFP1}\mu C_{OX})$. N_F is the current mirror ratio between M_{FN1} and M_{11} shown in Fig. 6.6(a) and $I_{p2}=V_{SGP}/R_{p2}$.

As implied by (114), since the magnitude of I_{p2} , V_{TH_FP1} , and V_{TH_FN2} exhibit a CTAT characteristic. They will reduce in value when the process corner changes from slow case to fast case, V_{OD} will increase accordingly, leading to high I_{BFH} . Of particular noted, V_{OD} is designed to ensure that $V_{OD} < 0$ at typical condition and room temperature in conjunction with low quiescent design. In this way, the I_{BFH} circuit will draw negligible power at low temperature and fast process corner. Fig. 6.7(a) shows the plots of I_{BFH} as a function of temperature under typical and two extreme process corners. It has revealed that this current will increase when temperature increases and it is dominate in FF corners. It has shown good consistency with the operation theory.

(II). At SS Process Corner and Low Temperature.

In this extreme condition, the I_{BFH} circuit is in the standby condition. As aforementioned in Section 6.1, a I_{BSL} , is generated to sustain high G_{mP} and low output impedance for maintaining good stability.

Refer to Fig. 6.6(b), this current is generated from the V_{GS} of the subthreshold transistor M_{SN1} and a poly resistor R_{S1} having a positive $T.C.$. As reported in [139], V_{SN1} shows a CTAT behaviour and this yields a CTAT current will be generated. In addition, a non-linear current mirror is used to enhance the temperature effect of the output I_{BSL} .

Fig. 6.7 The plots of (a) I_{BFH} (d) I_{BSL} as a function of temperature at different process corners.

From [139], the generated I_{BSL} can be expressed as follows:

$$I_{BSL}(T) = I_{S2}(T) \exp \left\{ \left[I_{S2}(T) R_{12}(T) \right] / (\eta V_T) \right\} \approx \frac{V_{SN1}(T)}{R_{S1}(T)} \exp \left\{ \left[V_{SN1}(T) \frac{R_{S2}(T_r)}{R_{S1}(T_r)} \right] / (\eta V_T) \right\} \quad (115)$$

Obviously, I_{BSL} exhibits a CTAT characteristic and increases when the process changes to slow-slow corner. As such, this current will achieve the stability at the low temperature and slow process.

Of particularly noted, to maintain the low power constraint at the high temperature and fast-fast process corner case, a self-biased threshold and temperature sensing device, M_{SP1} , is applied to serve as a switch to control the I_{BSL} circuit. The circuit is designed to be disabled at typical condition and room temperature. In this case, V_{SG} of M_{SP1} is so small that it disables the bias current, I_{B2} , thus turning off M_{SN1} as well as I_{BSL} . The I_{BSL} circuit will maintain in standby condition even at high temperature and fast process corner. On the contrary, under the slow process corner and low temperature, the increase of V_{SG} of M_{SP1} increases and the decrease of V_{SP1} as noted in Fig. 6.6(b) enables I_{B2} . As a consequence, V_{SN1} increases and the I_{BSL} circuit turns on to maintain low output impedance and good stability of the regulator.

The plots of I_{BSL} as a function of temperature under typical and two extreme process corners are depicted in Fig. 6.7(b). It can be seen that I_{BSL} mainly operates in the low temperature cases and is easily enabled at SS process corner. It maintains a negligible current level from the room temperature up to the extreme high temperature corner, pertaining to the low quiescent design.

6.2.3. Power Stage with Transient-assisted Current Sink

Fig. 6.8 Simplified schematic of (a) power transistor with transient-assisted current sink (b) ac small-signal model.

Fig. 6.8(a) depicts the schematic of power transistor stage with the transient-assisted current sink and the output load comprising R_L and C_L . As aforementioned in Section 6.1, the auxiliary bulk control is applied to M_P to mitigate the degradation effect from the potential low V_3 at the extreme slow process corner and low temperature at full load condition. With the bulk control, the magnitude of V_{TH} of M_P can be modified as follows:

$$|V_{TH_MP}| \approx |V_{TH_MP}|_{V_{SB}=0} - \gamma \left[\sqrt{2\phi_F + V_{SB_MP}} - \sqrt{2\phi_F} \right] \quad (116)$$

where γ is the body-effect constant and ϕ_F is the Fermi potential [170]. From (116), with the auxiliary bulk control, the V_{TH} magnitude can be reduced, thus counteracting the stability degradation effect arising from high V_{GS_MP1} in the extreme worst case. Moreover, with this auxiliary bulk control loop, the output impedance can be further reduced. The analysis is conducted as follows:

Fig. 6.8 (b) shows the simplified ac small-signal model in which M_{13} and M_{14} are treated as a current buffer. Based on the small-signal model shown in Fig. 6.8(b) and assuming $C_{n1} \gg C_{gsn1}$, the transfer function from V_3 to V_{OUT} can be obtained as

$$\frac{v_o}{v_3} = -\frac{R_O G_{mP}(s)}{1 + s C_L R_O} = -\frac{R_{ONB}}{g_{mbP} R_{ONB} + 1} \frac{g_{mP} \left[1 + s C_{n1} R_{n1} \left(A_{cb} g_{mn1} / g_{mP} + 1 \right) \right]}{\left(1 + s C_{n1} R_{n1} \right) \left(1 + s \left[R_{ONB} C_L / (g_{mbP} R_{ONB} + 1) \right] \right)} \quad (117)$$

where G_{mP} denotes the equivalent transconductance of power transistor stage with the transient-assisted current sink. g_{mP} is the transconductance of power transistor M_P and g_{mbP} denotes the transconductance due to the local bulk control of M_P . g_{mn1} is the transconductance of M_{n1} . A_{cb} is the current gain of the current buffer which is defined as $A_{cb} \approx I_{M14}/I_{M13}$. R_O represents the equivalent output resistance and R_{ONB} is the output resistance without bulk control loop. C_{n1} is the coupling capacitor for ac signal whereas R_{n1} is the resistor that passes the DC biasing voltage.

For the design consideration, since M_P will operate in the subthreshold region at no load condition, the bias current I_B will be a PTAT current source [139] to compensate the g_{mP} . It is noted that the current buffer (M_{13} , M_{14} , R_{S1} , and R_{S2}) is a non-linear current mirror with bulk control. From [139], the current gain A_{cb} can be expressed as

$$\begin{aligned} A_{cb} &= K_C \exp \left\{ \left[I_{M13}(T) R_S(T) + (V_{TH_M13} - V_{TH_M14}) \right] / (\eta V_T) \right\} \\ &\approx K_C \exp \left\{ \left[V_{RS}(T) + \gamma \left(\sqrt{2\phi_F + k_s V_{RS}(T)} - \sqrt{2\phi_F - V_{RS}(T)} \right) \right] / (\eta V_T) \right\} \end{aligned} \quad (118)$$

in which $K_C = K_{M14}/K_{M13}$ and $k_s = R_{S1}/(R_{S1}+R_{S2})$. V_{RS} is the voltage drop across the total source resistor, $(R_{S1}+R_{S2})$. As revealed from (118), A_{cb} is enhanced with the help of nonlinear current buffer having the bulk control on M_{14} . It allows a small I_B and K_C when compared to that of the conventional current mirror design, leading to low-power and area-efficient design.

Refer to (117), the G_{mP} of power transistor stage with transient-assisted current sink can be derived as

$$G_{mP} \approx \frac{g_{mP} \left[1 + sC_{n1}R_{n1} \left(A_{cb}g_{mn1}/g_{mP} + 1 \right) \right]}{(1 + sC_{n1}R_{n1})} \quad (119)$$

It can be seen from (119) that the transconductance of power transistor is enhanced owing to the transient-assisted technique. This implies that a higher g_m is obtained when the frequency increases. Even though a pole exists at $1/(C_{n1}R_{n1})$, the LHF zero can partially cancel this pole, contributing the reduction effect on the magnitude of G_{mP} . Of particularly noted that when the operating frequency, ω , satisfies the condition defined as $\omega \gg 1/(C_{n1}R_{n1})$, G_{mP} will become $(A_{dc}g_{mn1} + g_{mP})$. As a result, the transient response will be benefited from the enhancement of g_{mP} .

In addition, as noted from (117), the equivalent output resistance becomes

$$R_O = \frac{R_{ONB}}{g_{mbP}R_{ONB} + 1} \quad (120)$$

It can be observed that the output resistance is reduced due to the auxiliary bulk control feedback loop. This reduction will help the stability of the main feedback loop.

In the following simplified analysis, the equivalent output stage with an effective transconductance (G_{mP}) and an output resistance (R_O) will be employed.

6.2.4. Stability Analysis

Fig. 6.9 depicts the simplified ac small-signal model of the proposed LDO regulator. The stability of main feedback loop is analysed using this model through breaking the loop at input stage of regulator circuit as depicted in Fig. 6.2. The assumptions for this deviation are based on the conditions that: i) $g_{mi}R_i \gg 1$, $g_{mFF}R_P \gg 1$, and $g_{m2P}R_2 \gg 1$; ii) $C_L, C_{n1}, C_{p1}, C_{m1}, C_{m2}$, and $C_P \gg C_{i1}, C_1, C_2, C_{gs2P}$, and C_{gsn1} . iii) the higher-order parasitic poles are located in very high frequency and they are negligible for the analysis.

The loop-gain transfer function is derived and expressed in (121), where R_O is the effective output impedance (120). C_{m1} is the main compensation capacitor and C_{m2} is the compensation capacitor for damping factor control. C_{n1}, R_{n1} and C_{p1}, R_{p1} are the RC network components in the transient-assisted loop. g_{mi} represents the transconductance of each stage. C_i and R_i are the equivalent output parasitic capacitor and resistor of each gain stage, respectively. g_{mCB} is the transconductance of current buffer device, M_6 , in Fig. 6.2.

As noted from (121), there are four LHP zeros, z_1, z_2, z_3 and z_4 , which are given in (123). The two real poles, p_{-3dB} and p_2 are shown in (124) whereas the remaining two poles, which are either real poles or complex poles, depends on the load conditions. The stability of regulator is discussed in two scenarios as follows:

(I). Low I_L

Under this condition, p_2 is cancelled by z_1 . The open-loop gain transfer function is simplified as

Fig. 6.9 Simplified ac small-signal model of the PT-aware LDO regulator.

$$A(s) \approx \frac{A_{DC} (1 + sC_{n1}R_{n1})(1 + sC_{p1}R_{p1})(1 + sC_{m2}R_{m2}) \left(1 + s \frac{C_{m1}g_{mFF}}{g_{mCB}g_{m2N}g_{m3}R_2}\right)}{(1 + sC_{m1}g_{m2N}g_{m3}G_{mP}R_1R_2R_3R_O)(1 + sC_{n1}R_{n1})(1 + as + bs^2)} \quad (121)$$

in which,

$$A_{DC} = -Kg_{m1}g_{m2N}g_{m3}G_{mP}R_1R_2R_3R_O \quad (122)$$

$$z_1 = -\frac{1}{C_{n1}R_{n1}}, z_2 = -\frac{1}{C_{p1}R_{p1}}, z_3 = -\frac{1}{C_{m2}R_{m2}}, \text{ and } z_4 = -\frac{g_{mCB}g_{m2N}g_{m3}R_2}{C_{m1}g_{mFF}} \quad (123)$$

$$p_{-3dB} = -\frac{1}{C_{m1}g_{m2N}g_{m3}G_{mP}R_1R_2R_3R_O}, \text{ and } p_2 = -\frac{1}{C_{n1}R_{n1}} \quad (124)$$

$$a \approx \begin{cases} C_L \left(\frac{C_3R_3 + C_{n1}R_{n1}}{C_Ag_{m2N}g_{m3}G_{mP}R_2R_3R_{n1}} + \frac{C_{m2}K}{C_{m1}G_{mP}} \right) + C_{m2} \left(\frac{C_{p1}(g_{m2P} + g_{m2N})R_{m2}R_{p1}}{C_{n1}g_{m2N}R_{n1}} + \frac{C_{p1}R_{p1}K}{C_{m1}G_{mP}R_O} \right) + \\ \left(\frac{C_3}{g_{m2N}g_{m3}G_{mP}R_2R_O} + \frac{C_{p1}(g_{m2P} + g_{m2N})R_{p1}}{g_{m2N}} \right) \end{cases} \quad (125)$$

$$b \approx C_L \left(\frac{C_{p1}R_{p1} + C_3R_3 + C_{m2}R_{m2}}{g_{m2N}g_{m3}G_{mP}R_2R_3} + \frac{C_3C_{p1}R_{p1}}{C_{n1}g_{m2N}g_{m3}G_{mP}R_{n1}R_2} + \frac{C_{m2}C_{p1}R_{p1}K}{C_{m1}G_{mP}} \right) + \frac{C_3C_{p1}R_{p1}}{g_{m2N}g_{m3}G_{mP}R_2R_O} + \frac{C_{m2}C_{p1}R_{p1}R_{m2}(g_{m2P} + g_{m2N})}{g_{m2N}} \quad (126)$$

$$Q = \frac{\sqrt{b}}{a} \approx \frac{C_{n1} C_{m1} R_{n1} \sqrt{g_{m2N} g_{m3} G_{mP} R_3 R_O (C_{p1} C_L R_O R_{p1} + C_3 C_L R_3 R_O + C_3 C_{p1} R_3 R_{p1}) R_2}}{\left\langle R_{n1} \left\{ C_{n1} C_{m1} \left[C_{p1} (g_{m2P} + g_{m2N}) g_{m3} G_{mP} R_{p1} R_2 R_3 R_O + R_O C_L + C_3 R_3 \right] + C_{n1} C_{m2} g_{m2N} g_{m3} R_3 (R_O C_L + C_{p1} R_{p1}) K R_2 \right\} + \right. \\ \left. C_{m1} R_O R_3 \left[C_{m2} C_{p1} (g_{m2P} + g_{m2N}) g_{m3} G_{mP} R_{m2} R_{p1} R_2 + C_3 C_L \right] \right\rangle} \quad (127)$$

$$A(s) \approx \frac{A_{DC} (1 + sC_{p1}R_{p1})(1 + sC_{m2}R_{m2}) \left(1 + s \frac{C_{m1}g_{mFF}}{g_{mCB}g_{m2N}g_{m3}R_2} \right)}{(1 + sC_{m1}g_{m2N}g_{m3}G_{mP}R_1R_2R_3R_O)(1 + as + bs^2)} \quad (128)$$

As G_{mP} is not high enough, which results in the case of $(a^2 - 4b) < 0$ in the second-order term of (128). This implies that a pair of complex poles $|p_{3,4}|$ exists in this case. Equating the second-order term in (128) with a standard second-order linear system gives

$$1 + as + bs^2 = 1 + \frac{1}{Q} \left(\frac{s}{\omega_o} \right) + \left(\frac{s}{\omega_o} \right)^2 \quad (129)$$

where Q denotes the quality factor and is defined as $Q = 1/(2\zeta)$, in which ζ is the damping factor which determines the damping behaviour of the system. ω_o is the complex pole frequency. Using (129), it is obtained as

$$\omega_o \approx \sqrt{\frac{1}{b}} \quad (130)$$

It can be observed from (126) that with enhanced G_{mP} , small R_3 , relatively small C_L , and the added R_{n1} and C_{n1} , the complex pole can be located at a high frequency. This ensures the circuit stability.

Besides, the Q factor can be expressed from (129) as follows:

$$Q \approx \frac{1}{a} \times \frac{1}{\omega_o} = \frac{\sqrt{b}}{a} \quad (131)$$

Substituting (125) and (126) into (131), the Q factor can be approximated to be (127) and simplified as

$$Q = \frac{\sqrt{b}}{a} \approx \frac{\sqrt{k_{n1}}}{k_{d1}(k_{d2} + C_{m2}) + k_{d3} \frac{(C_{m2}R_{m2} + k_{d4})}{C_{n1}R_{n1}}} \quad (132)$$

where k_{n1} , k_{d1} , k_{d2} , k_{d3} , and k_{d4} are the parameters independent of R_{m2} , C_{m2} , C_{n1} and R_{n1} .

It can be seen from (132) that a high $R_{m2}C_{m2}$ product, a small $R_{n1}C_{n1}$ product can reduce the Q factor of the LDO regulator system.

(II). High I_L

In this case, G_{mP} turns out to be quite high. The condition of $(a^2-4b) > 0$ in the second-order term of (128) indicates that two real poles exist in this condition. The pole-zero cancellation occurs between z_1 and p_2 . The transfer function can then be simplified as

$$A(s)\Big|_{\text{High } I_L} \approx \frac{A_{DC} \left(1 + \frac{s}{z_2}\right) \left(1 + \frac{s}{z_3}\right) \left(1 + \frac{s}{z_4}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right) \left(1 + s \frac{C_{p1}(g_{m2P} + g_{m2N})R_{p1}}{g_{m2N}}\right) (1 + sC_{m2}R_{m2})} \quad (133)$$

As shown in (133), the two additional poles, $p_3 = g_{m2N}/[C_{p1}R_{p1}(g_{m2N} + g_{m2P})]$ and $p_4 = 1/(C_{m2}R_{m2})$ occur. It can be seen that p_3 and p_4 can be canceled by z_2 and z_3 , respectively. As a result, (133) can be simplified to be a one pole system with a LHP zero, z_4 and expressed as

$$A_S(s)\Big|_{\text{High } I_L} \approx \frac{A_{DC} (1 + s/z_4)}{(1 + s/p_{-3dB})} \quad (134)$$

Due to the relatively small g_{mFF} and enhanced g_{m3} in the high load condition, z_4 will be located beyond the unity-gain frequency (UGF) of the feedback loop. Therefore, this one pole system will provide good stability.

In summary, the LDO regulator can maintain good stability under different load currents. Fig. 6.10(a), Fig. 6.10(b) and Fig. 6.10(c) illustrates the loop gain and phase at different I_L levels including 0mA, 1 mA, 10 mA, and 100 mA at process and temperature corners of SS and -20 °C, TT and 25 °C, and FF and 80 °C, respectively. It

Fig. 6.10 Simulated ac response at $C_L=100\text{pF}$ under different load current levels and extreme process and temperature corners of (a) SS and -20°C , (b) TT and 25°C , and FF and 80°C .

TABLE 6-I SUMMARY OF THE AC PARAMETERS AT THE EXTREME PROCESS CORNERS UNDER DIFFERENT TEMPERATURES.

Parameter		-20 °C			25 °C			80 °C		
		SS	TT	FF	SS	TT	FF	SS	TT	FF
AC parameters of Regulator with PT-aware Technique	UGF (MHz)	1.52	1.65	1.74	1.8	1.75	1.85	1.73	1.77	1.89
	Phase Margin(Degree)	69.57	62.5	58.97	54.2	61.04	62.19	63.5	65.57	66.34
	Gain Margin(dB)	10	7.1	14	4	3.4	8	5.4	9.4	14.5
	DC Gain (dB)	65.35	61.8	56.96	62.1	58.66	54.31	57.89	54.97	50.78
	$g_{m1}(\mu S)$	28.26	29.91	31.73	29.08	30.54	32.28	28.95	30.41	33.09
AC parameters of Regulator without PT-aware Technique	UGF (MHz)	0.94	1.31	1.7	1.23	1.7	2.14	0.724	0.871	0.506
	Phase Margin(Degree)	26	23.5	19	14.1	25	15	11.9	15	35
	Gain Margin(dB)	3.4	4	2.6	1.7	2.7	2	3.6	5	15
	DC Gain (dB)	65	61.6	58	62	59.0	55	45.33	41	22.3
	$g_{m1}(\mu S)$	18	24.9	35.3	23.2	31.3	44	29.9	40.53	59.54

has validated that the regulator operates well at different I_L in the context of process and temperature variation. More importantly, the ac parameters such as UGF, PM, GM, DC loop gain, and g_{m1} of the first gain stage of the regulator with PT-aware technique and without PT-aware technique at the extreme process corners and temperatures are summarized in Table 6-I. It has confirmed that the proposed regulator is able to maintain stable UGF because of stable g_{m1} . It also achieves good PM and relatively high DC loop gain, leading to good stability in the feedback loop and high regulation accuracy comparing to the one without the PT-aware technique. Besides, the transient simulation results of the regulator for the load step transition between 0 and 100mA with and without PT-aware technique at the extreme process corners are shown in Fig. 6.11. It can be seen from Fig. 6.11 (a) that without the PT-aware technique at corner of SS and -20 oC, the undershoot is higher due to the slow response. Besides, the settling time is larger due to the poor PM. On the other hand, at the corner of FF and 80 oC shown in Fig. 6.11(b), the load regulation and undershoot is degraded due to the loop gain reduction without PT-aware technique. The simulation results with PT-aware technique have confirmed that the proposed regulator maintains a stable transient performance and load regulation for both corners.

Fig. 6.11 Transient simulation results of the regulator for the load step transition between 0 and 100mA with and without PT-aware technique at the extreme process corners of (a) SS and -20°C, and (b) FF and 80 °C.

6.3 Results and Discussions

This regulator is designed and fabricated using the TSMC 40nm CMOS technology. This Section presents the simulation results and measurement results of the proposed LDO regulator. The performance comparison with the reported state-of-art works will also be discussed.

6.3.1. Measurement Results

The chip micrograph of this regulator is depicted in Fig. 6.12. This regulator occupies an active area of 0.096mm^2 , where the power transistor area is 0.018mm^2 . It is noted that with a total on-chip capacitor of around 1.56 pF, in which the main compensation capacitor C_{m1} is only of 1 pF, the regulator can operate stably over different load current levels. The second compensation capacitor C_{m2} is 60 fF with R_{m2} of 200 k Ω . In the transient-assisted loop, R_{p1} and C_{p1} is 240 k Ω and 150 fF, respectively. Besides, R_{n1} and C_{n1} is 369 k Ω and 353.5 fF, respectively. The sensing resistor R_{p2} is about 30 k Ω . The regulator is measured using an external reference voltage over a temperature range from -20 °C to 80 °C with an effective C_L of 100 pF. The output voltage is regulated to be 0.55 V under a supply voltage down to 0.75 V. The dropout voltage is 200 mV when delivering a maximum I_L of 100 mA at the corner temperature of -20 °C. At room temperature, it consumes an average quiescent current of 26 μA over the measured 12 samples, having the minimum I_Q of 22 μA and maximum I_Q of 36 μA . Targeting for the low-power applications, like the medical SoC systems whose clock frequencies are as low as few MHz [165]–[167], a 200 ns edge time of load current step transition from 0 mA to 100 mA is used for evaluation of the load transient variation of this regulator.

Fig. 6.12 Chip microphotograph of the LDO regulator.

Due to the transient-assisted techniques, the auxiliary bulk control and the PT-aware power transistor biasing network, the regulator can guarantee a relatively small load transient voltage variation (ΔV_{OUT} , maximum voltage of undershoot/over shoot voltage) across a wide temperature range and different chips. The distribution of the load transient variations for the measured 12 chips is summarized in Fig. 6.13. It has shown that at room temperature, the regulator has achieved a small ΔV_{OUT} with a mean value of 23.9 mV and a standard deviation of 1.7 mV. When the temperature reduces to be -20 °C, the average value of ΔV_{OUT} turns out to be 26.4 mV with a standard deviation of 3.8 mV. At the high corner temperature of 80 °C, the average value of ΔV_{OUT} is 26.8 mV and the standard deviation is 2.5 mV. The relatively small ΔV_{OUT} for all three cases have demonstrated that this LDO regulator shows a process-temperature aware transient sustainability despite of the changes in process and temperature. The quiescent current (I_Q), the load regulation (LDR) and the settling time (t_{set}) which

(a)

(b)

(c)

Fig. 6.13 Distribution of the load transient voltage variations of the measured 12 regulator samples under different temperatures.

TABLE 6-II SUMMARY OF THE QUIESCENT CURRENT, LOAD REGULATION AND SETTLING TIME OF THE MEASURED 12 LDO REGULATOR SAMPLES AND SIMULATED RESULTS UNDER DIFFERENT TEMPERATURES.

Parameter		-20 °C		25 °C		80 °C	
		mean	sigma	mean	sigma	mean	sigma
Measured. Results	I_Q (μ A)	49.9	6.4	26	4	37	6.4
	LDR (μ V/mA)	7.5	2.3	11.9	3.1	12.6	2.2
	t_{set} (ns)	444.3	26	414	21	518	43
Simulated Results	I_Q (μ A)	45	22	33	9.9	56	15
	LDR (μ V/mA)	5.95	1.0	8.4	1	11.5	1.2
	t_{set} (ns)	445	12	398	7.4	346	4

takes into account of 1% accuracy of the finally settled output voltage, are summarized in Table 6-II. It is noted that this regulator can maintain a small LDR as well as settle down at about 500 ns at the corner temperature cases under a relatively low quiescent current. This has implied that a stable operation under process and temperature variations.

In addition, the load transient performance of one representative chip at different load current steps and temperatures under supply voltage of 0.75V is evaluated. Fig. 6.14(a), Fig. 6.14(b), and Fig. 6.14(c) show the load transient reponses of regulator for the load current step from 0 mA to 100 mA in 200 ns at -20 °C, 25 °C, and 80 °C, respectively. It can be observed that the regulator operates well across the temperature range whilst sustaining a small undershoot voltage (21mV, 23.5mV, and 21.3mV) and overshoot voltage (26 mV, 23.7 mV, and 25mV). The load transient responses at different temperatures are also measured for the load current step from 1mA to 100 mA. The results at -20 °C, 25 °C, and 80 °C are depicted in Fig. 6.14(d), Fig. 6.14(e) and Fig. 6.14(f), respectively. It has revealed that the transient voltage variations are consistency small in these cases. The obtained overshoot voltages are 26mV, 17.8mV, and 24mV whereas the undershoot voltages are 19.9mV, 13.4 mV, and 14.6 mV under three different temperatures.

Fig. 6.14 Load transient responses of the regulator at different load current steps and temperatures under 0.75V supply voltage.

Fig. 6.15 Load transient responses of the regulator at different load current steps and temperatures under 0.9 V supply voltage .

Fig. 6.16 Line transient responses of the regulator under different load current levels.

Fig. 6.15 illustrates the corresponding load transient response at two different load current steps and three temperatures when the supply voltage is increased to 0.9V. It has shown that the transient ΔV_{OUT} reduces in a higher supply voltage owing to the increased drain-source voltage of the power transistor. It is noted from Fig. 6.15(c) that when the current is switched from 0 mA to 100 mA in the T_H (80 $^{\circ}$ C) case, the ΔV_{OUT} slightly increases. This is due to the g_{mP} reduction caused by the increased leakage current of the bulk diode arising from the reduced V_{TH} at high temperature. However, this ΔV_{OUT} is still considerably small. In view of this effect, the voltage supply will be limited to 0.9 V for this work.

The line transient response of regulator is also measured under different load current levels. As shown in Fig. 6.16, the supply voltage is switched from 0.75 V to 0.9 V in 10 μ s under both (a) $I_L = 0$ mA and (b) $I_L = 1$ mA. It can be seen that the voltage variations for both cases are small and no voltage spikes occur. The line regulations for case (a) and (b) in Fig. 6.16 are 5.6 mV/V and 6.5 mV/V, respectively.

Fig. 6.17 The measured PSR of regulator under different load current levels.

Fig. 6.17 shows the plots of the measured PSR of the output voltage at different load current conditions. It can be observed that the regulator has achieved a minimum PSR of 49.9 dB at 100 Hz and 49.1 dB at 1kHz under the full load condition. The PSR at no load condition is around 51.6 dB at 100 Hz and 51.5 dB at 1kHz.

The output noise measurement is conducted using the Agilent 4395A network analyser and the measured result is depicted in Fig. 6.18. It has revealed that the output noise is about -90dBm/Hz at 10Hz, -129.2dBm/Hz at 100kHz. This corresponds to $7.07 \mu\text{V}/\sqrt{\text{Hz}}$ at 10Hz and $77.5 \text{ nV}/\sqrt{\text{Hz}}$ at 100kHz. They are considered reasonably small.

Fig. 6.18 Output noise of regulator under no load condition.

Furthermore, the transient figure-of-merit (FOM) [70] expressed in (103) of Section 5.33, which is based on the edge time effect of the load current transition, is applied to evaluate the load transient performance in comparison to the reported state-of-art OCL-LDO counterparts. The performance comparison between the representative chip and the previously-reported OCL-LDO regulators at room temperature is summarized in Table 6-III. It can be seen that this regulator has achieved the smallest load transient voltage variation, ΔV_{OUT} , with respect to other works while the regulator gives a comparable FOM value.

Finally, the distribution of the FOM for the measured 12 samples at different temperatures is illustrated in Fig. 6.19. It has shown that this regulator attains a small average FOM value of 12.6 mV with a standard deviation of 1.9 mV at room temperature. The average FOM value at -20 °C is about 26 mV with a standard

Fig. 6.19 Distribution of the transient FOM for the measured 12 samples at different temperatures.

deviation of 3.7 mV. At 80 °C, the obtained mean FOM value is 19.8 mV and the

standard deviation is 3.6 mV. Despite there is a change on the FOM value at corner temperature, they are still comparable with majority of the reported works in Table 6-III. This has validated the transient sustainability of the proposed regulator under process and temperature variation.

TABLE 6-III PERFORMANCE COMPARISON WITH REPORTED OCL-LDO REGULATORS

Parameters	[60] JSSC	[65] ASSCC	[67] JSSC	[70] JSSC	[73] TCASI	[85] TCASI	[84] JSSC	[83] TCASI	[81] TCASI	This Work
Year	2005	2008	2010	2010	2012	2013	2014	2014	2016	2017
Technology(μm)	0.09	0.35	0.35	0.09	0.35	0.065	0.065	0.13	0.5	0.04
V_{IN} (V)	1.2	0.9 -2	0.95 -1.4	0.75 -1.2	1.2	1.2	0.75-1.2	1.2	2.3-5.5	0.75-0.9
V_{OUT} (V)	0.9	0.5	0.7	0.5	1	1	0.55	1	1.2-5.4	0.55
I_{Q}(μA)	6000	0.103	43	8	28	0.9	15.9	99.04	40	23.7[#]
$I_{\text{L(min)}}$(μA)	0	0	1000	3000	0	0	0	1000	0	0
$I_{\text{L MAX}}$(mA)	100	50	100	100	100	100	50	5	150	100
C_{T} (pF)¹	600p	0	6	7	9	4.5	4.1	N/A	29	1.56
C_{L} (F)	600p	0	100p	50p	100p	100p	470p-10n	0	470p	100p
Settling Time (μs)	N/A	400	3	5	N/A	6	0.25	0.16	N/A	0.42
Line Reg. (mV/V)	N/A	21.76	N/A	3.78	0.39	4.7	4	N/A	0.06	5.6
Load Reg. ($\mu\text{V}/\text{mA}$)	1800	324	N/A	100	78.2	300	180	22k	1	12.5
ΔI_{LOAD} (mA)	100	50	99	97	100	100	50	5	150	100
ΔV_{OUT} (mV)	90	320	70	114	105	68.8	113	50	120	23.7
Edge Time (μs)	0.0001	80	1	0.1	1	0.3	0.1	0.2	1	0.2
Edge Time Ratio K	1	800k	10k	1k	10k	3k	1k	2k	10k	2k
FOM(mV)	5.4	527.4	67.5	9.4	294	1.9	36	1981	400	11.2

[#] The I_{Q} includes the current consumption of the biasing circuit.

¹ Total On-chip Capacitance.

6.4 Summary

A low-voltage output-capacitorless LDO regulator having process-temperature aware transient sustainability in 40nm CMOS technology is presented. It employs a new PT-aware current source as mentioned in Chapter 3 as well as a novel PT-aware power transistor biasing network to sustain the stability in the context of process and temperature variation. Besides, the transient-assisted circuit technique as mentioned in Chapter 5, the multiple feedback circuit topology on the basis of feedforward path as well as several feedback paths and the auxiliary bulk control loop enable the design of fast-transient LDO regulator under the condition of low quiescent power and zero minimum load current. More importantly, this regulator can sustain low undershoot/overshoot voltage, maintain good stability and eliminate the circuit trimming. It is particularly suitable for the power management IC applications where low power, low voltage, low transient spike and sustainability of transient metrics are concerned.

Chapter Seven

Conclusions and Future Works

This Chapter gives the concluding remarks of this research work and the recommendations for the future works.

7.1. Conclusions

A review of the background information and several PVT-aware circuits for power management applications is conducted. The non-ideal effects arising from the device scaling in advanced nanometer CMOS technology increase the difficulty in the design of robust circuits, especially for strong immunity against PVT variations. This project has addressed the above issues.

A new V_{TH} reference circuit having high PSR in 65nm CMOS is designed, analyzed and verified in silicon prototype. A new dual temperature compensation method is devised to reduce the $T.C.$ of threshold sensing output voltage. With the use of a pre-regulator loop, a high PSR is thus obtained, leading to good line sensitivity. In addition, the measured results are better than all the reported nanometer based voltage references whilst comparable with V_{TH0} reference counterparts using long channel-length technologies.

Similarly, the prior-art works using different circuit methods to realize a stable I_{REF} circuit are reviewed. This work presents a new current source architecture which is based on the embodiment of a process-tolerant bias current circuit and a scaled process-tracking bias voltage source for the dedicated temperature-compensated

voltage-to-current (VI) conversion. The measurement results have shown that the current source shows a better FOM than most of the reported works.

On top of that, a new electrical model is proposed to predict the stress effect that causes the impact on the electrical performance of reference circuits. The Monte-Carlo simulation results have validated that there is a reasonable correlation between the model prediction results and the measurement results obtained from the proposed voltage and current reference circuits.

The circuit techniques for fast transient OCL-LDO regulators are investigated. A transient-assisted driving stage is proposed to enhance the slew rate at the gate of power transistor whilst allowing low quiescent current under low supply design. Making use of this fast transient technique as well as the aforementioned process-temperature aware design techniques, a low-power PT-aware LDO regulator in 40nm CMOS technology is proposed, analyzed and implemented. It is of particularly noted that it can sustain fast transient merit under different process and temperature corners. Finally, it has shown that the performance is better than most of the reported state-of-art works.

7.2. Future Works

As discussed in the above Chapters, this research work has focused to investigate, analyse, design, and implement the novel PVT-aware and performance-aware circuits dedicated to power management IC applications in advanced nanometer CMOS technology. However, further research can still be conducted for the improvement of the PVT-aware circuits.

For the trend towards low-power IoT circuits and systems, the demand for the high precision reference circuits continues to grow. Since the proposed constant current source relies on the passive resistor, it is still subject to certain process variation. Therefore, the improvement methods are needed to achieve high DC current accuracy as well as temperature stability.

The OCL-LDO regulator is proposed with the achievement of process-temperature aware design for transient sustainability. However, in the applications that immunity against wide supply voltage range is required, the design of supply tolerant regulator dedicated to wide range becomes the continuing topic.

The quiescent current is around several ten μA for the LDO regulators in this research work. In order to further reduce the quiescent power for the IoT applications, the ultra-low quiescent power as well as ultra-low dropout voltage based LDO regulator with reasonably fast transient response can also be investigated in future.

List of Publications

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