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STUDIES ON THE CONTROL OF HIGH-GAIN DC-DC BOOST CONVERTERS

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ABSTRACT

The traditional dc-dc boost converter has been widely applied in industrial applications. However, due to the parasitic resistance of the inductor and the serious reverse-recovery problem, the voltage gain of this converter is very limited. To solve this problem, many high voltage gain dc-dc boost converters have been proposed in the last decade. The high voltage gain dc-dc boost converters can be roughly separated as isolated converters and non-isolated converters. Since most of the isolated converters suffer from large amount of power losses caused by the leakage current problem, the non-isolated converters are more preferred in applications where electrical isolation is not necessary.

Since the non-isolated high voltage gain dc-dc boost converters are generally high-order non-minimum phase systems, it is more difficult to regulate these converters as compared to regulating their traditional counterpart. In this thesis, some studies on the control aspects of such non-isolated high voltage gain dc-dc boost converters are presented.

Firstly, the study on how to select the most suitable state variables to design the current-mode controller for the high voltage gain dc-dc converter is presented. For the current-mode control technique, the measurement of the inductor current for feedback purpose is necessary. However, some of the high voltage gain converters, such as the hybrid-type dc-dc boost converter, contain two or more inductors. As such, the issues such as which inductor current is more suitable for the design of the controller should be answered. To address this, a comparative study of the adaptive current-mode controllers for the hybrid-type high-order dc-dc boost converter was carried out. The Routh-Hurwitz stability criterion was used to determine the most suitable inductor current for

the controller design. Some simulation as well as experimental results are also presented to verify the theoretical conclusions.

Next, the problem of regulation of high-order dc-dc converters using least number of state variables for feedback purposes is addressed. To this end, three output feedback control laws for various non-isolated high voltage gain dc-dc boost-type converters are proposed. In these control laws, only the converter output voltage is required for the feedback purposes. This feature results in that, these control laws are very suitable for the applications where there is a cost limit or power density constraint to accommodate the current sensor.

Initially, a voltage-mode controller for a dc-dc multilevel boost converter is presented. Unlike some of the existing voltage-mode controllers for the high-order dc-dc converters, the selection of the controller gains of the proposed controller does not rely on a trial and error approach. Since the proposed controller uses the new structure, the frequency domain method could be used to select the appropriate values for the controller gains to ensure robust stability. As such, it is easier to achieve the desired robust control performance.

Next, the development of a novel output feedback control strategy for the positive output super-lift re-lift Luo (POSRL) converter is presented. The main feature of this controller is that, despite the non-minimum phase obstacle presented by the converter, the output voltage is regulated directly. Apart from this, the structure of the proposed controller is such that there is no risk of saturation in the control law due to division by zero, and the “remaining dynamics” for the controlled converter has only one equilibrium point which is always stable.

Finally, an improved voltage-mode controller for the quadratic boost dc-dc converter is presented. A new structure for the integral action is adopted in this controller. Since the adopted integrand is bounded by a user-defined constant, the extreme changes in the control signal can be avoided. As such, the proposed controller provides better control performance as compared to its counterparts which use the traditional integral action.

LIST OF ACRONYMS

REGS	-	Renewable energy generation system
RES	-	Renewable energy sources
PV	-	Photovoltaics
HEV	-	Hybrid electric vehicle
UPS	-	Uninterruptible power supply
PBC	-	Passivity-based control
PV	-	Photovoltaic
MBC	-	Multi-level boost converter
POSRL	-	Positive Output Super-lift Re-lift Luo
EMI	-	Electromagnetic-interference
MOSFET	-	Metal–oxide–semiconductor field-effect transistor
IGBT	-	Insulated-gate bipolar transistor
KVL	-	Kirchhoff's voltage Law
KCL	-	Kirchhoff's current Law
CCM	-	Continuous conduction mode
PI	-	Proportional-integral
PBC	-	Passivity-based controller
PWM	-	Pulse width modulation
HVDC	-	High voltage direct current
VL	-	Voltage-lift
HM	-	Hysteresis modulation
CF	-	Constant frequency
SMC	-	Sliding-mode control
CPL	-	Constant power load
IEEE	-	Institute of Electrical and Electronics Engineers
IET	-	The Institution of Engineering and Technology

Chapter 1

Introduction

In this chapter, the background and motivation of the research are provided. The content includes the requirements of the high voltage gain dc-dc boost converters as well as the main challenges in designing the controllers for these converters. Besides, an overview of the controllers proposed in this thesis, the objectives of the research work, the main contribution of this thesis and the organization of this thesis are presented.

1.1 Background and Motivation

In the last decade, environmental problems have posed a growing concern. The increasingly severe air pollution and global warming problem have warned people of the consequences of abusing fossil fuels. Besides, due to the limited amount of fossil fuels, the energy crisis is also a problem. Considering all of these, utilizing renewable and clean energy resources are necessary.

Electricity is the most widely used energy in any modern society. It is already an indispensable part of our daily life. Regarding electricity generation, many renewable energy generation systems (REGSs) have been adopted to replace the traditional electricity generation systems [1]. The wind energy, photovoltaics (PV) and fuel cells are the primary sources adopted in the REGSs [2], [3]. However, the output voltage of these renewable energy sources (RESs) are quite low. More specifically, the output voltage of a single PV cell is around 0.5 V, and the nominal output voltage of a single fuel cell is approximately 0.6 V [4]. Hence, the RESs cannot be connected to the interface of the power grid directly [5]. Although serial connection of the PV cells and

stack of fuel cells can provide higher output voltage and power, the consequent problems, such as the limited flexibility in expansion and maintenance of the fuel cell stack and the shadow effect in the PV system, are not desirable. Also, due to nature of the RESs, their output voltages are varying. The voltage variations significantly deteriorate the power quality of the REGS. In order to solve the problems above, a dc-dc boost converter with a high voltage gain is placed between the RES and the interface with the power grid. As such, a stabilized output voltage of 400 V can be obtained to feed into the dc-ac interface of the power grid [5].

In addition, the dc-dc boost converters also have been used in other applications that are supplied by the RESs. In hybrid electric vehicles (HEVs), the high voltage gain dc-dc converter is placed after the PV panels and fuel cell stacks to regulate the output voltage of these RESs. Consequently, continuous and stable electrical power can be transmitted to the vehicle energy storage system and electric motor, which ensures the normal operation of the HEV systems [6]. Another example is the uninterruptible power supply (UPS). It plays an important role in industries as it provides emergency power to critical industrial loads. The UPS can generate a stable grid level ac voltage through a dc/ac converter, and the dc-dc boost converter is usually used to boost the low-level RES output voltage to around 400 V [7], [8]. Except the high power applications, the dc-dc boost-type converter is still widely adopted in the high voltage but low power applications. For example, the high-intensity discharge lamps require more than a 100 V start-up voltage at 35 W using a 12 V battery.

Ideally, the traditional dc-dc boost converter can provide a very high voltage gain with an extremely high duty ratio. However, it is impossible in practical implementation due to the resulting serious reverse-recovery problems, massive losses in circuit components and the existence of the inductor parasitic resistance [9] – [11]. To achieve a high voltage

gain with reasonable duty ratios and high conversion efficiency, various high-gain dc-dc boost converters have been explored in the past few years [12] – [25]. These converters can be categorized as isolated converters [12] – [16] and non-isolated converters [18] – [25]. Since the isolated converters utilize high-frequency transformers, their voltage gains can be easily tuned by changing the turn-ratios of the transformers. However, the leakage inductor problem dramatically affects the overall power conversion efficiency. Moreover, if the isolation property is not required in the applications, the use of isolated dc-dc converters only reduces the power density and increases the cost of the converter system. In order to overcome the drawbacks above, the non-isolated converter can be the better alternative.

With the development of high-gain dc-dc boost converters, there is also a keen interest to find suitable controllers for their regulation. However, since these converters are generally high-order systems, the control techniques for their traditional counterpart, which are second-order systems, may not be suitable. One of the main objectives of this research is to study the control aspects of such non-isolated high-gain boost dc-dc converters.

Similar to the traditional dc-dc boost converter, the high-gain boost converters are generally non-minimum phase systems due to the presence of right-half plane zeroes in their control-to-output transfer functions. This feature results in a small stability margin and extremely low control bandwidth for the closed-loop system if only the output voltage is used for feedback purposes [26]. However, the drawback of the non-minimum phase system can be avoided by adopting the current-mode control technique instead. Moreover, the current-mode control technique also provides the regulated converter system with several advantages, and one of them is over-current protection [27]. When using the current-mode control technique to regulate the converters, measurements of

the inductor current and output capacitor voltage for the feedback purposes are required. Unlike the traditional dc-dc boost converter that only has one inductor and one capacitor, the high-gain dc-dc boost converters have more energy storage elements. For instance, the cascaded boost converter has two inductors and two capacitors [28]. As such, more measurements such as two inductor currents and two capacitor voltages are available for the feedback purposes. The performance of the controlled system may differ when different state variables are used for feedback purposes. As such, it is necessary to select the minimum as well as the most suitable state variables to design the control system with best possible performance. To address this, the comparative study of current-mode controllers using different inductor currents for feedback purposes is carried out in Chapter 3 of the thesis. Note that the main feature of the current-mode controller used in Chapter 3 is that its use in the regulation of the dc-dc converter significantly reduces the overshoot as well as settling time of the closed-loop system as compared to the traditional current-mode controlled system.

For applications where power density limitations cannot accommodate the current sensors, the current-mode control is no longer suitable. However, due to the non-minimum phase characteristic of boost converters, the traditional voltage-mode control technique cannot provide robust output responses. In order to solve this problem, some parallel-damped passivity-based controllers (PBCs) have been proposed to regulate the boost dc-dc converters [29] – [34]. Despite the non-minimum phase obstacle presented by the boost dc-dc converters, using PBC, the desired regulation of the output voltage can be achieved without employing the current sensor. However, the state-of-the-art PBCs still has some shortcomings that need to be addressed, such as the risk of control signal saturation caused by the control law structure and no systematic guidelines to select the control gains. To fill the gap, the studies of the PBC or voltage-mode

controller for the high-order dc-dc boost converters are addressed in Chapter 4 of this thesis.

1.2 Objectives of this Study

The objectives of this study can be classified into two categories as follows:

1. To develop an approach to select the most suitable measurements for designing an adaptive current-mode controller for the high-gain dc-dc boost converters.
2. To develop improved voltage-mode controllers for regulating the high-gain dc-dc boost converters. The drawbacks of the state-of-the-art voltage-mode controllers [29] – [34] can be overcome by using the proposed controllers.

1.3 Contributions of the Thesis

The main contributions of this thesis can be summarized as follows:

- i. Adaptive current-mode controllers are proposed for a hybrid high-order boost converter. The weakness of the traditional current-mode controller is that it is unable to handle systems with unknown loads. The proposed controllers overcome the weakness of the traditional approach by employing a suitable adaptive law to generate the estimate of the load conductance so that the reference inductor current can be obtained. Moreover, two adaptive current-mode controllers using the input and output inductor currents are investigated to determine the most suitable inductor current for the controller design.
- ii. A voltage-mode controller has been proposed for the regulation of a dc-dc multilevel boost converter (MBC). Despite the non-minimum phase obstacle presented by this

boost dc-dc converter, the regulation of the output voltage is achieved without employing a current sensor. In contrast to some state-of-the-art voltage-mode controllers where the selection of the controller gains mainly relied on a trial and error approach, the proposed controller is designed using the frequency domain technique, where the Bode-plot is used to select the controller gains based on the system's phase margin and gain margin criteria.

- iii. The development of a new output feedback controller for the positive output super-lift re-lift Luo (POSRL) converter. The controller achieves the output voltage regulation in the sixth-order converter using only the output voltage for feedback purposes. Moreover, the new structure adopted in this controller avoids the risk of saturation by avoiding the possibility of division by zero that exists in some state-of-the-art output feedback controllers.
- iv. An improved voltage-mode controller has been proposed for a quadratic boost dc-dc converter. By using a new integrator technique, the proposed controller provides improved converter output responses in the presence of external disturbances, as compared to those obtained using the existing voltage-mode controller.

1.4 Organization of the Thesis

The organization of the thesis is as follows:

Chapter 2 details the limitations of the traditional boost dc-dc converter. Moreover, the advantages of the non-isolated high-gain boost dc-dc converters over its isolated counterpart are presented. A literature review of various existing high-gain boost dc-dc converters is also carried out. Besides, some previous works on the control and modelling aspects of the high-gain boost dc-dc converters are reviewed.

In Chapter 3, a study on the adaptive current-mode control for a high-order hybrid dc-dc boost converter is presented. In this work, the adaptive current-mode controllers using the input and output inductor currents of the converter are separately designed to find the most appropriate feedback inductor current for the implementation of the proposed adaptive controller. Besides, some simulation and experimental results comparing the performance of the adaptive controller using the output inductor current with that of the traditional current-mode controller are also presented.

In Chapter 4, several output-feedback (or voltage-mode) controllers are proposed for some high-gain dc-dc boost converters, such as the dc-dc MBC, the PSRB converter, and the quadratic boost dc-dc converter. Each of them overcomes some drawbacks of the state-of-the-art voltage-mode controllers. The stability analyses for all the regulated converter systems are carried out. Besides, some simulation and experimental results are provided to show the effectiveness of the proposed controllers.

In Chapter 5, a summary of the works reported in this thesis is presented, and the expected future research work is provided as well.

Chapter 2

Literature Review

Power converters use power semiconductors, such as power IGBT, power MOSFET, and power diode to convert and regulate electrical energy. Since the switching operation of the power semiconductor does not involve any mechanical movements, the switching-loss is very low. Therefore, a high operational efficiency can be obtained in the power converters. Moreover, the high efficiency also depends on the specific modulation and control strategy utilized, as well as on the proper circuit design layouts. This high-efficiency feature allows the power converters to play essential roles in various energy processing systems, such as HEV, UPS and REGS [35]. Based on the input and output power, the power converters can be classified as four categories, namely ac to dc converter (rectifier), dc to ac converter (inverter), dc to dc converter and ac to ac converter. Among these converters, the most widely used category in our daily life is the dc-dc converter. It can be found in various devices, such as smartphones, personal computers, game consoles, microwave ovens, etc. [36]. Besides the low power devices, the dc-dc converter is also adopted in high-power applications, e.g., the high-voltage direct current (HVDC) transmission system [12] – [25], [35], the interface between the medium-voltage DC bus and high-power applications [37], etc.. Generally, based on the value of the converter voltage gain, the dc-dc converter can be classified as a buck converter, a boost converter or a buck-boost converter. The voltage gain of the ideal buck converter is in the range of $[0, 1]$. As such, the buck converter generates an output voltage that is smaller than its input voltage. In contrast to the buck converter, the voltage gain of the boost converter is greater than one. Hence, the boost converter can

step-up its input voltage to a higher voltage level. The buck-boost converter possesses the functions of both the buck converter and boost converter. By changing its duty-ratio, the converter input voltage can be either stepped-up or stepped-down [38]. The focus of the thesis is on the studies of the boost dc-dc converter.

In this chapter, the limitations of the traditional boost dc-dc converter are described. Moreover, the advantages of the non-isolated high-gain boost dc-dc converter over its isolated counterpart are presented. A literature review for various existing high-gain boost dc-dc converters is also carried out. Besides, some previous works on the control and modelling aspects of the high-gain boost dc-dc converters are reviewed.

2.1 Limitations of the Traditional Boost Dc-Dc Converter

The traditional boost dc-dc converter was first proposed in 1968 by O. Kossov [39]. Its schematic diagram is shown in Fig. 2.1, where r_L is the parasitic resistance of the inductor L , R is load resistance and V_{in} and V_o are the input voltage and output voltage, respectively.

Fig. 2.1. Traditional boost dc-dc converter.

In the ideal case, the inductor parasitic resistor is not considered. The corresponding converter voltage gain can be obtained as

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \quad (2.1)$$

where D is the duty ratio of the power switch S . The voltage gain versus duty ratio curve of (2.1) is shown in Fig. 2.2(a).

Fig. 2.2. The voltage gain of the traditional boost converter with respect to the duty-ratio: (a) without inductor parasitic resistor; (b) with inductor parasitic resistor.

It can be seen that the voltage gain of the traditional boost converter can be infinity if the duty ratio $D = 1$. However, in practical applications, the value of the inductor parasitic resistor cannot be neglected. With the presence of the parasitic resistance r_L , the voltage gain is now given by

$$\frac{V_o}{V_{in}} = \frac{1}{\frac{r_L}{(1-D)R} + (1-D)} \quad (2.2)$$

For the purpose of illustration, $r_L/R = 0.01$ is considered. Substituting $r_L/R = 0.01$ into (2.2), the voltage gain versus duty ratio curve of (2.2) is shown in Fig. 2.2(b). It is obvious that the maximum voltage gain is limited to 5 when $D = 0.9$. Moreover, since the extremely high duty ratio will cause problems, such as diode reverse recovery problem, large power losses as well as large voltage and current stresses in the switching components, the maximum voltage gain of the traditional boost converter is further reduced [9] – [11].

It is clear that the traditional dc-dc boost converter is not very suitable for high output voltage applications. For instance, in the REGS, the low output voltage of the renewable energy sources (around 40 V) is required to be stepped-up to around 400 V to meet the voltage level requirement of the power grid [8].

2.2 Review of the State-of-the-art High-gain Dc-Dc Boost Converters

In recent years, many high-gain boost dc-dc converters have been explored. These converters can provide high voltage gain at low values of the duty ratio, which overcomes the limitations of the traditional boost dc-dc converter. Based on the structure, the high-gain converters can be classified into two categories, namely, isolated converters and transformerless converters.

The isolated converter, such as the dual active bridge (DAB) converter and the fly-back converter, provides a very high voltage gain through tuning the turn-ratio of the transformer [12] – [16]. In high power applications (few kilowatts), such as HEV [12], the DAB converter is commonly adopted. This type of converter supports bidirectional energy flow and hence the single converter is competent to charge and discharge the car battery in the HEV [12]. In addition, there are various isolated dc-dc converters proposed for medium and low power applications [13] – [16]. Although these converters cannot deliver high power levels as compared to the DAB type converter, they however, contain less switching components. This feature not only reduces the converter implementation cost but also increases the converter power efficiency.

The transformer is the core component in the isolated dc-dc converters. It can step up or step down time varying voltages and provides galvanic isolation between the source and the load. Typically, the use of the transformer results in a heavy and bulky converter as well as a higher cost. In order to reduce the size and weight of the isolated converters, the high-frequency transformer is normally used. However, this results in large switching losses. Besides, the spike voltage on the switch that is caused by the energy of the transformer leakage inductor tremendously increases the power switch voltage stress [13]. To solve the problems, a load-dependent snubber is presented in [14]. This

type of snubber circuit can recycle the energy of the leakage inductor between the input stage and the leakage inductor without any energy dissipated so that the high spike voltage is suppressed without decreasing the conversion efficiency. Besides, an auxiliary converter is introduced into the snubber circuit. It can regulate its output power according to the variable load. Therefore, the converter with this snubber can operate in a wide load range. However, the extra circuit components will increase the converter cost. In [15], an isolated dc/dc converter for fuel cell applications is proposed. An unregulated LLC resonant converter is used in this converter design to provide the galvanic isolation and high output voltage gain. As the transformer leakage energy is absorbed by the input and output capacitors of the LLC circuit, a snubber is not required in this converter. A new isolated high step-up dc-dc converter for a renewable energy system, based on the quasi-switched boost network, is proposed in [16]. Unlike the traditional isolated converters, this converter can operate in either the short-circuit mode and open-circuit mode safely. In addition, due to the adoption of a voltage double rectifier and shoot-through duty cycle technique, the proposed converter can achieve a higher voltage gain with a smaller transformer turn-ratio as compared to its counterparts. Although the isolated boost dc-dc converters can provide a high voltage gain, most of them suffer from the leakage inductor problem. Although various auxiliary circuits can be used to tackle this problem, the increased system complexity and cost are not desirable. Besides, in applications where galvanic isolation is not required, the use of isolated dc-dc converters only reduces the power density and increases the cost of the converter system [25].

In the past few years, various non-isolated high-gain dc-dc boost converters have been reported [17] – [25]. This type of converters are mainly designed for high voltage but medium or low power applications, like the laser beam system [19], battery backup

system, solar-cell energy conversion system [21], etc. For instance, in the automobile head lamp system, the high-intensity discharge lamps require a more than a 100 V start-up voltage at 35 W using a 12 V battery [20]. Since there is no transformer in the non-isolated boost dc-dc converter, the problems caused by the transformer are also avoided. This feature makes the non-isolated converter a better alternative to its isolated counterpart in some medium or low power applications. Due to the abovementioned advantages, the non-isolated dc-dc converters are chosen as the target converters in this thesis. Here, a brief overview of some of the state-of-the-art non-isolated high-gain boost dc-dc converters is provided.

In [17], the converter voltage gain is increased by cascading n traditional boost dc-dc converters. Since multiple switches are used, a low semiconductor component voltage stress is achieved. However, due to the considerable conduction losses of the input inductors, the efficiency of this cascaded boost converter is relatively low. In order to reduce the conduction losses, an improved cascaded boost converter is proposed in [18]. By utilizing a new topology, the value of the input inductor current ripple is significantly reduced. Consequently, the reduction in the current ripple results in the reduction of the input inductor conduction losses.

In [19], a diode-capacitor multiplier circuit was inserted into a traditional boost converter to increase the output voltage. The voltage gain can be easily enhanced through cascading the diode-capacitor multiplier to the converter output side. Unlike the high-gain converter using a multi-switch structure, only one active switch is used in this converter. This feature not only reduces the converter switch conduction losses, but also simplifies the controller design. Based on the experimental results, the proposed converter was able to provide a 600 V output voltage with a 360 W output power.

Recently, a dc-dc multi-level boost converter (MBC) was proposed in [20]. The structure of this MBC is similar to that of [19]. Hence, the proposed converter possesses all the merits of the converter presented in [19], such as high output voltage gain with a small duty-ratio and a low level switch voltage stress. Moreover, because of the structure modification, the new converter can achieve a higher voltage gain using fewer multiplier circuits, unlike the converter described in [19].

The voltage-lift (VL) technique is used in [21] – [22] to increase the voltage gain of the dc-dc boost converters. Through adding the voltage-lift cells, the converter voltage gain is effectively enhanced. As compared to some of the state-of-the-art non-isolated converters using other voltage gain improving techniques, the converters using the VL technique provide much higher voltage gain using fewer circuit components. This feature results in a converter with a high voltage gain but at a lower cost and small power density. Another main advantage of the VL converters is the reduced ripple in the voltage and current [22].

In [23], three high step-up non-isolated converters are presented. The employment of two power switches evenly divides the input current flow into two parts during the converter switch-on stage, which reduces the current stress of the power switches. Besides, the voltage stress on the power switches used in the proposed converters are nearly half of that used in the traditional boost converter. Considering all these, the low current and voltage ratings of the power switches can be selected for the proposed converters. As such, the implementation cost of the converter system can be reduced.

By combining the switching capacitor/inductor cell with the traditional boost converter, a new hybrid boost dc-dc converter is proposed in [24]. This converter provides a high voltage gain with small energy in the magnetic elements. This advantage leads to a

reduction in the size and cost of the inductors. Besides, the small current stresses of the switches results in small conduction losses and a higher converter efficiency.

In [25], a switching-capacitor boost dc-dc converter is presented. This type of converter is also known as the step-up charge pump. It step-ups the input voltage to a higher level using only the capacitors and semiconducting switches. Therefore, as compared to its counterpart which utilizes the power inductor, lighter weight, smaller size and higher power density are achieved in the proposed converter. These advantages make this type of converter very popular in portable devices, such as mobile phones, tablets, portable game consoles, etc.

In practical applications, unexpected bus line voltage interruption, load side disturbance and circuit uncertainties can cause a significant deterioration in the output performance of the converters. In order to overcome this problem, control techniques should be applied in the regulation of the converters. However, in general, mathematical models of physical systems are the prerequisite for controller design. Furthermore, based on the physical converter circuit, it is hard to carry out a stability analysis of the converter system. Considering all these, before designing the controllers, developing the mathematical models for the converters is necessary. In the following section, a brief overview of a commonly used method for describing dc-dc converters is presented.

2.3 Modelling of Boost Dc-Dc Converters in the continuous current mode

In this section, a brief overview of the state-space averaging method for the traditional boost dc-dc converter operating in continuous current mode (CCM) is first given. In addition, several examples of the state-space averaged models of high-gain boost dc-dc converters operating in CCM are also provided. Although the average models presented

in the following sections can be found in the literature, it is still important to know how they are derived.

2.3.1 Overview of the State-Space Averaging Approach

The state-space averaging modelling approach was first proposed by R. D. Middlebrook and S. Cuk in 1976 [40]. To date, it has become one of the most popular modelling methods for dc-dc converters. In this modelling approach, the effective converter output low-pass filter corner frequency is required to be much smaller than the converter switching frequency. As such, some modelling limitations caused by the large output voltage ripple can be avoided.

Fig. 2.3. The traditional boost converter circuit: (a) equivalent circuit for switch-on operation mode; (b) equivalent circuit for switch-off operation mode.

Consider the traditional boost converter of Fig. 2.1 that operates in CCM. The boost converter has two operating stages, namely, switch-on stage and switch-off stage. The duration of the switch-on stage is dT_s , where $d \in [0,1]$ is the duty ratio of the switch and T_s is the switching period. The schematic diagram of the switch-on stage is shown in Fig. 2.3(a). During this stage, inductor L is charged from the input source v_{in} and the energy stored in the capacitor C is transferred to the load resistor R . Fig. 2.3(b) shows the schematic diagram of the switch-off stage. The duration of this stage is $(1 - d)T_s$. In this stage, both the source and the energy stored in the inductor are charging

the capacitor C and feeding the load.

Next, the state-space model of each operation stage is considered. The inductor current i_L and output capacitor voltage v_C are chosen as the state-variables for the converter. Using Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) in Fig. 2.3(a), the state equation for this stage is

$$\dot{x} = A_{on}x + B_{on}v_{in} \quad (2.3)$$

where $x = [x_1, x_2]^T = [i_L, v_C]^T$, $A_{on} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$ and $B_{on} = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T$.

Again, using KCL and KVL in Fig. 2.3 (b), the state equation for this stage

$$\dot{x} = A_{off}x + B_{off}v_{in} \quad (2.4)$$

where $A_{off} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$, $B_{off} = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T$.

Since A_{on} , A_{off} , B_{on} , B_{off} , and v_{in} are constant, applying the basic averaging concept gives the average value of $\dot{x}$ over one switching period (considering $t \in [0, T_s]$) as

$$\begin{aligned} \dot{\bar{x}} = \frac{1}{T_s} \left\{ A_{on} \int_0^{dT_s} x(\tau) d\tau + A_{off} \int_{dT_s}^{T_s} x(\tau) d\tau \right. \\ \left. + [B_{on}d + B_{off}(1-d)]T_s v_{in} \right\} \end{aligned} \quad (2.5)$$

Using (2.5), the averaged state-space model of the traditional boost dc-dc boost converter operating in CCM is given by

$$\dot{\bar{x}} = [A_{on}d + A_{off}(1-d)]\bar{x} + [B_{on}d + B_{off}(1-d)]v_{in} \quad (2.6)$$

where $\bar{x} = [\bar{x}_1, \bar{x}_2]^T = [\bar{i}_L, \bar{v}_C]^T$ is the averaged state variable vector. Letting $A_{ave} = A_{on}d + A_{off}(1-d)$ and $B_{ave} = B_{on}d + B_{off}(1-d)$, (2.6) can be written as

$$\dot{\bar{x}} = A_{avg}\bar{x} + B_{avg}v_{in} \quad (2.7)$$

where

$$A_{avg} = \begin{bmatrix} 0 & -\frac{1-d}{L} \\ \frac{d}{C} & -\frac{1}{RC} \end{bmatrix}, B_{avg} = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T.$$

2.3.2 Averaged State-Space Model of the Quadratic Boost Converter

In this section, the derivation of the averaged state-space model of the quadratic boost converter shown in Fig. 2.4 is given. As compared to the traditional boost converter, this converter can provide a much higher voltage gain using a smaller duty cycle. It also has a better trade-off between efficiency and duty cycle operation range as compared to its cubic counterparts [28].

Fig. 2.4. The quadratic boost converter circuit: (a) equivalent circuit for switch-on operation mode; (b) equivalent circuit for switch-off operation mode.

Like the traditional boost converter, there are also two switched models. It is assumed that the converter is operating in CCM. The schematic diagram of the switch-on stage is shown in Fig. 2.4(a). The duration time of this stage is dT_s , where $d \in [0,1]$ is the duty ratio and T_s is the switching period. In this stage, the power switch S and the

diode D_1 are turned on while the diodes D_2 and D_3 are turned off. The power supply v_{in} and capacitor C_1 supply energy to the inductors L_1 and L_2 . The load R is fed by the capacitor C_o .

The schematic diagram of the switch-off stage is given in Fig. 2.4(b). At the start of this stage, the power switch S and the diode D_1 are blocked, and the diodes D_2 and D_3 are forward-biased. The capacitor C_1 is charged by both the power supply v_{in} and energy stored in inductor L_1 . Meanwhile, all the inductors transfer energy to the output capacitor C_o and feed the load R .

The inductor currents i_{L1} and i_{L2} and the capacitor voltages v_{C1} and v_{Co} are selected as the state variables for the converter. Using KCL and KVL in Fig. 2.4(a), the state equation for this stage is

$$\dot{x} = A_{on}x + B_{on}v_{in} \quad (2.8)$$

where $x = [x_1, x_2, x_3, x_4]^T = [i_{L1}, i_{L2}, v_{C1}, v_{Co}]^T$,

$$A_{on} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix}, \quad B_{on} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

Similarly, using KCL and KVL in Fig. 2.4(b), the state equation for this stage is

$$\dot{x} = A_{off}x + B_{off}v_{in} \quad (2.9)$$

where

$$A_{off} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix}, \quad B_{off} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

Using (2.8), (2.9) and the state-space averaging approach, the averaged state-space model of the quadratic boost converter operating in CCM can be easily obtained as [32]:

$$\dot{\bar{x}} = A_{avg}\bar{x} + B_{avg}v_{in} \quad (2.10)$$

where $\bar{x} = [\bar{x}_1, \bar{x}_2, \bar{x}_3, \bar{x}_4]^T$, $\bar{x}_i$ ($i = 1, 2, 3, 4$) represents the averaged value of the state variable x_i ($i = 1, 2, 3, 4$), and

$$A_{avg} = \begin{bmatrix} 0 & 0 & -\frac{1-d}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{1-d}{L_2} \\ \frac{1-d}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1-d}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix}, \quad B_{avg} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

Thus far, the derived state-space averaged models of the converters consist of the dynamical equations of all the state variables. This type of state-space averaged model is called the full-order state-space model (FOSM). Although the FOSM can accurately describe the dynamics and steady-state behaviors of the converter system, its high-order property poses difficulties regarding calculations and analysis.

In next section, the derivation of a reduced-order averaged model for a Positive Output Super-lift Re-lift Luo (POSRL) converter will be addressed. By properly omitting several dynamical equations, the averaged model obtained has a lower order, but the model accuracy is not compromised.

2.3.3 Reduced-Order Averaged Model of the Super-lift re-lift Luo Converter

In this section, a reduced-order averaged state-space model of the POSRL converter is derived. By analyzing the operation of the POSRL converter, the POSRL converter's switch-on schematic diagram and its switch-off schematic diagram can be obtained, as shown in Fig. 2.5(a) and Fig. 2.5(b), respectively, where v_{in} is the voltage of power

supply, v_{C1} , v_{C2} , v_{C3} and v_{Co} are the voltages of capacitors C_1 , C_2 , C_3 and C_o , respectively. Besides, the currents of inductors L_1 and L_2 are represented by i_{L1} and i_{L2} , respectively, and R is the load resistance.

Fig. 2.5. The POSRL converter circuit: (a) equivalent circuit for switch-on operation mode; (b) equivalent circuit for switch-off operation mode.

It can be seen from Fig. 2.5(a) that capacitor C_1 and the input source v_{in} are in parallel, and capacitors C_2 and C_3 are also in parallel. Since the capacitance of all the capacitors are large enough, it is reasonable to assume $v_{C1} = v_{in}$ and $v_{C2} = v_{C3}$ for the whole switching period [41]. As such, it is only necessary to select i_{L1} , i_{L2} , v_{C2} and v_{Co} as the state variables for the converter.

Using KCL and KVL in Fig. 2.5(a), the state equation for the switch-on stage is

$$\dot{x} = A_{on}x + B_{on}v_{in} \quad (2.11)$$

where $x = [x_1, x_2, x_3, x_4]^T = [i_{L1}, i_{L2}, v_{C2}, v_{Co}]^T$,

$$A_{on} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_2} - \frac{C_3 \frac{dv_{C3}}{dt}}{i_{L2} C_2} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix}, \quad B_{on} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

Similarly, using KCL and KVL in Fig. 2.5(b), the state equation for this stage is

$$\dot{x} = A_{off}x + B_{off}v_{in} \quad (2.12)$$

where

$$A_{off} = \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & \frac{2}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_2} & -\frac{1}{C_2} & 0 & 0 \\ 0 & \frac{1}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix}, \quad B_{off} = \begin{bmatrix} \frac{2}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

As usual, the duration of the switch-on stage is dT_s , while the duration of the switch-off stage is $(1-d)T_s$. Also, $d \in [0,1]$ is the duty-ratio and T_s represents the switching period.

Based on the ampere-second characteristic of the capacitor in dc-dc converters, the following equation can be obtained [41]:

$$dC_3\dot{v}_{C3} + (1-d)i_{L2} = 0 \quad (2.13)$$

Using (2.11) – (2.13), the reduced-order averaged state-space model of the POSRL converter is given by [41]:

$$\dot{\bar{x}} = A_{avg}\bar{x} + B_{avg}v_{in} \quad (2.14)$$

$$A_{avg} = \begin{bmatrix} 0 & 0 & -\frac{1-d}{L_1} & 0 \\ 0 & 0 & \frac{2-d}{L_2} & -\frac{1-d}{L_2} \\ \frac{1-d}{C_2} & -\frac{2-d}{C_2} & 0 & 0 \\ 0 & \frac{1-d}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix}, B_{avg} = \begin{bmatrix} \frac{2-d}{L_1} & 0 & 0 & 0 \end{bmatrix}^T \quad (2.15)$$

where $\bar{x} = [\bar{x}_1, \bar{x}_2, \bar{x}_3, \bar{x}_4]^T$ is the averaged state variable vector, and $\bar{x}_i$ ($i = 1, 2, 3, 4$) denotes the averaged value of the state variable x_i ($i = 1, 2, 3, 4$).

It can be seen from (2.14) that the sixth-order POSRL converter system is represented by a fourth-order averaged state-space model.

2.3.4 General Averaged Model of the Multilevel Boost Converter

In recent years, many extendable high-gain dc-dc converters have been proposed [19] – [24]. The voltage gain of this type of converter can be increased exponentially by adding the voltage pull-up cells, such as the voltage multiplier and switching capacitor cell. However, the added voltage pull-up cells definitely introduce more energy storage elements, viz., inductors and capacitors into the converter system. With the additional energy storage elements, the full-order state-space models of this type of converter are variable in both order and structure. To overcome the problem of the state-space model variation and further reduce the difficulties of system analysis for the extendable dc-dc converter, the concept of the general averaged reduced-order model is proposed [42].

In this section, a brief review of the general averaged reduced-order model for an MBC is given. The schematic diagram of the N -level MBC is shown in Fig. 2.6.

Fig. 2.6. Schematic diagram of the N -level MBC.

To obtain the general averaged reduced-order model of the N -level MBC, the derivation of the averaged reduced-order model for the 2-level MBC has to be carried out first. Similar to the converters addressed in the previous sections, the MBC also has two operation stages, viz., switch-on stage and switch-off stage. After analysing the operation of the 2-level MBC, the topologies of the switch-on and switch-off stages are shown in Fig. 2.7(a) and Fig. 2.7(b), respectively.

Fig. 2.7. The 2-level MBC circuit: (a) equivalent circuit for switch-on operation mode; (b) equivalent circuit for switch-off operation mode.

Using Kirchhoff's laws in Fig. 2.7(a), the state equation is

$$\frac{di_L}{dt} = \frac{v_{in}}{L} \quad (2.16)$$

$$\frac{d}{dt} \left(\frac{v_o}{2} \right) = - \frac{v_o}{RC_{eq1}} \quad (2.17)$$

where the i_L is the input inductor current, v_{in} is the converter input voltage, v_o is total

output voltage (summation of capacitor voltage at the output side) and C_{eq1} is the equivalent capacitor which equals to $(C_1//C_3)$.

Similarly, using Kirchhoff's laws in Fig. 2.7(b), the state equation of the switch-off stage can be obtained as,

$$\frac{di_L}{dt} = \frac{1}{L} \left(v_{in} - \frac{v_o}{2} \right) \quad (2.18)$$

$$\frac{d}{dt} \left(\frac{v_o}{2} \right) = \frac{1}{C_{eq2}} \left(\frac{i_L}{2} - \frac{v_o}{R} \right) \quad (2.19)$$

where C_{eq2} is the equivalent capacitor which equals to C_1 .

Using (2.16) – (2.19) yields the averaged reduced-order model of the 2-level MBC described by:

$$\frac{di_L}{dt} = \frac{1}{L} \left[v_{in} - \frac{(1-d)}{2} v_o \right] \quad (2.20)$$

$$\frac{d}{dt} \left(\frac{v_o}{2} \right) = \frac{1}{dC_{eq1} + (1-d)C_{eq2}} \left[(1-d) \left(\frac{i_L}{2} - \frac{v_o}{R} \right) - \frac{v_o}{R} \right] \quad (2.21)$$

where R is the value of load resistance and $d \in (0,1)$ is the duty-ratio. Assuming that all the capacitors have the same capacitance, i.e., $C_1 = C_2 = C_3 = C$, the capacitance of the equivalent capacitor $C_{eq1} = 2C$ and $C_{eq2} = C$ can be obtained. Therefore, substituting $C_{eq1} = 2C$ and $C_{eq2} = C$ into (2.21) yields

$$\frac{dv_o}{dt} = \frac{1}{C(1+d)} \left[(1-d)i_L - \frac{2v_o}{R} \right] \quad (2.22)$$

Next, using N to replace the “2” in (2.20) and (2.22), the general averaged reduced-order model of the N -level MBC can be obtained as [42]:

$$\frac{di_L}{dt} = \frac{1}{L} \left[v_{in} - \frac{(1-d)}{N} v_o \right] \quad (2.23)$$

$$\frac{dv_o}{dt} = \frac{1}{C(1+d)} \left[(1-d)i_L - \frac{Nv_o}{R} \right] \quad (2.24)$$

It is evident that the number of the level N does not impact the structure and order of the derived model (2.23) – (2.24).

2.3.5 Averaged Model of the Hybrid High-Order Dc-Dc Boost Converter

The hybrid dc-dc boost converter will be covered separately in Chapter 3, together with the proposed adaptive controllers for its regulation.

2.4 Review of State-of-the-art Controllers for High-Gain Dc-Dc Boost Converters

In dc-dc converter applications, the use of a controller is necessary to ensure that the converter output voltage tracks the reference input under various operating conditions. In this section, a brief review of the state-of-the-art controllers for the high-gain dc-dc boost converters is presented. The controllers' advantages and disadvantages are also highlighted.

2.4.1 Current-Mode Controller

Similar to the traditional boost dc-dc converter, most of the high-gain boost dc-dc converters are non-minimum phase systems. This is because there exist right-half plane zeroes in the control to output voltage transfer functions of these converters. This type of transfer function, which is derived by linearizing the converter model around its steady-state equilibrium point, makes it slightly difficult to design the controller for the boost converters using a single voltage-loop [26], [43]. To solve this problem, an indirect approach OF control in which the output voltage is regulated via the inductor current control can be employed. This control approach is known as current-mode

control. Besides, the current-mode control method also provides some advantages, such as wide control bandwidth and over-current protection [27].

A widely used state-of-the-art current-mode controller is [26], [43] – [44]:

$$d = D - K_P(i_L - I_{Lref}) - K_I \int_0^t (v_o(\tau) - V_{ref}) d\tau \quad (2.25)$$

where d is the converter duty-ratio, D is desired steady-state value of the duty ratio d , i_L is the measured inductor current, I_{Lref} is the reference value of i_L , and both K_P and K_I are positive user defined controller gains. Due to the presence of the integral action $K_I \int_0^t (v_o(\tau) - V_{ref}) d\tau$, the system steady-state error is negligible. However, in this type of controller, an external current reference I_{Lref} is required to compute the control signal. Since the value of this reference signal is calculated using the nominal value of the load resistance, i.e., R , this type of controller is not suitable for applications where the value of the load resistance is unknown. To overcome this problem, an adaptive current-mode controller has been proposed in [45]. A real-time estimate of the load conductance is used to generate the control signal in the proposed controller. Although the value of the load conductance is unknown, the estimator can still provide an estimate of the load conductance to the controller. As compared to the controller given in (2.25), the adaptive current-mode controller significantly improves the converter regulation performance in the presence of load disturbances [45]. Unlike the aforementioned current-mode controllers which are designed using the time-domain method, in [46] the converter controllers are designed using the frequency-domain techniques. The system robust stability is achieved based on the system's phase margin and gain margin criteria.

2.4.2 Sliding-Mode Controllers

The sliding-mode controller plays an important role in the regulation of high-gain boost dc-dc converters [28], [47] – [53]. It can provide the controlled system robustness against the large-signal perturbation and circuit component uncertainties. Moreover, the dynamic response of the sliding-mode controlled system is not affected even in the presence of a large input voltage change or load disturbance. Besides, the implementation of the sliding-mode controller can be easily carried out as compared to that of the other non-linear controllers due to its high degree of flexibility [47]. The implementation of a hysteresis-modulation based sliding-mode controller (HMSMC) for several high-order dc-dc converters is addressed in [28], [47], [48]. The proposed controller has various advantages, such as simple implementation and low risk of control signal saturation [28]. The sliding-surface of this controller is given by [48]:

$$s = i_L - I_{ref} \quad (2.26)$$

$$I_{ref} = -K_1(v_o(t) - V_{ref}) - K_2 \int_0^t (v_o(\tau) - V_{ref}) d\tau \quad (2.27)$$

where s is the sliding variable, i_L is the inductor current, K_1 and K_2 are positive controller gains, and V_{ref} is the desired value of the converter output voltage.

The corresponding switched control law is given by:

$$u = \begin{cases} 1, & \text{when } s < 0 \\ 0, & \text{when } s > 0 \end{cases} \quad (2.28)$$

where $u = 1$ denotes the power switch is on, while $u = 0$ denotes the power switch is off.

However, since the state of the power switch is determined by the sign of s , the resulting switching frequency is variable. This phenomenon may cause electromagnetic-

interference (EMI) problems and excessive switching losses. Besides, due to the variability of the frequency, the difficulties of input and output filter design are significantly increased [49]. In [49] – [52], some constant frequency sliding-mode control (CFSMC) schemes have been proposed. This type of controller avoids the problems caused by the variable switching frequency. By using the equivalent control signal and the pulse-width modulation technique, the PWM waveform for the converter power switch can be obtained. Therefore, the converter switching frequency is fixed, and it is determined by the frequency of the PWM carrier wave. Unlike the sliding surface of the HMSMC, which uses a single integral term, the double integral term is usually adopted in the sliding surface of the CFSMC to remove the system steady-state error. This is because in the equivalent control equation, only the double integral action is explicitly shown while the single integral action is eliminated [51] – [52]. However, due to the double integral term, the implementation of the CFSMC requires more computations and becomes rather complex as compared to that of the HMSMC.

Apart from the controllers above, an adaptive sliding-mode controller has been proposed in [53]. An estimator that is used to estimate the reference value of the inductor current is adopted in the proposed controller. Therefore, even if the actual value of the load resistance is unknown, an estimate of the inductor current reference can be generated by the estimator. However, in this control scheme, in order to ensure that the estimators achieve accurate results, the number of converter power switches is required to be equal to the number of estimators. Therefore, this controller may not be suitable for regulating converters that contain more inductors than power switches.

2.4.3 The Voltage-Mode Controller

Since most of the boost dc-dc converters are non-minimum phase systems, the traditional voltage-mode control scheme is not suitable for regulating this kind of converters. However, due to the merits of the voltage-mode control scheme, such as avoiding a current sensor in its implementation and hence cost reduction, voltage-mode control of high-gain boost converters has attracted some attention.

Recently, some voltage-mode controllers have been proposed for dc-dc boost-converters [29] – [34]. Unlike the aforementioned current-mode controllers and sliding-mode controllers, only the output voltage measurement is required for feedback purposes. In [30], a voltage-mode controller for the traditional boost converter has been proposed. The simplified parallel-damped passivity-based control technique is adopted in this controller. Although the regulated converter system is non-minimum phase, the proposed controller is still able to achieve good control performance over a wide range of operating conditions. The control law is given by

$$d = 1 - \frac{v_{in}}{x_d} \quad (2.29)$$

$$\dot{x}_d = \frac{1}{c_o} [-(K_1 + K_2)x_d + K_1 V_{ref} + K_2 v_o] \quad (2.30)$$

where d is duty-ratio, v_{in} and v_o are the converter input voltage and output voltage, respectively, x_d is an artificial voltage variable and V_{ref} is the reference of output voltage. Besides, K_1 and K_2 are the controller gains.

However, since the converter model that was used to derive (2.29) – (2.30) is an ideal model, the performance will be affected in the presence of parasitic elements. In order to overcome this problem, additional proportional and integral (PI) terms are added to the controller (2.29) – (2.30) to eliminate the steady-state error as well as to improve the

system output transient response [31] – [34]. However, there still exist several drawbacks in these state-of-the-art voltage-mode controllers, such as the risk of saturation in the control signal and no clear guidelines to select the controller gains. Hence, developing voltage-mode controllers for the high-gain boost dc-dc converters is still an open problem. In Chapter 4, some improved structures of this type of controller for the high-gain converters are addressed.

Chapter 3

A Comparative Study of Adaptive Current-Mode Controllers for a Hybrid-High-Order Boost Converter

3.1 Introduction

Since most of the high-gain boost converters are non-minimum phase systems, it is difficult to regulate these converter systems using a single-voltage loop [45]. In order to overcome this problem, the indirect approach of control in which the output voltage is regulated via the inductor current control can be employed. This control scheme is known as current-mode control. In [44], a current-mode controller for the hybrid dc-dc boost converter has been addressed. Even though this control scheme offers ease of implementation and inherent overcurrent protection, it has a particular drawback. In this controller, an external current reference is required to compute the control signal. Since the value of this reference signal is calculated using the nominal value of the load resistance, the control law cannot be used in applications where the load resistance is unknown.

In this chapter, the regulation of the hybrid dc-dc boost converter using adaptive current-mode controllers is investigated. This type of controller solves the problem of the traditional current-mode controller, in that it is unable to handle systems with unknown loads, by employing an estimator to estimate the load conductance to compute the reference inductor current. The estimate is generated using an adaptive law in which the derivative of the estimator is both optimized and bounded [45]. Moreover, for the hybrid dc-dc boost converter, two inductor currents could be used for feedback purposes.

However, only one of them will be used to achieve output voltage regulation. As mentioned in the previous chapter, the choice of the inductor current for feedback purposes needs to be addressed. To this end, two adaptive nonlinear controllers using the input and output inductor currents of the hybrid dc-dc converter are investigated. The objective of the study is to determine the most suitable inductor current for designing the adaptive controller. The stability analyses of the two adaptive current-mode controlled converter systems are also presented. Finally, some simulation and experimental results are provided to show the effectiveness of the chosen controller for the hybrid high-order dc-dc converter.

3.2 Averaged State-Space Model of the Hybrid Dc-Dc Boost Converter

Fig. 3.1 shows the circuit schematic diagram of the hybrid dc-dc boost converter, which was first proposed in [24]. A switched-capacitor cell, made up of capacitors C_1 , C_2 and diodes D_1 , D_2 , is inserted into the traditional boost converter to obtain the integrated structure. Inductor L_2 is added to prevent rapid changes in the output current when C_1 , C_2 change from a parallel connection to a series connection. The operating principle of the converter is given in [24], and thus not mentioned in full here.

Suffice to say that the hybrid boost converter has two operating modes, namely, the switch turn-on mode and the switch turn-off mode. The two modes are shown in Fig. 3.1(b) and 3.1(c), respectively. In the first mode, L_1 is charged from the source, D_1, D_2 are reversed-biased, and C_1 , C_2 are discharged through S . In the second mode, the source and L_1 are charging C_1 , C_2 and C as well as supplying power to the load.

Fig. 3.1. The hybrid dc-dc boost converter: (a) overall converter circuit; (b) equivalent circuit for switch-on operation mode; (c) equivalent circuit for switch-off operation mode.

Letting $C_1 = C_2 = C$ and $x_4 = x_5$ and following the modelling procedure given in Chapter 2, the averaged state-space model of the hybrid dc-dc converter operating in CCM can be obtained as [44]:

$$\frac{d\bar{x}}{dt} = A\bar{x} + BV_{in} \quad (3.1)$$

where $\bar{x}^T = [\bar{x}_1 \quad \bar{x}_2 \quad \bar{x}_3 \quad \bar{x}_4]$ represents the vector of averaged state variables of the system. Here, $\bar{x}_1$ and $\bar{x}_2$ represent the average value of the inductor currents flowing through L_1 and L_2 , respectively, and $\bar{x}_3$ and $\bar{x}_4$ are the average voltages across capacitors C_o and C_1 , respectively. Also, matrices A and B are given by:

$$A = \begin{bmatrix} 0 & 0 & 0 & -\frac{1-d}{L_1} \\ 0 & 0 & -\frac{1}{L_2} & \frac{1+d}{L_2} \\ 0 & \frac{1}{C_0} & -\frac{1}{RC_0} & 0 \\ \frac{1-d}{2C} & -\frac{1+d}{2C} & 0 & 0 \end{bmatrix}, \quad B = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Here, d denotes the converter duty ratio, where $d \in [0,1]$.

By setting (3.1) to zero, the following equilibrium values are obtained:

$$X_1 = \frac{V_{ref}^2}{RV_{in}}, \quad X_2 = \frac{V_{ref}}{R}, \quad X_3 = V_{ref}, \quad X_4 = \frac{V_{ref}+V_{in}}{2}, \quad D = \frac{V_{ref}-V_{in}}{V_{ref}+V_{in}} \quad (3.2)$$

where X_1 , X_2 , X_3 , X_4 and D denote the equilibrium values of the averaged state variable $\bar{x}_1$, $\bar{x}_2$, $\bar{x}_3$, $\bar{x}_4$ and d , respectively. The symbols v_{in} and v_{ref} represent the input voltage and the reference converter output voltage, respectively.

3.3 Traditional Current-Mode Controller for the Hybrid Dc-Dc Boost Converter

The traditional current-mode controller (of the form used in [26], [43] – [44]) is given first to demonstrate its shortcoming in regulating systems with unknown load resistances.

In [44], a linear current-mode controller for the hybrid dc-dc boost converter has been proposed. The controller using the output inductor current for feedback purposes is given by:

$$d = D - K_P(\bar{x}_2(t) - X_2) - K_I \int (\bar{x}_3(\tau) - V_{ref}) d\tau \quad (3.3)$$

where K_P and K_I are the positive gains of the controller and $X_2 = \frac{V_{ref}}{R}$ represents the reference value of the output inductor current. The main drawback of this controller is that it requires the nominal value of the load resistance R to compute the control signal.

Therefore, this control law may not be applicable when R is unknown. To overcome this problem, the nonlinear adaptive current-mode controller is proposed in the following section.

3.4 Adaptive Current-Mode Controller for the Hybrid-Dc-Dc Boost Converter

In this section, the design of the nonlinear adaptive current-mode controllers for the hybrid boost converter is presented. The structure of the adaptive controllers follows that of (3.3) without the integral term and the estimated value of $1/R$ is generated using an adaptive law which now provides the integral action.

3.4.1 Proposed Adaptive Control Law

The adaptive current-mode control law for the hybrid boost converter is given by:

$$d = D - K_c[\bar{x}_i - \hat{X}_i(\hat{\theta})] \quad i = 1, 2 \quad (3.4)$$

where K_c is the gain of the adaptive controller, D is given by (3.2), x_i is the inductor current of the converter whose reference value $\hat{X}_i(\hat{\theta})$ is calculated using the estimate $\hat{\theta}$ of the load conductance. The estimate $\hat{\theta}$ is generated by the adaptive law given by [45]:

$$\frac{d\hat{\theta}}{dt} = -\frac{2\beta m e_3}{1 + \beta^2 e_3^2} \quad (3.5)$$

where β and m are the positive controller gains and $e_3 = \bar{x}_3 - V_{ref}$ denotes the output voltage error.

Setting $\frac{d\hat{\theta}}{dt} = h$, the first- and second-order time derivatives of h with respect to e_3 are:

$$\frac{dh}{de_3} = -\frac{2\beta m(1 - \beta^2 e_3^2)}{(1 + \beta^2 e_3^2)^2} \quad (3.6a)$$

$$\frac{d^2 h}{de_3^2} = \frac{8\beta^3 e_3 m(1-\beta^2 e_3^2)}{(1+\beta^2 e_3^2)^3} + \frac{4\beta^3 m e_3}{(1+\beta^2 e_3^2)^2} \quad (3.6b)$$

By setting (3.6a) to zero, the solutions of (3.6) can be obtained as $e_3 = \pm \frac{1}{\beta}$.

Substituting these solutions into (3.5) and (3.6b) gives $\frac{d^2 h}{de_3^2} < 0$ for $h = m$ and $\frac{d^2 h}{de_3^2} > 0$ for $h = -m$, respectively. Thus, m and $-m$ represent the global maximum and global minimum of h , respectively. Therefore, $\left| \frac{d\hat{\theta}}{dt} \right|$ is optimized and bounded by a user defined value m .

3.4.2 Adaptive Current-Mode Controller Using Input Inductor Current

Unlike the traditional boost converter, the hybrid dc-dc boost converter has more than one inductor current for feedback purposes. Thus, when using current-mode control of the converter, it is necessary to select the most appropriate inductor current for the controller design. The choice of the inductor current not only determines the range of controller parameters to ensure system stability, but it also affects the dynamic response of the controlled converter [26], [43] – [44]. Considering this, a detailed comparative study of two nonlinear adaptive current-mode controllers using the input and output inductor currents of the converter has been conducted. The adaptive current-mode controller using the input inductor current for feedback purposes is first studied.

The control law using the input inductor current is given by:

$$d = D - K_c[\bar{x}_1 - \hat{X}_1] \quad (3.7)$$

where

$$\hat{X}_1 = \frac{\hat{\theta} V_{ref}^2}{V_{in}} \quad (3.8)$$

Here, $\hat{X}_1$ is the estimated value of X_1 and $\hat{\theta}$ is obtained from (3.5). To gain an insight into the adaptive current-mode controlled system, the stability analysis is now provided.

The following errors are defined:

$$e_1 = \bar{x}_1 - X_1, \quad e_2 = \bar{x}_2 - X_2, \quad e_3 = \bar{x}_3 - X_3,$$

$$e_4 = \bar{x}_4 - X_4, \quad \tilde{\theta} = \hat{\theta} - \frac{1}{R} \quad (3.9)$$

Substituting (3.7) – (3.9) into (3.1) yields the error dynamics described by:

$$\frac{de_1}{dt} = \frac{1}{L_1} [-(1 - d_{e1})e_1 - (1 - d_{e1})X_4 + V_{in}] \quad (3.10a)$$

$$\frac{de_2}{dt} = \frac{1}{L_2} [-e_3 + (1 - d_{e1})e_4 - X_3 + (1 - d_{e1})X_4] \quad (3.10b)$$

$$\frac{de_3}{dt} = \frac{1}{C_o} (e_2 - \frac{1}{R} e_3) \quad (3.10c)$$

$$\frac{de_4}{dt} = \frac{1}{2C} [(1 - d_{e1})e_1 - (1 + d_{e1})e_2 + (1 - d_{e1})X_1 - (1 + d_{e1})X_2] \quad (3.10d)$$

$$\frac{d\tilde{\theta}}{dt} = -\frac{2\beta m e_3}{1 + \beta^2 e_3^2} \quad (3.10e)$$

where $d_{e1} = D - K_c(e_1 - \frac{\tilde{\theta} V_{ref}^2}{V_{in}})$. The equilibrium point of (3.10) can be obtained as:

$$e_{1\infty} = e_{2\infty} = e_{3\infty} = e_{4\infty} = \tilde{\theta}_\infty = 0 \quad (3.11)$$

Linearization of (3.10) about the equilibrium point (3.11) yields the following linearized system:

$$\dot{z} = M_{in} z \quad (3.12)$$

where $z^T = [z_1 \quad z_2 \quad z_3 \quad z_4 \quad z_5]$, $z_i = e_i - e_{i\infty}$, $j = 1, \dots, 4$, $z_5 = \tilde{\theta} - \tilde{\theta}_\infty$ and

$$M_{in} = \begin{bmatrix} -\frac{K_c X_4}{L_1} & 0 & 0 & -\frac{1-D}{L_1} & \frac{K_c X_4 V_{ref}^2}{L_1 V_{in}} \\ -\frac{K_c X_4}{L_2} & 0 & -\frac{1}{L_2} & \frac{1+D}{L_2} & \frac{K_c X_4 V_{ref}^2}{L_2 V_{in}} \\ 0 & \frac{1}{C_o} & -\frac{1}{RC_o} & 0 & 0 \\ \frac{(1-D)+K_c(X_1+X_2)}{2C} & -\frac{1+D}{2C} & 0 & 0 & \frac{K_c(X_1+X_2)V_{ref}^2}{2C V_{in}} \\ 0 & 0 & -2\beta m & 0 & 0 \end{bmatrix} \quad (3.13)$$

The linearized system (3.12) will be stable if the coefficients of the characteristic polynomial $p_{in}(s) = |sI - M_{in}|$, where s is a complex variable, meet the Routh-Hurwitz stability criterion.

For the purpose of illustration, consider the set of circuit parameters given in Table 3.1:

Table 3.1 Main parameters of the hybrid dc-dc boost converter system

Parameter	Value
V_{in}	5 V
V_{ref}	25 V
L_1, L_2	680 μH
C_1, C_2, C_o	220 μH (470 μH^*)
R	470 Ω (950 Ω^*)

* The value of the corresponding parameters used in the experiments.

Now, using the parameter given in Table 3.1 in (3.13), the characteristic polynomial of M_{in} is given as

$$p_{in}(s) = s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0 \quad (3.14)$$

where

$$a_4 = 2.21 \times 10^4 K_c + 9.67, \quad a_3 = 5.69 \times 10^5 K_c + 1.63 \times 10^7,$$

$$a_2 = 3.93 \times 10^{11} K_c + 2.51 \times 10^{10} K_c K_a + 9.34 \times 10^7,$$

$$a_1 = 4.75 \times 10^{12} K_c - 2.02 \times 10^{12} K_c K_a + 2.48 \times 10^{12}, \quad a_0 = 5.59 \times 10^{16} K_c K_a,$$

$$K_a = \beta m.$$

The Routh table for (3.14) is given by

$$\begin{array}{c|ccc} s^5 & 1 & a_3 & a_1 \\ s^4 & a_4 & a_2 & a_0 \\ s^3 & b_1 & b_2 & 0 \\ s^2 & c_1 & c_2 & 0 \\ s^1 & d_1 & 0 & 0 \\ s^0 & e_1 & 0 & 0 \end{array} \quad (3.15)$$

Where,

$$b_1 = \frac{a_3 a_4 - a_2}{a_4}, b_2 = \frac{a_1 a_4 - a_0}{a_4}, c_1 = \frac{b_1 a_2 - b_2 a_4}{b_1}, c_2 = a_0, d_1 = \frac{c_1 b_2 - c_2 b_1}{c_1}, e_1 = a_0.$$

According to the Routh-Hurwitz stability criterion, system (3.12) is asymptotically stable if and only if all the coefficients of the characteristic polynomial (3.14), viz., $a_i (i = 0, \dots, 4)$, and the first column of the Routh table (3.15), viz., b_1, c_1, d_1 and e_1 , are greater than zero. Since all $a_i (i = 0, \dots, 4)$, b_1, c_1, d_1 and e_1 are functions of K_a and K_c , a system stability region can be determined in the $K_c - K_a$ plane. If K_a and K_c are selected in the system stability region, the linearized system (3.12) is asymptotically stable. Solving $a_0 > 0, a_2 > 0, a_3 > 0$ and $a_4 > 0$ yields $K_c > 0$ and $K_a > 0$. Then, a second-degree relation between K_a and K_c , which is given as a hyperbola in the $K_c - K_a$ plane, is obtained by solving $b_1 > 0$. Finally, by solving $c_1 > 0$ and $d_1 > 0$, two high-degree relations between K_a and K_c are also identified. The stability region of linearized system (3.12) using the circuit parameters given in Table 3.1 is shown in Fig. 3.2.

The plots of $a_1 > 0$ and $c_1 > 0$ are quite far from the origin, and thus, are not shown in this figure. The shaded area represents the stability region. It is evident that, for the nonlinear adaptive controller designed using the input inductor current, the ranges of the controller gains to ensure system stability are quite narrow.

Fig. 3.2. Stability region for system using adaptive current-mode controller based on input inductor current.

3.4.3 Adaptive Current-Mode Controller Using Output Inductor Current

This section presents the nonlinear adaptive current-mode controller using the output inductor current x_2 for feedback purposes. The adaptive control law is given by:

$$d = D - K_c[x_2 - \hat{X}_2] \quad (3.16)$$

where

$$\hat{X}_2 = \hat{\theta}V_d \quad (3.17)$$

Here, $\hat{X}_2$ is the estimated value of X_2 . Like what was done in the previous section, substituting (3.9) and (3.16) – (3.17) into (3.1) yields a set of dynamic equations with a unique equilibrium point (3.11). The corresponding linearized model has a coefficient matrix M_{out} given by:

$$\dot{z} = M_{out}z \quad (3.18)$$

where

$$M_{out} = \begin{bmatrix} 0 & -\frac{K_c X_4}{L_1} & 0 & -\frac{1-D}{L_1} & \frac{K_c X_4 V_{ref}}{L_1} \\ 0 & -\frac{K_c X_4}{L_2} & -\frac{1}{L_2} & \frac{1+D}{L_2} & \frac{K_c X_4 V_{ref}}{L_2} \\ 0 & \frac{1}{C_o} & -\frac{1}{RC_o} & 0 & 0 \\ \frac{1-D}{2C} & \frac{K_c(X_1+X_2)-(1+D)}{2C} & 0 & 0 & -\frac{K_c(X_1+X_2)V_{ref}}{2C} \\ 0 & 0 & -2\beta m & 0 & 0 \end{bmatrix}$$

Using the same set of circuit parameter values given in Table 3.1, the characteristic polynomial of M_{out} obtained is

$$p_{out}(s) = s^5 + \hat{a}_4 s^4 + \hat{a}_3 s^3 + \hat{a}_2 s^2 + \hat{a}_1 s + \hat{a}_0 \quad (3.19)$$

where

$$\hat{a}_4 = 2.21 \times 10^4 K_c + 9.67, \quad \hat{a}_3 = -1.56 \times 10^6 K_c + 1.63 \times 10^7,$$

$$\hat{a}_2 = 4.91 \times 10^{10} K_c + 5.01 \times 10^9 K_c K_a + 9.34 \times 10^7,$$

$$\hat{a}_1 = 4.91 \times 10^{11} K_c - 4.04 \times 10^{11} K_c K_a + 2.48 \times 10^{12}, \quad \hat{a}_0 = 1.12 \times 10^{16} K_c K_a,$$

$$K_a = \beta m.$$

Following the same procedure that was used in the previous section, the stability region of (3.19) can be obtained and is shown in Fig. 3.3, where $\hat{b}_1$, $\hat{c}_1$ and $\hat{d}_1$ are the coefficients in the first column of the Routh table for (3.19). Again, the shaded area represents the stability ranges for K_c and K_a . Since K_c and K_a are positive, the conditions of $\hat{a}_0 > 0$, $\hat{a}_2 > 0$ and $\hat{a}_4 > 0$ are naturally achieved. As such, these conditions are not shown in Fig. 3.3.

Fig. 3.3. Stability region for the system using adaptive current-mode controller based on output inductor current.

It can be seen from Fig. 3.3 that the adaptive current-mode controller using the output inductor current leads to a broader range of controller gains to be used to give a stable system. This allows the designer to vary the controller gains over a wider range to achieve the desired output response. Therefore, the adaptive controller using the output inductor current should be preferred over the controller using the input inductor current.

3.4.4 Validation of Results

In order to verify the theoretical conclusions obtained in sections 3.4.2 and 3.4.3, some simulations were carried out using MATLAB. The output response of the adaptive current-mode controller using the input inductor current was compared with that of the adaptive controller using the output inductor current. The same set of circuit parameter values given in Table 3.1 was used to obtain the results.

Figs. 3.4(a) and 3.4(b) show the transient responses of the adaptive controller using the input inductor current. From Fig. 3.4(a), it is seen that as the value of K_c increases, the oscillations in the transient response were reduced and the settling time of the response was much shorter. However, there is a limit to the maximum value of K_c which can be used to ensure system stability, and the response becomes unstable even for very small values of K_c (see Fig. 3.4(b)).

To solve this problem, the adaptive controller using the output inductor current was used. Figs. 3.4(c) and 3.4(d) show the transient output response obtained. It can be seen that even though there are oscillations for small values of K_c , these oscillations can be suppressed by increasing K_c to a sufficiently large value without losing the system stability. This is in agreement with the theoretical conclusion that the range of controller

gains to ensure system stability increases considerably when the output inductor current was used for feedback purposes.

Fig. 3.4. Output responses of the controlled hybrid dc-dc boost converter: (a) for controller using input inductor current with $K_c = 0.0005$, $K_a = 0.1$ ($\beta = 0.1$ and $m = 1$) (red dotted) and $K_c = 0.0015$, $\beta = 0.1$ and $m = 1$ (blue); (b) for controller using input inductor current with $K_c = 0.005$, $K_a = 0.1$ ($\beta = 0.1$ and $m = 1$); (c) for controller using output inductor current with $K_c = 0.1$, $K_a = 0.1$ ($\beta = 0.1$ and $m = 1$); (d) for controller using output inductor current with $K_c = 2$, $K_a = 0.1$ ($\beta = 0.1$ and $m = 1$).

3.5 Simulation and Experimental Results

In this section, simulation and experimental results are provided to show the effectiveness of the proposed controller using the output inductor current for the regulation of the hybrid high-order dc-dc boost converter. The following parameter values of the converter circuit were used in both simulations and experiments.

3.5.1 Simulation Results

In order to show the merits of the proposed controller using the output inductor current, a comparison study between the traditional current-mode controller (3.3) and the

proposed controller (3.16) was carried out. In this comparison study, the value of the load resistance R was changed from $950\ \Omega$ to $470\ \Omega$ at $t = 2\text{ s}$ and was restored to $950\ \Omega$ at $t = 3\text{ s}$.

Fig. 3.5 shows the output voltage responses of the controlled hybrid boost converter using different controllers. The dashed blue waveform shows the output response obtained using the traditional current-mode control while the solid red waveform shows the output response obtained using the proposed controller. It can be seen from Fig. 3.5(a) that when the small value of the integral gain K_I of the traditional current-mode controller, i.e., $K_I = 0.1$ was employed, both controllers provide similar control performance at the converter start-up stage. However, the proposed controller has better performance in the presence of load disturbances as compared to that obtained using the traditional current-mode controller. When the value of the integral gain K_I was increased to $K_I = 0.8$, it can be seen from Fig. 3.5(b) that even though both controllers have similar performance in the presence of load disturbances, the proposed controller provides an output voltage response with a smaller overshoot and a shorter settling time at the converter start-up stage.

Considering both Figs. 3.5(a) and 3.5(b), it is evident that when the converter is regulated by the traditional current-mode controller, there exists a “trade-off” between the transient performances at the converter start-up stage and that after the onset of the load disturbances. However, this trade-off problem is avoided if the proposed controller is adopted. Both excellent transient responses at the start-up stage and that after the onset of load disturbances can be achieved simultaneously. Hence, the proposed controller is more suitable for regulating the hybrid dc-dc boost converter than its traditional counterpart.

Fig. 3.5. Output voltage responses of the regulated hybrid boost converter (the dashed blue line is the output response obtained using the traditional current-mode controller while the solid red line is the output response obtained using the proposed controller based on the output inductor current): (a) $K_P = 0.2$, $K_I = 0.1$ for the traditional controller, $K_c = 0.05$, $\beta = 0.5$, $m = 0.12$ for the proposed controller; (b) $K_P = 0.2$, $K_I = 0.8$ for the traditional controller, $K_c = 0.05$, $\beta = 0.5$, $m = 0.12$ for the proposed controller.

3.5.2 Experimental Results

To verify the effectiveness of the proposed adaptive controller in regulating the practical hybrid boost converter, a laboratory prototype of regulated converter circuit was built. The prototype and the controller circuit schematic are shown in Figs. 3.6 and Fig. 3.7, respectively. Also, to compare the performance of the proposed adaptive controller with that of the traditional current-mode controller, the later were also built. The controllers were implemented using analog components. More specifically, LM 741 was used to

implement some basic mathematical functions, such as summer, integrator, etc., and the LEM LTS-6NP current transducer was used to measure the inductor current. The division and square functions were achieved by using the combination of AD633 and AD711. The optical-coupler HCPL3140 was used to drive the MOSFET IRFP250 at a switching frequency of 20 kHz. To avoid the saturation problem in the analog implementations, the feedback gain of the output voltage was set as 0.1, and, correspondingly, the reference output voltage V_{ref} and input voltage v_{in} were also set at 0.1 times their nominal values.

Fig. 3.6. Laboratory prototype of: (a) hybrid dc-dc boost converter, and (b) the proposed controller.

3.5.2.1 Traditional Current-Mode Controller

In this section, the regulation performance of the traditional current-mode controller (3.3) is presented. Figs. 3.8(a) and 3.8(b) show the output voltage responses in the presence of load changes for $K_P = 3$ and $K_I = 1.5$ and $K_P = 3$ and $K_I = 7$, respectively. The load resistance R was changed from 950Ω to 470Ω and then back to 950Ω . As can be seen from Fig. 3.8(a), the worst-case overshoot and settling time of the load change response were $\sim 16\%$ of V_{ref} and ~ 1.2 s, respectively, when

the traditional current-mode controller was employed. When the value of K_I was increased to improve the load change response, the overshoot and settling time in the start-up transient output response were found to be $\sim 28\%$ and ~ 1.2 s, respectively (see Fig. 3.8(b)). As such, there is a trade-off between the qualities of the transient response and the load change response when the traditional current-mode controller is used.

Fig. 3.8. Output responses using traditional current-mode control: (a) in the presence of load changes for $K_P = 3$ and $K_I = 1.5$; (b). Output response in the presence of load changes for $K_P = 3$ and $K_I = 7$.

3.5.2.2 Adaptive Current-Mode Controller

Based on the conclusion of section 3.4.3, the controller (3.16) using the output inductor current was implemented, with $\beta = 1$, $m = 1$ and $K_c = 3.33$. The specifications of the desired control performance ~~is~~ are given in Table 3.2.

Fig. 3.9(a) shows the output voltage start up response and the output response when the load resistance R was changed from 950Ω to 470Ω and then back to 950Ω . As compared to the output responses given in Figs. 3.8(a) and 3.8(b), the “trade-off” problem was avoided and a faster output voltage response with a reduced overshoot was obtained for both the start-up response and the load change response. The settling time and overshoot of the start-up output voltage response were reduced to ~ 0.7 s and $\sim 4\%$ of V_{ref} , respectively, and the settling time of the load change response was reduced to ~ 0.5 s when the proposed controller was employed. The output voltage response under

Table 3.2 Specifications of the desired control performance using controller (3.16)

Performance	Value
Start-up overshoot	$\leq 5\%$
Start-up settling time	$\leq 1s$
Voltage dip (swell) in the presence of load resistance changes	$\leq 10\%$
Settling time in the presence of load resistance changes	$\leq 1s$
Voltage dip (swell) in the presence of input voltage changes	$\leq 10\%$
Settling time in the presence of input voltage changes	$\leq 1s$

the input voltage changes is shown in Fig. 3.7(b). Again, the output voltage was restored to its nominal value (25 V) after the onset of the input voltage changes with a considerably small variation and short settling time. Fig. 3.9(c) shows the output voltage response when V_{ref} was changed from 25 V to 15 V and then back to 25 V. An accurate and fast tracking was achieved. These results show that the proposed controller is competent to regulate the converter, and meets all the specified control requirements given in Table 3.2. Besides, it provides better performance as compared to the traditional current-mode controller. The experimental results are in good agreement with the simulation results.

Fig. 3.9. Output responses using adaptive current-mode control: (a) in the presence of load changes; (b) in the presence of input voltage changes; (c) in the presence of reference input changes.

3.6 Conclusion

In this chapter, nonlinear adaptive current-mode controllers for the regulation of the hybrid high-order boost converter in the presence of an unknown load were presented. A comparative study involving the adaptive controllers using the input and output inductor currents was carried out. By using the Routh-Hurwitz stability criterion, the controller based on the output inductor current was found to be more suitable for regulating the hybrid boost converter. Besides, some simulation and experimental results comparing the performance of the traditional and the proposed adaptive current-mode controllers were obtained and they show that the latter is more superior to the former.

Chapter 4

Improved Voltage-Mode Controllers for High-Gain DC-DC Converters

4.1 Introduction

The voltage-mode control scheme is a type of output-feedback control technique. In this control scheme, the converter output voltage is the only required measurement for feedback purposes. Therefore, its implementation does not require the current sensor. As a consequence, the complexity and cost of the regulated converter system implementation are reduced. Besides, the space needed to accommodate the current sensor in the aforementioned implementation is not needed anymore. Therefore, this current sensor-less feature also increases the power density of the regulated converter system. However, due the non-minimum phase feature of the boost converters, the use of the traditional voltage-mode controller results in a very limited control bandwidth and an extremely low robustness for the closed-loop converter systems [26]. In order to overcome these disadvantages, several voltage-mode controllers using the simplified parallel-damped passivity-based control technique have been proposed for high-gain converters [29] – [34]. Although these voltage-mode controllers were found to give a satisfactory performance, there still exists some areas that need to be improved. They are as follows:

- There are no systematic guidelines for the controller gain selection. As such, the controller gains are mainly selected based on a trial and error approach.
- In the control law, there is a risk of control signal saturation due to division by zero. The saturation of the control law will result in a deterioration in the control

performance.

- There is a “trade-off” between the performances of the transient responses after the onset of a reference input and load disturbance changes.

Considering all these, some studies on the voltage-mode control of high-gain boost dc-dc converters are addressed in this chapter. Three improved voltage-mode controllers are separately proposed for three different converters. The corresponding closed-loop stability analyses are carried out. In addition, the simulation results as well as the experimental results are provided to support the theoretical conclusions.

4.2 Investigation of a voltage-mode controller for a dc-dc multilevel boost converter

In this section, a voltage-mode controller is proposed for the regulation of a MBC [42]. The schematic of an N-level MBC is shown in Fig. 4.1. Despite the non-minimum phase obstacle presented by this boost dc-dc converter, the regulation of the output voltage is achieved without employing the current sensor. Unlike some state-of-the-art voltage-mode controllers where the selection of controller gains mainly relies on a trial and error approach and contains a significant empirical component, the design of the proposed controller is carried out using the classical frequency domain technique, and the Bode-plot is used to directly select the controller gains based on the system’s phase margin and gain margin criteria. The feasibility of the controller is also shown. Finally, some experimental results are provided to show the effectiveness of the proposed controller in regulating a 3-level MBC in the presence of load and line voltage disturbances.

Fig. 4.1. Schematic diagram of an N -level MBC.

4.2.1 Model of The Dc-Dc Multi-Level Boost Converter

In section 2.3.4, the reduced-order model for the N -Level MBC is presented. Because of the simple structure and generality of the reduce-order model, it is very suitable for the controller design.

From section 2.3.4, the reduced-order model is given by:

$$\frac{di_L}{dt} = -\frac{1-d}{NL} v_o + \frac{v_{in}}{L} \quad (4.1)$$

$$\frac{dv_o}{dt} = \frac{1}{C(1+d)} \left[(1-d)i_L - \frac{N}{R} v_o \right] \quad (4.2)$$

where i_L and v_o represent the inductor current and output voltage of the converter and N is the level of the MBC. Also, v_{in} and R represent the input voltage and load resistance, respectively, and L and C are the inductor and capacitor values respectively. Here, d is the converter duty ratio, where $d \in [0,1]$.

Now, by setting (4.1) and (4.2) to zero, the equilibrium values of the state variables v_o and i_L and control signal d are obtained as:

$$V_o = V_{ref}, \quad I_L = \frac{V_{ref}^2}{v_{in}R}, \quad D = 1 - \frac{Nv_{in}}{V_{ref}} \quad (4.3)$$

where V_{ref} is the desired reference output voltage of the converter.

4.2.2 Proposed Voltage-Mode Controller

In this section, the proposed voltage-mode controller for the regulation of the MBC is described. The limitation of the traditional voltage-mode controller for the MBC is shown first in order to appreciate the significance of the proposed controller.

4.2.2.1 Traditional voltage-mode controller or PI controller

The transfer function of the traditional PI control law for the dc-dc converters is given by [30], [32]:

$$G_C(s) = \frac{d(s)}{e(s)} = K_{P1} + \frac{K_{I1}}{s} \quad (4.4)$$

where $d(s)$ is the controller output, $e(s) = (V_{ref}(s) - v_o(s))$ is the output voltage error, which is the controller input, $K_{P1} > 0$ and $K_{P2} > 0$ are controller gains and s is a complex variable.

Now, by linearizing (4.1) – (4.2) around the equilibrium point (4.3) and applying the Laplace transform to the resulting linearized system, the control input (d) to output voltage (v_o) transfer function can be obtained as:

$$G_{plant}(s) = \frac{v_o(s)}{d(s)} = -\frac{b_1s+b_0}{a_2s^2+a_1s+a_0} \quad (4.5)$$

where $b_1 = LV_{ref}^4$, $b_0 = -Rv_{in}^2V_{ref}^2$, $a_2 = v_{in}RCLV_{ref}(2V_{ref} - Nv_{in})$, $a_1 = v_{in}LNV_{ref}^2$, and $a_0 = v_{in}^3NR$.

Using (4.4) and (4.5), the loop gain $G_L(s)$ of the resulting controlled system is given by:

$$G_L(s) = G_{plant}(s)G_C(s) = -\frac{K_{P1}\left(s+\frac{K_{I1}}{K_{P1}}\right)(b_1s+b_0)}{s(a_2s^2+a_1s+a_0)} \quad (4.6)$$

Now, consider the converter parameter values given in Table 4.1:

Table 4.1 Main parameters of the MBC system

Parameter	Value
v_{in}	5 V
V_{ref}	25 V
L	1 mH
C	1 mF
R	500 Ω
N	3
f_{sw}	40 kHz

Substituting the parameters given in Table 4.1 in (4.6), the Bode-plot of the loop-gain $G_L(s)$ for varying values of K_{P1} is shown in Fig. 4.2.

Fig. 4.2. Frequency responses of $G_L(s)$ using different values of K_{P1} .

It can be seen that there exists a resonance peak in the low-frequency range of the Bode-plot of $G_L(s)$. This happens for a wide range of controller gains. As such, it is difficult to design a stable controlled system while ensuring a good system dynamic response [54]. Hence, the traditional voltage-mode controller is not quite suitable for the

regulation of the MBC. In next section, the proposed voltage-mode controller for the regulation of the MBC is described.

4.2.2.2 The proposed controller

The proposed control law to be considered is given by:

$$d = 1 - \frac{Nv_{in}}{z_d} \quad (4.7)$$

$$\frac{dz_d}{dt} = \frac{1}{C_{eq}} [-(K_1 + K_2)z_d + K_2v_o + K_1z_{d_ref}] \quad (4.8)$$

$$z_{d_ref} = K_{P2}(V_{ref} - v_o) + K_{I2} \int (V_{ref} - v_o) dt \quad (4.9)$$

Here, K_{P2} , K_{I2} , K_1 , and K_2 are the controller gains and $C_{eq} = C \left(2 - \frac{Nv_{in}}{V_{ref}} \right)$ is the value of the equivalent output capacitor, z_d is an artificial voltage variable. This controller structure is motivated by the structure of the simplified parallel-damped passivity-based controller (PBC) for the traditional boost converter [30]. The structure given by (4.7) – (4.8) is derived based on the expression of the equilibrium value of the averaged duty ratio, i.e., $D = 1 - \frac{Nv_{in}}{V_{ref}}$ (given in (4.3)) like what was done in [30] for the traditional boost converter. Also, additional integral and proportional actions (4.9) are incorporated in (4.8) for improved performance of the controlled system.

Unlike [31] – [33], the structure of the proposed controller is such that the controller design can be carried out using the classical frequency domain approach. This avoids the use of a trial and error method for the selection of the controller gains. The Bode-plot can now be employed to design the controller gains based on the system's phase margin and gain margin criteria. Also, note that in contrast to [26] – [27] and [44], the proposed control law is independent of the load resistance R . This allows the implementation of the proposed controller for some practical applications wherein R

is unknown. Fig. 4.3 shows the block diagram of the proposed closed-loop controlled converter system. The augmented converter dynamic shown in Fig.4.3 is actually obtained by substituting (4.7) into the reduced-order model of the MBC (4.1) – (4.2) and then combining the resulting dynamics with the proposed control law (4.8) – (4.9).

Fig. 4.3. Block diagram of the proposed closed-loop MBC system.

4.2.2.3 Controller design

In order to obtain the equilibrium point of the overall closed-loop system, the closed-loop converter dynamics is first analyzed. Substituting (4.7) and (4.9) into (4.1) – (4.2) and (4.8) yields the following system dynamics:

$$\frac{di_L}{dt} = -\frac{v_{in}}{Lz_d}v_o + \frac{v_{in}}{L} \quad (4.10)$$

$$\frac{dv_o}{dt} = \frac{z_d}{C(2z_d - N)} \left(\frac{Nv_{in}}{z_d}i_L - \frac{N}{R}v_o \right) \quad (4.11)$$

$$\frac{dz_d}{dt} = \frac{1}{C_{eq}} \{ -(K_1 + K_2)z_d + K_2v_o + K_1[K_{P2}(V_{ref} - v_o) + \theta] \} \quad (4.12)$$

$$\frac{d\theta}{dt} = K_{I2}(V_{ref} - v_o) \quad (4.13)$$

where $\theta = K_{I2} \int (V_{ref} - v_o) dt$. By setting (4.10) – (4.13) to zero, the unique equilibrium point of the system can be obtained as:

$$(I_L, V_o, Z_d, \theta_\infty) = \left(\frac{V_{ref}^2}{v_{in}R}, V_{ref}, V_{ref}, V_{ref} \right) \quad (4.14)$$

where Z_d and θ_∞ are the steady-state values of z_d and θ , respectively. Using (4.9), (4.13) and (4.14), the steady-state value of z_{d_ref} is given by:

$$Z_{d_ref} = \theta_\infty = V_{ref} \quad (4.15)$$

Next, the design of the augmented converter dynamics is presented. Linearizing the augmented converter dynamics shown in Fig. 4.2 around the equilibrium point (I_L, V_o, Z_d) given by (4.14) and using (4.15), the corresponding small-signal model of the augmented converter system can be obtained as:

$$\dot{\tilde{x}} = A_{acd}\tilde{x} + B_{acd}\tilde{z}_{d_ref} \quad (4.16)$$

where

$\tilde{x} = [\tilde{i}_L, \tilde{v}_o, \tilde{z}_d]^T$, $\tilde{i}_L = i_L - I_L$, $\tilde{v}_o = v_o - V_o$, $\tilde{z}_d = z_d - Z_d$, $\tilde{z}_{d_ref} = z_{d_ref} - Z_{d_ref}$ and matrices A_{acd} and B_{acd} are given by:

$$A_{acd} = \begin{bmatrix} 0 & -\frac{v_{in}}{LV_{ref}} & \frac{v_{in}}{LV_{ref}} \\ \frac{Nv_{in}}{C_{eq}V_{ref}} & -\frac{N}{C_{eq}R} & -\frac{N}{C_{eq}R} \\ 0 & \frac{K_2}{C_{eq}} & -\frac{K_1+K_2}{C_{eq}} \end{bmatrix}, B_{acd} = \begin{bmatrix} 0 \\ 0 \\ \frac{K_1}{C_{eq}} \end{bmatrix}$$

Now, applying the Laplace transform to (4.16) and assuming $\tilde{x}(0) = 0$ and $\tilde{z}_{d_ref}(0) = 0$ gives:

$$\frac{\tilde{x}(s)}{\tilde{z}_{d_ref}(s)} = M_{acd}(sI - A_{acd})^{-1}B_{acd} \quad (4.17)$$

where M_{acd} is the output vector, I is the 3x3 identity matrix. Setting $M_{acd} = [0 \quad 1 \quad 0]$, the transfer function $G_{Aug}(s) = \tilde{v}_o(s)/\tilde{z}_{d_ref}(s)$ can be obtained as:

$$G_{Aug}(s) = \frac{\tilde{v}_o(s)}{\tilde{z}_{d_ref}(s)} = \frac{c_1s+c_0}{d_3s^3+d_2s^2+d_1s+d_0} \quad (4.18)$$

where

$$c_1 = -K_1 L N V_d^2, \quad c_0 = K_1 N R v_{in}^2, \quad d_3 = L R C_{eq}^2 V_d^2,$$

$$d_2 = C_{eq} L V_d^2 (N + K_1 R + K_2 R), \quad d_1 = C_{eq} N R v_{in}^2 + L N V_d^2 (K_1 + 2K_2),$$

$$d_0 = K_1 N R v_{in}^2$$

From (4.18), it can be seen that the controller gains K_1 and K_2 can directly affect the frequency response of the augmented converter dynamics. Now, the Bode-plot can be applied to select the values of the controller gains for the augmented converter system. For the purpose of illustration, consider the converter parameter values given by Table 4.1. Substituting the given parameters into (4.18) gives

$$G_{Aug}(s) = -\frac{c_1' s + c_0'}{d_3' s^3 + d_2' s^2 + d_1' s + d_0'} \quad (4.19)$$

where

$$c_1' = -(1.5 \times 10^5) K_1, \quad c_0' = (3 \times 10^9) K_1, \quad d_3' = 49,$$

$$d_2' = (3.5 \times 10^4 K_1 + 3.5 \times 10^4 K_2 + 210),$$

$$d_1' = (1.5 \times 10^5 K_1 + 3 \times 10^5 K_2 + 4.2 \times 10^6), \quad d_0' = (3 \times 10^9 K_1)$$

Fig. 4.4 shows the effects of varying the controller gains K_1 and K_2 on the Bode-plot of $G_{Aug}(s)$ given by (4.19). The dotted blue line shows the frequency response of $G_{Aug}(s)$ obtained using $K_1 = 0.1$ and $K_2 = 0.05$.

It can be seen that there exists a small resonance peak with magnitude 5.46 dB in the low-frequency region of the Bode-plot. The frequency response $G_{Aug}(s)$ using $K_1 = 0.8$ and $K_2 = 0.05$ is shown by the dashed green line in Fig. 4.4. It can also be seen

Fig. 4.4. Frequency responses of $G_{Aug}(s)$ for different values of K_1 and K_2 .

that the magnitude of the resonance peak in the low-frequency region became larger, i.e., 27.1 dB when K_1 was increased. Hence, increasing K_1 increases the magnitude of the resonance peak in the low-frequency region of the Bode-plot. The frequency response of $G_{Aug}(s)$ using $K_1 = 0.1$ and $K_2 = 0.3$ is shown by the solid red line in Fig. 4.4. It is seen that increasing K_2 can suppress the resonance peak in the low-frequency region. Since the presence of the resonance peak in the low frequency region of the Bode-plot of $G_{Aug}(s)$ complicates the design of the outer voltage-loop controller, a small value of K_1 and a large value of K_2 should be used to achieve a good resonance damping [54]. Therefore, to achieve a satisfactory frequency response, the values of K_1 and K_2 used were 0.1 and 0.3, respectively.

Next, the design of the outer voltage-loop controller is addressed. From (4.9), the transfer function of the voltage-loop PI controller $G_{PI}(s)$ is given by:

$$G_{PI}(s) = \frac{K_{P2}s + K_{I2}}{s} \quad (4.20)$$

Using (4.19) and (4.20), the open-loop transfer function of the controlled system can be obtained as:

$$G_v(s) = G_{PI}(s) \quad G_{Aug}(s) = \frac{-306.12K_{P2}(s-2 \times 10^4)\left(s+\frac{K_{I2}}{K_{P2}}\right)}{s(s+87.26)(s^2+202.7s+7.02 \times 10^4)} \quad (4.21)$$

In order to achieve a stable and robust closed-loop output voltage response, the following design criteria are chosen [46], [54]: (a) the system should have a sufficient gain margin and phase margin to ensure robust stability; (b) high gain in the low-frequency region of the Bode-plot to achieve a small steady-state output error; (c) a slope of -20dB/dec near the gain crossover frequency to ensure system relative stability.

Fig.4.5. Frequency responses of loop gain $G_v(s)$ for $K_1 = 0.1$, $K_2 = 0.3$, $K_{P2} = 0.7$ and $K_{I2} = 120.4$.

Based on above criteria, $K_{P2} = 0.7$ and $K_{I2} = 120.4$ were selected. The Bode-plot of the corresponding loop-gain $G_v(s)$ is shown in Fig. 4.5. It can be seen that the magnitude of the Bode-plot in the low-frequency region, i.e., at 1 Hz, is ~ 26 dB which ensures a small steady-state output error and a slope of -20dB/dec is achieved near the gain crossover frequency of ~ 16 Hz. Also, the gain margin and phase margin are obtained as 7.54 dB and 52.1° , respectively.

4.2.2.4 Controller feasibility

Next, the feasibility of the proposed controller is investigated by analyzing the internal stability of the closed-loop system. By rearranging (4.7), z_d can be rewritten as:

$$z_d = \frac{Nv_{in}}{1-d} \quad (4.22)$$

Substituting (4.2), (4.8) and (4.22) into the derivative of (4.7) yields:

$$\dot{d} = \frac{(1-d)^2}{CNv_{in}(1+d)} (K_1 z_{dref} + K_2 v_o) - \frac{1-d}{C(1+d)} (K_1 + K_2) \quad (4.23)$$

where $\dot{d}$ is the time derivative of the control signal d .

Using the steady-state values of v_o and z_{dref} , i.e., $V_o = V_{ref}$ and $Z_{dref} = V_{ref}$ in (4.23) gives

$$\dot{d} = \frac{(K_1 + K_2)(1-d)}{C(1+d)} \left[\frac{(1-d)V_{ref}}{Nv_{in}} - 1 \right] \quad (4.24)$$

Fig. 4.6 shows the phase-portrait of (4.24). It can be seen $D = 1 - \frac{Nv_{in}}{V_{ref}}$ is the unique stable equilibrium point of the system.

Fig. 4.6. ‘Remaining dynamics’ for the voltage-controlled converter.

From the preceding analyses, it is seen that the proposed control law given by (4.7) – (4.9) locally asymptotically stabilizes the reduced-order model of the MBC system (4.1) – (4.2) for appropriate values of K_{P2} , K_{I2} , K_1 and K_2 , and the state variables i_L and

v_o will asymptotically converge to their equilibrium values given by $\frac{V_{ref}^2}{v_{in}R}$ and V_{ref} , respectively for any $0 < R < \infty$.

4.2.3 *Simulation and Experimental Results*

To show the effectiveness of the proposed control law for the MBC, some simulation as well as laboratory experiments were carried out. The same set of circuit parameter values used in section 4.2.2, given by Table 4.1, was also used to obtain the results.

4.2.3.1 *Simulation results*

In order to show the effectiveness of the proposed controller over a wide range of operating conditions, some simulations were first carried out using MATLAB version R2014a. Fig. 4.7(a) shows the output voltage responses of the controlled converter system in the presence of some load variations. It can be seen that the proposed controller can successfully regulate the dc-dc converter for a wide range of load ranging from $R = 1 \text{ k}\Omega$ to $R = 50 \text{ }\Omega$. Also, Fig. 4.7(b) shows the output voltage responses in the presence of some input voltage variations. Again, it can be seen that the proposed controller is able to handle some large variations in the input voltage, i.e., from $E = 15 \text{ V}$ to $E = 3.5 \text{ V}$. All these results verify the ability of the proposed controller to regulate the dc-dc converter over a wide range of operating conditions.

4.2.3.2 *Experimental results*

Next, some experimental results are presented to show the effectiveness of the proposed voltage-mode controller for the high-gain dc-dc converter. The laboratory prototype of the regulated 3-level MBC and the circuit schematic of the propose controller are shown

(a)

(b)

Fig. 4.7. Output voltage v_o of the controlled converter system: (a) in the presence of load changes; (b) in the presence of input voltage changes.

in Figs. 4.8 and 4.9, respectively. Again, the controller was realized using simple analog devices, and the division function was implemented using AD633 IC and AD711 IC. Also, the switching frequency used was 40 kHz, as shown in Table 4.1. The specifications of the desired control performance is given in Table 4.2.

The various output voltage responses obtained under different operating conditions are given in Fig. 4.10. Fig. 4.10(a) shows the step output voltage response of the system. The

Fig 4.8. Laboratory prototype of the regulated 3-level MBC.

values of the controller gains used to achieve a satisfactory response were $K_{p2} = 0.7$, $K_{I2} = 120.4$, $K_1 = 0.1$ and $K_2 = 0.3$. It can be seen that the output voltage rapidly reached the desired reference voltage with a small overshoot and a negligible steady-state error. Also, the settling time obtained was ~ 0.1 s. Fig 4.8(b) shows the output voltage response when the load resistance R was changed from $500\ \Omega$ to $250\ \Omega$ and then back to $500\ \Omega$. The disturbances in the output voltage were rejected in a worst-case settling time of ~ 0.2 s with a very small overshoot of $\sim 8\%$ of the nominal output voltage.

Next, the ability of the proposed controller to handle the line input voltage and reference voltage variations were investigated. Fig. 4.10(c) shows the system response in the presence of changes in the line input voltage v_{in} from 5 V to 3.3 V and then back to 5 V. Again, the output voltage was rapidly restored to its nominal value with a settling time of ~ 0.1 s and a small overshoot. Fig. 4.10(d) shows the system response when the reference voltage V_{ref} was changed from 25 V to 30 V and then back to 25 V. Again a

fast and accurate voltage tracking was achieved. All these results show that the proposed controller met the control performance specifications given in Table 4.2. Therefore, the proposed voltage-mode controller is competent to regulate the 3-level MBC.

Table 4.2 Specifications of the desired control performance

Performance	Value
Start-up overshoot	$\leq 5\%$
Start-up settling time	$\leq 0.5s$
Voltage dip (swell) in the presence of load resistance changes	$\leq 10\%$
Settling time in the presence of load resistance changes	$\leq 0.5s$
Voltage dip (swell) in the presence of input voltage changes	$\leq 10\%$
Settling time in the presence of input voltage changes	$\leq 0.5s$

4.2.4 Conclusion

In this section, an improved voltage-mode control law for the regulation of the dc-dc MBC was proposed. The structure of the proposed controller is such that it allows the direct use of the Bode-plot to select the appropriate values of the controller gains to ensure system robust stability. The proposed controller was shown to be feasible. Besides, some simulation and experimental results for a 3-level MBC verified the ability of the controller to regulate the dc-dc converter over a wide range of operation conditions. The proposed voltage-mode control law can also be applied to regulate other high-order dc-dc boost converters, noting that its structure may vary slightly as per the expression of an equilibrium value of the duty-ratio of the specific converter.

Fig. 4.10. System output voltage v_o (CH. 1) and control signal u (CH. 2) of the controlled converter system: (a) at the start-up stage; (b) in the presence of load changes from 500Ω to 250Ω (and vice versa); (c) in the presence of input voltage changes from 5 V to 3.3 V (and vice versa); (d) in the presence of reference voltage changes from 25 V to 30 V (and vice versa).

4.3 An Improved Output Feedback Controller Design for The Super-Lift Re-Lift Luo Converter

In this section, the development of an improved output feedback controller for the POSRL converter is presented. The schematic of the POSRL converter is shown in Fig. 4.11. The main advantage of the proposed controller is that it achieves the output voltage regulation of a sixth-order dc-dc converter using only the output voltage. The proposed controller adopts the basic structure of the output feedback controller for the traditional boost converter [30]. However, in contrast to [30], a constant reference voltage term is used in the denominator of the proposed control law which not only simplifies the implementation of the controller, but also avoids the risk of saturation by avoiding the

possibility of division by zero. Also, both proportional and integral actions are also included to give a desired control performance. In addition, the stability analysis of the proposed output feedback controlled high-order dc-dc converter is carried out, and the feasibility of the controller is shown. The feasibility analysis shows that the “remaining dynamics” of the controlled converter has only one equilibrium point which is always stable. Finally, some experimental results are provided to illustrate the features of the proposed controller in the presence of load, input voltage and reference voltage variations.

Fig. 4.11. Schematic of the POSRL converter.

4.3.1 Model of The POSRL Converter

In section 2.3.3, the averaged reduced-order model of the POSRL converter was presented. The averaged model is given by

$$\dot{\bar{x}} = A_{avg}\bar{x} + B_{avg}v_{in} \quad (4.25)$$

where $\bar{x} = [\bar{x}_1, \bar{x}_2, \bar{x}_3, \bar{x}_4]^T$ is the averaged state variable vector, and $\bar{x}_1$, $\bar{x}_2$, $\bar{x}_3$ and $\bar{x}_4$ represents the averaged value of the current of inductor L_1 , current of inductor L_2 , voltage across the capacitor C_2 and the converter output voltage v_o , respectively.

Matrices A_{avg} and B_{avg} are given by

$$A_{avg} = \begin{bmatrix} 0 & 0 & -\frac{1-d}{L_1} & 0 \\ 0 & 0 & \frac{2-d}{L_2} & -\frac{1-d}{L_2} \\ \frac{1-d}{C_2} & -\frac{2-d}{C_2} & 0 & 0 \\ 0 & \frac{1-d}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix}, \quad B_{avg} = \begin{bmatrix} \frac{2-d}{L_1} & 0 & 0 & 0 \end{bmatrix}^T.$$

By setting (4.25) to zero and letting the desired converter output voltage $v_{o\infty} = V_{ref}$, the following system equilibrium values are obtained:

$$\begin{aligned} X_1 &= \frac{V_{ref}}{Rv_{in}} \sqrt{\frac{V_{ref}}{v_{in}}} (\sqrt{v_{in}V_{ref}} - v_{in}), \quad X_2 = \frac{V_{ref}}{Rv_{in}} (\sqrt{v_{in}V_{ref}} - v_{in}), \\ X_3 &= \sqrt{v_{in}V_{ref}}, \quad X_4 = V_{ref}, \quad D = \frac{\sqrt{v_{in}V_{ref}} - 2v_{in}}{\sqrt{v_{in}V_{ref}} - v_{in}} \end{aligned} \quad (4.26)$$

Here X_1 , X_2 , X_3 , X_4 and D are the equilibrium values of $\bar{x}_1$, $\bar{x}_2$, $\bar{x}_3$, $\bar{x}_4$ and d , respectively.

4.3.2 Control of The POSRL Converter

In this section, the detailed description of the proposed output feedback controller for the POSRL converter is given. Also, in order to better appreciate the significance of the proposed controller, it will be shown that the traditional voltage-mode controller is not suitable for this high-order converter.

4.3.2.1 Traditional voltage-mode controller

The traditional voltage-mode controller or PI controller is given by

$$d = D - K_{p1}(\bar{x}_4 - V_{ref}) - K_{i1} \int (\bar{x}_4(\tau) - V_{ref}) d\tau \quad (4.27)$$

where $K_{p1} > 0$, $K_{i1} > 0$ and D is given in (4.26). In order to analyse the stability of the closed-loop system, the following error variables are defined:

$$\tilde{x}_1 = \bar{x}_1 - X_1, \quad \tilde{x}_2 = \bar{x}_2 - X_2, \quad \tilde{x}_3 = \bar{x}_3 - X_3, \quad \tilde{x}_4 = \bar{x}_4 - X_4 \quad (4.28)$$

Using (4.27) and (4.28) in (4.25) and letting $\sigma = K_{i1} \int (\bar{x}_4(\tau) - V_d) d\tau$ yields the following error dynamics:

$$\dot{\tilde{x}}_1 = \frac{(2-D+K_{p1} \tilde{x}_4 - \sigma)}{L_1} v_{in} - \frac{(1-D+K_{p1} \tilde{x}_4 - \sigma)}{L_1} (\tilde{x}_2 + X_2) \quad (4.29)$$

$$\dot{\tilde{x}}_2 = \frac{(2-D+K_{p1} \tilde{x}_4 - \sigma)}{L_2} (\tilde{x}_2 + X_2) - \frac{(1-D+K_{p1} \tilde{x}_4 - \sigma)}{L_2} (\tilde{x}_4 + V_{ref}) \quad (4.30)$$

$$\dot{\tilde{x}}_3 = \frac{(1-D+K_{p1} \tilde{x}_4 - \sigma)}{C_2} (\tilde{x}_1 + X_1) - \frac{(2-D+K_{p1} \tilde{x}_4 - \sigma)}{C_2} (\tilde{x}_2 + X_2) \quad (4.31)$$

$$\dot{\tilde{x}}_4 = \frac{(1-D+K_{p1} \tilde{x}_4 - \sigma)}{C_4} (\tilde{x}_2 + X_2) - \frac{1}{R_L C_4} (\tilde{x}_4 + V_{ref}) \quad (4.32)$$

$$\dot{\sigma} = K_{i1} \tilde{x}_4 \quad (4.33)$$

The unique equilibrium point of (4.29) – (4.33) is given by:

$$(\tilde{x}_{1\infty}, \tilde{x}_{2\infty}, \tilde{x}_{3\infty}, \tilde{x}_{4\infty}, \sigma_\infty) = (0, 0, 0, 0, 0) \quad (4.34)$$

Now, linearizing (4.29) – (4.33) about the equilibrium point (4.34) yields the following system of the form:

$$\dot{z} = M_{PI} z \quad (4.35)$$

where $z = [\tilde{x}_1 - \tilde{x}_{1\infty}, \tilde{x}_2 - \tilde{x}_{2\infty}, \tilde{x}_3 - \tilde{x}_{3\infty}, \tilde{x}_4 - \tilde{x}_{4\infty}, \sigma - \sigma_\infty]^T$ and

$$M_{PI} = \begin{bmatrix} 0 & 0 & -\frac{v_{in} + \sqrt{v_{in} V_{ref}}}{L_1 (V_{ref} - v_{in})} \\ 0 & 0 & \frac{V_{ref} + \sqrt{v_{in} V_{ref}}}{L_2 (V_d - v_{in})} \\ \frac{v_{in} + \sqrt{v_{in} V_{ref}}}{C_2 (V_{ref} - v_{in})} & -\frac{V_{ref} + \sqrt{v_{in} V_{ref}}}{C_2 (V_{ref} - v_{in})} & 0 \\ 0 & \frac{v_{in} + \sqrt{v_{in} V_{ref}}}{C_4 (V_{ref} - v_{in})} & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$- \frac{1}{L_2} \begin{bmatrix} \frac{K_{p1} (v_{in} - \sqrt{v_{in} V_{ref}})}{L_1} & \frac{v_{in} - \sqrt{v_{in} V_{ref}}}{L_1} \\ \left[K_{p1} (V_{ref} - \sqrt{v_{in} V_{ref}}) - \frac{v_{in} + \sqrt{v_{in} V_{ref}}}{V_{ref} - v_{in}} \right] & -\frac{V_{ref} - \sqrt{v_{in} V_{ref}}}{L_2} \\ \frac{K_{p1} V_{ref}}{C_2 R v_{in}} (\sqrt{V_{ref}} - \sqrt{v_{in}})^2 & \frac{K_{p1}}{C_2 R v_{in}} (\sqrt{V_{ref}} - \sqrt{v_{in}})^2 \\ -\frac{1}{C_4 R} \left[1 + \frac{K_{p1} V_{ref} (v_{in} - \sqrt{v_{in} V_{ref}})}{v_{in}} \right] & -\frac{V_{ref} (v_{in} - \sqrt{v_{in} V_{ref}})}{C_4 R v_{in}} \end{bmatrix}$$

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

The linearized system (4.35) will be stable if the real parts of all the roots of the characteristic polynomial $m_{PI}(s) = |sI_{5 \times 5} - M_{PI}| = 0$, where s is a complex variable and $I_{5 \times 5}$ is the 5 x 5 identity matrix, are negative. The root locus method can be used to analyse the system stability as illustrated in the following.

Table 4.3 Main parameters of the POSRL converter system

Parameter	Value
v_{in}	10 V
V_{ref}	120 V
L_1, L_2	10 mH
C_2, C_4	100 μ H
R	10 k Ω (4.36)

Considering the POSRL converter with the circuit parameter values given in Table 4.3, the corresponding characteristic polynomial can be obtained as:

$$\begin{aligned}
 m_{PI}(s) = & s^5 + (707.88K_{p1} + 1)s^4 \\
 & + (707.88K_{i1} - 2.45 \times 10^7 K_{p1} + 7.47 \times 10^5)s^3 \\
 & + (1.10 \times 10^9 K_{p1} - 2.45 \times 10^7 K_{i1} + 7.18 \times 10^5)s^2 \\
 & + (1.10 \times 10^9 K_{i1} - 1.41 \times 10^{12} K_{p1} + 8.26 \times 10^8)s \\
 & - 1.41 \times 10^{12} K_{i1}
 \end{aligned} \tag{4.36}$$

Fig. 4.12(a) shows the root-locus plot of (4.36) for $K_{p1} = 0.001$ and $0 < K_{i1} \leq 0.01$. Also, Fig. 4.12(b) shows the root-locus plot for $K_{i1} = 0.001$ and $0 < K_{p1} \leq 0.01$. The arrows show how the poles are moving for increasing values of the controller gains. From Fig. 4.12(a), it can be seen that the two most dominant poles cross the imaginary axis when $K_{i1} = 0.0004$. Also, Fig. 4.12(b) shows that the dominant poles enter the right half of complex s-plane when $K_{p1} = 0.0006$. This shows that the closed-loop controlled system is stable for very small ranges of K_{p1} and K_{i1} and the dominant

Fig. 4.12. Root-locus of the controlled converter system: (a) using traditional voltage-mode controller for $K_{p1} = 0.001$ and $0 < K_{i1} \leq 0.01$; (b) using traditional voltage-mode controller for $0 < K_{p1} \leq 0.01$ and $K_{i1} = 0.001$; (c) using proposed controller for $K_{p2} = 0.1$, $0 < K_{i2} \leq 5$, $K_1 = 0.01$ and $K_2 = 0.01$; (d) using proposed controller for $0 < K_{p2} \leq 2$, $K_{i2} = 1$, $K_1 = 0.01$ and $K_2 = 0.01$.

poles are very close to the imaginary axis. This makes it quite difficult to achieve the desired output response using the traditional voltage-mode controller, as there is less room available for tuning of the controller gains. Hence, the traditional voltage-mode controller is not quite suitable for regulating the POSRL converter.

4.3.2.2 Proposed control law

As demonstrated in section 4.3.2.1, the traditional PI controller is not suitable for the POSRL converter. In this section, an improved voltage-mode controller that overcomes this shortcoming is presented. The control law of the proposed output feedback controller can be obtained from the expression for D in (4.26), namely,

$$d = \frac{\sqrt{x_d v_{in}} - 2v_{in}}{\sqrt{V_{ref} v_{in}} - v_{in}} \quad (4.37)$$

where x_d is the solution of the linear differential equation given by:

$$\frac{dx_d}{dt} = \frac{1}{c_4} [-(K_1 + K_2)x_d + K_2\bar{x}_4 + K_1V_{ref}] \quad (4.38)$$

By replacing V_{ref} in the denominator of the open-loop control structure (see (4.26)) with a new state variable x_d yields a controller (4.37) which is independent of the load resistance R . Here, a constant reference voltage term is used in the denominator of (4.37) which not only simplifies the implementation of the controller, but also avoids the risk of saturation as there is no possibility of division by zero. Also, additional proportional and integral actions are incorporated in (4.37) to give:

$$d = \frac{\sqrt{x_d v_{in} - 2v_{in} - K_{p2}(\bar{x}_4 - V_{ref}) - K_{i2} \int (\bar{x}_4(\tau) - V_{ref}) d\tau}}{\sqrt{V_{ref} v_{in} - v_{in}}} \quad (4.39)$$

where K_{p2} and K_{i2} are the positive constants. The additional proportional and integral actions are mainly added to reduce the steady-state error as well as to improve the overall dynamic performance of the system. This inclusion does not require any extra state variables and thus the control scheme can still be implemented by using only the output voltage for feedback purposes.

4.3.2.3 Stability analysis

Substituting (4.28) and (4.39) into (4.22) – (4.25) and using (4.38) yields the following set of equations:

$$\begin{aligned} \dot{\tilde{x}}_1 = & \frac{v_{in}}{L_1} \left(\frac{2\sqrt{V_{ref}v_{in}} - \sqrt{x_d v_{in}} + K_{p2}\tilde{x}_4 + \sigma}{\sqrt{V_{ref}v_{in} - v_{in}}} \right) \\ & - \frac{(\tilde{x}_2 + X_2)}{L_1} \left(\frac{\sqrt{V_{ref}v_{in} + v_{in}} - \sqrt{x_d v_{in}} + K_{p2}\tilde{x}_4 + \sigma}{\sqrt{V_{ref}v_{in} - v_{in}}} \right) \end{aligned} \quad (4.40)$$

$$\begin{aligned} \dot{\tilde{x}}_2 = & \frac{(\tilde{x}_2 + X_2)}{L_2} \left(\frac{2\sqrt{V_{ref}v_{in}} - \sqrt{x_d v_{in}} + K_{p2}\tilde{x}_4 + \sigma}{\sqrt{V_{ref}v_{in} - v_{in}}} \right) \\ & - \frac{(\tilde{x}_4 + V_{ref})}{L_2} \left(\frac{\sqrt{V_{ref}v_{in} + v_{in}} - \sqrt{x_d v_{in}} + K_{p2}\tilde{x}_4 + \sigma}{\sqrt{V_{ref}v_{in} - v_{in}}} \right) \end{aligned} \quad (4.41)$$

$$\begin{aligned}\dot{\tilde{x}}_3 = & \frac{(\tilde{x}_1 + X_1)}{C_2} \left(\frac{\sqrt{V_{ref}v_{in}} + v_{in} - \sqrt{x_d v_{in}} + K_{p2}\tilde{x}_4 + \sigma}{\sqrt{V_{ref}v_{in}} - v_{in}} \right) \\ & - \frac{(\tilde{x}_2 + X_2)}{C_2} \left(\frac{2\sqrt{V_{ref}v_{in}} - \sqrt{x_d v_{in}} + K_{p2}\tilde{x}_4 + \sigma}{\sqrt{V_{ref}v_{in}} - v_{in}} \right)\end{aligned}\quad (4.42)$$

$$\dot{\tilde{x}}_4 = \frac{(\tilde{x}_2 + X_2)}{C_4} \left(\frac{\sqrt{V_{ref}v_{in}} + v_{in} - \sqrt{x_d v_{in}} + K_{p2}\tilde{x}_4 + \sigma}{\sqrt{V_{ref}v_{in}} - v_{in}} \right) - \frac{(\tilde{x}_4 + V_{ref})}{RC_4} \quad (4.43)$$

$$\dot{x}_d = \frac{-(K_1 + K_2)}{C_4} x_d + \frac{K_2}{C_4} (\tilde{x}_4 + V_{ref}) + \frac{K_1}{C_4} V_{ref} \quad (4.44)$$

$$\dot{\sigma} = K_{i2} \tilde{x}_4 \quad (4.45)$$

The equilibrium point of (4.40) – (4.26) can be obtained as,

$$(\tilde{x}_{1\infty}, \tilde{x}_{2\infty}, \tilde{x}_{3\infty}, \tilde{x}_{4\infty}, x_{d\infty}, \sigma_{\infty}) = (0, 0, 0, 0, V_{ref}, 0) \quad (4.46)$$

Like what was done previously in section 4.2.3.1, linearizing (4.40) – (4.45) about the equilibrium point (4.46) yields the system of the form:

$$\dot{y} = M_V y \quad (4.47)$$

where $y = [y_1 \ y_2 \ y_3 \ y_4 \ y_5 \ y_6]^T$, $y_1 = \tilde{x}_1 - \tilde{x}_{1\infty}$, $y_2 = \tilde{x}_2 - \tilde{x}_{2\infty}$, $y_3 = \tilde{x}_3 - \tilde{x}_{3\infty}$, $y_4 = \tilde{x}_4 - \tilde{x}_{4\infty}$, $y_5 = \tilde{x}_d - \tilde{x}_{d\infty}$, $y_6 = \sigma - \sigma_{\infty}$. The matrix M_V is given as

$$M_V = \begin{bmatrix} 0 & 0 & -\frac{\sqrt{v_{in}}}{L_1(\sqrt{V_{ref}} - \sqrt{v_{in}})} \\ 0 & 0 & \frac{\sqrt{V_{ref}}}{L_2(\sqrt{V_{ref}} - \sqrt{v_{in}})} \\ \frac{\sqrt{v_{in}}}{C_2(\sqrt{V_{ref}} - \sqrt{v_{in}})} & -\frac{\sqrt{V_{ref}}}{C_2(\sqrt{V_{ref}} - \sqrt{v_{in}})} & 0 \\ 0 & \frac{\sqrt{V_{ref}}}{C_4(\sqrt{V_{ref}} - \sqrt{v_{in}})} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -\frac{K_{p2}}{L_1} & \frac{\sqrt{v_{in}}}{2L_1\sqrt{V_{ref}}} & -\frac{1}{L_1} \\ -\frac{K_{p2}(V_{ref} - \sqrt{v_{in}V_{ref}}) + v_{in}}{L_2(\sqrt{v_{in}V_{ref}} - v_{in})} & \frac{1}{2L_2} & -\frac{\sqrt{V_{ref}}}{L_2\sqrt{v_{in}}} \\ \frac{K_{p2}V_{ref}(\sqrt{V_{ref}} - \sqrt{v_{in}})}{RC_2v_{in}\sqrt{v_{in}}} & -\frac{\sqrt{V_{ref}}(\sqrt{V_{ref}} - \sqrt{v_{in}})}{2RC_2v_{in}} & \frac{V_{ref}(\sqrt{V_{ref}} - \sqrt{v_{in}})}{RC_2v_{in}\sqrt{v_{in}}} \\ \frac{1}{RC_4} \left(\frac{K_{p2}V_{ref}}{v_{in}} - 1 \right) & -\frac{\sqrt{V_{ref}}}{2RC_4\sqrt{v_{in}}} & \frac{V_{ref}}{RC_4v_{in}} \\ \frac{K_2}{C_4} & -\frac{(K_1 + K_2)}{C_4} & 0 \\ K_{i2} & 0 & 0 \end{bmatrix}$$

The stability analysis can now be performed by finding the eigenvalues of matrix M_V , i.e., the roots of $m_V(s) = |sI_{5 \times 5} - M_V| = 0$. The system will be stable if and only if all the eigenvalues of M_V lie in the open left-half complex plane. The root locus method can be used again to analyse the system stability.

Using the set of circuit parameters given in (4.36), the corresponding characteristic polynomial is described by:

$$m_V(s) = s^6 + a_5s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0 \quad (4.48)$$

where

$$a_5 = 10^4(K_1 + K_2) - 24K_{p2} + 1,$$

$$a_4 = 10^4K_1 + 3.45 \times 10^4K_2 + 1.26 \times 10^6K_{p2} \\ - 24K_{i2} - 2.4 \times 10^5K_{p2}(K_1 + K_2),$$

$$a_3 = 1.71 \times 10^{10}K_1 + 1.58 \times 10^{10}K_2 + 1.26 \times 10^6K_{i2} - 6.96 \times 10^7K_{p2} \\ + (1.26 \times 10^{10}K_{p2} - 2.4 \times 10^5K_{i2})(K_1 + K_2) + 1.64 \times 10^6,$$

$$a_2 = 1.64 \times 10^{10}K_1 + 8.75 \times 10^{10}K_2 + 1.65 \times 10^{11}K_{p2} - 6.96 \times 10^7K_{i2} \\ + (-6.96 \times 10^{11}K_{p2} + 1.26 \times 10^{10}K_{i2})(K_1 + K_2) + 4.33 \times 10^9,$$

$$a_1 = 4.33 \times 10^{13}K_1 - 1.25 \times 10^{14}K_2 + 1.65 \times 10^{11}K_{i2} \\ + (1.65 \times 10^{15}K_{p2} - 6.96 \times 10^{11}K_{i2})(K_1 + K_2),$$

$$a_0 = 1.65 \times 10^{15}K_{i2}(K_1 + K_2).$$

Fig. 4.12(c) shows the root locus plot of $m_V(s)$ for $K_1 = 0.01$, $K_2 = 0.01$, $K_{p2} = 0.1$ and $0 < K_{i2} \leq 5$. The arrows show how the poles are moving for the increasing value of K_{i2} . It can be seen that as K_{i2} increases, the dominant poles move towards the imaginary axis and further enter into the right-half of complex s-plane when $K_{i2} \geq 1.55$. Thus, the closed-loop system is stable for $K_{i2} < 1.55$. Similarly, Fig. 4.12(d) shows the root locus plot of $m_V(s)$ obtained using $K_1 = 0.01$, $K_2 = 0.01$, $K_{i2} = 1$,

and $0 < K_{p2} \leq 2$. Again, it is clear that the value of K_{p2} should be less than 0.29, i.e., $0 < K_{p2} < 0.29$, to ensure system stability. This shows that there are upper bound limits to the values of K_{p2} and K_{i2} to ensure that the closed-loop system is stable. As compared to the traditional voltage-mode controller, the range of stability is much wider for the controller gains of the proposed controller. This allows the designer to tune the controller gains over a wide range to achieve the desired stable output response.

4.3.2.4 Feasibility of the proposed controller

In order to ensure that the proposed controller is internally stable at the equilibrium condition, the feasibility of the proposed controller for the POSRL converter is demonstrated here. Using $\dot{\sigma} = K_{i2}(\bar{x}_4 - V_d)$ in (4.39), the time derivative of the control signal d can be obtained as:

$$\dot{d} = \frac{1}{\sqrt{V_{ref}v_{in}} - v_{in}} \left(\frac{\sqrt{v_{in}}}{2\sqrt{x_d}} \dot{x_d} - K_{p2}\dot{\tilde{x}}_4 - \sigma \right) \quad (4.49)$$

Substituting $x_d = \frac{[d(\sqrt{V_{ref}v_{in}} - v_{in}) + 2v_{in} + K_{p2}\tilde{x}_4 + \sigma]^2}{v_{in}}$ (see (4.39)) into (4.49) and using (4.25) and (4.38) gives

$$\begin{aligned} \dot{d} = & \frac{1}{\sqrt{V_{ref}v_{in}} - v_{in}} \left(\frac{v_{in}}{2} \frac{\frac{1}{C_4} [-(K_1 + K_2) \{ [d(\sqrt{V_{ref}v_{in}} - v_{in}) + 2v_{in} + K_{p2}\tilde{x}_4 + \sigma]^2 / v_{in} \} + K_2\tilde{x}_4 + K_1V_{ref}]}{[d(\sqrt{V_{ref}v_{in}} - v_{in}) + 2v_{in} + K_{p2}\tilde{x}_4 + \sigma]} \right) \\ & - K_{p2} \left[\frac{(1-d)}{C_4} \bar{x}_2 - \frac{1}{C_4} \bar{x}_4 \right] - \sigma \end{aligned} \quad (4.50)$$

Now, by letting $\bar{x}_4$, σ , $\tilde{x}_4$ and $\bar{x}_2$ coincide with their equilibrium values, namely,

$$\bar{x}_4 = V_d, \quad \sigma = \tilde{x}_4 = 0, \quad \text{and} \quad \bar{x}_2 = \frac{V_{ref}}{Rv_{in}} (\sqrt{v_{in}V_{ref}} - v_{in}) \quad \text{gives}$$

$$\begin{aligned} \dot{d} = & -K_{p2} \left[\frac{(1-d)}{C_4} \frac{V_{ref}}{Rv_{in}} (\sqrt{v_{in}V_{ref}} - v_{in}) - \frac{V_{ref}}{RC_4} \right] \\ & + \frac{1}{\sqrt{V_{ref}v_{in}} - v_{in}} \left(\frac{v_{in}}{2C_4} \frac{-(K_1 + K_2) \{ [d(\sqrt{V_{ref}v_{in}} - v_{in}) + 2v_{in}]^2 / v_{in} \} + (K_1 + K_2)V_{ref}}{[d(\sqrt{V_{ref}v_{in}} - v_{in}) + 2v_{in}]} \right) \end{aligned} \quad (4.51)$$

Using the same set of circuit parameter values given by (4.36) and $K_1 = 0.01$, $K_2 = 0.01$ and $K_{p2} = 0.1$, the phase-portrait of (4.51) is shown in Fig. 4.13.

It is evident that the “remaining dynamics” for the controlled POSRL converter system has only one equilibrium point, i.e., $D \cong 0.7435$, as compared to two equilibrium points (one of which is unstable) in [29]. The results are summarized in the following proposition.

Fig. 4.13. Phase-portrait of (4.51) using (4.36) and, $K_1 = K_2 = 0.01$ and $K_{p2} = 0.1$.

Proposition: For a given reference voltage V_{ref} , such that $v_{in} < V_{ref} < \infty$, the controller described by (4.38) and (4.39) with suitably chosen values of controller gains locally asymptotically stabilizes the POSRL converter to the equilibrium point $(\tilde{x}_{1\infty}, \tilde{x}_{2\infty}, \tilde{x}_{3\infty}, \tilde{x}_{4\infty}, x_{d\infty}, \sigma_{\infty}) = (0, 0, 0, 0, V_{ref}, 0)$ for any $0 < R < \infty$.

4.3.2.5 Validation of the stability analysis

To verify the theoretical conclusions obtained in the previous sections, a comparative study involving the traditional voltage-mode controller and the proposed output feedback controller was carried out. The same set of converter circuit parameters, given by (4.36), was used to obtain the results.

Fig. 4.14(a) shows the start-up transient response of the system obtained using the

traditional voltage-mode controller (4.27). Here, K_{p1} was fixed at 10^{-4} and K_{i1} was varied to illustrate its effect on the output response. It can be seen that the oscillations in the response were considerably suppressed when the value of K_{i1} was reduced. However, even after using an extremely small value of K_{i1} i.e., $K_{i1} = 10^{-11}$, the transient output response was still very oscillatory. When the values of controller gains were increased to solve this problem, the response became unstable. The output voltage response obtained using $K_{p1} = 0.0007$ and $K_{i1} = 0.001$ is shown in Fig. 4.14(b). It can be seen that the output response became unstable which is in agreement with the previous theoretical analysis.

Fig. 4.14. Output responses of the controlled POSRL converter: (a) using traditional voltage-mode controller with $K_{p1} = 10^{-4}$ and $K_{i1} = 10^{-3}$ (blue solid line) and $K_{p1} = 10^{-4}$ and $K_{i1} = 10^{-11}$ (red dotted line); (b) using traditional voltage-mode controller with $K_{p1} = 7 \times 10^{-4}$ and $K_{i1} = 10^{-3}$; (c) using proposed controller with $K_{p2} = 0.03$, $K_{i2} = 0.02$, $K_1 = 0.01$ and $K_2 = 0.01$; (d) using proposed controller with $K_{p2} = 0.08$, $K_{i2} = 0.1$, $K_1 = 0.01$ and $K_2 = 0.01$.

To overcome the limitation of the traditional voltage-mode controller, the proposed output feedback controller (4.38) – (4.39) was used to regulate the POSRL converter.

Fig. 4.14(c) shows the output voltage response of the system obtained using $K_1 = 0.01$,

$K_2 = 0.01$, $K_{p2} = 0.03$, and $K_{i2} = 0.02$. It can be seen that the oscillations in the response were considerably reduced as compared to the case of the traditional voltage-mode controller and the stable output voltage response was easily obtained. The oscillations were further reduced by increasing the values of the controller gains and Fig. 4.14(d) shows the corresponding start-up output response obtained using $K_{p2} = 0.08$ and $K_{i2} = 0.01$.

All these results confirm that the proposed controller, as compared to the traditional voltage-mode controller, is more suitable for the regulation of the POSRL converter.

Remark: Since the proposed controller does not use any inductor current for feedback purposes, it therefore cannot provide the over-current protection directly. However, some current-limiting circuits can be used to protect the system against over-current [55] – [56].

4.3.3 Simulation and Experimental Results

In order to verify the effectiveness of the proposed output feedback controller for the POSRL converter, some simulations as well as laboratory experiments were carried out. The same set of converter parameter values used in section 4.3.2, given by (4.36) was also used to obtain the results.

4.3.3.1 Simulation results

Fig. 4.16 shows the converter output responses obtained under various operating conditions. These simulation results were obtained using MATLAB Version R2014a. Fig. 4.15(a) shows the output voltage response of the converter when the load resistance R was changed from $10\text{ k}\Omega$ to $3.3\text{ k}\Omega$ at $t = 1\text{ s}$ and then back to $10\text{ k}\Omega$ at $t = 2\text{ s}$. The output voltage was restored to its nominal value in $\sim 0.2\text{ s}$ with a small voltage

deviation (of $\sim 1.66\%$ of the nominal value) after the onset of load disturbances. Fig. 4.15(b) shows the output voltage response when the converter input voltage v_{in} was changed from 10 V to 6 V at $t = 3\text{ s}$, and then back to 10 V at $t = 4\text{ s}$. In this case, the output response was restored to its nominal value in $\sim 0.3\text{ s}$ with negligible overshoot. Fig. 4.15(c) shows the output response for a step change in the reference voltage V_{ref} from 120 V to 140 V at $t = 5\text{ s}$ and then back to 120 V at $t = 6\text{ s}$. A fast and accurate output voltage tracking was achieved.

Fig. 4.15. System output responses: (a) for change in load resistance from $R = 10\text{ k}\Omega$ to $R = 3.3\text{ k}\Omega$ (and vice-versa); (b) for change in input voltage from $v_{in} = 10\text{ V}$ to $v_{in} = 6\text{ V}$ (and vice-versa); (c) for change in reference voltage from $V_{ref} = 120\text{ V}$ to $V_{ref} = 140\text{ V}$ (and vice-versa).

4.3.3.2 Experimental results

In order to obtain the experimental validation, a prototype of the regulated POSRL converter system was built. This laboratory prototype is shown in Fig. 4.16. The MOSFET IRFP460 and the diode STTH2002C were used in the prototype and the

switching frequency used was 20 kHz. In addition, the specifications of the desired control performance ~~is~~ are given in Table 4.4

Table 4.4 Specifications of the desired control performance

Performance	Value
Start-up overshoot	$\leq 5\%$
Start-up settling time	$\leq 0.5s$
Voltage dip (swell) in the presence of load resistance changes	$\leq 5\%$
Settling time in the presence of load resistance changes	$\leq 0.5s$
Voltage dip (swell) in the presence of input voltage changes	$\leq 5\%$
Settling time in the presence of input voltage changes	$\leq 0.5s$

Fig. 4.16. Laboratory prototype of: (a) POSRL converter; (b) proposed controller.

Fig. 4.17 shows the block diagram of the closed-loop controlled system. For implementation purposes, a voltage feedback factor $\beta = 1/20$ was employed. To achieve satisfactory responses, the values of the controller gains used were, $K_{p2} = 0.2$, $K_{i2} = 3.9$, and $K_1 = K_2 = 1$. The corresponding circuit schematic of the proposed controller is shown in Fig. 4.18.

Fig. 4.17. Block diagram of the controlled converter system.

Fig. 4.19(a) shows the transient output response of the converter using a reference voltage $V_{ref} = 120 \text{ V}$. The response has a settling time of $\sim 0.28 \text{ s}$ with almost no overshoot. Also, a good output tracking was obtained with a negligible steady-state error. The ability of the controller to handle the load and input voltage variations was then observed. Fig. 4.19(b) shows the output voltage response of the converter when the load resistance R was changed from $10 \text{ k}\Omega$ to $3.3 \text{ k}\Omega$ and then back to $10 \text{ k}\Omega$. These disturbances were rejected in a worst-case settling time of $\sim 0.16 \text{ s}$ with a maximum transient voltage deviation which was always below 3.5% of the nominal output voltage.

Next, to show that the proposed controller also works for another set of circuit parameters, a converter was designed to operate at an output voltage of 80 V for an input voltage ranging from 10 V to 15 V and an output power ranging from 6.4 W to 12.8 W . To achieve satisfactorily responses, the values of K_1 , K_2 , K_{p2} and K_{i2} used were 0.5, 0.5, 0.1 and 1.8, respectively.

Fig. 4.18. Circuit schematic of the proposed controller

Fig. 4.19. System experimental responses: (a) for a step-up input; (b) for change in the load resistance from $R = 10 \text{ k}\Omega$ to $R = 3.3 \text{ k}\Omega$ (and vice-versa); (c) for change in the input voltage from $v_{in} = 10 \text{ V}$ to $v_{in} = 6 \text{ V}$ (and vice-versa); (d) for step change in the reference voltage from $V_{ref} = 120 \text{ V}$ to $V_{ref} = 140 \text{ V}$ and then back to $V_{ref} = 120 \text{ V}$.

Fig. 4.20(a) shows the output voltage response for a step change in the output power from 6.4 W to 12.8 W and vice-versa. It can be seen that these disturbances produced a maximum transient deviation of the output voltage that was always below $\sim 5\%$ of the nominal output voltage, which was rejected in $\sim 0.2 \text{ s}$ in the worst case. Note also that the output voltage was quickly restored to its nominal value after the onset of the disturbances. Fig. 4.20(b) shows the output voltage response when the input voltage v_{in} was changed from 10 V to 15 V . Again, the output voltage was restored to its nominal value with a small settling time of $\sim 0.2 \text{ s}$ and the maximum transient voltage deviation was $\sim 5\%$ of the nominal output voltage.

Lastly, the ability of the proposed controller to handle the reference voltage variations was studied. Fig. 4.20(c) shows the output response for a step change in the reference

Fig. 4.20. System experimental output voltage responses: (a) for change in the output power from $P_{out} = 6.4 \text{ W}$ to $P_{out} = 12.8 \text{ W}$ (and vice-versa); (b) for change in the input voltage from $v_{in} = 10 \text{ V}$ to $v_{in} = 15 \text{ V}$; (c) for step change in the reference voltage from $V_{ref} = 100 \text{ V}$ to $V_{ref} = 80 \text{ V}$.

voltage V_{ref} from 100 V to 80 V . It can be seen that the output voltage was quickly restored to the desired reference voltage with negligible or no steady-state error.

All these results verify that the proposed output feedback controller is able to regulate the POSRL converter to meet the predefined control objectives given in Table 4.4 over a wide range of operating conditions.

4.3.4 Conclusion

In this section, the development of an improved output feedback controller for the POSRL converter was presented. The proposed controller only uses the output voltage to regulate the sixth-order dc-dc converter. Also, the structure of the controller is such that it is insensitive to the load variations and it eliminates the risk of saturation due to the possibility of division by zero in the control law. The controller design was

accompanied by the detailed stability analysis and the feasibility of the proposed controller was shown. The feasibility analysis shows that the “remaining dynamics” of the controlled converter has a unique equilibrium point which is always stable. In addition, a comparative study involving the traditional voltage-mode controller and the proposed controller was carried out to show the advantages of the proposed controller. Some simulation as well as experimental results were also provided to validate the use of the proposed controller to regulate the POSRL converter. Finally, it should be noted that the proposed output feedback control law for the POSRL converter can also be applied to regulate other high-order dc-dc boost converters. However, the structure of the controller may vary slightly as per the steady-state duty-ratio expression of the specific converter.

4.4 An Improved Voltage-Mode Controller for the Quadratic Boost Dc-Dc Converter

In this section, an improved voltage-mode controller is proposed for the quadratic boost dc-dc converter. The schematic of this converter is shown in Fig. 4.21. The main contributions of this section are as follows. A novel structure of the voltage-mode control law is adopted which avoids the control signal saturation problem that exists in [32] – [34]. Besides, instead of the traditional integral action, a normalized integral action is used in which the time derivative of the integrand is bounded by a user-defined constant. This avoid the extreme changes in the control signal. As a result, improved transient output responses are achieved. The stability analysis of the proposed voltage-mode controlled quadratic boost dc-dc converter system is carried out. Also, the feasibility of the proposed controller is verified. Finally, simulation and experimental results showing the effectiveness of the proposed controller for the regulation of the quadratic boost dc-dc converter under various operation conditions are provided.

Fig. 4.21. Schematic of the quadratic boost converter.

4.4.1 Model of The Quadratic Dc-Dc Boost Converter

As compared to the traditional boost converter, the quadratic boost converter shown in Fig. 2.4 can provide a higher voltage gain using a smaller duty cycle. It also has a better trade-off between efficiency and duty cycle operation range as compared to its cubic counterpart [28].

In section 2.3.2, the averaged state-space model of the quadratic boost converter was presented and is given by

$$\dot{\bar{x}} = A_{avg}\bar{x} + B_{avg}v_{in} \quad (4.52)$$

where $\bar{x} = [\bar{x}_1, \bar{x}_2, \bar{x}_3, \bar{x}_4]^T$, $\bar{x}_1$, $\bar{x}_2$, $\bar{x}_3$ and $\bar{x}_4$ represents the averaged value of the inductor currents of L_1 and L_2 and capacitor voltages of C and C_o , respectively.

Matrices A_{avg} and B_{avg} are given by

$$A_{avg} = \begin{bmatrix} 0 & 0 & -\frac{1-d}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{1-d}{L_2} \\ \frac{1-d}{C} & -\frac{1}{C} & 0 & 0 \\ 0 & \frac{1-d}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix}, \quad B_{avg} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

Setting the left-hand-side of (4.52) to zero, the unique system equilibrium point can be obtained as,

$$\begin{aligned}
X_1 &= \frac{V_{ref}^2}{Rv_{in}}, X_2 = \sqrt{\frac{V_{ref}^3}{R^2v_{in}}}, X_3 = \sqrt{v_{in}V_{ref}}, \\
X_4 &= V_{ref}, D = \frac{\sqrt{V_{ref}} - \sqrt{v_{in}}}{\sqrt{V_{ref}}}
\end{aligned} \tag{4.53}$$

where X_1, X_2, X_3, X_4 and D are the steady-state values of $\bar{x}_1, \bar{x}_2, \bar{x}_3, \bar{x}_4$ and d , respectively. The symbol of V_{ref} represents the reference of the converter output voltage.

4.4.2 Proposed Voltage-Mode Controller

Firstly, the structure of the state-of-the-art voltage-mode controller for the quadratic boost converter is given. The expression of the existing voltage feedback control law is given as [32]:

$$d = 1 - \frac{\sqrt{v_{in} + K_{Pe}(\bar{x}_4 - V_{ref}) + K_{Ie} \int (\bar{x}_4(t) - V_{ref}) dt}}{\sqrt{x_d}} \tag{4.54}$$

$$\frac{dx_d}{dt} = \frac{1}{C_o} [K_{1e}(\bar{x}_4 - x_d) + K_{2e}(V_{ref} - x_d)] \tag{4.55}$$

where K_{Pe}, K_{Ie}, K_{1e} and K_{2e} are positive controller gains and x_d is an artificial voltage variable. Although the control law (4.54) – (4.55) is able to successfully regulate the quadratic boost converter in the presence of load and line variations [32], there still exists several drawbacks in this control law. One of the main drawbacks is the risk of saturation in the control signal d . Since the artificial voltage variable x_d is the only term that constitutes the denominator of d , the control signal saturation may happen when $x_d = 0$. Besides, investigations revealed that there exists a “trade-off” between the control performances of the transient responses after the onset of a reference input and a load disturbance. In order to overcome these drawbacks, an improved voltage-mode controller is proposed in this section. In addition, the stability analysis of the voltage-mode controlled system and the feasibility of the controller are also presented.

4.4.2.1 Proposed control law

The proposed voltage-mode controller for the quadratic boost converter is described by:

$$d = \frac{\sqrt{z_d} - \sqrt{v_{in} + K_P(\bar{x}_4 - V_{ref}) + K_I\gamma}}{\sqrt{V_{ref}}} \quad (4.56)$$

$$\gamma = \int \frac{2\alpha h(\bar{x}_4 - V_{ref})}{1 + [\alpha(\bar{x}_4 - V_{ref})]^2} dt \quad (4.57)$$

$$\frac{dz_d}{dt} = \frac{1}{c_o} [-(K_1 + K_2)z_d + K_1\bar{x}_4 + K_2V_{ref}] \quad (4.58)$$

where K_P , K_I , K_1 , K_2 , α and h are the positive controller gains defined by the user and z_d is an artificial voltage variable. It can be seen that the denominator of the proposed control law (4.56) is a predefined positive constant. Hence, the risk of saturation due to division by zero which exists in the state-of-the-art control law (4.54) is avoided. Besides, since the first-order derivative of the integral action γ is bounded (see Chapter 1), γ cannot be extremely large or small when the output voltage deviates from its reference value. This feature improves the transient response of the converter output voltage.

4.4.2.2 Stability analysis

By substituting (4.56) into (4.52) and using (4.57) and (4.58), the converter model (4.52) can be written as

$$\frac{d\bar{x}_4}{dt} = \frac{1}{L_1} (-\bar{x}_3\hat{d} + v_{in}) \quad (4.59)$$

$$\frac{d\bar{x}_2}{dt} = \frac{1}{L_2} (\bar{x}_3 - \bar{x}_4\hat{d}) \quad (4.60)$$

$$\frac{d\bar{x}_3}{dt} = \frac{1}{C} (\bar{x}_1\hat{d} - \bar{x}_2) \quad (4.61)$$

$$\frac{dv_{C_o}}{dt} = \frac{1}{RC_o} (R\bar{x}_2\hat{d} - \bar{x}_4) \quad (4.62)$$

$$\frac{dz_d}{dt} = \frac{1}{c_o} [-(K_1 + K_2)z_d + K_2\bar{x}_4 + K_1V_{ref}] \quad (4.63)$$

$$\frac{d\gamma}{dt} = \frac{2\alpha h(\bar{x}_4 - V_{ref})}{1 + [\alpha(\bar{x}_4 - V_{ref})]^2} \quad (4.64)$$

where $\hat{d} = 1 - d = 1 - \frac{\sqrt{z_d} - \sqrt{v_{in} + K_P(\bar{x}_4 - V_{ref}) + K_I\gamma}}{\sqrt{V_{ref}}}$. By setting (4.59) – (4.64) to zero,

the unique equilibrium point of the closed-loop dynamics is given by

$$(X_1, X_2, X_3, X_4, z_{d\infty}, \gamma_\infty) = \left(\frac{V_{ref}^2}{Rv_{in}}, \sqrt{\frac{V_{ref}^3}{R^2v_{in}}}, \sqrt{v_{in}V_{ref}}, V_{ref}, V_{ref}, 0 \right) \quad (4.65)$$

where $z_{d\infty}$ and γ_∞ are the steady-state values of z_d and γ , respectively.

To directly carry out a stability analysis of the closed-loop system (4.59) – (4.64) is rather difficult. Hence, the linearization method is used here to enable an approximate stability analysis to be carried out to get some insight into the performance of the voltage-mode controlled system. Note that this method has been used in the stability analysis of high-order converter systems in several previous studies [19], [23], [26], [43] – [45], [57].

Now, linearizing (15) – (19) about (20) and setting $h = 1$ yields the following system:

$$\dot{\tilde{x}} = A\tilde{x} \quad (4.66)$$

where $\tilde{x} = [\tilde{x}_1, \tilde{x}_2, \tilde{x}_3, \tilde{x}_4, \tilde{z}_d, \tilde{\gamma}]^T$, $\tilde{x}_1 = \bar{x}_1 - X_1$, $\tilde{x}_2 = \bar{x}_2 - X_2$, $\tilde{x}_3 = \bar{x}_3 - X_3$, $\tilde{x}_4 = \bar{x}_4 - X_4$, $\tilde{z}_d = z_d - z_{d\infty}$, $\tilde{\gamma} = \gamma - \gamma_\infty$ and

$$A = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1}\sqrt{\frac{v_{in}}{V_{ref}}} & -\frac{K_P}{2L_1} & \frac{1}{2L_1}\sqrt{\frac{v_{in}}{V_{ref}}} & -\frac{K_I}{2L_1} \\ 0 & 0 & \frac{1}{L_2} & -\frac{2v_{in} + K_P V_{ref}}{2L_2\sqrt{v_{in}V_{ref}}} & \frac{1}{2L_2} & -\frac{K_I}{2L_2}\sqrt{\frac{V_{ref}}{v_{in}}} \\ \frac{1}{C}\sqrt{\frac{v_{in}}{V_{ref}}} & -\frac{1}{C} & 0 & \frac{K_P}{2CR}\sqrt{\frac{V_{ref}}{v_{in}}} & -\frac{V_{ref}}{2Cv_{in}R} & \frac{K_I}{2CR}\sqrt{\frac{V_{ref}}{v_{in}}} \\ 0 & \frac{1}{C_o}\sqrt{\frac{v_{in}}{V_{ref}}} & 0 & \frac{K_P V_{ref} - 2v_{in}}{2C_o v_{in} R} & -\frac{1}{2C_o R}\sqrt{\frac{V_{ref}}{v_{in}}} & \frac{K_I V_{ref}}{2C_o v_{in} R} \\ 0 & 0 & 0 & \frac{K_2}{C_o} & -\frac{K_1 + K_2}{C_o} & 0 \\ 0 & 0 & 0 & 2\alpha & 0 & 0 \end{bmatrix}$$

The system (4.66) will be stable if all the eigenvalues of A have negative real-parts[58],

namely, all the roots of the system characteristic polynomial $P_A(s) = |sI - A| = 0$,

where s is a complex variable, lie in the left-hand-side of the complex plane. Since $P_A(s)$ is of high order, it is not easy to use the analytical Routh-Hurwitz stability criterion to ensure system stability. Instead, the root-locus method is adopted. In this method, only one controller gain, say, K_P is varied from its initial value until some roots of $P_A(s)$ leave the left half of the complex plane, meanwhile the other controller gains K_I , K_1 , K_2 and α are fixed. As such, the stability range of K_P can be obtained. Using the same procedure, the stability range of the other controller gains under a specific operation condition can also be obtained.

For the purpose of illustration, consider the converter circuit parameter values given in Table 4.5.

Table 4.5 Main parameters of the quadratic boost converter system

Parameter	Value
v_{in}	10V
V_d	70 V
L_1	680 μH
L_2	560 μH
C, C_o	470 μH
R	470 Ω (4.69)

Substituting component parameters given in Table 4.5 into (4.66) gives the following characteristic polynomial P_A :

$$P_A(s) = s^6 + m_5 s^5 + m_4 s^4 + m_3 s^3 + m_2 s^2 + m_1 s + m_0 \quad (4.67)$$

where

$$m_0 = 7.23 \times 10^{15} (K_1 + K_2) \alpha K_I,$$

$$m_1 = 5.16 \times 10^{14} K_1 - 8.5 \times 10^{14} K_2 + 3.61 \times 10^{15} (K_1 + K_2) K_P + 3.4 \times$$

$$10^{12} \alpha K_I - 5.42 \times 10^{11} (K_1 + K_2) \alpha K_I,$$

$$m_2 = 4.1 \times 10^{10} K_1 + 1.43 \times 10^{11} K_2 + [1.7 \times 10^{12} - 2.71 \times 10^8 (K_1 + K_2)] K_P - 2.55 \times 10^8 \alpha K_I + 8.1 \times 10^9 (K_1 + K_2) \alpha K_I + 2.43 \times 10^{11},$$

$$m_3 = 1.02 \times 10^{10} K_1 + 8.66 \times 10^9 K_2 + [4.04 \times 10^9 (K_1 + K_2) - 1.27 \times 10^8] K_P + 3.8 \times 10^6 \alpha K_I - 67422 (K_1 + K_2) \alpha K_I + 1.92 \times 10^7,$$

$$m_4 = 9631.8 K_1 + 22373 K_2 + [1.9 \times 10^6 - 33711 (K_1 + K_2)] K_P - 31.69 \alpha K_I + 4.79 \times 10^6,$$

$$m_5 = 2127.7 (K_1 + K_2) - 15.84 K_P + 4.52.$$

Fig. 4.22. Root-locus plots of the controlled converter system: (a) for $0 < K_P < 2.5$, $\alpha K_I = 0.1$, $K_1 = 0.1$ and $K_2 = 0.1$; (b) for $K_P = 0.1$, $0 < \alpha K_I < 4$, $K_1 = 0.1$ and $K_2 = 0.1$; (c) for $K_P = 0.1$, $\alpha K_I = 0.1$, $0 < K_1 < 100$ and $K_2 = 0.1$; (d) For $K_P = 0.1$, $\alpha K_I = 0.1$, $K_1 = 0.1$ and $0 < K_2 < 5$.

The roots locus of (4.67) for various gains are shown in Fig. 4.22. To avoid the tedious calculations, the term αK_I is treated as one variable. In Fig. 4.22(a), the controller gains used are $0 < K_P < 2.5$, $\alpha K_I = 0.1$, $K_1 = 0.1$ and $K_2 = 0.1$. The movements of the poles with increasing K_P are indicated by the arrows. It is seen that two poles are in the

right-half complex plane initially. As K_P is increased, the poles move towards the imaginary axis and the left-half complex plane at $K_P = 0.047$. However, when $K_P = 1.42$, two dominant poles enter and stay in the right-half complex plane. Hence, the system is stable for $0.047 < K_P < 1.42$. Fig. 4.22(b) shows the root locus of (4.67) for $K_P = 0.1$, $0 < \alpha K_I < 4$, $K_1 = 0.1$ and $K_2 = 0.1$. In contrast to Fig. 4.22(a), initially, all the poles shown in Fig. 4.22(b) are located at the left-half complex plane, and four of them move toward to the imaginary axis as αK_I is increased. Since two of the poles enter the right-half plane at $\alpha K_I = 5.85$, the stability range of αK_I for the converter is $0 < \alpha K_I < 5.85$. Figs. 4.22(c) and 4.22(d) show the root loci for $K_P = 0.1$, $\alpha K_I = 0.1$, $0 < K_1 < 100$, $K_2 = 0.1$ and $K_P = 0.1$, $\alpha K_I = 0.1$, $K_1 = 0.1$, $0 < K_2 < 5$, respectively. The system is stable for $0.06 < K_1 < 100$ and $0 < K_2 < 0.18$.

4.4.2.3 Controller feasibility

Next, the internal stability of the regulated converter system is addressed. Equation (4.56) can be rewritten as:

$$z_d = \left(\sqrt{V_{ref}}d + \sqrt{v_{in} + K_P(\bar{x}_4 - V_{ref}) + K_I\gamma} \right)^2 \quad (4.68)$$

The time derivative of the control signal d in (4.56) is given by

$$\dot{d} = \frac{1}{2\sqrt{V_{ref}}} \left(\frac{\dot{z}_d}{\sqrt{z_d}} - \frac{K_P\dot{\bar{x}}_4 + K_I\dot{\gamma}}{\sqrt{E + K_P(\bar{x}_4 - V_{ref}) + K_I\gamma}} \right) \quad (4.69)$$

where $\dot{z}_d$, $\dot{\bar{x}}_4$ and $\dot{\gamma}$ are the time derivatives of z_d , $\bar{x}_4$ and γ , respectively.

Now, substituting (4.52), (4.63), (4.64) and (4.68) into (4.69) yields

$$\dot{d} = \frac{1}{2\sqrt{V_d}} \left\{ \frac{1}{C_o} \left[\frac{K_2 \bar{x}_4 + K_1 V_{ref}}{\sqrt{V_{ref}} d + \sqrt{E + K_P(\bar{x}_4 - V_{ref}) + K_I \gamma}} - (K_1 + K_2) \left(\sqrt{V_{ref}} d + \sqrt{E + K_P(\bar{x}_4 - V_{ref}) + K_I \gamma} \right) \right] - \frac{[K_P[R\bar{x}_2(1-d) - \bar{x}_4]/(RC_o)] + \{2\alpha K_I(\bar{x}_4 - V_{ref})/\{1 + [\alpha(\bar{x}_4 - V_{ref})]^2\}\}}{\sqrt{E + K_P(\bar{x}_4 - V_{ref}) + K_I \gamma}} \right\} \quad (4.70)$$

Setting $\bar{x}_2$, $\bar{x}_4$ and γ equal to their equilibrium values X_1 , X_4 and γ_∞ , respectively, gives the following internal dynamics of the closed-loop system:

$$\dot{d} = \frac{1}{2\sqrt{V_{ref}}} \left\{ \frac{(K_1 + K_2)}{C_o} \left[\frac{V_{ref}}{\sqrt{V_{ref}} d + \sqrt{v_{in}}} - \left(\sqrt{V_{ref}} d + \sqrt{v_{in}} \right) \right] - \frac{K_P V_{ref} [\sqrt{V_{ref}}(1-d) - \sqrt{v_{in}}]}{v_{in} RC_o} \right\} \quad (4.71)$$

For the purpose of illustration, the circuit parameters given in (4.69) are used here.

Substituting (4.69) into (4.71), the resulting phase-portrait of (4.71) is shown in Fig. 4.23.

Fig. 4.23. ‘Remaining dynamics’ for the voltage-controlled converter.

It can be seen that $D = 1 - \sqrt{v_{in}/V_{ref}}$ is the unique equilibrium point of the internal dynamics of the closed-loop system, and it is stable. Finally, the key result is given in the following proposition:

Proposition: Given a reference voltage V_{ref} , where $v_{in} < V_{ref} < \infty$, the proposed control law (4.56) – (4.58) together with an appropriate set of controller gains, locally

asymptotically stabilizes the averaged model of the quadratic boost converter (4.54) to

its equilibrium point $(X_1, X_2, X_3, X_4) = \left(\frac{V_{ref}^2}{Rv_{in}}, \sqrt{\frac{V_{ref}^3}{R^2v_{in}}}, \sqrt{v_{in}V_{ref}}, V_{ref} \right)$ for $0 < R < \infty$.

4.4.3 Simulation and Experimental Results

In this section, simulation and experimental results are provided to show the effectiveness of the proposed controller for the quadratic boost converter. In addition, guidelines for selecting the controller gains to achieve the desired output response are also presented. The same set of converter circuit parameter values in (4.69) were used in both simulation and experiments. The block diagram of the closed-loop converter system is shown in Fig. 4.24.

Fig. 4.24. Block diagram of the closed-loop quadratic boost dc-dc converter system.

4.4.3.1 Tuning guidelines for the controller gains

The proposed controller has four controller gains, viz., K_P , αK_I , K_1 and K_2 . It is not obvious how these controller gains can be selected to achieve the desired converter output response. In order to select the controller gains properly, the effects of the

controller gains on the converter output responses need to be addressed. The initial values of the controller gains used in the simulations were set as $K_p = 0.12$, $\alpha K_I = 4$, $K_1 = 0.2$ and $K_2 = 0.15$ to ensure the regulated converter system is stable with negligible steady-state error.

Fig. 4.25 shows the output responses for various controller gains. These simulation results were obtained from a controlled quadratic boost converter system built in MATLAB/SIMULINK. In these simulations, the value of the load resistance R was changed from $470\ \Omega$ to $235\ \Omega$ at $t = 2\text{ s}$. Fig. 4.25(a) shows the output responses for various values of K_p . It is seen that increasing K_p led to an increased overshoot in the transient response. On the other hand, it also resulted in a smaller voltage variation as well as a smoother transient response. The output responses for different values of αK_I are given in Fig. 4.25(b). It is seen that increasing αK_I results in a larger overshoot and more oscillations in the start-up response. However, it led to a smaller voltage variation and a faster convergence to the desired voltage after the onset of a load change. Similar to K_p and αK_I , the values of K_1 and K_2 also affected the transient response. Fig. 4.25(c) shows the output responses for various values of K_1 . As the value of K_1 was increased, the overshoot in the transient response was also increased and the settling time became larger. However, after the onset of a load change, a smoother transient response with a smaller variation was obtained. The output response for a varying K_2 is shown in Fig. 4.25(d).

Next, the effects of α and K_I on the output voltage response were investigated individually. The output voltage responses for a constant value of αK_I but varying values of α and K_I are shown in Fig. 4.26.

Fig. 4.25. Output voltage responses: (a) for varying K_p , (b) for varying αK_I , (c) for varying K_I and (d) for varying K_2 .

Fig. 4.26. Output voltage response for constant αK_I but varying α and varying K_I .

It can be seen that if αK_I is constant, varying the values of α and K_I did not have

much effect on the transient response in the presence of a load disturbance. But a large value of K_I (or a small value of α) resulted in a large overshoot during startup. This is the main feature of the proposed controller. Since the overshoot during start-up can be suppressed without affecting the response after the onset of a load disturbance, the aforementioned “trade-off” problem in the existing voltage-mode controllers can be overcome.

In view of these observations, a heuristic controller gain tuning guidelines can be summarized as follows: An appropriately large value of K_P is first selected to achieve a fast response after the onset of load disturbances. Next, a relatively small value of αK_I is chosen to improve the transient of the output response. Since increasing K_1 and K_2 has opposite effects on the output response, the optimum values for K_1 and K_2 can be found to achieve the desired output response. Finally, if the overshoot during startup is large, a small α can be selected to suppress the overshoot while keeping αK_I unchanged.

4.4.3.2 Comparison with existing voltage-mode controller

In order to show the advantages of the proposed controller, a comparative study involving the existing state-of-the-art voltage-mode controller (4.54) – (4.55) and the proposed controller was carried out. In the comparative study, the circuit parameters given in (4.69) were used. Besides, the value of load resistance R was changed from 470 Ω to 235 Ω at $t = 2$ s.

Fig. 4.27 shows the output voltage responses of the quadratic boost converter, where the solid blue line and the dashed red line are the output voltage responses obtained using the existing voltage-mode controller (4.54) – (4.55) for different controller gains. It is evident that there

Fig. 4.27. Output voltage responses of the regulated quadratic dc-dc boost converter (the solid blue line and the dashed red line are output responses obtained using the existing voltage-mode controller, while the dotted black line is the output response obtained using the proposed controller).

exists a trade-off between the transient performances after the onset of a step reference input and the load disturbances. The output voltage response obtained using the proposed controller is given by the dotted black line. It can be seen that after the onset of a reference input and a load resistance change, the desired output transient responses were obtained. The simulation results indicate that the proposed controller provides a better performance as compared to that obtained using the existing voltage-mode controller.

4.4.3.3 Experimental results

In this section, some experimental results, obtained using dSPACE (see. Fig. 4.28(a)), to show the effectiveness and advantages of the proposed controller in regulating the quadratic boost converter are provided. Besides, in order to carry out the experiments, a laboratory prototype of the quadratic boost converter was built, and its photo is shown in Fig. 4.28(b). The circuit parameter values used were those in Table 4.5, and the switching frequency used was 30 kHz. In addition, the specifications of the desired

regulated converter system performance and the schematic of the proposed controller, built using SIMULINK, are given in Table 4.6 and Fig. 4.29, respectively.

Table 4.6 Specifications of the desired regulated converter system performance

Performance	Value
Voltage dip (swell) in the presence of load resistance changes	$\leq 10\%$
Settling time in the presence of load resistance changes	$\leq 0.5s$
Voltage dip (swell) in the presence of input voltage changes	$\leq 15\%$
Settling time in the presence of input voltage changes	$\leq 0.5s$

Fig. 4.28. Experimental facilities: (a) dSPACE experimental platform; (b) laboratory prototype of the quadratic boost DC-DC converter.

Fig. 4.30 shows the output voltage responses of the quadratic boost converter in the presence of step changes in the output power, where the output power P_{out} was changed from 10.4 W to 20.8 W and then restored to 10.4 W. The output voltage responses of the system obtained using the existing voltage-mode controller (given by (4.54) – (4.55)) and the proposed controller are given in Figs. 4.30(a), 4.30(b) and Figs. 4.30(c), 4.30(d), respectively. It can be seen that both controllers provide similar control performance in the presence of output power disturbances. More specifically, the output voltage deviation was less than 8% of its nominal value.

Fig. 4.30. Output voltage v_o of the quadratic converter in the presence of output power changes: (a) using the existing voltage mode controller (P_{out} was changed from 10.4 W to 20.8 W); (b) using the existing voltage mode controller (P_{out} was changed from 20.8 W to 10.4 W); (c) using the proposed controller (P_{out} was changed from 10.4 W to 20.8 W); (d) using the proposed controller (P_{out} changes from 20.8 W to 10.4 W).

Next, the ability of the proposed controller to handle the reference voltage and input voltage changes was compared with that of the existing voltage-mode controller. Fig. 4.31(a) shows the output voltage response obtained using the existing voltage-mode controller in the presence of a step change in the reference voltage V_{ref} from 60 V to 70 V. The overshoot of the output voltage was relatively large, which was around 10% of the desired value of the output voltage. Besides, the settling time of the voltage response was around 0.15 s. Fig. 4.31(b) shows the output voltage response obtained using the existing voltage-mode controller in the presence of an input voltage change from $E = 10$ V to $E = 7$ V. Again, the overshoot in the transient response was large, i.e., around 17% of the desired value of the output voltage, and the output response was restored to its desired value in 0.7 s.

Fig. 4.31. Output voltage v_o of the quadratic converter system: (a) in the presence of reference voltage change using the existing voltage mode controller; (b) in the presence of input voltage change using the existing voltage mode controller; (c) in the presence of reference voltage change using the proposed controller; (d) in the presence of input voltage change using the proposed controller.

Next, the output performance obtained using the proposed voltage-mode controller (4.56) – (4.58) under the previous changes in V_{ref} and v_{in} was investigated. Fig. 4.31(c) shows the output response under a step change in V_{ref} . It can be seen that the output voltage was quickly restored to its desired reference value with a small overshoot (around 2% of the desired voltage) and a small settling time (smaller than 0.1 s). Also, the output response under the input voltage disturbance is shown in Fig. 4.24(d). In Fig. 4.31(d), the maximum voltage deviation was below 14% of the desired output voltage, and the settling time of the output response was nearly half of that shown in Fig. 4.31(b) (around 0.35 s).

The experimental results shown Figs. 4.30 – 4.31 are seen to be in agreement with the analytical analyses and the simulation results showing the performance of the proposed controller is better than the state-of-the-art voltage-mode controller. It was observed that even though both controllers can regulate the quadratic boost converter and provide

similar performance in the presence of load disturbances, the proposed controller has a better performance in the presence of input and reference voltage changes. Besides, the performance of the converter system using the proposed controller fully met ~~fulfills~~ the control performance specifications given in Table 4.6.

4.4.4 Conclusion

In this section, an improved voltage-mode control law for the regulation of the quadratic boost dc-dc converter was proposed. To overcome the disadvantages of the existing voltage-mode controller, a controller structure different from the existing one and an integral action using the normalized output voltage error were adopted in the proposed controller. The stability and feasibility of the closed-loop system were verified. Besides, some simulation and experimental results showed that, as compared with the existing voltage-mode controller, the proposed control law provides superior control performance for the quadratic boost converter over a wide range of operation conditions.

4.5 Conclusion

In this chapter, three improved voltage-mode controller were proposed. In the first section, a voltage-mode controller using a new structure was proposed for regulating the MBC. In contrast to some existing voltage-mode controller, this structure allows the use of the frequency-domain technique and stability margin criteria to select the appropriate controller gains for the regulated converter system. As a result, a robust closed-loop MBC system can be achieved. The simulation and experimental results showed that the proposed controller has good performance in wide converter operation conditions.

Next, an output feedback controller for the POSRL converter was presented. In some state-of-the-art output feedback controllers, there exists the risk of control signal

saturation due to the possibility of division by zero. In the proposed controller, a new structure is adopted. The denominator of the control law is the user defined constant. As such, the saturation problem is avoided.

Finally, an improved voltage-mode controller for a quadratic boost converter is proposed. A normalized integral action is used in the proposed controller to improve the converter output responses. The simulation and experimental results showed that the “trade-off” between the transient output responses after the onset of a reference input and a load disturbance when the quadratic converter regulated by a state-of-the-art voltage-mode controller is avoided when the proposed controller is adopted instead.

It is worth noting that all the voltage-mode controllers can be applied to other high-order boost converters. However, since the basic structure of this type of voltage-mode controller is decided by the expression of the steady-state duty-ratio of the specific converter, the controller structure may differ slightly from each other.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this thesis, some studies on the control of high-gain boost converters are presented. More specifically, in Chapter 1, the background of this study is introduced. Besides, the necessity of carrying out this study is also presented. A literature review of this study is presented in Chapter 2. The pros and cons of some state-of-the-art high-gain boost converters, the modelling of several high-gain boost converters and some state-of-the-art control techniques are reviewed. The main contribution and detailed work of this thesis are given in Chapter 3 and Chapter 4.

In Chapter 3, the adaptive current-mode controllers for controlling the hybrid-high-order boost converter are presented. Due to the use of an estimator in estimating the load conductance, the proposed adaptive controller has a better control performance as compared to the existing current-mode controller. This is confirmed by both simulation and experimental results. For high-gain boost converters with more than one inductor, it is necessary to carry out stability analyses of the inductor-current controlled converter systems to determine the most suitable inductor current for feedback purposes before implementing the current-mode controller.

In Chapter 4, some improved voltage-mode controller are proposed for regulating high-order boost converters. These controllers not only possess the merits of the existing voltage-mode controllers, such as the current sensor is not needed in the controller

implementation, but also overcome several shortcomings of some state-of-the-art voltage-mode controllers. More specifically, a voltage-mode controller for the regulation of the MBC is first proposed. The proposed controller adopts a new structure which allows the direct usage of Bode-plot and stability margin criteria to select appropriate controller gains. As compared to some previous literature using the trial and error method to find the desired controller gains, the proposed controller structure simplifies the controller gain selection procedure without compromising the control performance. Next, an output feedback controller for the POSRL converter is proposed. Although some existing voltage-mode controllers can provide stable control performance for the high-gain dc-dc converter, there exists the risk of control signal saturation due to the possibility of division by zero. The proposed controller adopts a new structure which uses a positive constant as its denominator. As such, the possible saturation problem is avoided. In addition, the simulation and experimental results show that the proposed controller provides good control performance when regulating the POSRL converter in a wide range of operation conditions. In the last section of Chapter 4, a voltage-mode controller using the normalized integral action for a quadratic boost converter is addressed. Since the first-order derivative of the integrand with respect to the voltage error is bounded, the extreme change in the control signal is avoided although the output voltage can vary greatly. Compared to the existing voltage-mode controller, the proposed controller provides superior output performance, especially in the presence of input and reference voltage changes, and is confirmed by both simulation and experimental results.

5.2 Recommendations for Future Works

Despite some studies on the control of high-gain boost converters have been carried out as reported in this thesis, there remain numerous works to be done to improve the control performance of the regulated converter systems as well as to address some open problems. The recommendations for the future work are as follows:

1. The voltage-mode controller proposed in Chapter 4, section 4.2 uses the PI control technique to regulate the high-gain boost converter. Although the Bode-plot and stability margin criteria can help the user to select the appropriate controller gains, the chosen controller gains are not optimum. Therefore, optimal control techniques, such as H_2 and H_∞ control technique, can be adopted in the voltage-mode controller instead. The resulting optimal voltage-mode controller will lead to a more robust converter system. How to combine the optimal control techniques and the voltage-mode controller is certainly worth looking into.
2. In Chapter 4, all the proposed voltage-mode controllers are designed based on the converter systems with purely resistive loads. However, in practical applications, the constant power load (CPL) also plays an important role in power electronics systems [59] – [64]. Although the voltage-mode control scheme has several merits, a voltage-mode controller for high-gain boost dc-dc converters with CPL has not been reported. Therefore, developing appropriate voltage-mode control laws for high-gain converters with CPL can be one of the future works.
3. In Chapters 3 and 4, the normalized integral action shows superior performance as compared to its linear integral counterpart. As a future work, this advanced

integral action could be combined with other control techniques to further improve the control performance of high-gain boost converters.

Author's Publications

Journal Papers:

1. **W. Jiang**, S. H. Chincholkar, and C.-Y. Chan, "An improved output feedback controller design for the super-lift re-lift Luo converter," *IET Power Electronics*, vol. 10, no. 10, pp. 1147-1155, 2017.
2. **W. Jiang**, S. H. Chincholkar, and C.-Y. Chan, "Investigation of a voltage-mode controller for a dc-dc multilevel boost converter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol.65, no. 7, pp.908-912, 2018.
3. **W. Jiang**, S. H. Chincholkar, and C.-Y. Chan, "A comparative of adaptive current-mode controllers for a hybrid high-order boost converter," *IET Power Electronics*, vol. 11, no. 3, pp. 524-530, 2018.
4. **W. Jiang**, S. Chincholkar, C. Y. Chan, "An Improved Voltage-Mode Controller for the Quadratic Boost Dc-Dc Converter," *IET Power Electronics*, (Accepted)
5. C.-Y. Chan, S. H. Chincholkar and **W. Jiang**, "Adaptive current-mode control of a high step-up dc-dc converter", *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7297-7305, 2017.
6. S. H. Chincholkar, **W. Jiang** and C.-Y. Chan, "On the PWM-based Adaptive Sliding-Mode Control of a Dc-Dc Cascade Boost Converter", *IEEE Transactions on Circuits and Systems II: Express Briefs* (Accepted).
7. S. H. Chincholkar, **W. Jiang** and C.-Y. Chan, "A modified Hysteresis-modulation-based Sliding Mode Control for Improved Performance in Hybrid Dc-Dc Boost Converter", *IEEE Transactions on Circuits and Systems II: Express Briefs* (Early Access).

Conference Papers:

1. **W. Jiang** and C.-Y. Chan, “A sliding-mode controller for a multilevel DC-DC boost converter,” *2016, IECON 2016 – 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, Italy, Dec. 2016, pp. 1239-1244.

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