Low power AC-DC converters for wireless power transfer application

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**NANYANG
TECHNOLOGICAL
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**LOW POWER AC-DC CONVERTERS
FOR
WIRELESS POWER TRANSFER APPLICATIONS**

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Abstract

Wireless power transfer (WPT) technology is gaining its popularity in recent years, which is largely motivated by extensive research work. It is attractive as the power and data transmission can be done through the magnetic field between two coils without the usage of power wires. It offers the convenience of charging or operating a device without having to plug-in. For example, electronic devices such as cell phones and smart watches or electric vehicles could be charged without utilizing power cord as in the conventional way. WPT technology is advantageous to various applications with different specifications and constraints. Besides wireless charging, it contributes greatly to RFID and medical fields as well, such as wireless capsule endoscopy for early detection screening, biomedical implants like cochlear implants, RFID animal tag for prevention of infectious disease, etc. The emerging WPT technology has become an appealing approach in industrial applications and it is expected to continually grow in near future.

In this research, the focus is on the power management integrated circuits (PMIC) design of the wireless power receiver in an inductively WPT system. Several designs are proposed to improve the performance of the receiver for the applications with output power in the range of 1 to 100 mW, operating in an ISM band of 125 kHz, such as for RFID animal tag or biomedical implants. In a wireless power receiver, a rectifier and a voltage regulator are the crucial blocks for AC-DC conversion and DC-DC regulation. An unbalanced biasing comparator design is proposed to solve the reverse leakage current issue of the rectifier block. A buck regulator with a proposed energy-efficient pulse frequency modulation (PFM) controller is implemented as well. Measurement results show that the rectifier achieves a peak efficiency of 85.92% while the buck regulator achieves a peak efficiency of 91.00%.

However, the two-stage design restricts the overall power efficiency of the receiver. In order to improve the power efficiency, a one-stage AC-DC regulator is proposed by introducing a dual-mode concept. As a result, the power losses

incurred have been reduced from two-stage to one-stage, improving the power efficiency substantially. Fabricated in a 0.18 μ m CMOS process, the measured peak efficiency is 93.48% in an output power range of 2 to 80 mW.

To maximize the circuits' performances in embedded applications, more than one supply voltage is often required in a system. Hence, a new architecture which is able to rectify and regulate multiple outputs concurrently in a single-stage is developed. In addition, a multi-mode controller is also proposed to control the multiple switches of the structure efficiently. As a proof of concept, a prototype has been validated for the tri-mode dual-output design. Nonetheless, the concept is applicable and extendable to N outputs. The measured peak power efficiency of the tri-mode dual-output design is 91.68% in an output power range of 3.8 to 114 mW.

Lastly, a single-stage voltage doubler regulator is proposed. The previous designs operate with a criterion that the input voltage has to be greater than the output voltage. To solve the limitation, a voltage doubler structure is utilized. By embedding the regulation capability in the voltage doubler structure, the voltage rectification and regulation are achieved at an output voltage which is twice of the input voltage amplitude. The simulated peak power efficiency is 94.40%.

The major contributions of this dissertation are the design of two-stage receiver with improvement done on the rectifier block as well as the buck regulator block, a single-stage receiver design which aims to improve the power efficiency from two-stage to one-stage, a single-stage dual-output design to maximize the power efficiency of a system that requires more than one regulated output voltage and a single-stage voltage doubler design to extend the power transmission range.

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List of Abbreviations

WPT	Wireless power transfer
EM	Electromagnetic wave
ISM	Industrial, scientific and medical radio band
UHF	Ultra-high frequency
IPT	Inductive power transfer
MR	Magnetic resonance
RFID	Radio frequency identification
WPC	Wireless power consortium
SPS	Solar power satellite
SHARP	Stationary high altitude relay platform
LF	Low frequency
HF	High frequency
ISO	International organization for standardization
PMIC	Power management integrated circuits
AC	Alternating current
DC	Direct current
M	Mutual inductance
k	Coupling coefficient
LDO	Low-dropout regulator
ESR	Equivalent series resistance
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
PWM	Pulse width modulation
PFM	Pulse frequency modulation
PSM	Pulse skipping modulation
EMI	Electromagnetic interference
TM	Time-multiplexing
OPDC	Ordered power distributive control

ZCD	Zero current detector
DA-AOT	Digitally-assisted adaptive on-time
AOT	Adaptive on-time
FSM	Finite state machine
DIP	Dual in-line package
QFN	Quad flat no-leads package
SIDO	Single inductor dual-output
PMU	Power management unit
IA	Instrumental amplifier

Chapter 1 Introduction

1.1 Background

The concept of wireless power transfer (WPT) was first introduced by Nikola Tesla, who is also known as the ‘Father of Wireless’. Tesla implemented a principle that apply today, that is an alternating current can be induced in a nearby secondary coil by having an alternating magnetic field generated from an alternating current in a wire loop. In 1899, he conducted his first experiment by transmitting power wirelessly in Colorado Spring with the Tesla Coil fed with 300 kW at a low frequency of 150 kHz. The emphasis of Tesla’s invention is much more on the wireless power transfer capability rather than the communication aspect of a system [1-3]. The electromagnetic (EM) wave power transmission is a far-field power transfer. It consists of 3 steps, in which the dc electrical power is firstly converted into RF power and the RF power is transmitted into the space to reach the receiving destination. Lastly, the RF power is converted back to the dc power at the receiver. The EM wave power transmission is typically done at the ISM frequency band of 860-960 MHz or 2.4-2.5 GHz. Numerous works have been published in the area of EM WPT [4-9]. Even though the power transmission in the ultra-high frequency (UHF) or microwave enables a smaller size of antenna element, the power losses incurred from the transmission is high and the microwave radiation that exposed to human body is a great concern as well. There is a trade-off between the beam control and power transmission efficiency. Several attempts have been made in [4-5] to wirelessly charge up a portable device via far-field transmission. But the energy transferred under the RF safety standard [10] is inefficient and insufficient to charge up a cell phone. Hence, far-field power transmission technique is more suitable for low power applications where the efficiency is not a prime concern. It is beneficial to high-power systems as well, such as for space exploration and military, where the prime goal is receiving power wirelessly and the cost is the

secondary concern [11].

Near-field power transfer can be categorized into two types, which are the inductive power transfer (IPT) and magnetic resonance (MR) power transfer [11]. They are non-radiative power transfer and thus the power losses are lower as compared to the EM wave WPT. An ideal example of IPT is a transformer which makes use of the magnetic induction principle to transfer energy wirelessly. IPT technology is widely used in consumer electronic products such as electric vehicles, electric toothbrushes, RFID control, wireless charging for portable devices, etc [12-15]. The IPT is based on the 'Qi' standard developed by the Wireless Power Consortium (WPC) and the power level is achievable in the range from several microwatts to a few kilowatts. The operating frequency is typically in the range of 20 kHz-1 MHz. By operating at frequencies below 1 MHz, the probability of interference and RF safe issues can be minimized. The main advantages of closely coupled IPT are high power transfer efficiency, simple and mature. However, it requires proper alignment between a transmitting and a receiving unit. The power transfer efficiency degrades as the distance between a transmitter and a receiver increases [16-17].

The operation of the MR power transfer was demonstrated by a group of researchers from Massachusetts Institute of Technology (MIT) in 2007. They used a system of two coupled magnetic resonances to wirelessly power up a 60 W light bulb with the efficiency of around 40% over a distance of more than 2 meters, as shown in Fig. 1.1 [18]. The MR power transfer is supported by Rezence standard which is developed by the Alliance for Wireless Power (A4WP) based on the magnetic resonance principle [19]. The operating frequency is in the range of 1 MHz - 20 MHz, which is higher than the IPT. The MR power transfer offers the spatial freedom and the flexibility in the coils' alignment. The coils can be loosely coupled but high quality factor coils are required in order to maintain a power transmission distance of several centimeters [19-23]. The drawback of the MR power transfer is the low power transfer efficiency due to flux leakage even at a close distance of several centimeters. Since the operating frequency is

higher, the circuits' complexity increases as well. Compared to the IPT, even though the MR power transfer offers the convenience of spatial freedom, the power transfer efficiency is lower than the IPT, as shown in Fig. 1.2 [19].

Fig. 1.1 The MR power transfer experiment conductor in MIT in 2007 [20].

Fig. 1.2 Efficiency comparison between IPT (Qi) and MR WPT (Rezence) [19].

1.2 Motivation

In today's modern world, the rapid growth of technology has changed human's life greatly and continually. With the expansion of semiconductor industry, WPT technology with intelligent control at affordable cost has become an appealing approach for industrial applications nowadays. WPT technology is advantageous to a wide range of applications with different specifications and constraints. It is an attractive choice for consumer electronic products due to numerous reasons. One of the reasons is it allows the power to be transferred wirelessly to inaccessible loads, such as bio-medical implants, pill capsules, RFID animal control, etc. Another reason is it offers the spatial freedom by enabling multiple portable devices such as cell phones, smart watches and laptops to be charged at the same time. Furthermore, it is a safe and convenient power transfer method since it removes the use of exposed conductor.

In entertainment field like virtual reality games, by making use of the WPT technology, a wireless link between a headset and its host computer can be realized without the need of using dangling cables. Apart from these, one of the WPT applications like solar power satellites (SPS) has the potential to solve some of the drawbacks of the current renewable energy systems. The SPS is a better alternative than the ground-based solar power harvesting. For instance, the operation of the ground-based solar power harvesting is restricted by the weather. The obstacles such as having heavy clouds or lack of sunlight during rainy days or nights could impede the operation of the approach. On the other hand, the SPS harvest the solar energy in the space and transmit it to the earth by using EM wave radiation. The sun energy available in the space is unlimited and unaffected by the weather. Therefore, the SPS is a preferred choice to the ground-based solar power harvesting [24]. Another interesting future application of the WPT is the unmanned plane, which is called stationary high altitude relay platform (SHARP) which serves as a communication relay. It is still under research and development. By installing a large antenna behind the plane wings, the power can be

transmitted from the earth and enables the plane to stay in the air for some periods of time [25]. Fig 1.3 shows different applications of the WPT systems and Table 1.1 summarizes the different types of WPT systems with different properties, standards and applications.

In spite of the advantages, it is still a challenging task to design a high efficiency and high performance WPT system. The power efficiency of the wireless power receiver is the prime goal of the research work. Thus, designing high efficiency circuits designs and circuits' solutions are the main challenges of this research. Nonetheless, the attractive benefits and the challenges of the WPT systems have motivated this research work greatly.

Fig. 1.3 The applications of WPT systems.

Table 1.1 Different types of WPT system for different applications [30].

	Near-field power transfer		Far-field power transfer	
Types	Short-range (LF)	Mid-range (HF)	Ultra-high frequency (UHF)	EM wave
Frequency	30 kHz – 300 kHz	3 MHz – 30 MHz	860 – 960 MHz	2.45-2.5 GHz / 5.8 GHz
Relevant RFID standards	ISO 11784 & 11785, ISO 14223-1, ISO 18000-2	ISO 14443, ISO 18000-3, ISO 15693	ISO 18000-6, EPC class-0, class-1	ISO/IEC 18000-4
Typical read range	< 0.5 m	~ 1 m	~ 4-5 m	~ 1 m
Characteristics	<p>i) It has the best skin depth and best affixed to wood or plastic glasses.</p> <p>ii) It is not very sensitive to radio wave interference compared to HF but it has a slower read speed.</p>	It has spatial freedom and flexibility in the coils' alignment.	<p>i) It is radiative power transfer and the power losses are huge.</p> <p>ii) It is suitable for low power applications where efficiency is not a priority or high-power systems where the power transfer capability outweighs the cost.</p>	
Typical applications	Animal tracking control includes ear tag for identification and glass tag for temperature or pressure tracking, biomedical implants, electric vehicles, wireless charging for portable devices.	Smart card, wireless charging for portable devices, biomedical implants.	Wireless sensor network, solar power satellites (SPS), unmanned plane (SHARP)	
Skin depth & Ability to read near metal/wet surfaces	Best Worst			

1.3 Objectives and Scopes

This research work is targeting at applications in the output power range of 1 to 100 mW, such as for animal tracking control or biomedical implantation. For an effective power transfer through living bodies, the operating frequency is limited from kHz to MHz range as the living bodies which consist of more than 50% of water. The skin depth is the best in the kHz range of frequency and it degrades as the frequency increases [31]. Hence, the system operates at an ISM band of 125 kHz in order to minimize the power losses.

The objectives are listed below:

- To design high efficiency and high performance power management integrated circuits (PMIC) of wireless power receivers for IPT systems by utilizing innovative circuit designs and solutions.
- To develop an intelligent control, affordable cost and energy-efficient one-stage regulation method for IPT systems.
- To develop a multiple-output alternating current (AC)-direct current (DC) regulator structure for maximizing the circuits' performances and minimizing the power consumption of embedded applications that require more than one supply voltage.

1.4 Thesis Contributions

The thesis contributions are listed below:

- i. Design of two crucial blocks for a wireless power receiver. These include a rectifier block for AC-DC conversion and an energy-efficient buck regulator for DC-DC regulation. An unbalanced biasing comparator is proposed to overcome the reverse leakage problem that occurred in the rectifier design. A buck regulator with proposed energy-efficient pulse frequency modulation (PFM) is implemented to regulate the rectified

voltage.

- ii. Design of a single-stage AC-DC converter to rectify and regulate the output voltage concurrently. This is to solve the limitation of the two-stage design in (i). The power losses incurred from the two-stage have been reduced to one-stage, improving the power efficiency substantially. This is accomplished by incorporating PFM and pulse skipping modulation (PSM) control into the active rectifier structure. In addition, a unique PFM algorithm is proposed to enhance the power efficiency during light-load conditions.
- iii. Design of a single-stage multiple-output (SSMO) AC-DC regulator to enable multiple outputs to be rectified and regulated simultaneously in one-stage. A new architecture is developed to provide rectification and regulation for two or more outputs concurrently. In addition, a multi-mode controller is also proposed to control the multiple switches of the structure. As a proof of concept, a prototype has been validated for tri-mode dual-output design. Nonetheless, the concept is applicable and extendable to N outputs, where $N \geq 2$. This SSMO AC-DC design helps to optimize the circuits' performances of applications that require multiple supply voltages.
- iv. Design of a single-stage voltage doubler (SSVB) regulator to rectify and regulate an output voltage that is twice of the input amplitude. This helps to solve the limitation of the designs from (i) to (iii) as they operate well under a criterion that the input amplitude has to be greater than the output voltage by at least two turn-on resistance voltage drops of the power switches. With a voltage doubler structure, the rectification and regulation can still be performed even when the input amplitude is lower than the output voltage.

1.5 Thesis Organization

This dissertation constitutes seven chapters. Chapter 1 gives a brief introduction to the background of WPT and specifies the objective and scopes of the research work. Chapter 2 reviews the past literature regarding the following:

- (i) WPT basic concepts.
- (ii) Different rectifier designs and structures for WPT system.
- (iii) Control methodologies for DC-DC converters especially for a buck regulator.
- (iv) Single inductor multiple-output (SIMO) DC-DC converter and its control methodologies.
- (v) Several advanced power control or regulation methods.

Next, Chapter 3 discusses a two-stage receiver with the proposed rectifier design and the proposed PFM controlled buck regulator. Chapter 4 presents the proposed single-stage AC-DC converter for IPT applications and Chapter 5 discusses the proposed single-stage multiple-output (SSMO) AC-DC regulator with its flexible controller.

In Chapter 6, a single-stage voltage doubler (SSVB) regulator is presented. Finally, Chapter 7 concludes the thesis and provides some recommendations for the future work.

Chapter 2 Literature Review

2.1 WPT basic concepts

An inductively powered WPT system utilizes the fundamental of magnetic induction principles to transfer the power between two air coils. As illustrated in Fig. 2.1, L_1 is the primary coil while L_2 is the secondary coil and R_2 is the secondary coil resistance and R_L is the load. The electric current i_1 that flows in the primary coil L_1 produces a magnetic field around it. The secondary coil L_2 which is in the vicinity of the primary coil intersects with the magnetic field and induces a voltage U_2 in the coil itself. According to the Faraday's Law, the induced voltage (electromotive force) on the secondary coil is equal to the time rate of change of the magnetic flux, as shown in Eq. (2.1.1) [32].

$$u_i = \oint E_i \cdot ds = -\frac{d\phi(t)}{dt} \quad (2.1.1)$$

Fig. 2.1 Two parallel magnetically coupled loops and their equivalent circuit diagram [32].

In order to improve the power transfer efficiency of the WPT system, a capacitor is usually added on both sides to resonate at the operating frequency of

the system and the resonant frequency of both primary (ω_p) and secondary (ω_s) sides can be expressed as in Eq. (2.1.2).

$$\omega_p = \omega_s = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} \quad (2.1.2)$$

Since the resonance capacitor can be placed either in series or in parallel with the inductor, there are four different possible compensation topologies which are the series-series (SS), series-parallel (SP), parallel-series (PS) and parallel-parallel (PP), as illustrated in Fig. 2.2.

Fig. 2.2 Different resonant topologies : (a) SS, (b) SP, (c) PS, (d) PP.

The first letter S or P represents a capacitor is in series or parallel with the primary coil while the second letter S or P denotes either a series or parallel compensation of the secondary coil. Each of the compensation topology has its own characteristics. A series compensated secondary yields a constant-voltage capability while a parallel compensated secondary behaves like a constant-

current source [33]. Another advantage of the parallel compensated secondary is that the parasitic capacitances of the coil L_s can be used as resonance capacitance at higher operating frequency. Hence, the use of C_s can be omitted. The reflected impedance of the series and parallel compensated secondary at the resonance frequency (ω_o) can be expressed in Eq. (2.1.3) [34].

$$Z_{ro} = \begin{cases} \frac{\omega_o^2 M^2}{R} & ; \text{series compensated secondary} \\ \frac{M^2 R}{L_s^2} - j \frac{\omega_o M^2}{L_s} & ; \text{parallel compensated secondary} \end{cases} \quad (2.1.3)$$

As can be inferred from Eq. (2.1.3), the major difference between the series and parallel compensated secondary topology is that the series compensation is purely resistive with zero reflected reactance, whereas a parallel compensation has a capacitive load.

The load impedance (Z_t) seen by the power supply for both series and parallel compensated primary can be derived in the equations from Eq. (2.1.4) to (2.1.6), where Z_r is the reflected impedance of the secondary on the primary side and Z_s is the secondary load impedance [34].

$$Z_t = \begin{cases} \frac{1}{j\omega C_p} + j\omega L_p + Z_r & ; \text{series compensated primary} \\ \frac{1}{j\omega C_p + \frac{1}{j\omega L_p + Z_r}} & ; \text{parallel compensated primary} \end{cases} \quad (2.1.4)$$

$$Z_r = \frac{\omega^2 M^2}{Z_s} \quad (2.1.5)$$

$$Z_s = \begin{cases} j\omega L_s + \frac{1}{j\omega C_s} + R & ; \text{series compensated secondary} \\ j\omega L_s + \frac{1}{j\omega C_s + \frac{1}{R}} & ; \text{parallel compensated secondary} \end{cases} \quad (2.1.6)$$

By having the input voltage and current in phase, a zero phase angle (ZPA) condition can be achieved. At ZPA frequency, the load reactance seen by the source is zero. The ZPA condition is desirable in order to have a minimum voltage-ampere (VA) rating of a WPT system.

Mutual inductance (M) is a quantitative description that describes the coupling of two conductor loops in the medium of magnetic field while coupling coefficient (k) is a qualitative description of the conductor loops regardless of the geometric dimension and it can be expressed in Eq. (2.1.7) [32].

$$k = \frac{M}{\sqrt{L_1 L_2}} \quad (2.1.7)$$

The value k always lies between two extreme values, $0 \leq k \leq 1$,

- (i) $k=0$; full decoupling due to magnetic shielding.
- (ii) $k=1$; full coupling where both coils are exposed to the same magnetic flux.

For example, the transformer is a technical application of full coupling. By taking into consideration of the distance between two conductor loops (x), k can be expressed as in Eq. (2.1.8), where r_p is the transmitter coil radius and r_s is the receiver coil radius [32].

$$k(x) \approx \frac{r_s^2 r_p^2}{\sqrt{r_s r_p}} \cdot \frac{1}{(\sqrt{x^2 + r_p^2})^3} \quad (2.1.8)$$

Fig. 2.3 Graph of k versus distance for different sizes of transmitter coil [32].

Fig. 2.3 shows the coupling coefficient for different transmitter coil sizes, in which $r_1 = 10$ cm, $r_2 = 7.5$ cm and $r_3 = 1$ cm while the receiver coil radius is 2 cm.

2.2 Rectifier Designs

In an inductively coupled WPT system (shown in Fig. 2.4), the wireless power receiver consists of a rectifier for AC-DC conversion and a voltage regulator in the form of LDO or switching regulator for DC-DC regulator. Hence, the efficiency of the rectifier and the regulator are crucial specifications of the design in order to ensure that the heat dissipation of the devices is minimized. This section reviews several rectifier designs, aiming to enhance the power efficiency.

Fig. 2.4 Inductively coupled WPT system.

The turn-on voltage drop of the conventional diodes is around $0.6V \sim 0.7V$. As a result, it causes a huge degradation in the power efficiency of the rectifier circuits. Even though low voltage Schottky diodes are used in [35] for RFID tags, they require special process at additional cost. Some designs utilize native transistors to replace the Schottky diodes but severe reverse leakage current happens. Moreover, they are not available in some CMOS process [36]. Therefore, rectifier designs using standard CMOS transistors have been implemented to maximize the power efficiency. Some of the works have utilized the voltage doubler structure while some works have adopted full-wave rectifier structure.

Fig 2.5 shows the diode-connected NMOS rectifier in [37]. It utilizes the voltage doubler structure in which the output voltage is twice of the input amplitude.

Fig. 2.5 Conventional diode-connected NMOS rectifier [37].

During negative cycle, transistor M_2 is turned on and capacitor C_1 is charged with a voltage of $(V_{RF} - V_{th})$. During positive cycle, M_1 is turned on and the output capacitor C_2 is charged by the input source as well as the charge stored in the capacitor C_1 . Thus, the rectified voltage is $2(V_{RF} - V_{th})$. Instead of the two diodes forward voltage drop, the voltage drop has become two threshold voltages. The maximum rectified voltage can be obtained if the V_{th} value is minimized. In order to minimize the voltage drops, two extra voltage sources are introduced to cancel the transistor's threshold voltage drop, as illustrated in Fig 2.6.

During each cycles, either transistor M_1 or M_2 is turned on. With the external voltage sources V_{bth} , the capacitor C_1 is charged to a voltage of $V_{RF} - (V_{th} - V_{bth})$. The rectified voltage V_R has now become $2(V_{RF} - V_{th} + V_{bth})$. If V_{bth} is made to be the same value as V_{th} , we can get V_R to be approximately equal to $2V_{RF}$ [13]. Instead of using an external battery to supply the bias voltage, the bias voltage can be generated internally using the rectified DC voltage as in [38].

Fig. 2.6 Rectifier circuit with external V_{th} cancellation [37].

Fig. 2.7 Voltage doubler structure with internal V_{th} cancellation technique [38].

Fig. 2.7 shows the rectifier design using the internal threshold voltage cancellation technique [38]. The capacitor C_{bp} holds the bias voltage which is the threshold voltage of M_{p1} while the capacitor C_{bn} holds the threshold voltage value of M_{n2} . The CMOS diodes, M_{p1} and M_{n2} replicate their threshold voltage with M_{pb} and M_{nb} respectively. This internal threshold cancellation technique can track the process and temperature variations in these CMOS diodes accurately by matching M_{pb} with M_{p1} and M_{nb} with M_{n2} . The ferroelectric

capacitor is utilized in this design as it has large permittivity and it is able to reduce the area and the input parasitic capacitor C_{pr} in the Fig. 2.7 shown [38].

With the internal and external threshold voltage cancellation techniques shown above, the effective threshold voltage of the CMOS diode can be made to be close to zero. Even though both of the techniques [37] and [38] have managed to reduce the large voltage drop, both of the designs also suffered from severe reverse leakage current when the CMOS diode is reversed-biased and this will degrade the power conversion efficiency as well.

Fig. 2.8 Self- V_{th} cancellation in CMOS rectifier [39].

Another technique is the self-threshold voltage (V_{th}) cancellation technique, as shown in Fig. 2.8. It is the same as the conventional voltage doubler structure discussed in the previous section except that the gate terminals of the CMOS diodes are connected to the ground and the rectified output DC voltage respectively. This design is simpler compared to the design in [37] and [38]. No additional power is consumed by the cancellation circuits such as in [37] and [38]. The threshold voltage of the CMOS diode is effectively reduced by the same amount to the output DC voltage [39]. Effective threshold voltage of the CMOS diode is equal to zero if the output DC voltage is approximately equal to the threshold voltage of the transistor. Therefore, a maximum efficiency is achieved only when the DC output voltage is around the threshold voltage value of the transistors. However, further increasing the output DC voltage to be more than

the transistors' threshold voltage value will cause both the NMOS and PMOS diodes to turn on at the same time. This causes a large reverse leakage current to flow and it will lead to a large degradation in the power conversion efficiency of the rectifier.

The designs in [37-39] are simple and they are suitable for applications operating in the UHF range as the complexity of the circuit design is limited at such a high frequency range. For applications in the frequency range from kHz to MHz, the active diodes are often used to replace the diodes in the rectifier designs to improve the power efficiency.

Fig. 2.9 Active rectifier with offset-controlled comparators and its output voltage and input current waveforms [40].

Fig. 2.9 shows the implementation of the active diode technique in [40]. As illustrated in Fig. 2.9, the PMOS switches are controlled by the comparators and the bottom diodes are replaced by cross-coupled NMOS switches. When the input voltage is higher than the V_{REC} voltage, either P_1 or P_2 is turned on. In contrary, the PMOS switches are turned off when the input voltage falls below V_{REC} . However, due to the delay of the comparator as well as the gate drivers, the PMOS switches are turned off after a certain delay. As a result, the reverse or back current flows in the rectifier, as shown in the waveforms of Fig. 2.9, would degrade the power efficiency. Hence, a high speed comparator as shown in Fig.

2.10 is proposed to resolve the issue. Several works in [40-45] and [116- 129] propose different comparator designs to speed up the turn-off response in order to overcome the reverse current problem.

As shown in Fig. 2.10, the comparator consists of two offset-control functions (Offset_R and Offset_F). When the input V_{IN1} is greater than V_{REC} , node V_A is pulled high and V_{OUT} will go ‘low’ to turn on the PMOS switch. The offset block, Offset_F helps to speed up the turn-on transition to maximize the conduction time. When V_{REC} is higher than V_{IN1} , node V_A is pulled down and V_{OUT} will go ‘high’ to turn-off the PMOS switch. The offset block, Offset_R aids to speed up the turning-off of the PMOS switch to prevent the reverse current from flowing. However, by having offsets for both turning on and off transition, the comparator may fall into an unstable state and lead to self-oscillation. To make it work, a delay cell is added in the offset control path and off-chip control signals are required to programme the offset current in response to the process variations.

Fig. 2.10 The high speed comparator with two offsets control in [40].

The four-input cross-coupled latched comparator is proposed in [41] to enhance the efficiency of the rectifier for biomedical implantations, as shown in Fig. 2.11. The proposed comparator consists of a main comparator and a speed-up comparator. The four inputs to the common-gate main comparator are RF+,

RF-, DC_{out} and GND. The unbalanced sizing is used to enhance the pull-up response of the comparator to minimize the reverse conduction time. When RF+ is higher than DC_{out}, M_{N2} is turned-on and output OUT_{PM} is being pulled ‘low’. The signal is coupled to C_{C3} and C_{C4} and hence it turns on M_{P5} in the speed-up comparator and pulls node X ‘high’ to enhance the turning-on of M_{N2} through the coupling of C_{C2} and C_{C1}. This helps to accelerate the turning-on of the PMOS switch in the rectifier. A similar effect happens when DC_{out} is greater than RF+, output OUT_{PM} is pulled ‘high’ and the signal couples to C_{C3} and C_{C4}, turning on M_{N4} in the speed-up comparator which pulls node X ‘low’ to enhance the turning-on of M_{P2}. As a result, the turning-off of PMOS switch is speed up to minimize the reverse current conduction time.

Fig. 2.11 The four-input cross-coupled latched comparator in [41].

The work in [42] has proposed a two-stage rectifier as shown in Fig. 2.12. The two-stage rectifier consists of a negative voltage converter block and a comparator controlled switch. The negative voltage converter is made up of four switches implemented by four power transistors. During positive cycle, transistors, MP1 and MN2 will be turned on. During negative cycle, transistors MP2 and MN1 will be turned on. The second stage of the rectifier can be implemented with an active diode. The comparator will compare the output

voltage of the negative voltage converter, V_{NVC} with the rectified voltage to turn on or turn off the PMOS switch, MPS. The size of the transistors in the negative voltage converter can be designed to be large so as to reduce the voltage drop of the CMOS switches. Even though only one permanent current consumption comparator is utilized in the design, it has five switches in the structure compared to the full-wave rectifier structure which has only four power switches. The trade-offs of the design are the dynamic power losses of the negative voltage converter, area consumption as well as the input voltage drop consideration. For low load current applications, the power consumed by the comparator may be larger than the power consumption of the negative voltage converter. Thus, this structure is advantageous for low load current applications.

The comparison between the full-wave rectifier and the two-stage rectifier is shown in Table 2.1.

Fig. 2.12 The two-stage rectifier in [42].

Table 2.1 Comparison between two structures.

Features	Two-stage rectifier	Full-wave rectifier
No. of power transistors	5	4
Comparator count	1	2
Voltage drop	$3 V_{ds}$	$2 V_{ds}$

2.3 DC-DC converter

After the rectification stage, a voltage regulator is required to regulate the output voltage to cater for different load requirements. A low-dropout regulator (LDO) can be used to regulate the output voltage but a large voltage drop across the power transistor would degrade the efficiency. Switching regulator can provide higher power efficiency but an off-chip inductor is required.

Fig. 2.13 Voltage regulator block in an inductively powered WPT system.

Basically, switching regulators can be categorized into three main topologies, which are the buck, boost and buck-boost converters. The buck converter is as shown in the Fig. 2.14. It will implement the step-down voltage conversion in which we can get an output voltage that is lower than the input voltage.

Fig. 2.14 Buck Converter.

According to Fig. 2.14, each time only one switch is turned on. When S_1 is turned on, the energy is transferred to the inductor, L . When S_2 is turned on, S_1 will be turned off, the previous charge stored in the inductor will now be delivered to the load, R . Due to the volt-second balance, the charge that is stored in the inductor is equal to the charge that it releases to the load. Thus, at steady-state, the equation can be derived as below:

$$D(V_{IN} - V_{OUT}) + (1-D) \cdot (-V_{OUT}) = 0$$

$$\therefore V_{OUT} = DV_{IN}$$

where $D = T_{ON}/T$, D is the duty ratio, T_{ON} is the period when the switch S_1 is turned on and T is the switching frequency of the converter.

Fig. 2.15 Boost Converter.

Fig. 2.15 shows the boost converter. It is able to realize a step-up conversion voltage. The output voltage will be higher than the input voltage. When S_1 is

turned on and S_2 is off, the inductor builds up its energy. When S_2 is turned on and S_1 is turned off, the inductor releases its energy to the load and the output capacitor. Similarly, at steady-state, the equation is derived as below with D is the duty ratio:

$$DV_{IN} + (1-D) \cdot (V_{IN} - V_{OUT}) = 0$$

$$\therefore V_{OUT} = [1/(1-D)]V_{IN}$$

Fig. 2.16 Non-inverting buck-boost converter.

Fig. 2.16 shows a buck-boost converter. It provides a positive output voltage that is either higher or lower than the input voltage. Similarly, the average output voltage can be derived as shown below:

$$V_{OUT} = [D / (1-D)] V_{IN}$$

2.3.1 Modeling and Stability

In the switched mode DC-DC converter design, the AC equivalent circuit model is required to analyze the stability of the system as the feedback is often employed in the system. For example, a voltage-mode DC-DC converter with pulse-width modulation (PWM) controller can be modeled as shown in Fig. 2.17 [46].

A few approaches, such as state-space averaging approach [47] and averaged switch modeling approach have been used to model the closed-loop converter

system. The detailed derivation of the closed-loop transfer function with state-space averaging approach is shown in the Appendix A.

Fig. 2.17 Small-signal model of a voltage mode DC-DC converter [46].

Fig. 2.18 Buck converter with parasitic ESR and DCR.

The transfer function of an uncompensated buck converter as shown in Fig. 2.18 can be derived as below:

$$G(s) = \frac{V_o}{V_i} = \frac{(1 + ESR \cdot C)s}{1 + (ESR \cdot DCR)Cs + LCs^2} \quad (2.3.1)$$

The ESR and DCR are the parasitic resistances of the inductor and the output capacitor respectively. The transfer function of the power stage consists of double poles due to the low pass filter of LC and a zero caused by the ESR. If there is variation in the input or loads, the converter may be unstable. In order to make the converter unconditionally stable, a compensator is usually added to improve the phase margin by introducing zero in the system's transfer function.

Generally, there are 3 types of compensators employed, namely Type I, Type II and Type III. Fig. 2.19 shows the Type I compensator. The transfer function of the Type I compensator can be derived as in Eq. (2.3.2).

$$\frac{V_E}{V_{OUT}} = -\frac{1}{R_1 C_1 s} \quad (2.3.2)$$

Fig. 2.19 Type I compensation network.

It is a single pole compensation which is not very practical due to its limited bandwidth and low phase margin. Usually Type II and Type III are preferred choices for improving the phase margin and bandwidth of the system.

Type II compensator is shown in Fig. 2.20. It is useful when the ESR of the output capacitor is high. If the phase boost at the unity gain bandwidth can be provided by the zero generated by the ESR, then a type II compensator is adequate. Otherwise, Type III compensator is required to add additional zero. The transfer function of the Type II compensator can be derived as in Eq. (2.3.3).

$$\frac{V_E}{V_{OUT}} = -\frac{1}{R_1 C_1 s} \cdot \left(\frac{s + \frac{1}{R_2 C_2}}{s + \frac{C_1 + C_2}{R_2 C_1 C_2}} \right) \quad (2.3.3)$$

The transfer function consist of two poles and one zero. The capacitor C_2 is usually designed to be larger than C_1 so that the zero is generated at a lower frequency than the pole.

Fig. 2.20 Type II compensation network.

Fig. 2.21 Type III compensation network

Type III compensator is shown in Fig. 2.21. It is a general solution for any

types of capacitor with a wide range of ESR values. The transfer function can be derived as shown in Eq. (2.3.4). It consists of two zeroes and three poles. The basic idea of having compensators in a buck converter is to compensate the poles generated by the LC filter by having a phase boost. It is to ensure that the magnitude of the slope at the unity gain frequency is less than or equal to -20dB/dec for a stable system. However, the limiting factor of a compensator is that the compensation gain has to be less than the error amplifier open loop gain.

$$\frac{V_E}{V_{OUT}} = -\frac{R_1 + R_3}{R_1 R_3 C_1 s} \cdot \frac{\left(s + \frac{1}{R_2 C_2}\right) \left(s + \frac{1}{C_3 (R_1 + R_3)}\right)}{\left(s + \frac{C_1 + C_2}{R_2 C_1 C_2}\right) \left(s + \frac{1}{R_3 C_3}\right)} \quad (2.3.4)$$

The transfer function of the buck converter consists of two low-frequency poles while the boost and buck-boost converter constitute a right half-plane zero. The converter can work in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM). The transfer functions of buck, boost and buck-boost converters operating in DCM consist of only a single-pole as the second pole of the buck converter and the right half-plane zero of the boost and buck-boost are at high frequencies and they are negligible in DCM [46]. Hence, the converters operating in DCM is inherently stable and easier to control.

2.3.2 Control Methodologies

There are several modulation techniques that used to be employed in a converter, such as Pulse Width Modulation (PWM) [65-70], Pulse Frequency Modulation (PFM) [71-75] and Pulse Skipping Modulation (PSM) [76-85]. PWM is a modulation technique that varies the duty ratio at a fixed switching frequency. The efficiency of this modulation technique is good at the heavy loads rather than at the light loads.

PFM is another technique that varies the frequency according to the load conditions while keeping the duty ratio (on/off time) at constant. It is usually used to improve the efficiency at the light loads. But the switching frequency of PFM control is unpredictable and thus it results in Electro-Magnetic Interference (EMI) problems. In addition, the unpredictable frequency complicates the input filter design. Hence, PSM modulation technique is introduced to overcome the EMI problems. It operates at a fixed frequency but it will skip the pulses according to the load conditions to save power. A few modulation techniques can be implemented together to improve the efficiency for a wider load range.

Apart from the above, there is another control technique, which is the hysteretic control [86-94] and it is also known as the non-linear bang-bang control. This control technique is gaining its popularity nowadays due to its simpler design as compared to the PWM modulation technique. Each of the modulation technique will be discussed in detail in Sections A, B, C and D respectively.

A. Pulse Width Modulation (PWM)

PWM controlled DC-DC converter regulates the output voltage by changing the duty ratio at a fixed switching frequency. It can work in either voltage-mode or current-mode control. Fig. 2.22 shows that the DC-DC converter is controlled by a voltage-mode PWM. Type III compensator is commonly utilized to ensure the stability of the converter. The ramp voltage is synchronized with the clock. A fraction of the output voltage is feedback to the error amplifier. The error between the output voltage and the reference voltage is amplified and compared to a ramp voltage to generate the comparator output signal. A duty cycle can be initiated by the comparator signal and terminated by the clock signal or vice-versa.

The PWM can operate in current-mode as well. Fig. 2.23 shows the peak current-mode PWM controlled buck converter. The inductor current is programmed by the error amplifier output. In peak current-mode control, the clock signal initiates the duty cycle and the comparator signal terminates it.

Besides the peak current-mode control, there are also valley current-mode and average current-mode control, which can be found in [49].

Fig. 2.22 Voltage-mode PWM controlled buck converter in (a) and its waveform in (b) [48].

Fig. 2.23 Current-mode PWM controlled buck converter in (a) and its waveform in (b).

B. Pulse Frequency Modulation (PFM)

PFM controlled DC-DC converter regulates the output voltage by changing the frequency according to the load conditions. There are several methods, such as fixed on-time PFM control, fixed off-time PFM control, single-pulse PFM, multi-pulse PFM, etc. PFM controller is usually used to improve the light load efficiency and thus most of them operate in discontinuous conduction mode (DCM). Hence, a zero current detector is commonly utilized to sense the moment when the inductor current falls to zero.

Fig. 2.24 Fixed on-time PFM controlled buck DC-DC converter [48].

Fig. 2.24 shows a fixed on-time PFM controlled DC-DC converter working in the discontinuous conduction mode (DCM) [50]. The output voltage, V_{OUT} is compared to a reference voltage, V_{REF} . If V_{OUT} falls below V_{REF} , the on-time is initiated. The charging switch is turned on for a fixed on-time then after a dead time, the discharging switch will be turned on to deliver the power to the load. The zero-current detector is used to sense the time when the inductor current falls to zero then the discharging switch will be turned off.

Fig. 2.25 shows the inductor waveform of the single-pulse and multi-pulse operations of PFM in [51]. When the average load current demand is more than the current that can be provided by the single-pulse operation, the converter will shift into multi-pulse operation, in which the inductor current ramps to higher

peak inductor current in the successive cycles and after two to three cycles then only the inductor current starts to ramp down. The limitation of this control method is that it has poor efficiency during heavy loads and the unpredictable switching frequency will cause EMI problems.

Fig. 2.25 Single-pulse and multi-pulse of PFM operation [51].

C. Pulse Skipping Modulation (PSM)

PSM modulation technique will skip the pulse when the load current decreases [52]. As shown in Fig. 2.26, the duty ratio and the switching frequency are fixed by the clock signal. When the output voltage falls below the reference voltage, the duty cycle will be activated. In contrast, when the output voltage rises above the reference voltage, the clock pulses will be skipped to save power. This modulation technique has better efficiency during light to medium load.

Fig. 2.26 PSM controlled buck converter in (a) and its waveform in (b).

D. Hysteretic Control

Fig. 2.27 shows the voltage mode hysteretic control which is also known as bang-bang control [53]. The hysteresis comparator is used to compare a portion of the output voltage. There are two reference voltages, which are V_{HB} and V_{LB} . If the output voltage is lower than the reference voltage V_{LB} , then the charging switch is turned on to charge up the output voltage. When the output voltage rises above the reference voltage V_{HB} , then the discharging switch is turned on. The process repeats when the output voltage falls below V_{LB} again. Hysteretic controlled converter is simpler compared to the PWM control. Moreover, it has been proven to be inherently stable under every condition in [54].

Fig. 2.27 Voltage-mode hysteretic controlled buck converter [53].

2.4 SIMO Converter

Single inductor multiple output (SIMO) DC-DC converter is used to provide for more than one output voltage in a system. There are three configurations for the SIMO converter, such as buck topology in Fig. 2.28, boost topology in Fig. 2.29 and buck-boost topology in Fig. 2.30. Due to the multiple-output configurations, each of the output switches can only conduct for a fraction of the time in order to prevent the short-circuiting of outputs from happening.

The SIMO buck configuration is shown in the Fig. 2.28. During charging phase, the switch S_{E1} and one of the output switches are turned on to energize the inductor. During discharging phase, the switch S_D and one of the output switches will be turned on to deliver the stored power to the load. At steady-state, the

average voltage across the inductor L_O is zero and thus the average terminal voltages are equal and can be expressed as below [55]:

$$V_{SW(avg)} = D_{IN} V_{IN} = \sum_{k=1}^N D_{O(k)} V_{O(k)}$$

where D_{IN} is the input duty cycle, $D_{O(k)}$ is the output duty cycle for the output $V_{O(k)}$ and k can be from 1 to N .

This configuration allows some of the outputs but not all to exceed V_{IN} if the corresponding duty cycle is short enough. But at least one of the outputs needs to fall below V_{IN} in order to cause the inductor current to increase and energize the inductor L_O [55].

Fig. 2.28 SIMO in buck configuration [55].

Fig. 2.29 SIMO in boost configuration [55].

Fig. 2.29 shows the SIMO converter in boost configuration. During energizing cycle, the switch S_{E1} will be turned on to charge up the inductor L_O . During de-

energizing cycle, S_{E1} will be turned off and one of the output switches will be turned on to charge up the corresponding output. In steady-state, the inductor's average voltages are zero; therefore the equation can be expressed as [55]:

$$V_{SW(avg)} = \sum_{k=1}^N D_{O(k)} V_{O(k)} = V_{IN}$$

where $D_{O(k)}$ is the output duty cycle for the output $V_{O(k)}$ and k can be from 1 to N. Similar to the buck case, one of the outputs (but not all) of the converter can fall below V_{IN} . However, at least one of the outputs must be higher than the V_{IN} in order to induce the inductor current to decrease to de-energize the L_O .

Fig. 2.30 SIMO in buck-boost configuration [55].

The equation for the SIMO non-inverting buck-boost configuration can be derived as below [55]:

$$V_{SW1(avg)} = V_{SW0(avg)}$$

$$\therefore D_{IN} V_{IN} = \sum_{k=1}^N D_{O(k)} V_{O(k)}$$

where D_{IN} is the input duty cycle, $D_{O(k)}$ is the output duty cycle for the output $V_{O(k)}$ and k can be from 1 to N. For this configuration, the inductor current can always rise or fall irrespective of how the V_{IN} and $V_{O(k)}$ are related. The outputs can exceed or less than V_{IN} . The inductor current will rise with V_{IN} independently of $V_{O(k)}$ and it will fall with $V_{O(k)}$ independently of V_{IN} .

2.4.1 Control Methodologies

For multiple outputs converter, the inductor current is required to be shared among the various loads. The multi-feedback loop that regulates the output voltage has problems of stability and causes ringing at the outputs. The main problem faced in the multiple outputs converter is the cross regulation problem. Cross regulation means that any load change at one output will cause the instability of voltage at another output due to insufficient or excess charge [56-60], which is shown in Fig. 2.31.

Fig. 2.31 Cross regulation that happened in SIMO converter [56].

As can be seen from Fig. 2.31, the overshoot or undershoot of the output V_{o1} causes the voltage V_{o2} to change as well. The cross regulation problem leads to the degradation of the system performance and affect the regulator stability as well.

To mitigate the problem, the error of the energy transfer needs to be minimized. The control methods that are commonly used in a multiple-output converter are the Time-Multiplexing (TM) control and the Ordered Power Distributive Control (OPDC).

A. Time-Multiplexing (TM) control

For time-multiplexing control, each output receives all the energy stored in the inductor [61-62].

Fig. 2.32 SIDO boost converter with TM control [56].

As shown in Fig. 2.32, the switching period T_s is divided into two phases, which are the phase 1 and phase 2. During phase 1, the inductor L is energized and the energy is delivered to the output V_{oa} . During phase 2, the inductor L is charged and the energy is transferred to the second output V_{ob} . A freewheeling switch S_f is usually added in parallel to the inductor to suppress the ringing that happened during the discontinuous conduction mode (DCM). When the switches, S_a , S_b and S_n are turned off, the inductor L and the parasitic capacitance at node V_x will form a resonant circuit which leads to severe ringing as shown in Fig. 2.33. Thus, a free-wheeling switch is required to suppress the ringing.

Fig. 2.33 The free-wheeling switch S_f is added to suppress the ringing [56].

The problem of TM control is that it has limited driving capability even though it has a good isolation between the two outputs. If one of the load currents is higher than the limited driving capability, the cross regulation will occur. Hence, a Pseudo-Continuous Conduction Mode (PCCM) control has been proposed in

[63] to improve the driving capability of each output. As shown in Fig. 2.34, the free-wheeling switch S_f is turned on when the inductor current I_L drops to a fixed I_{dc} level instead of at the zero level. But a large S_f is needed to implement the switch and this will lead to switching loss as well. Thus, it is not a very effective way to compensate the trade-off between the power losses and the driving capability limitation.

Fig. 2.34 PCCM control to increase the driving capability of outputs [56].

B. Ordered Power Distributive Control (OPDC)

Fig. 2.35 OPDC control in a SIDO converter [56].

Ordered power distributive control is also known as single energizing method. For a dual-output converter, both of the output voltages share the same energy in the inductor [58],[64]. The inductor is only charged once and the energy is transferred to the output one by one within one period. The inductor current waveform is as shown in the Fig. 2.35. It can operate in either DCM or PCCM.

But this method is vulnerable to the cross regulation problem as well. When the previous load draws more energy from the inductor, it will cause the subsequent output to suffer the effects of reduced energy in the inductor and thus cross regulation occurs.

C. Comparison between TM and OPDC control

Fig. 2.36 Inductor current waveform for TM and OPDC control of a SIDO boost converter [56].

Within one period, OPDC control has less switching activity compared to the TM control. Thus, its switching losses are lower than the TM control. However, it has larger conduction losses due to higher peak inductor current. Compared to the TM control, OPDC control has a higher driving capability and smaller output voltage ripples besides faster control loops. As for OPDC control, it receives less energy per cycle but more frequent. Therefore, there is less time for each of the output to droop and hence output voltage ripples can be smaller [55]. Both of the control methods are also sensitive to the load transient step which could lead to cross regulation eventually. Therefore, an in-depth research has to be done to find out a better way to balance the cross regulation and the driving capability.

2.5 Power losses and efficiency

The power efficiency of a DC-DC converter is defined as the ratio of the output power to the input power. The output power is the load power and the input power drawn from the power supply includes the load power and the total power losses of the converter. The power efficiency can be expressed as:

$$\eta = \frac{P_{LOAD}}{P_{LOAD} + P_{LOSSES}} \quad (2.5.1)$$

In order to maximize the power efficiency of a converter, the power losses should be minimized as much as possible. At a system level, the power losses of a switching regulator can be categorized into two main groups, which are the static power losses and the dynamic power losses [130-132].

<i>Load-Dependent (Conduction) Losses</i>
MOSFET on resistance
Diode forward voltage drop
Inductor winding resistance
Capacitor equivalent series resistance
<i>Frequency-Dependent (Switching) Losses</i>
MOSFET output capacitance
MOSFET gate capacitance
Diode capacitance
Diode stored minority charge
Inductor and transformer core loss
Snubber loss
Gate driver losses
<i>Other Fixed Losses</i>
Controller standby current
MOSFET, diode, and capacitor leakage currents

Fig. 2.37 Origin power losses of a fixed-frequency converter [130].

Fig. 2.37 shows the power losses in a typical fixed-frequency converter. The static power losses are the fixed-frequency losses which include the quiescent power of the analog blocks such as bandgap reference voltage, clock generator, operational amplifier, etc. The dynamic power losses are line and load dependent, such as conduction power losses and switching power losses. Conduction power

losses are dependent on the loads and they are caused by the voltage drop across power transistors and the equivalent series resistance (ESR) of the inductor and the capacitor. Larger load current will lead to higher conduction loss. Switching power losses are dependent on the switching frequency. They are the losses caused by turning on and off of the transistors, gate drive losses, body diode conduction losses, etc. Fig. 2.38 shows the comparison of power losses versus load current between a fixed-frequency and a variable frequency converter. The fixed-frequency converter consumes a significant amount of fixed power losses and switching power losses. The switching power loss is a fixed loss for a constant frequency converter. However, if the switching frequency can be varied accordingly to the load current, then the switching loss is varied with the loads as well. Hence, it is desirable to reduce the switching frequency during light-loads in order to minimize the switching power losses and improve the converter efficiency.

Fig. 2.38 Power losses versus load current: (a) fixed-frequency converter, (b) varying frequency converter [130].

For a high efficiency converter, the power losses need to be reduced as much as possible. By increasing the size of the power transistor (i.e. increasing the width but the length is fixed at minimum), the on-resistance of the power transistor is reduced and hence the conduction power losses is reduced as well.

However, a larger power transistor size consumes a larger silicon area and increases the gate driving losses which contributes to higher switching power losses. Hence, different layout techniques are discussed in [133-135] for the power transistor design. Table 2.2 summarizes the methods that help to minimize different types of power losses.

Table 2.2 Methods on minimizing the power losses of converter.

Static Power Losses	<ul style="list-style-type: none"> • To reduce switching power losses, one common approach is to shut down the internal circuitry blocks that are not in-used during sleep-mode or light-load condition [136].
Dynamic Power Losses	<ul style="list-style-type: none"> • To reduce the switching power losses, pulse frequency modulation control can be utilized to reduce the switching frequency at light loads [136]. • To minimize the body diode conduction loss, a dead time controller is used to avoid the shoot-through current and the body diode conduction of the power switches [137-146]. • To reduce the gate driving loss, a dynamic width control by segmentation technique can be used to divide the power transistor into many segments [147-151]. The segments are turned on according to the load requirements.

2.6 Advanced Power Control or Regulation Methods

Instead of having a two-stage receiver design [95-101], some advanced power control or regulation techniques have been proposed in [102-115]. The proposed advanced methods regulate the output voltage with either the transmitter or the receiver control.

Fig. 2.39 Wireless power transceiver in [102].

The output voltage regulation can be achieved by controlling the transmitter power as in [102-103]. Fig. 2.39 shows the wireless power transceiver proposed in [102]. The output voltage of the receiver is feedback to the transmitter in order to adjust the transmitter power for different load requirements. The resonant frequency of the system is tuned to in order to adjust the transmitter power for different loads. However, this would slow down the transient response of the receiver as the feedback has to go through the transmitter to adjust the power transferred in response to a load change in the receiver.

An adaptive reconfigurable active voltage doubler/rectifier is presented in [104] to extend the inductive power transmission range. The voltage doubler and rectifier are integrated into a single structure as shown in Fig. 2.40. In order to accommodate a wider range of coil arrangements, the topology can work in either rectifier or voltage doubler mode, depending on the input voltage. The input voltage level is determined by comparing the output voltage with a reference

voltage. The power transmission range has been improved by 33% in relative to the coil distance and 41.5% in relative to the coil orientation. The peak efficiency for rectifier and voltage doubler modes are 77% and 70% respectively at an output voltage of 3.1 V.

Fig. 2.40 The reconfigurable voltage doubler/rectifier topology in [104].

The work in [105] presents a resonant regulating rectifier (3R) for wireless charger. The circuit for 3R rectifier design is shown in Fig. 2.41. It has adopted a one-step concept which utilizes no inductor. But the design consists of five off-chip diodes and three off-chip capacitors which increase the footprint of the receiver. The node V_{XH} is controlled up and down in every eight resonant cycles. The resonant current is built up slowly when the node V_{XH} is low whereas the resonant current is decreased when the node V_{XH} is high. The load change

information is fed back to the transmitter in order to tune the V_{DRN} which is controlled by a MCU using 3-bit duty signals. Zero current switching is utilized to ensure that the on/off switching time synchronizes with the zero crossing time of the resonant current to avoid power losses. The design achieves a peak efficiency of 86.00 % at an output power of around 3.4 W.

Fig. 2.41 The circuit of 3R rectifier design in [105].

The reconfigurable resonant regulating (R^3) rectifier is proposed in [106] to extend the coupling and loading range for biomedical implants. The primary-assisted regulation principle is introduced in the work and Fig. 2.42 shows the proposed design. The highlight of the work is the tri-loop control: 1) A local PWM loop at the receiver to regulate the output voltage between 1X mode and 2X mode. 2) A global loop to adjust the transmission power externally to ensure that the output voltage is in the $[V_{1X}, V_{2X}]$ window. 3) A PWM control loop at

the transmitter to regulate the V_{eq} to V_{REF1} in order to widen the $[V_{1X}, V_{2X}]$ window to improve the coupling and loading range of the system. The maximum output power and the peak efficiency of the receiver are 234 mW and 92.50% respectively.

Fig. 2.42 The tri-mode control of R^3 rectifier in [106].

The rectifying regulator in [107] operates with pulse-width modulation (PWM) and pulse frequency modulation (PFM) controls. The architecture is shown in Fig. 2.43. The PWM mode is used to meet the transient requirement while PFM mode is used to power the stimulator in sleep mode. The PFM mode is discontinuous,

that is a single shot pulse is generated only when the output voltage falls below the reference voltage. A low-dropout regulator is used to generate a 1 V supply rail from the 2.5 V output voltage to supply the control circuitry.

Fig. 2.43 Rectifying rectifier in [107].

The 3-mode reconfigurable resonant regulating (R^3) rectifier is presented in [108], as shown in Fig. 2.44. It is able to provide for higher power applications at 1 to 2A of output current. Depending on the load conditions, the reconfigurable rectifier can operate in 1X/1/2X/0X mode. The PWM control is used to regulate the output voltage across different loads. Besides, adaptive sizing method is employed to reduce the conduction power losses of the power switches. Table 2.3 shows the summary of the prior arts.

Fig. 2.44 The 3-mode R^3 rectifier structure in [108].

Table 2.3 A summary of the prior arts.

References	Structures	Features/ Pros and Cons
[40-45] & [116-129]	Active rectifier	<ul style="list-style-type: none"> - Circuit solutions are proposed to solve the reverse current issue to enhance the power efficiency. - However, they still require a second stage to regulate the rectified voltage.
[95-101]	Rectifier + LDO/Buck converter	<ul style="list-style-type: none"> - Two-stage design with LDO or buck converter to regulate the rectified voltage.
[102-103]	Rectifier with transmitter control	<ul style="list-style-type: none"> - By tuning the transmitter power, the output voltage of the rectifier is regulated across different loads without a second-stage regulator. - However, this may slow down the transient response of the receiver as the feedback has to go through the transmitter in response to a load change in the receiver.
[104]	Reconfigurable voltage doubler /rectifier	<ul style="list-style-type: none"> - The power transmission distance has been extended greatly with the reconfigurable topology. - Nonetheless, a voltage regulator is required in the second stage to regulate the output voltage.
[105]	3R rectifier	<ul style="list-style-type: none"> - The advantage of the design is no inductor is used. - However, it consists of 5 off-chip diodes and 3 off-chip capacitors which increase the footprint of the receiver. - The output voltage regulation is done manually with the help of the resonant tanks on both sides.
[106]	R ³ rectifier	<ul style="list-style-type: none"> - 3 control loops are utilized to extend the coupling and loading range of the design. - The output voltage regulation is done with the assistance of the transmitter control.
[108]	3-mode rectifier	<ul style="list-style-type: none"> - A single-stage regulation design which is suitable for higher power applications at 1-2A of output current.

Chapter 3 Design of Two-Stage Receiver

In this chapter, a two-stage receiver design will be presented. In Section 3.1, an active rectifier design with a prevention technique on reverse leakage current will be discussed. The second-stage which consists of a buck regulator with an energy-efficient controller will be discussed in Section 3.2. Lastly, the combination of the two-stage design and its performance will be presented in Section 3.3.

3.1 Active Rectifier

Fig. 3.1 Two-stage active rectifier.

The two-stage active rectifier structure as shown in Fig. 3.1 has been adopted in the design due to its simplicity. It utilizes two-stage design concept which consists of a first passive stage and a second active diode stage [42]. As compared

to the full-wave rectifier, only one comparator controlled switch is required. As a result, it could reduce the total power consumed by the control circuits. The first passive stage is a negative voltage converter as shown in Fig. 3.1. It converts the negative portion of the waveform into positive waveform. During positive cycle, the transistors MP1 and MN2 are turned on. Thus, the current flows from the input source V_{ac} to the node V_{nvc} through MP1 and MN2. During negative cycle, the current flows through the transistors MP2 and MN1. Dynamic bulk biasing (DBB) is used by tying the body of the active diode PMOS transistor to the highest potential as the two nodes of the active diodes, which are the node V_{nvc} and V_{rect} are changing all the time. With the dynamic bulk biasing, it can avoid latch up and to enhance the power transmission efficiency as well [152].

The second stage is an active diode stage. It consists of the proposed comparator controlled switch. The comparator will compare the node voltage V_{nvc} and the voltage V_{rect} to decide when to turn on or turn off the transistor MPS in Fig. 3.1. The voltage V_{nvc} consists of only positive waveform of the AC voltage after going through the negative voltage converter. When the voltage V_{nvc} is greater than V_{rect} , the comparator output will pull the gate of MPS 'low' to turn on the transistor and thus the current flows to charge up the output capacitor C_{out} . When the voltage V_{rect} is greater than the voltage V_{nvc} , the transistor MPS will be turned off to avoid any reverse leakage current from flowing back to the source. The delay due to the comparator circuit and the gate driver cause the reverse leakage current to flow for a short duration of time. For larger load current applications, the reverse leakage current may become a severe problem and it degrades the efficiency of the rectifier. Thus, a high speed comparator is required to solve this issue.

3.1.1 Proposed Comparator

An unbalanced biasing wide-swing cascode comparator is proposed to solve the reverse leakage current issue that occurred in the rectifier. Fig. 3.2 shows the proposed unbalanced biasing wide-swing biasing cascode comparator. The

design was fabricated in 0.18 μm standard CMOS process. The wide-swing cascode structure is adopted to increase the accuracy of the current mirror comparator. The comparator requires a minimum voltage of $(V_{th_n} + 4V_{dsat})$ to operate. The resistors RB1 and RB3 are used to provide the required biasing voltage while the resistor RB2 is used to provide the required biasing current. The comparator requires a minimum voltage of $(V_{th_n} + 4V_{dsat})$ to operate. The resistors RB1 and RB3 are used to provide the required biasing voltage while the resistor RB2 is used to provide the required biasing current.

Fig. 3.2 The proposed comparator [153].

Node A is biased at a voltage of $(V_{th_n} + 2V_{dsat})$ while node B is biased at a voltage of $VDD - (|V_{th_p}| + 2V_{dsat})$. The operation of the comparator can be explained by observing the input nodes V_{in+} and V_{in-} .

i) Current mirror (When $V_{in+} = V_{in-} = V_{DD}$)

When the input nodes, V_{in+} and V_{in-} are of the same voltage as the supply voltage V_{DD} , the biasing current I_{REF} can be expressed as:

$$I_{REF} = \frac{V_{DD} - (|V_{thp}| + 2V_{dsat})}{R_{B2}} \quad (3.1.1)$$

Since the gate of the transistors Mp1, Mp3 and Mp5 are connected together, they have the same V_{sg} and the current I_{REF} is mirrored to I_1 and I_2 through Mp3 and Mp5 respectively. The sizes of the transistors are designed to be the same, which is $[\left(\frac{W}{L}\right)_{Mp1} = \left(\frac{W}{L}\right)_{Mp3} = \left(\frac{W}{L}\right)_{Mp5}]$. The resistor R_{B1} is used to provide the biasing voltage at the node B to match the V_{ds} of the transistors in order to increase the accuracy of the current mirror. As the gate of the transistors Mn3 and Mn5 are connected together, they have the same V_{gs} , so the current I_2 is mirrored to the current $I_{pull-down}$. The transistors' size of Mn3 and Mn5 are designed to be the same. Since the gate of the transistors Mn1 and Mn7 are connected together, the current I_1 is mirrored to the current I_3 . Depending on the ratio of the transistors, their currents can be designed to be equal or non-equal. There are two cases as shown below:

➤ Case 1 : If $\left(\frac{W}{L}\right)_{Mn1} = \left(\frac{W}{L}\right)_{Mn7}$, then $I_1 = I_3$

➤ Case 2 : If $\left(\frac{W}{L}\right)_{Mn1} < \left(\frac{W}{L}\right)_{Mn7}$, then $I_1 < I_3$ as $I_3 = I_1 \times \frac{\left(\frac{W}{L}\right)_{Mn7}}{\left(\frac{W}{L}\right)_{Mn1}}$

As the gate of the transistors Mp7 and Mp9 are connected together, the current I_3 is mirrored to the current $I_{pull-up}$. The transistors' size of Mp7 and Mp9 are designed to be the same.

ii) Comparator (When $V_{in+} \neq V_{in-}$)

When the input nodes V_{in+} and V_{in-} are not the same, the currents $I_{pull-up}$ and $I_{pull-down}$ will change accordingly. When the node voltage V_{in-} is greater than V_{in+} , the current I_2 will increase and it will be mirrored to $I_{pull-down}$. At the same time, the node voltage C increases with the node voltage V_{in-} which limits the $I_{pull-up}$. Thus, the current $I_{pull-down}$ is greater than the current $I_{pull-up}$ so the output node $VCMP$ will be pulled low to turn on the PMOS active diode transistor. But when the node voltage V_{in+} is greater than V_{in-} , $I_{pull-up}$ will increase and at the same time, I_2 and $I_{pull-down}$ will decrease. Therefore, the current $I_{pull-up}$ is greater than the current $I_{pull-down}$ and the output node $VCMP$ will be pulled high to turn off the PMOS active diode transistor.

In our design, at the equilibrium state (when $V_{in+} = V_{in-} = VDD$), we design the current I_3 to be larger than the current I_1 (Case 2 shown above). The current I_2 is designed to be the same as the current I_1 . That means, at the equilibrium state, the current $I_{pull-up}$ is designed to be greater than the current $I_{pull-down}$. This is to further speed up the pull up of the output node $VCMP$ to suppress the reverse leakage current that happened in the rectifier. An additional offset voltage is inserted by having unbalanced biasing current between the transistors $Mn3$ and $Mp9$ with the current I_3 greater than the current I_2 . The appropriate offset voltage can be expressed as in Eq. (3.1.2).

$$\begin{aligned} V_{offset} &= V_{sg(Mp9)} - V_{gs(Mn3)} \\ &= \sqrt{\frac{2(I_3)}{\alpha}} - \sqrt{\frac{2(I_2)}{\beta}} \end{aligned} \quad (3.1.2)$$

$$\text{Where } \alpha = \mu_p C_{ox} \left(\frac{W}{L} \right)_{Mp9}, \quad \beta = \mu_n C_{ox} \left(\frac{W}{L} \right)_{Mn3}$$

Fig. 3.3 Simulated waveforms at 125 kHz with: (a) Conventional comparator and (b) Proposed comparator.

Fig. 3.3 (a) shows the reverse leakage current that happened when the conventional comparator is used due to the turn off delay of the comparator. Fig. 3.3 (b) shows that with the proposed unbalanced biasing wide-swing cascode comparator controlled switch, the reverse leakage current has been successfully suppressed. Both of the waveforms are simulated at the frequency of 125 kHz with input amplitude of 2.5 V. The VDD of the comparator as seen in Fig. 3.2 is supplied from the output voltage of the rectifier V_{rect} . The proposed comparator is supply dependent so that V_{offset} increases with V_{rect} . The increase in V_{offset} will speed up the transition time and therefore eliminate any reverse leakage current that may happen when the output voltage increases since the delay time of the comparator increases with the input amplitude.

3.1.2 Self-startup Ability

Fig. 3.4 Parasitic capacitances of the active diode MPS.

During start-up, the output voltage, $V_{rect} = 0$ and the gate voltage of the active diode power transistor MPS can be expressed as in the equation (3.1.3).

$$V_{drive} \approx \left(\frac{C_{gd}}{C_{gs} + C_{gd}} \right) V_{nvc} \quad (3.1.3)$$

Initially, the power transistor MPS is in cut-off region, thus the parasitic gate to source capacitance C_{gs} and the parasitic gate to drain capacitance C_{gd} of the transistor are almost of the same value and equal to the overlapping capacitances [43]. Thus, the voltage V_{drive} is approximately half of the value of V_{nvc} . When the difference between the gate voltages V_{drive} and the V_{nvc} is greater than the threshold value of the transistor MPS, the transistor MPS will conduct and slowly charge up the output capacitor. When the output voltage exceeds the minimum operating supply voltage of the comparator, the active diodes start to operate as described in Section 3.1.1. Fig. 3.5 shows the simulated waveform of the rectifier during the start-up.

Fig. 3.5 Simulated waveforms during start-up of the rectifier.

3.1.3 Measurement Results

Fig. 3.6 Chip micrograph of the proposed design.

Fig. 3.6 shows the chip micrograph of the rectifier with the proposed comparator. Common centroid and interdigitated layout techniques are applied to the proposed comparator layout design in order to improve the matching of the cascode current mirror transistors. Dummy transistors are also added to improve

the matching between the transistors so as to provide a similar environment to the circuits that are on the boundary of the layout. The measurement setup is shown in Fig. 3.7. A sense resistor is inserted in the input path for input current measurement. The average output voltage is measured by using a multimeter and the power can be obtained by squaring the average voltage divided by the load resistance. The power efficiency (PCE) is defined as the ratio of the output dc power to the input ac power which can be expressed in Eq. (3.1.4). The load current can be varied by using a variable resistor as a load. Each time the load current is varied by tuning the variable resistor. Alternatively, an electronic load can be used to replace the variable resistor. The detailed calculation of the input ac power is shown in Appendix B.

$$PCE(\%) = \frac{V_{rect}^2/R_L}{\frac{1}{nT} \int_{t_0}^{t_0+nT} V_{AC(t)} \cdot I_{AC(t)} dt} \times 100\% \quad (3.1.4)$$

Fig. 3.7 Test measurement setup for the rectifier chip.

Fig. 3.8 shows the measured steady-state waveforms of the input voltage, input current and output voltage at a load R_L of 40Ω with an output capacitor of $1 \mu\text{F}$. The testing frequency is at 125 kHz . The design is optimized at around 35 mA of load current which is at 40Ω of R_L . However, due to process variation, the peak efficiency has been shifted to around 40 mA of load current. The design has been tested at both $1 \mu\text{H}$ and $10 \mu\text{H}$ of output capacitors to examine the voltage ripples. Fig. 3.9 shows the input and output voltage waveform at a load

of $70\ \Omega$ with an output capacitor of $1\ \mu\text{F}$ in (a) and $10\ \mu\text{F}$ output capacitor is used in (b). The measured output voltage ripple is $141\ \text{mV}$ when $1\ \mu\text{F}$ output capacitor is utilized and the ripple voltage is reduced to $74\ \text{mV}$ when an output capacitor of $10\ \mu\text{F}$ is used.

Fig. 3.8 Measured steady-state waveforms at $40\ \Omega$ of load resistance.

Fig. 3.9 Measured waveforms at $70\ \Omega$ with output capacitor of (a) $1\ \mu\text{F}$ and (b) $10\ \mu\text{F}$.

Fig. 3.10 Measured PCE versus load current.

Fig. 3.11 Measured PCE versus varying output voltage Vrect at a load of 60 Ω .

Fig. 3.10 shows the measured PCE versus different load currents with an output capacitor of 10 μF . The measured peak power efficiency is 85.92% at 40 mA of load current. Fig. 3.11 shows the PCE versus varying output voltage Vrect at a load of 60 Ω . The work is designed for a maximum current of 60 mA by sizing the power transistors. Hence, when the output voltage is varied from 1.8 V to 3.4 V, it is important to ensure that the maximum load current is within the

limit and therefore $60\ \Omega$ is used for the test. For instance, with $60\ \Omega$ at maximum output voltage of 3.4 V, the load current is around 57 mA which is within the maximum current limit. The output voltage is used to supply the gate drivers. When the output voltage decreases, the power efficiency decreases as the on-resistance of the power transistors increases due to reduced gate overdrive. The fixed offset voltage is designed to optimize the efficiency around 2.2 V to 2.6 V. Hence, when output voltage is further increased, the efficiency decreases. The comparison with state-of-the-art work is shown in Table 3.1. The proposed work is compared with the reference works that have the nearest possible output power.

Table 3.1 Comparison table with state-of-the-art designs.

	[121] TBCAS 2008	[156] TBCAS 2013	[40] TCAS-I 2011	[117] TPEL 2011	Proposed work
Technology	0.5 μm CMOS	0.5 μm CMOS	0.5 μm CMOS	Discrete (TLV3702)	0.18 μm CMOS
Structure	Active Rectifier	Active Voltage doubler	Active Rectifier	Active Voltage doubler	Active Rectifier
Input Amplitude, $ V_{in} $	5 V	1.46 V	3.8 V	1.2 V	1.2 V- 2.5 V
Output Voltage	4.36 V	2.39 V	3.12 V	2.24 V	0.96 V-2.14 V
$P_{out\ (MAX)}$	19 mW	38 mW	20 mW	49 mW	120 mW
Frequency	125 kHz- 1 MHz	13.56 MHz	13.56 MHz	20 Hz	125 kHz
Active Area (mm^2)	0.400	0.144	0.180	N/A	0.437
Measured PCE (%)	84.80 @ 19 mW	68.00 @ 38 mW	80.20 @ 20 mW	83.00 @ 49 mW	84.76 @ 42 mW, 85.08 @ 64 mW, 85.92 @ 86 mW, 85.10@ 94.5 mW

3.1.4 Power Losses Analysis

Fig. 3.12 Power loss estimation of the proposed active rectifier.

The optimal efficiency for the design is at around 93 mW of output power. Figure 3.12 shows the total power and its power loss under the optimal condition. With an input power of 108.2 mW, the total power loss is approximately 15.25 mW, which includes the power consumption of the controller and the power losses of the design. The controller power includes the power consumed by the comparator and the driver, where the proposed comparator consumes around 60 uW of the power. The power loss of around 15.06 mW is contributed by the conduction loss and switching loss of the power switches, leakage power loss of the transistors, bonding wires conduction loss as well as the PCB traces power loss. The dominant power losses are the conduction loss and switching loss of the power switches and they can be estimated from Eq. (3.1.5) and Eq. (3.1.6) [40].

$$P_{conduction} = 2 \times I_p^2 R_{onp} D_{eff} + I_n^2 R_{onn} D_{eff} \quad (3.1.5)$$

$$P_{switching} = 2 \times (C_{gp} + C_{gn}) V_{rectf}^2 f \quad (3.1.6)$$

Each cycle, there are 3 power switches conduct, with 2 switches in the negative voltage converter and an active diode switch. I_p and I_n are the conducting current of the high-side and low-side switches respectively while R_{onp} and R_{onn}

are the on-resistance of the high-side and low-side switches respectively. D_{eff} is the effective duty cycle of the rectifier, which is the conduction time over one period. C_{gp} and C_{gn} are the total gate capacitance of the high-side and low-side switches respectively. The power switches turn-on and off twice in each period. Under heavy-load condition, the conduction loss due to the conducting current will dominate the power loss. On the other hand, under light-load condition, the switching loss due to charging and discharging of the gate capacitance will dominate.

3.2 Buck Regulator

The rectified voltage is required to be regulated by a buck regulator before supplying the functional blocks in the receiver, such as for sensor or memory circuits. In order to regulate the rectified voltage, a buck regulator is required after the active rectifier block. Practically, in an inductive coupling system, the orientation of the coils and the distance between them affect the power and thus the voltage received at the receiver [157]. As a result, the rectified voltage which is the input voltage to a buck regulator can vary as much as from 2.6 V to 3.9 V [40]. Hence, a regulator is required to be adaptive to a range of varying input voltage in order not to affect the system operation.

3.2.1 Proposed Controller

Fig. 3.13 Buck regulator with the proposed controller.

Pulse skipping modulation (PSM) and pulse frequency modulation (PFM) are utilized to control the buck regulator across a wide load range. The control scheme is implemented by using a proposed Digitally-Assisted Adaptive On-Time (DA-AOT) controller, with the aim of providing good power efficiency for the entire load range of 0 – 40 mA. Fig 3.12 shows the buck regulator with the proposed PFM-based DA-AOT controller. The proposed buck regulator operates in Discontinuous Conduction Mode (DCM) which is inherently stable due to a single-pole transfer function characteristic [46].

The regulation scheme is a combination of PSM and digitally-assisted adaptive on-time (DA-AOT) PFM controls. In order to optimize the efficiency, the converter is active only when there is a load requirement. The converter is awakened by the rising edge of the system clock in each switching cycle. The comparator is activated according to the system clock and it compares the output voltage V_{OUT} with a reference voltage V_{REF} . If the output voltage is above the reference voltage, implying that it is under light-load condition and the switching activity will be skipped for that particular cycle. On the contrary, if the output voltage is below the reference voltage, the charging switch M_p will be turned-on for an adaptive on-time which is adaptive to the varying input voltage and the load conditions. After M_p is turned-off, the discharging switch M_N will be turned-on after a fixed dead-time to transfer the inductor energy to the output load. When the inductor current reaches zero, M_N will be turned-off and this is implemented by a zero-current detector (ZCD). After M_N is turned-off due to zero-current condition, the comparator and the control blocks that are not in used will be turned-off except the system clock. Fig. 3.13 shows the PSM control scheme, the output voltage information is stored in ' m ' which indicates the load conditions. If m is logic '1', it indicates that the output voltage is below the reference voltage and hence the switching activity is implemented as discussed earlier. In contrast, if m is logic '0', it implies that the output voltage is above the reference voltage and therefore the switching activity is skipped to reduce the power losses. However, PSM control itself is inefficient to cater for a wide load range. Hence,

the PFM control with DA-AOT controller is utilized to vary the switching frequency and the on-time in order to optimize the efficiency for the range of 0-40 mA of output current.

Fig. 3.14 PSM control scheme.

As shown in Fig. 3.12, the PFM controller consists of a low power clock oscillator and counters are used to generate the system clock of lower frequency with predictable switching frequency. There are four frequencies available for the selection which are f , $f/2$, $f/4$ and $f/8$, where f is the maximum frequency and $f/8$ is the minimum frequency.

The proposed DA-AOT control block is shown in Fig. 3.14. The DA-AOT block is enabled only when the switching activity is required. During the charging phase, the on-time of the high-side power switch M_p can be generated by charging up a capacitor, C_{ON} with a current that is proportional to the input voltage. Instead of having only one adaptive on-time (AOT) as in [50], an array of AOT can be implemented by having different values of C_{ON} . Besides adaptive to the varying input voltage, the AOTs are designed to be dependent on the load conditions as well in order to improve the efficiency during light-load. The on-time equation can be expressed as in Eq. (3.2.1).

$$t_{ON,n} = \frac{C_{ON,n} \times V_{REF}}{I_{BIAS}} ; n = 0,1,2,3 \quad (3.2.1)$$

Fig. 3.15 Proposed DA-AOT control block.

The reference voltage V_{REF} represents the output voltage V_{OUT} and I_{BIAS} is the biasing current. There are four AOTs available for the selection, with each being controlled by the selection signal $D_0 - D_3$. Each cycle only one AOT will be selected based on a proposed algorithm. The selected C_{ON} will be charged up to the reference voltage to generate the required on-time. When the capacitor voltage reaches the reference voltage value, which is the desired output voltage value, the signal t_{off} will go 'high' to end the charging phase. After the selected AOT is generated, the discharging transistors (M_0-M_3) are enabled to discharge all the residue charges in the charging capacitors and be ready for the next cycle. Then, the DA-AOT block will be shut down to save power.

In total there are four frequencies and four adaptive on-times (AOT) available for the selection. With the four AOTs and four frequencies, there are 16 different combinations of AOT and frequency available for the selection. In each switching cycle, only one frequency and one AOT will be chosen. The selection of the system clock frequency and AOT is done based on the PFM-based AOT Finite State Machine (FSM) as shown in Fig. 3.15, depending on the load conditions. The algorithm is designed such that the power efficiency is optimized

and the output voltage ripples is minimized. Eq. (3.2.2) shows that the output voltage of a DCM buck regulator can be regulated by manipulating the variables $D^2 T_{sw}$, in which T_{sw} is the switching period, D is the duty ratio and AOT is the adaptive on-time. Different AOT results in different duty cycles. R represents the load and L is the inductor value. To ensure that the regulator operates well in DCM, the total of the maximum on-time and off-time are designed to be less than the minimum switching period, as expressed in Eq. (3.2.3).

$$V_{OUT} = \frac{2 V_{IN}}{1 + \sqrt{1 + \frac{8L}{R(D_x^2 T_{sw,y})}}} ; x, y = 0, 1, 2, 3 \quad (3.2.2)$$

$$\text{where, } D = \frac{AOT}{T_{sw}}$$

$$t_{on,max} + t_{off,max} < T_{min} \quad (3.2.3)$$

Fig. 3.16 Flow chart describing the operation of the proposed PFM-based AOT selecting FSM.

Initially, during start-up, the controller is supplied with the input voltage. After the converter is stabilized and a sufficient output voltage is obtained, the controller will then be supplied with the output voltage. When the regulator is first powered up as shown in Fig. 3.15, a power-on reset (POR) signal is generated to reset the selection by initiating it with a minimum D^2T_{sw} option. The load condition is observed by comparing the output voltage to a reference voltage. The comparison result (m) is stored in a flip-flop which is updated during each switching cycle. If the output voltage is detected to be below the reference voltage ($m = 1$) for two consecutive cycles, the D^2T_{sw} counter will be incremented by one. In contrast, if the output voltage is detected to be above the reference voltage ($m = 0$) for two consecutive cycles, the D^2T_{sw} counter will be decreased by one. The minimum D^2T_{sw} option will be selected if the system enters ultra-light load condition. With that, the inductor peak current and switching frequency can be minimized, contributing to decreased conduction power losses and switching power losses. On the other hand, if the system enters heavy-load conditions, the D^2T_{sw} counter will increase accordingly to cater for the load requirements.

Fig. 3.17 Operation waveforms of PFM and PSM controls.

The detailed operation waveforms are shown in Fig. 3.16. The selection signals ($S0-S3$) are used to select the 16 options; with the ‘0000’ choice corresponds to the minimum duty cycle and frequency (minimum D^2T_{sw}) and ‘1111’ corresponds to the maximum duty cycle and frequency (maximum D^2T_{sw}). According to the load condition information (m), the selection signals are updated periodically by a MUX_CLK. The MUX_CLK is generated after the low-side switching ends. The output will be regulated with the updated duty cycle and switching frequency in the next cycle. The use of 16 selections in the design is sufficient for the application. However, a larger number of selections can be designed for a more accurate regulation but at the trade-off of increased power consumption.

3.2.2 Measurement Results

Fig. 3.18 The die photo of the buck regulator with the proposed controller.

The buck regulator with the proposed PSM and PFM-based DA-AOT controller has been fabricated in a standard $0.18\ \mu\text{m}$ CMOS process as part of the power management block in the inductively powered receiver. The chip micrograph of the proposed design is shown in Fig. 3.17. The power switches

with gate drivers occupy an area of 0.153 mm^2 and the area of the control circuits is 0.079 mm^2 . The chip is packaged in a 48-pin QFN package. In order to minimize the resistive wire-bonding parasitic at the critical nodes, triple bonding is utilized at the input, output and switching node. The buck regulator uses an off-chip inductor of $2.2 \mu\text{H}$ and a $10 \mu\text{F}$ off-chip output filtering capacitor.

To verify the control scheme, the proposed design is tested under different load conditions. The measured steady-state output voltage V_{OUT} , switching node V_{X} , inductor current I_{L} and system clock SYS_CLK are shown from Fig. 3.18 to Fig. 3.20 at load currents of 1 mA, 10 mA and 40 mA respectively. As can be observed, the PSM control is applied by skipping the switching pulses when it is necessary. During light-load at 1 mA, the minimum adaptive on-time (AOT) and the minimum switching frequency are selected to regulate the output voltage. As the load current increases gradually from 1 mA to 40 mA as shown from Fig. 3.18 to Fig. 3.20, the adaptive on-time (AOT) and the switching frequency increase gradually (based on the PFM-based AOT selecting algorithm) to cater for the increasing load requirements. At an output voltage of 1.4 V, the maximum and minimum switching frequencies are measured to be 965 kHz and 120 kHz respectively.

Fig. 3.19 The steady-state waveforms at 1 mA of load current, $V_{\text{IN}}=3 \text{ V}$ and $V_{\text{OUT}}=1.4 \text{ V}$.

Fig. 3.20 The steady-state waveforms at 10 mA of load current, $V_{IN}=3$ V and $V_{OUT}=1.4$ V.

Fig. 3.21 The steady-state waveforms at 40 mA of load current, $V_{IN}=3$ V and $V_{OUT}=1.4$ V.

Fig. 3.21 shows the waveforms of the output voltage, switching node and inductor current when the load current is changing from 1 mA to 40 mA. As can be observed, the switching activity increases as expected when the load current

is increased from 1 mA to 40 mA. Fig. 3.22 shows the waveforms when the load current is reduced from 40 mA to 1 mA. As can be seen, the switching activity reduces during the load transition period.

Fig. 3.22 The waveforms during load transition from 1 mA to 40 mA at $V_{IN}=3$ V and $V_{OUT}=1.4$ V.

Fig. 3.23 The waveforms during load transition from 40 mA to 1 mA at $V_{IN}=3$ V and $V_{OUT}=1.4$ V.

The measured power conversion efficiency of the proposed regulator is plotted against the load current under various input voltages as shown in Fig. 3.23. The power conversion efficiency can be obtained by taking the ratio of the output power to the input power. The average input current is measured by using a multimeter and then it is multiplied with the input dc voltage as input power. For the output dc power, the average output voltage and current are measured using a multimeter and they are multiplied together to get the output power. Eventually the PCE obtained is plotted against the load current (V_{out}/R_L). The load current is varied by using a variable resistor as a load. By varying the resistor, different load currents can be obtained. The measured performance covers the maximum and minimum of the input voltage range under different load conditions. For a same output voltage of 1.4 V, the power efficiency decreases as the input voltage increases gradually from 2.6 V to 4.2 V. A higher input voltage causes the inductor peak current to be higher and thus it leads to higher conduction power losses. Therefore, the best efficiency is achieved when the input voltage is of minimum value. A peak efficiency of 91.00% is achieved at an input voltage of 2.6 V and an output voltage of 1.4 V.

Fig. 3.24 Measured power efficiency versus load current of the proposed design for various input voltages.

The performance of the proposed buck regulator is summarized in Table 3.2. The key performance aspects of the proposed regulator are compared to the other relevant start-of-the-art work. In order to have an objective comparison, the power efficiency is compared with the reference designs that have the closest possible input and output voltage in the load range of 0 - 40 mA. For the reference designs that target at loads higher than 40 mA, the performance comparison are done with the efficiency reported using the light-load controller. As shown in Table 3.3, the proposed design achieves a peak power efficiency of 91.00% and 89.03% at the input voltage of 2.6 V and 3 V respectively. The proposed controller minimizes the total power consumption by skipping the switching activity when necessary and shutting down the unused blocks. The converter is active only when there is a load requirement and it is awakened by the rising edge of the system clock in each switching cycle. In addition, the on-time and the switching frequency are designed to be dependent on the load conditions in order to optimize the efficiency across the load range. With these features, the power losses and the quiescent power of the design can be minimized and hence a better efficiency can be achieved. Besides, the area consumed by the proposed work is comparable to the other work despite the difference in the process.

Table 3.2 Performance summary of the proposed buck regulator.

Specifications	Value
Inductor	2.2 μ H
Output Capacitor	10 μ H
Switching frequency	120 kHz - 965 kHz
Load regulation	0.51 mV/mA
Max. Load current	40 mA
Load transient response (1 - 40 mA)	18 μ s (20 mV voltage undershoot)

Table 3.3 Performance comparison with state-of-the-art work.

		JSSC 2004 [158]	TCAS-I 2011 [159]	JSSC 2011 [160]	TPEL 2016 [161]	Proposed Work	
Technology		0.25 μ m	0.18 μ m	45nm	90nm	0.18 μ m	
Light-load Control Method		Voltage-Mode Digitally- Controlled (PFM)	PWM with Dynamic Power FET Segmentation	Voltage- Mode COT (PFM)	Voltage- Mode HA- AMOT (PFM)	Voltage-Mode DA-AOT (PFM)	
Controller Area (mm ²)		Not Reported	0.077	0.07	0.06	0.079	
Max Load (mA)		40 (with only light-load controller)	60 (with only light-load controller)	15 (with only light- load controller)	40	40	
Input Voltage Range (V)		2.8-5.5	2.7-4.2	2.8-4.2	1.8-4.2	2.6-4.2	
Output voltage range (V)		1-1.8	1-1.8	0.4-1.2	0.9-1.4	1.2-1.8	
External Inductor (μ H)		47	2	10	4.7	2.2	
External Capacitor (μ F)		10	4.7	2	2.2-10	10	
Measured efficiency (%)	Conditions (V _{IN} & V _{OUT})	V _{IN} =4 V, V _{OUT} =1.5 V	V _{IN} =3.6 V, V _{OUT} =1.8 V	V _{IN} =3 V, V _{OUT} =1 V	V _{IN} =3.3 V, V _{OUT} =1.2 V	V _{IN} = 3 V, V _{OUT} = 1.4 V	V _{IN} = 2.6 V, V _{OUT} = 1.4 V
	Load current range : 0 - 40mA	88.00 @ 37.5 mW	75.00 @ 36 mW	87.40 @ 12 mW, 83.00 @ 15 mW	85.70 @ 12 mW	88.93 @ 14 mW, 87.00 @ 42 mW	91.00 @ 14 mW, 88.56 @ 42 mW

3.2.3 Power Losses Analysis

In the DA-AOT control block, each cycle only one capacitor will be selected and charged up based on the proposed algorithm. Hence, during the discharging of all 4 capacitors' residue charge, the power loss is dominated by the selected capacitor. As the design work under different on-time and operating frequency, the maximum and minimum losses of the capacitor discharging can be estimated from Eq. (3.2.4) and Eq. (3.2.5) respectively.

$$P_{loss(max)} = \frac{1}{2} C_{max} V^2 f_{max} \quad (3.2.4)$$

$$P_{loss(min)} = \frac{1}{2} C_{min} V^2 f_{min} \quad (3.2.5)$$

The maximum loss during the discharging of capacitor with maximum capacitance and maximum frequency is around 1.75 μ W. On the other hand, the minimum loss due to the minimum capacitance and minimum frequency can be estimated to be around 73 nW. As the proposed buck regulator operates in discontinuous conduction mode (DCM), the dominant power losses which are the conduction loss and the switching loss of the design can be estimated from Eq. (3.2.6) to Eq. (3.2.10), as described in [172].

$$\begin{aligned} P_{conduction} &= P_{FET} + P_{DCR-ESR} + P_{diode} \\ &= R_{dson} \left(\frac{2 \times \Delta I \times I_{RL}}{3} \right) + (R_{DCR} + R_{ESR}) \left(\frac{2 \times \Delta I \times I_{RL}}{3} \right) - R_{ESR} I_{RL}^2 + \\ &\quad [V_D \times \Delta I \times \left(\frac{T_d}{T_s} \right)] \end{aligned} \quad (3.2.6)$$

$$P_{switching} = P_{Tran} + P_{gate_charge-loss} + P_{Vx-node} \quad (3.2.7)$$

$$P_{Tran} = \frac{(V_{IN} + 2V_D) \times \Delta I \times T_{ran}}{4T_s} \quad (3.2.8)$$

$$P_{gate_charge-loss} = \frac{(C_{gsp}+C_{gsn}) \times V_{IN}^2}{T_s} + \frac{1}{T_s} C_{gdp} \left[(V_{IN} - V_{OUT})^2 + V_{IN}^2 + \frac{V_D^2}{2} \right] + \frac{1}{T_s} C_{gdn} [(V_{IN} - V_{OUT})^2 + 2V_{IN}V_{OUT}] \quad (3.2.9)$$

$$P_{Vx-node} = \frac{1}{2T_s} C_x [(V_{IN} - V_{OUT})^2 + V_{OUT}^2 + V_D^2] \quad (3.2.10)$$

The conduction loss includes the power loss due to the high-side and low-side switches during conduction with the assumptions that $R_{dson-p}=R_{dson-n}=R_{dson}$, the power loss of the parasitic resistance DCR and ESR of the inductor and the capacitor respectively and the power loss of the body-diode conduction of the low-side switch during the dead-time period T_d . In the equations, I_{RL} is the load current, ΔI is the peak inductor current (also known as ripple current) and T_s is the switching period.

The switching loss includes the transitional loss of the power switches during the finite rise or fall time of the gate control signals with the assumption that the rise and fall time are equal and it is denoted as T_{ran} , the power loss due to the charging and discharging of the gate capacitance and the switching node capacitance of the converter. In the equations, V_D is the forward voltage of the body-diode of the low-side switch and C_x is the total parasitic capacitance at the switching node V_x of the converter.

The power losses are estimated during heavy-load and light-load condition respectively, as shown in Fig. 3.25. As shown in Fig. 3.25, the conduction power loss dominates the power loss during heavy-load condition in (a) and the switching loss dominates the power loss during light-load condition in (b). The power loss due to the discharging of all 4 capacitors' residue charge is included in the controller power consumption. Other losses include the transistors' leakage power loss, the bonding wires conduction loss, the PCB traces power loss, etc.

Fig. 3.25 Power loss estimation during heavy-load in (a) and light-load in (b).

3.3 Two-Stage Performance

Fig. 3.24 shows a cascaded two-stage receiver with the proposed rectifier block and the proposed buck regulator. The boards for the rectifier and the buck regulator chips are shown in Fig. 3.25.

Fig. 3.26 Two-stage receiver with the proposed rectifier and the proposed buck regulator.

Fig. 3.27 Test boards of the 2-stage receiver and the transmitter.

Fig. 3.26 shows the measured steady-state waveform of input AC voltage VAC, rectified voltage Vrect, regulated output voltage Vout and the inductor current I_L for the two-stage receiver with a load of $240\ \Omega$. The measured power efficiency of the two-stage receiver is plotted in Fig. 3.27. A peak efficiency of

75.35% is achieved for the two-stage design at a regulated output voltage of 1.4 V.

Fig. 3.28 The measured steady-state waveforms of the 2-stage receiver at a load of 240 Ω .

Fig. 3.29 The measured two-stage PCE versus load current at $V_{OUT} = 1.4$ V.

3.3.1 Discussion and Conclusion

With the proposed techniques and the circuits' improvement done on the rectifier block as well as the buck regulator block, the two-stage receiver achieves a peak efficiency of 75.35%. However, due to the cascaded two-stage design, the power losses incurred are significant and thus the overall power efficiency is limited. In order to have a power efficiency of at least 90% for a two-stage design, each stage of the design needs to achieve at least a 95% of power efficiency which is a great challenge. Hence, an energy-efficient one-stage receiver design with embedded regulation capability is required to solve the limitation. The proposed one-stage receiver design with efficiency improvement will be presented in Chapter 4.

Chapter 4 Design of Single-Stage Direct-Conversion AC-DC Converter

In this chapter, a one-stage receiver design which consists of a single-stage AC-DC converter will be presented. The concept and the structure of the single-stage converter will be introduced. Besides, the topology and its operating principle as well as the controller implementation will be explained as well. Lastly, measurement results and discussion will be presented at the end of the chapter.

4.1 Introduction

Fig. 4.1 Inductively couple WPT system with the proposed one-stage AC-DC converter.

Fig. 4.1 shows a generic inductively coupled wireless power transfer system. Two magnetically coupled inductors $L1$ and $L2$ are used to transmit the power from the transmitter or reader to a receiver or tag. To maximize the power transfer efficiency between the coils, the resonant tanks at both transmitter and receiver sides are usually designed to resonate at the same frequency. The coupling between the coils induces an AC voltage at the secondary coil $L2$. The induced AC voltage is required to be converted to a DC voltage to power up the microchip

in the receiver for useful operations. For a typical wireless power receiver, the power is usually transferred through two stages, in which a rectifier is used for an AC to DC conversion while a DC-DC converter in the form of switching regulator or LDO would regulate the DC output voltage [95-101]. Thus, the power efficiency of the receiver is mainly dominated by the efficiencies of both of the rectifier and the voltage regulator, which can be expressed as in Eq. (4.1.1).

$$\eta_{receiver} \approx \eta_{rect} \times \eta_{regulator} \quad (4.1.1)$$

However, the power losses incurred from the cascaded two-stage design often restrict the overall power efficiency of the receiver. The high power losses generated from the cascaded two-stage blocks would cause the thermal emission of the device to increase, which may cause danger to the consumers in certain applications. Besides, greater power losses also imply that more power is required to be transmitted from the transmitter in order to cater for the receiver requirements. This is not desirable as in real life applications; the power transferred from the transmitter may be limited due to the orientation and the distance between the coils. Apart from the power losses issues, the footprint and size of the receiver are of main concern as well. The usual way of cascading an inductive DC-DC converter which utilizes an inductor is undesirable as it increases the footprint and cost of the receiver [95-97]. Even though an LDO is frequently used in [98-101] to regulate the rectified voltage with the aim of extending the power transmission range, the power efficiency is degraded greatly due to the losses incurred from the LDO. Hence, instead of having a two-stage design in the receiver, we propose a one-stage AC-DC converter with embedded regulation capability, which is an energy-efficient solution in a WPT system.

Various state-of-the-art works have been proposed with the objective of implementing the power conversion in a single-stage. The works in [102-103] achieve the voltage regulation by controlling the transmitter power. However, this would slow down the transient response of the receiver as the feedback has

to go through the transmitter to adjust the power transferred in response to a load change in the receiver. The resonant regulating rectifier (3R) in [105] consists of five off-chip diodes and three off-chip capacitors which increase the footprint of the receiver. Moreover, the output voltage is regulated manually with the help of the resonant tanks on both sides. The regulation is not done by the on-chip design or the converter independently, but it needs the help of the off-chip components such as the microcontroller and resonant tanks to execute the regulation. The pulse frequency modulation (PFM) control is used in tandem with the pulse width modulation (PWM) control scheme in [112]. The pulse frequency is increased or decreased based on the upper or lower threshold limit of the pulse-width regulated by the PWM control. However, the efficiency may be degraded due to the varying pulse-width especially when the pulse-width is at its minimum. In [107], a rectifying regulator with PWM and PFM control schemes is proposed. The PFM control utilized in [107] is discontinuous, that is a single short pulse is generated only when the output voltage falls below the reference voltage. By adaptively operating in resonant voltage or current mode (VM or CM) as in [109-110], high voltage conversion efficiency can be achieved in CM while high power conversion efficiency can be obtained in VM for a wide load range. In [111], a one-stage reconfigurable resonant regulating rectifier is used to widen the operation region by avoiding the variation in the system voltage conversion ratio. Besides, the 3-mode reconfigurable resonant regulating rectifier in [108] employs a 3-level configuration that is able to provide for higher power applications at 1 to 2A of output current.

4.2 Proposed One-stage AC-DC Converter

In this chapter, we propose a one-stage AC-DC converter, utilizing a unique controller which consists of the Pulse Skipping Modulation (PSM) and the Pulse Frequency Modulation (PFM) control to produce a regulated output voltage. As compared to the PWM control, the proposed control scheme reduces the complexity of the design. Compared to the work in [112], the on-time of the

proposed work is maximized whenever it is in the ‘ON’ mode in order to optimize the efficiency for the entire load range. Besides, with an adaptive clock, the proposed scheme operates by periodically checking on the loads instead of the discontinuous operation as in [107]. Hence, the regulating operation is more predictable. Moreover, a unique PFM algorithm is proposed in our work, aiming to reduce the switching power losses during light loads and to maximize the transient response during heavy loads. The proposed design retains an active rectifier structure, constituting four power transistors and two comparators. With the proposed ON-/OFF-mode controller, at least 81% of power efficiency is obtained in the range of 2mW-80mW of output power with a 2V output voltage. In addition, switching synchronization is accomplished smoothly without any calibration as in [105] and a good transient response is also observed during measurement. The output voltage has been tested at 1.8V and 2V respectively. The details of the proposed design are discussed in the subsequent sections.

4.2.1 Concept and Structure of the proposed design

Fig. 4.2 Basic concept of the ON-/OFF-mode controller.

The basic idea of regulating an output voltage is to have two operations, which are the charging and the discharging operations. When the output load demands for more power, the converter must be able to provide the required output power and thus the occurrence of charging is increased. In contrast, when the system enters light-load conditions, in which lesser power is required by the load, the converter must be able to reduce the power transferred and hence the occurrence

of discharging is increased.

Fig. 4.3 (a) ON-mode operation and (b) OFF-mode operation of the proposed design.

Fig. 4.2 illustrates the basic concept of the proposed ON-/OFF-mode controller. PSM control is incorporated in the design in order to cater for the charging and discharging operations. The one-stage converter works in either

ON-mode or OFF-mode, in which ON-mode refers to the charging operation while OFF-mode refers to the discharging operation. During ON-mode, the converter works as a normal rectifier, transferring the input power to the output as usual. However, no power is transmitted to the output during OFF-mode and the output voltage is sustained by the charge in the output capacitor.

To gain a better insight of the ON-/OFF-mode operation, the implementation of ON-mode and OFF-mode is described in Fig. 4.3 (a) and (b) respectively. As shown in Fig. 4.3, the induced AC voltage is represented by the source V_{AC} , where $V_{AC} = V_{in+} - V_{in-}$. The dc smoothing capacitor is represented by C_L and R_L denotes the load resistor. Fig. 4.3(a) shows the structure works as a full-wave rectifier in ON-mode operation. When the input node V_{in+} is greater than the output voltage V_{DC} , the power transistors MP2 and MN1 will be turned on to charge up the output. On the other hand, the power switches MP1 and MN2 will be turned on when the node V_{in-} is higher than the output voltage V_{DC} . Fig. 4.3(b) illustrates the OFF-mode operation. In this mode, both of the high-side power switches MP1 and MP2 are turned off. Under this condition, one of the low-side switches (either MN1 or MN2) is turned on, depending on the input nodes V_{in+} and V_{in-} . However, there is no electrical connecting path for the current to flow to the output, so the input current is almost zero. Hence, no power is being transferred to the output and the output capacitor is discharged to the load to maintain the output voltage. As the input node is varying all the time, a dynamic body bias (DBB) circuit is used to tie the body of the high-side power switches, MP1 and MP2 to the highest voltage and therefore to prevent latch-up [152].

Fig. 4.4 Illustration of waveforms of the ON-/OFF-mode controller.

The waveforms of the ON-/OFF-mode operation are illustrated in Fig. 4.4. The system clock is generated from the input voltages V_{in+} and V_{in-} . Therefore, it is synchronized with the input frequency. A feedback comparator is enabled periodically to compare the output voltage with a reference voltage. If the output voltage is below the reference voltage, the converter will operate in ON-mode to charge up the output. In contrast, if the output voltage is detected to be above the reference voltage, the converter will work in OFF-mode to skip the power transmission. As can be seen from Fig. 4.4, during OFF-mode, the input current is almost zero, which means no power will be transferred to the output. Besides, the comparator is disabled after each comparison and will only wake up at the next rising edge of the system clock. Consequently, the overall power consumption of the converter can be minimized. Hence, by utilizing the ON-/OFF-mode controller, the output voltage regulation is achieved over a wide load range with minimal power consumption.

4.2.2 Proposed PFM Control

To further enhance the performance of the one-stage converter, PFM control

is incorporated in the design as well. The system clock frequency can be reduced in order to decrease the switching power losses under light-load conditions. By reducing the system clock frequency, the frequency of turning on the comparator is reduced as well and thus the overall quiescent power can be minimized under light-load conditions.

In order to ensure that the mode transition occurs only at the zero-crossing instant of the input current, the switching frequency is required to be synchronized with the input frequency. Hence, the switching frequency is designed to be in multiple of the input frequency f_{in} . There are two frequencies $2f_{in}$ and f_{in} available to be selected for the system. The selection of the system clock frequency is done based on the load conditions and the PFM algorithm as shown in Fig. 4.5. The PFM algorithm is designed such that the transient response of the converter is maximized while at the same time the power consumed is minimized during light-load conditions. When heavy-load condition is detected, the frequency is increased in order to speed up the transient response. On the contrary, when light-load condition is detected, the frequency is decreased to reduce the switching power losses.

As shown in Fig. 4.5, if the output voltage is detected to be below the reference voltage for at least once, the system clock frequency will be increased by two times. In contrast, if the output voltage is detected to be above the reference voltage thrice consecutively, indicating that the system enters light-load condition and thus the system clock frequency will be reduced by half. Fig. 4.6 shows the simulated waveform of the PFM control. As can be observed, the system clock frequency is changing from f_{in} to $2f_{in}$ during the increment of output power from 2 mW to 80 mW. On the contrary, the system clock frequency is reduced from $2f_{in}$ to f_{in} when the output power is stepped down from 80 mW to 2 mW.

Fig. 4.5 Flow chart of the proposed PFM algorithm.

Fig. 4.6 Simulated waveforms of the converter operating in PFM mode.

4.2.3 Topology and Power Losses

Fig. 4.7 The configurations and input waveforms of (a) ON-mode and (b) OFF-mode.

Fig. 4.7 shows the ON and OFF-mode configurations and their respective input waveforms. For ON-mode configuration as shown in Fig. 4.7(a), the structure works as a normal rectifier by turning on one high-side and one low-side power switches for each conducting cycle. For example, when V_{IN+} is greater than V_{IN-} , MN1 is turned on and the node V_{IN-} is limited to $-V_{ds(ON)}$, which is the drain to source voltage drop of MN1. The current flows through MN1 and MP2 to charge up the output. Under this mode, the power losses are the conduction loss and switching loss of both conducting switches (MP2 and MN1) and the leakage power losses which include the reverse current conduction loss and the leakage power loss of the transistors. The total power losses for the ON-mode can be expressed as in Eq. (4.2.1).

$$P_{losses(ON-mode)} = P_{conduction\ loss(Mp\&Mn)} + P_{switching\ loss(Mp\&Mn)} + P_{leakage} \quad (4.2.1)$$

For OFF-mode configuration as shown in Fig. 4.7(b), the output is isolated from the input source by turning off both high-side power switches. There is no electrical connecting path for the power to flow from the input source to the output. Therefore, the input current is almost zero and the output voltage is sustained by the output charge of the output capacitor C_L . Under this mode, the gates of the low-side switches (MN1 and MN2) are still connected to the input source and hence a small power is used to charge up the gate of any of the switches. For example, when V_{IN+} is higher than the threshold voltage of MN1, MN1 is turned on and the node V_{IN-} is clamped to ground. On the other hand, when V_{IN-} is greater than the threshold voltage of MN2, MN2 will be turned on and the node V_{IN+} will be clamped to ground. Hence, the power losses during OFF-mode are the switching power loss of MN1 or MN2 and the leakage power losses which can be expressed as in Eq. (4.2.2).

$$P_{losses(OFF-mode)} = P_{switching\ loss(Mn)} + P_{leakage} \quad (4.2.2)$$

The total efficiency of the ON-/OFF-mode converter can be expressed as in Eq. (4.2.3), where P_{Load} is the output power, P_{con} represents the conduction power losses, P_{sw} denotes the total switching power losses, $P_{controller}$ is the power consumption of the controller which includes the active diode comparators and all the control blocks and P_{leak} represents the total leakage power losses which include the reverse current conduction loss and the leakage power loss of the transistors.

$$\eta_{ON-/OFF-mode} = \frac{P_{Load}}{P_{Load} + P_{con} * (n \cdot T) + P_{sw} + P_{controller} + P_{leak}}, n \geq \frac{1}{2} \quad (4.2.3)$$

4.2.4 Mathematical Analysis of One-stage Converter

Fig. 4.8 The equivalent circuit model and the associated half-time period waveform of the converter.

In this section, we develop an analytical model for the ON-/OFF-mode controller of the one-stage converter. During each conduction cycle, one PMOS switch and one NMOS switch will be turned on and their equivalent on-resistance can be modeled as in Fig. 4.8. The $V_{AC}(t)$ denotes the AC power source and the total on-resistances of both switches can be simplified as R_{ds} . The smoothing dc capacitor and the output load are represented by C_L and R_L respectively. Both of the power switches operate in triode region which minimize the voltage drop across them. The criteria for the converter to function normally is that the input amplitude has to be greater than the voltage drop across the on-resistance of both of the high-side and low-side power switches, as expressed in Eq. (4.2.4).

$$|V_{AC}| > V_{ds(p)} + V_{ds(n)} \quad (4.2.4)$$

Assumed that the positive and negative half cycles are symmetrical and the converter conducts a maximum duration of $(t_2 - t_1)$ during each conduction cycle, as illustrated in Fig. 4.8. During steady-state, the total input charge supplied by the input AC source and the total output charge delivered to the output can be derived as in Eq. (4.2.5) and (4.2.6) respectively.

$$Q_{in} = \int_{t_1}^{t_2} \frac{V_{AC} \sin \frac{4\pi}{m \cdot T} t - V_{DC}}{R_{ds}} dt, \quad m \geq 1 \quad (4.2.5)$$

$$Q_{out} = \int_0^{n \cdot \frac{T}{2}} \frac{V_{DC}}{R_L} dt = \frac{V_{DC}}{R_L} \left(n \cdot \frac{T}{2} \right), \quad n \geq 1 \quad (4.2.6)$$

By applying the principle of conservation of charge, the output voltage can be expressed in Eq. (4.2.7) by equating the total input and output charge, where $m \cdot T$ is the rate of charging and $n \cdot \frac{T}{2}$ is the rate of discharging.

$$V_{DC} = \frac{\frac{V_{AC} \cdot m \cdot T}{4\pi} \left(\cos \frac{4\pi}{m \cdot T} t_1 - \cos \frac{4\pi}{m \cdot T} t_2 \right)}{(t_2 - t_1) + \frac{R_{ds}}{R_L} \cdot n \cdot \frac{T}{2}} ; m, n \geq 1 \quad (4.2.7)$$

From Eq. (4.2.7), it can be inferred that under light-load conditions when R_L increases to conduct lesser load current, the output voltage V_{DC} is maintained by increasing the rate of discharging or reducing the rate of charging. In contrast, during heavy-load condition, the output voltage is regulated by increasing the charging rate or reducing the discharging rate. Hence, by modulating the conduction rate of the converter, the output voltage regulation is accomplished over a wide load range.

Under steady-state, the voltage drop due to the ESR of the output capacitor C_L and the discharging of C_L into the load R_L contribute to the output voltage ripples. Hence, the output voltage ripples can be approximated as in Eq. (4.2.8).

$$\Delta V_{ripples} \approx I_o \cdot R_{ESR} + V_{DC} \cdot \left(1 - e^{\frac{-n \cdot T}{R_L \cdot C_L}} \right) \quad (4.2.8)$$

As can be inferred from Eq. (4.2.8), the output voltage ripples can be reduced by increasing the output capacitor value or the operating frequency.

4.2.5 Self-startup Mechanism

Fig. 4.9 Parasitic capacitances of power transistor MP2.

The proposed structure possesses self-startup ability. During startup, a reset pulse is used to trigger the mode selection to ON-mode, enabling the converter to work as a full-wave rectifier. The parasitic capacitances of the high-side power switch MP2 can be modeled as in the Fig. 4.9. During startup, the output voltage VDC is zero and therefore the gate-source voltage V_{sg2} can be approximated as in the Fig. 4.9, which is a capacitive ratio of the input voltage V_{in+} . Initially, as MP2 is in the cut-off region, the parasitic capacitances C_{gd} and C_{gs} are almost of the same value and thus the voltage V_{sg2} is roughly half of the voltage V_{in+} . As V_{in+} increases gradually, the voltage V_{sg2} increases as well. Eventually it will exceed the threshold voltage of the transistor MP2 and MP2 will be turned on, acting as a passive diode to slowly charge up the output capacitor. The same applies to the negative cycles as well, the transistor MP1 will act as a passive diode and the current will flow through the transistors MP1 and MN2 to slowly charge up the output capacitor. After several cycles, the output voltage will reach the minimum supply of the control blocks and thus the structure will start to work

in the ON-/OFF-mode operation as described earlier. The simulated waveform during startup is shown in Fig.4.10.

Fig. 4.10 Simulated waveforms during startup.

4.2.6 Implementation of key circuit blocks

Fig. 4.11 shows the block diagram of the wireless power receiver with the proposed single-stage AC-DC converter. It consists of the ON-/OFF-mode reconfigurable topology as the power stage and the controller. The ON-/OFF-mode controller determines the operation modes of the reconfigurable topology based on the load requirements to achieve voltage regulation. In addition, the PFM control is utilized to select the switching frequency of the system in order to maximize the transient response during heavy-load and to minimize the switching power losses during light-load. To cater for different reference voltage values, a non-inverting gain amplifier can be used to tune the reference voltage by manipulating the value of the feedback resistor, R_{adjust} . The equation of the tuning is as shown in Eq. (4.2.9).

$$V_{ref_adjust} = \left(1 + \frac{R_2}{R_{adjust}}\right) V_{ref} \quad (4.2.9)$$

Fig. 4.11 Block diagram of the wireless power receiver with the proposed single-stage AC-DC converter.

The implementation of the controller is illustrated in Fig. 4.12. Instead of using error amplifier that requires compensator and constant power consumption as in PWM control, a comparator based feedback loop that is inherently stable [54] is used. It reduces the complexity of the design as well as minimizes the power consumption of the controller. A feedback comparator CMP_FB is utilized to compare a fraction of the output voltage VDC with a reference voltage. After each comparison is done, the comparator is shut-off to reduce the power consumption. The comparison result is stored in a flip-flop which is updated according to the system clock. The system clock will first activate the comparator circuit and after a certain delay only activate the flip-flop. This is to ensure that the correct comparison result is stored as the comparator circuit takes some time

[illegible]

The bandgap circuit is shown in Fig. 4.13. Initially the voltage VDC and node B are low, when the output voltage is being charged up, node B slowly rises up to the threshold voltage of the transistor Mn1 and the current I_{start} starts to flow and mirror to the transistor Mn2. Thus, node C is being pulled low and all the PMOS transistors are turned on. After the I_{PTAT} current is established, it is being mirrored to transistor Mp4. As a result, node A is being charged up and the transistor Mn3 is turned on, pulling node B low and switching off the start-up transistors Mn1 and Mn2. After the bandgap circuit stabilizes, the voltage

reference can be obtained by adding up the base-emitter voltage of transistor B3 and the PTAT voltage as expressed in Eq. (4.2.10).

$$V_{ref} = V_{EB} + (I_{PTAT} \times R_{ref}) \quad (4.2.10)$$

Fig. 4.13 The bandgap reference circuit.

4.3 Measurement Results and Discussions

Fig. 4.14 shows the output voltage waveforms of a typical rectifier in (a) and the proposed one-stage design in (b) during the load-step of 1 mA – 40 mA - 1 mA. The typical rectifier structure does not possess regulation capability and therefore the output voltage is fluctuating during load-step occurrence. A voltage regulator is often required to regulate the rectified voltage in a second-stage. The proposed one-stage AC-DC converter has the regulation capability and thus the output voltage is able to track the reference voltage despite the load is stepped from 1 mA to 40 mA and vice-versa.

Fig. 4.14 Simulated output voltage waveforms of (a) a typical rectifier and (b) the proposed one-stage design for load-step of 1 mA - 40 mA - 1 mA.

Table 4.1 shows the comparison of the proposed one-stage converter with the typical active rectifier structure and the voltage regulators. The proposed one-stage converter has the features of a rectifier as well as a switched-mode DC-DC converter. Compared to a typical rectifier structure which is always in constant-on operation, the proposed design operates in either ON-mode or OFF-mode with the PSM control. As result, it reduces the conduction power losses and the overall power consumption of the design. Hence, it has better efficiency with the embedded regulation features. Furthermore, the PFM control enables the reduction of switching frequency during light-load which helps to minimize the switching power losses.

Table 4.1 Comparison of the proposed design to the typical active rectifier/voltage regulators.

Topology	Features
Active Rectifier	- For AC-DC conversion without regulation capability.
LDO	- A linear regulator which consists of a pass transistor.
Inductive DC-DC converter	- A switched-mode regulator which consists of an inductor. - Power-efficient.
Proposed one-stage AC-DC converter	- Has the features of the rectifier and the DC-DC converter. - Retains the active rectifier structure but it behaves like a switched-mode DC-DC converter. - Embedded regulation capability without inductor usage.

The proposed one-stage AC-DC converter was fabricated in a standard 0.18 μm CMOS process. The chip micrograph photo of the size $1.5\text{ mm} \times 1.2\text{ mm}$ is as shown in Fig. 4.15. The total active area is 0.4246 mm^2 , in which the power transistors occupy an area of 0.2964 mm^2 and the controller takes up an area of 0.1282 mm^2 . The design has been tested at the ISM band of 125 kHz. Fig. 4.16 shows the transmitter and the receiver boards of the inductively powered system. A power amplifier is used to drive the primary side and the secondary side provides the input to the chip through inductive coupling. The coils of 4.3 cm diameter are used for the power transmission. In order to weigh the trade-offs between the voltage ripples and the capacitor value, an off-chip dc filtering capacitor of $4.7\text{ }\mu\text{F}$ is used to store the output charge. For safety purpose, zener diodes are connected externally at the input to prevent the voltage from going higher than the breakdown voltage of the 5.5 V devices.

Fig. 4.15 Chip micrograph photo of the proposed one-stage design.

As illustrated in Fig. 4.16, a sense resistor, R_{sense} is inserted into the input path to measure the input AC current I_{AC} . The input AC power is obtained by taking the average of the product of the input voltage and the input current over several period cycles. The detailed calculation of the AC input power is shown in Appendix B. The power conversion efficiency (PCE) of an AC-DC converter can be calculated from Eq. (4.3.1).

$$\eta_{AC-DC} = \frac{P_{DC}}{P_{AC}} = \frac{\frac{V_{DC}^2}{R_L}}{\frac{1}{nT} \int_{t_0}^{t_0+nT} V_{AC}(t) * I_{AC}(t) dt} \quad (4.3.1)$$

Fig. 4.17 shows the measured steady-state waveforms of input voltage, input current, output voltage and system clock at 5mA load current. The input voltage V_{AC} denotes ($V_{in+} - V_{in-}$). As can be observed, the input current is almost zero when no power transfer is required. In order to synchronize with the input frequency, the system clock frequency changes between 125 kHz (f_{in}) and 250 kHz ($2 \times f_{in}$) according to the proposed PFM algorithm. Under the conditions that no power transfer is required, the system clock frequency changes to the

minimum frequency, as shown in Fig. 4.17 in order to reduce the switching power losses and enhance the power efficiency.

Fig. 4.16 The test boards for the proposed design.

Fig. 4.17 The measured steady-state waveforms of input voltage, input current, output voltage and system clock.

To verify the modulation scheme, the converter has been tested at different load currents, such as 1 mA, 5 mA and 40 mA as shown from Fig. 4.18 to Fig. 4.20. The input voltage, output voltage and the signal ‘Mode’ waveforms at different load conditions are shown from Fig. 4.18 to Fig. 4.20. The signal ‘Mode’ in the figures represents the modulation of the conduction rate of the converter. As discussed earlier, ON-mode denotes the charging operation while OFF-mode represents the discharging operation. The frequency of the mode transition is synchronized with the system clock frequency, which is at the moment when the input current is zero to avoid any power losses. The output voltage and ‘Mode’ signal are compared among different load current scenarios. In the waveforms, ON-mode is indicated by logic ‘0’ while OFF-mode is represented by logic ‘1’. As can be seen from Fig. 4.18, OFF-mode is performed more often when the load current is 1 mA, implying that the discharging operation is executed more frequently under this light-load condition. However, as the load current increases gradually from 1 mA to 40 mA as shown from Fig. 4.18 to Fig. 4.20, ON-mode operation is executed more frequently, indicating that more power is required to be transferred to the output in order to cater for the increasing load requirements. Hence, by regulating the charging or discharging rate of the converter, the output voltage regulation is achieved successfully.

Fig. 4.18 Measure steady-state waveforms at 1mA.

Fig. 4.19 Measured steady-state waveforms at 5mA.

Fig. 4.20 Measured steady-state waveforms at 40 mA.

To further investigate the regulation capability of the proposed one-stage converter, the output load current is stepped from 1 mA to 40 mA. The regulator is able to track the reference voltage despite a load-step of 40 times is applied to it. With an output capacitor of 4.7 μF , a voltage undershoot of 200 mV is shown in Fig. 4.21 (a) during the load-step from 1 mA to 40 mA while Fig. 4.21 (b) shows a voltage overshoot of 180 mV during a load-step from 40 mA to 1 mA. The regulator takes 68 μs to recover from the voltage undershoot and it takes 290 μs to recover from the voltage overshoot.

Fig. 4.21 Measured load transient-response at zoom-in view of the proposed converter with load-step of (a) 1 mA – 40 mA, (b) 40 mA – 1 mA.

Fig. 4.22 Voltage undershoot in (a) and voltage overshoot in (b) for 3 different output capacitor values of 100 nF, 4.7 μF and 10 μF respectively.

The measurements of the voltage undershoot and overshoot have been tested with 3 different output capacitor values. The voltage undershoot is shown in Fig. 4.22(a) and the voltage overshoot is shown in Fig. 4.22(b) for the 3 different output capacitor values of 100 nF, 4.7 μF and 10 μF respectively. As the operating frequency of the design is low, a larger output capacitor value is required to suppress the voltage ripples. As can be observed from Fig. 4.22, when a smaller capacitor value (100 nF) is used, the voltage undershoot and overshoot are more obvious but the voltage ripples are larger. However, the voltage ripples are smaller when larger capacitor values (4.7 μF & 10 μF) are used. But, the voltage undershoot and overshoot are not obvious as shown in Fig. 4.22. Since the proposed regulator is meant to produce a regulated voltage with minimum ripples, a larger capacitor value is used to reduce the ripples but at the expense of not seeing the voltage-shoots clearly. In order to weigh the trade-offs between the voltage ripples and the capacitor value, a capacitor of 4.7 μF is chosen in the design.

Fig. 4.23 shows the graph of measured power conversion efficiency (PCE) against the output power. By adjusting the bandgap reference voltage, the output voltage is tested at 1.8 V and 2 V respectively. When the output voltage is changed from 2 V to 1.8 V due to the adjustment of reference voltage, the power efficiency degrades. With a lower output voltage, the on-resistance of the power transistor is higher as the gate voltage driving the transistor is lower. Hence, the power losses are higher, causing the efficiency to be lower. Measurement results show that a peak power efficiency of 93.48% is achieved at the output voltage of 2 V in an output power range of 2 mW - 80 mW. The maximum output voltage ripples is measured to be around 140 mV. Compared to the two-stage design in Chapter 3, the receiver efficiency has been improved substantially. As shown in Fig. 4.24, the efficiency can be improved by as much as 23.10%.

Table 4.2 summarizes the performance of the proposed receiver. The line and load regulation are measured to be 60 mV/V and 2.56 mV/mA respectively. The maximum link efficiency is measured to be 11.20%. The link efficiency is not yet optimized as the main focus of the work is the receiver efficiency. Table 4.3 shows the comparison between the proposed work and the relevant state-of-the-art-works. There are different active rectifier designs done at different operating frequency to cater for different load power applications. The proposed design is compared with the reference works that have the nearest possible output power range. The works in [114, 117] are designed for a maximum output power of 10 mW and their efficiency is optimized at around 4 to 5 mW whereas the work in [162] is optimized at around 65 mW for a maximum power of 102 mW. The output power range and optimal efficiency point are different for different application. The proposed work is designed for animal tracking control application with an output power up to 80 mW and the optimal efficiency is at around 50 mW. The work in [117] is designed for piezoelectric application, [113-114] are designed for biomedical implantation and [101] and [108] are used for wireless charging for portable devices. The proposed design is suitable for the

applications that are working in the ISM band of 125 kHz to 134 kHz, such as for animal tracking control to track the temperature or pressure of the animals.

The work in [43,117,121] utilizes a typical active rectifier structure that does not possess regulation capability. In order to regulate the rectified voltage, a LDO is used as in [101] and a buck converter is used in [95-97]. However, due to the two-stage design, the power efficiency is degraded. Even though the work in [114] eliminates the use of an inductor, the input voltage is rectified before supplying the two converter cores in the design. Thus, the power is still being transferred through two stages.

Fig. 4.23 Measured power conversion efficiency (PCE) versus output power at 2 V and 1.8 V output voltage.

Fig. 4.24 Comparison of efficiency between two-stage receiver and the proposed one-stage receiver.

Table 4.2 Performance Summary.

Transmitter and Receiver Coil	24 μ H/0.1 Ω @ 125 kHz
Distance between Transmitter/Receiver	0.5 cm
Output Capacitor C_L	4.7 μ F
Active area	0.425 mm ²
Load regulation ($\Delta V_{DC}/\Delta I_{LOAD}$)	2.56 mV/mA
Line regulation ($\Delta V_{DC}/\Delta V_{IN}$)	60 mV/V
Max. link efficiency (η_{LINK})	11.20%
Max. receiver efficiency ($\eta_{RECEIVER}$)	93.48%
Total efficiency ($\eta_{TOTAL}=\eta_{LINK}\times\eta_{RECEIVER}$)	10.47%

Table 4.3 Performance comparison with other state-of-the-art work.

References	TBCAS 2008 [121]	ISSCC 2010 [114]	TPEL 2011 [117]	JSSC 2013 [113]	ISSCC 2013 [100]	JSSC 2015 [162]	Proposed Work
Technology	0.5 μm CMOS	0.18 μm CMOS	Discrete	0.5 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Structure	Active rectifier	Timing AC-DC	Active voltage doubler	Adaptive output active rectifier	1X/2X Active rectifier	R ³ rectifier	One-stage AC-DC Converter
Regulation Capability	No	Yes	No	Yes	No	Yes	Yes
Chip Area (mm ²)	*0.40	*0.10	N.A	**2.25	*0.11	3.06	1.80
Frequency	125 kHz - 1 MHz	200 kHz – 3.3 MHz	20 Hz	2 MHz	13.56 MHz	13.56 MHz	125 kHz – 250 kHz
Output Voltage (V)	4.36	1.8	2.24	2.5 - 4.6	1.27 - 4	3.6	1.8 - 2.0
Max. P _{OUT}	19 mW	10 mW	10 mW	~ 13 mW	32 mW	102 mW	80 mW
Measured PCE (%)	84.80 @ 19 mW	87.10 @ 4 mW	83.00 @ 5 mW	87.00 @ 13 mW	84.20 @ 32 mW	92.60 @ 64. 8mW	81.80 @ 2 mW 87.43 @ 20 mW, 91.15 @ 30 mW, 93.48 @ 50 mW, 91.31 @ 60 mW

*Active area. **Including stimulating system.

The proposed work has adopted an energy-efficient one-stage design, achieving a peak power efficiency of 93.48% at a regulated output voltage of 2 V. In spite of the simplicity of the structure, the proposed design achieves the best power efficiency compared to the other state-of-the-art-works as shown in the Table II. In addition, it possesses a good regulation capability while having a minimal footprint in the receiver.

4.4 Power Losses Analysis

The single-stage AC-DC converter regulates the output by operating in either ON-mode or OFF-mode and the power losses in each mode can be estimated using the equations from Eq. (4.4.1) to Eq. (4.4.6).

$$P_{loss(ON-mode)} = P_{conduction\ loss(Mp\&Mn)} + P_{switching\ loss(Mp\&Mn)} + P_{leakage} \quad (4.4.1)$$

$$P_{conduction\ loss(Mp\&Mn)} = I_p \cdot V_{SD(sat)} \cdot D_{eff} + I_n \cdot V_{DS(sat)} \cdot D_{eff} \quad (4.4.2)$$

$$P_{switching\ loss(Mp\&Mn)} = (C_{gp} + C_{gn}) \cdot V_{DC}^2 \cdot f \quad (4.4.3)$$

$$P_{loss(OFF-mode)} = P_{switching\ loss(Mn)} + P_{leakage} \quad (4.4.4)$$

$$P_{losses} = P_{conduction} * (n \cdot T) + P_{switching} + P_{leakage} + P_{others}, n \geq 0 \quad (4.4.5)$$

$$P_{total_losses} = P_{losses} + P_{controller} \quad (4.4.6)$$

During ON-mode, the power losses are dominated by the conduction loss and the switching loss of the power switches. D_{eff} is the effective duty cycle of the regulator, which is the conduction time over period. During OFF-mode, the power loss includes the switching loss of the low-side switches and the leakage power loss. Under OFF-mode, none of the switches conducts and therefore the conduction loss can be minimized. In addition, the operating frequency f will be reduced to half during light-load or when no power transfer is required. Hence, the switching loss can be minimized as well. $P_{controller}$ is the power consumption of the controller, $P_{leakage}$ is the transistors' leakage power loss and P_{others} includes the bonding wires conduction loss, PCB traces power loss, etc.

The total power loss of the single-stage AC-DC converter is compared with the total power loss of the active rectifier in Chapter 3.

Fig. 4.25 Power loss comparison between single-stage AC-DC converter in (a) and active rectifier in (b).

As shown in Fig. 4.25, compared to the active rectifier at the same output power, the total power losses can be reduced by as much as 64.30%. This is because the active rectifier is in constant conduction mode at a fixed frequency without regulating the output voltage. In contrast, the single-stage work operates in switched-mode and skips the power conduction (in OFF-mode) when necessary to reduce the conduction loss. Instead of operating at a fixed frequency, the single-stage design works with dual-frequency. The frequency is reduced to half when no power transfer is required to minimize the switching loss. Thus, the overall power loss of the single-stage design is reduced as compared to the active rectifier.

4.5 Discussion and Conclusions

This chapter presents a one-stage AC-DC converter for inductively powered applications, such as in RFID and IMD. The proposed converter has improved the power conversion efficiency from a typical two-stage design to a one-stage design. In addition, it minimizes the cost and footprint of the receiver by omitting

the use of an inductor from the design. The unique modulation scheme implemented has successfully regulated the output voltage across a wide load range. Owing to the energy-efficiency modulation technique, a peak power efficiency of 93.48% is achieved in an output power range of 2 to 80 mW. The proposed work is suitable for the applications that require minimal footprint while operating in the range of mW power at the ISM band of 125 kHz to 134 kHz, such as for RFID animal tag or biomedical implantation. The proposed work is applicable to higher voltage applications as well provided if the voltage level is within the allowable voltage limit of the CMOS process.

However, the design is limited to only one regulated output voltage. It may not be sufficient for a system that requires more than one regulated output voltage. Therefore, to overcome the limitation, the one-stage design concept can be extended to multiple-output structure as well. Thus, the single-stage design with two or more outputs will be presented and discussed in Chapter 5.

Chapter 5 Design of Single-Stage Dual-Output AC-DC Converter

In this chapter, the design of a single-stage dual-output AC-DC converter will be presented. The concept and working principle of the single-stage multiple-output architecture will be introduced. As a proof of concept, the single-stage dual-output design is implemented and its topology as well as its implementation method will be explained. Eventually, measurement results are shown and compared to the state-of-the-art work at the end of the chapter.

5.1 Introduction

Fig. 5.1 Block diagram of an inductively powered WPT system with the typical two-stage design and the proposed SSMO design.

In order to maximize the circuit performances and minimize the overall power consumption, more than one independent regulated output voltage is often required to cater for different sub-modules in a system. For example, the multiple-supply can be used to supply the sensor circuits and memory blocks in

a RFID animal tag or the analog, digital or RF functional blocks for biomedical implant applications. The typical two-stage implementation which consists of a rectifier and a multiple-output DC-DC converter (shown in Fig. 5.1) limits the overall power conversion efficiency of the receiver. The multiple-output DC-DC converter can be implemented in several ways, such as having multiple independent switching converters, as described in [163]. However, having multiple independent switching converters would increase the use of inductor which is undesirable. To reduce the footprint of the receiver, a single-inductor-multiple-output (SIMO) [164-166] is used to replace multiple independent switching converters in [163]. Nevertheless, the cross regulation problem exists in SIDO design as one inductor is being shared by multiple-output. Due to the sharing of the inductor current between various loads, the load change at one output will cause instability of voltage at another output due to insufficient or excess charge. To mitigate the problem, time-multiplexing control and ordered power distributive control are employed to minimize the error of the energy transfer. However, both of the controls are still susceptible to cross regulation problem when one of the loads draw more energy than the others [61-62], [58, 64]. The multiple-output LDO (MOLDO) is proposed in [167] to cater for multiple LDO outputs. Nonetheless, the use of LDO requires a rectifier stage for rectification before the regulation and the power losses incurred from the two-stage will degrade the power efficiency. Table 5.1 shows the comparison between different existing implementation methods and the proposed architecture in terms of the power transistor count and the number of power conversion stages for a dual-output design. For a typical two-stage implementation, a rectifier consists of four power transistors. As can be inferred from Table 5.1, the proposed structure utilizes the least number of power transistors and the power conversion is done in only one-stage.

Recent work [168] has adopted a 2X active rectifier and a three-level single-inductor dual-output dc-dc converter. But the power conversion is still done in two-stage. Even though there are numerous works that focus on implementing

the power conversion in one-stage [106-112], they are operated for only one-output. Hence, they are not supportive for applications that require more than one supply voltage.

Table 5.1 Existing methods Vs the proposed architecture for (N=2)

	Rectifier + 2-switching converters	Rectifier + SIDO	Rectifier + dual-output LDO	Proposed SSDO AC-DC structure
No. of power conversion stages	2	2	2	1
Power transistor count	4+4=8	4+4=8	4+3=7	6
Inductor count	2	1	0	0

5.2 The proposed single-stage multiple-output AC-DC converter

5.2.1 Proposed Architecture

To tackle the issue, the concept of the single-stage topology in Chapter 4 can be extended for multiple-output functions. Due to the simplicity of the structure, multiple-output can be integrated easily by adding two additional high-side power switches for each output. The proposed extended architecture is able to rectify and regulate two or more output voltages simultaneously in a single-stage efficiently. Fig. 5.2 shows the proposed extended topology for multiple-output. The proposed architecture consists of $2(N + 1)$ power transistors and N output capacitors for N outputs, where $N \geq 1$ (shown in Table 5.2).

In addition, a multi-mode controller is also proposed to control the multiple switches of the structure efficiently. By taking into account of the multiple-output configuration, the multi-mode controller is able to work in $(N + 1)$ modes to

cater for N outputs (shown in Table 5.3), in which N-mode is used to charge up the N-output and one discharging mode.

Fig. 5.2 The proposed SSMO AC-DC regulator topology with the multi-mode controller.

Table 5.2 Component counts of the topology for N outputs

No. of outputs	No. of power transistors	No. of output capacitors
1	4	1
2	6	2
3	8	3
$\vdots$	$\vdots$	$\vdots$
N	$2(N + 1)$	N

Table 5.3 Multi-mode operations of the controller.

No. of outputs	No. of Modes	Operations
1	2	1 charging mode + 1 discharging mode
2	3	2 charging modes for dual-output + 1 discharging mode
3	4	3 charging modes for dual-output + 1 discharging mode
$\vdots$	$\vdots$	$\vdots$
N	$N + 1$	N charging modes for N -output + 1 discharging mode

5.2.2 Working Principles for (N=2)

As a proof of concept, the tri-mode dual-output (N=2) design is implemented. As such, only the detailed of the tri-mode controller is discussed in this chapter. However, due to the flexible nature of the controller, the concept is the same and extendable to (N+1) modes for N outputs. However, an increase in the number of outputs will cause each individual output to have lesser output power as the total sum of the output power is the same.

For the dual-output tri-mode topology as shown in Fig. 5.3, there are six power transistors, in which the high-side power switches P_1 and P_2 are used for charging the output voltage V_{o1} while P_3 and P_4 are used for charging the output voltage V_{o2} and the low-side power switches N_1 and N_2 are shared by both outputs. Instead of charging up multiple-output at the same time which will increase the input current to incur extra power losses, the topology is configured into a single-output active rectifier configuration by operating in different modes as shown in Figure 5.3.

Fig. 5.3 The tri-mode configuration of the proposed SSDO AC-DC regulator.

Table 5.4 The control logic and the operations of the tri-mode controller.

Type of Modes	S ₁	S ₂	Output V _{o1}	Output V _{o2}	ON	OFF
Mode ₁	0	1	Charging	Discharging	(P ₁ & N ₂) / (P ₂ & N ₁)	P ₃ & P ₄
Mode ₂	1	0	Discharging	Charging	(P ₃ & N ₂) / (P ₄ & N ₁)	P ₂ & P ₁
Mode ₃	1	1	Discharging	Discharging	N ₁ / N ₂	P ₁ to P ₄

As shown in Table 5.4, the tri-mode controller is designed to work in Mode₁, Mode₂ or Mode₃, in which Mode₁ and Mode₂ are the discharging operation for V_{o1} and V_{o2} respectively and Mode₃ represents the discharging operation for both outputs. The dual-output are time-shared in one cycle and thus they regulated in each half-cycle respectively. The time-sharing controller ensures that only one-output is activated during each half-cycle by reconfiguring the topology into a single-output active rectifier structure (shown in Fig. 5.3). The regulation scheme utilized for the dual-output is pulse skipping modulation (PSM) as discussed in Chapter 4. To regulate the outputs, the structure will work in either charging or discharging operation, depending on the load requirements. As shown in Table 4.1 (in Chapter 4), the proposed topology behaves like a switched-mode DC-DC converter. Moreover, the control scheme is simple which utilizes comparators

instead of error amplifier which requires compensation circuits. Hence, it reduces the complexity of the entire system.

To explain the operations, the clock cycle is divided into even cycle and odd cycle. In even cycles, the first output V_{o1} is activated or enabled and the second output V_{o2} is activated or enabled in odd cycles. In even cycles, when the output V_{o1} is enabled, the output V_{o2} will enter discharging operation by turning off the switches P_3 and P_4 and the output V_{o2} is sustained by the output charge in C_{L2} . The output V_{o1} is compared with its reference voltage V_{REF1} to determine whether a charging or a discharging operation is required. If V_{o1} falls below V_{REF1} , indicating that power transfer is required by the load and thus charging operation will be executed (shown in Case1). If the input node V_{in+} is greater than V_{o1} , then the switches P_1 and N_2 will be turned on to charge up the output V_{o1} . The switches P_2 and N_1 will be turned on if the input node V_{in-} is greater than V_{o1} . In contrast, if V_{o1} is greater than V_{REF1} , implying that the output does not require power transfer and thus the discharging operation will be implemented by turning off the switches P_1 and P_2 as shown in Case 3.

Similarly, during odd cycles, when the output V_{o2} is enabled, the output V_{o1} will enter discharging operation by turning off the switches P_1 and P_2 and the output V_{o1} is sustained by the charge in the output capacitor C_{L1} . The output V_{o2} is compared with its reference voltage V_{REF2} to determine its mode operation. If V_{o2} falls below its reference voltage V_{REF2} , then the charging operation will be executed (shown in Case 2). If the input node V_{in-} is greater than V_{o2} , then the switches P_4 and N_1 will be turned on to charge up the output V_{o2} . The switches P_3 and N_2 will be turned on if V_{in+} is higher than V_{o2} . On the other hand, if V_{o2} is detected to be above its reference voltage, then the discharging operation will be implemented by turning off the switches P_3 and P_4 as shown in Case 3.

In Mode3, both of the outputs enter discharging operation and the switches P_1 to P_4 are turned off while one of the low-side switches (either N_1 or N_2) is turned on (depending on input nodes V_{in+} and V_{in-}). For example, when V_{in+} is higher than the threshold voltage of N_2 , N_2 will be turned on and the node V_{in-} is

clamped to ground. On the other hand, when V_{IN-} is greater than the threshold voltage of N_1 , N_1 will be turned on and the node V_{IN+} will be clamped to ground. Mode₃ is similar to the OFF-mode configuration as described in Section 4.2.3 in Chapter 4. Under this condition, there is no electrical connecting path between the input source and the outputs. Hence, there is no input current I_{AC} flows to charge up the outputs. Thus, the outputs are sustained by the charge in their respective output capacitors ($C_{L1, 2}$). Under heavy-load conditions where both of the outputs require power transfer, the output V_{o1} will be charged up in the even cycles and the output V_{o2} will be charged up in the odd cycles alternatively. Dynamic body bias (DBB) circuits are used to tie the body of all the high-side power switches to the highest voltage and therefore to prevent latch-up [152].

To gain an insight of how the architecture works, the timing diagram and the control switches function are illustrated in Fig. 5.4. The control signals S_1 and S_2 represent the modulation of the charging and discharging operation of the outputs V_{o1} and V_{o2} respectively, in which S_1 controls the switches P_1 and P_2 while S_2 controls the switches P_3 and P_4 . A logic ‘0’ of S_1 or S_2 represents the charging operation while a logic ‘1’ denotes the discharging operation (as shown in Fig. 5.3). To ensure that the switching occurs only at the zero-current moment of the input current I_{AC} , the switching frequency is required to be synchronized with the input frequency f_{in} . Hence, a system clock of twice of the input frequency ($2 \times f_{in}$) is generated from the input AC voltages.

Fig. 5.4 Timing diagram of the proposed tri-mode dual-output controller.

As shown in Fig. 5.4, the system clock is divided into odd and even cycles. The output V_{o1} is activated during even cycles and the output V_{o2} is activated during odd cycles alternatively. When EN1 is of logic ‘high’ (during even cycles), the load condition of output V_{o1} is checked to determine whether a charging or a discharging operation is required. Similarly, when EN2 is logic ‘high’ in odd cycles, the output V_{o2} is activated and a periodical checking is done on the load R_{L2} to determine whether a charging or a discharging operation will be implemented. When no power transfer is required by both of the outputs, the outputs enter discharging operation and the input current is almost zero as illustrated by Mode₃ in Fig. 5.4.

Fig. 5.5 shows the flow chart that summarizes the tri-mode dual-output control sequence. As discussed earlier, the dual-output are regulated in even and odd cycles alternatively. With the proposed time-sharing controller, the voltage rectification and regulation for dual-output are achieved simultaneously in one-stage at minimal power consumption.

Fig. 5.5 Flow chart describing the control sequence and operation of the tri-mode dual-output controller.

5.2.3 Start-up Mechanism

Fig. 5.6 Parasitic capacitances of P₁ and P₃ during start-up.

Parallel self-startup mechanism is embedded in the proposed architecture. A reset pulse is used to trigger the signal $S_{1,2}$ to zero, enabling the structure to work in a passive diode configuration during start-up. During start-up, the output V_{o1} and V_{o2} are equal to zero, the parasitic capacitances of the power switches P₁ and P₃ and their V_{sg} voltages can be modeled as in Fig. 5.6. As the input voltage V_{in+} slowly rises up, the V_{sg} of the power transistors increase as well and eventually they will become greater than the threshold voltage of the power transistors. Thus, the power transistors P₁ and P₃ will act as passive diode to charge up the outputs respectively. Similarly, for the negative cycles, transistors P₂ and P₄ will act as passive diode to charge up the outputs. When the outputs are charged up to a voltage level that is sufficient for the controller to operate, the switches P₁ to P₄ will be controlled by the proposed tri-mode dual-output controller. Both of the outputs are charged up to their respective reference voltage values in alternate cycles. Fig. 5.7 shows the simulated waveforms during parallel start-up.

Fig. 5.7 Simulated waveform during start-up.

5.2.4 Mathematical Analysis of SSDO Tri-mode AC-DC Converter

Fig. 5.8 The on-resistances modeling of the regulator and its associated waveform in one cycle time T .

During each conduction period, only one low-side switch and one high-side switch are turned on, behaving like a single-output active rectifier. The on-resistances of the switches can be modeled as in Fig. 5.8. $R_{on,p}$ and $R_{on,n}$ are the on-resistances of the PMOS and NMOS switches respectively. $C_{L,i}$ denotes the

output dc filtering capacitor while $R_{L,i}$ represents the output load. The switches operate in triode region and therefore the voltage drop can be minimized. Similar to the single-stage AC-DC converter in Chapter 4, the criterion for the design to function normally is that the input amplitude has to be greater than the turn-on voltage drop of both of the switches, which is as shown in Eq. (5.2.1).

$$|V_{AC}| > V_{ds,p} + V_{ds,n} \quad (5.2.1)$$

Assuming that the positive and negative half cycles are symmetrical and during each conduction cycle, the regulator conducts the same conduction time of (t_2-t_1) in each half cycle. Under steady-state, the total input charge supplied and the total output charge can be expressed as in Eq. (5.2.2) and (5.2.3) respectively.

$$Q_{in} = 2 \times \int_{t_1}^{t_2} \frac{V_{AC} \sin \omega t - V_{o,i}}{R_{ds,i}} dt \quad (5.2.2)$$

$$Q_{out} = \int_0^{n \cdot T} \frac{V_{o,i}}{R_{L,i}} dt = \frac{V_{o,i}}{R_{L,i}} (n \cdot T), n \geq 1 \quad (5.2.3)$$

By applying the theory of conservation of charge, the total input and output charge are equated and the output voltage $V_{o,i}$ can be expressed as in Eq. (5.2.4), where $n_i \cdot T$ is the rate of the discharging operation of the outputs.

$$V_{o,i} = \frac{\frac{V_{AC} \cdot T}{\pi} \left[\cos \frac{2\pi}{T} t_1 - \cos \frac{2\pi}{T} t_2 \right]}{2 \cdot (t_2 - t_1) + \frac{R_{ds}}{R_{L,i}} (n_i \cdot T)}, n_i \geq 1, i = 1, 2 \quad (5.2.4)$$

As can be inferred from Eq. (5.2.4), under light-load condition, $R_{L,i}$ increases to conduct lesser load current. In order to keep the output voltage, $V_{o,i}$ constant, the term $n_i \cdot T$ has to be increased as well, implying that the discharging operation will be executed more frequently. In contrast, when $R_{L,i}$ decreases under heavy-load conditions, the rate of discharging mode has to be reduced by increasing the rate of charging in order to keep the output regulated. Thus, by modulating the rate of the discharging mode, the dual-output voltage regulation is achieved across a wide load range.

Under steady-state, the voltage drop due to the ESR of the output capacitor $C_{L,i}$ and the discharging of $C_{L,i}$ into the load $R_{L,i}$ contribute to the output voltage ripples. Hence, the output voltage ripples can be approximated as in Eq. (5.2.5).

$$\Delta V_{ripples,i} \approx I_{o,i} \cdot R_{ESR} + V_{o,i} \cdot \left(1 - e^{\frac{-n_i \cdot T}{R_{L,i} C_{L,i}}} \right), i = 1, 2 \quad (5.2.5)$$

As can be seen from Eq. (5.2.5), the output voltage ripples can be reduced by increasing the output capacitor value or the operating frequency.

5.2.5 Implementation of key circuit blocks

Fig. 5.9 Block diagram of the WPT system with the proposed Single-stage dual-output tri-mode wireless receiver.

Fig. 5.9 shows the block diagram of the wireless power receiver with the proposed single-stage dual-output (SSDO) tri-mode AC-DC converter. The tri-mode controller enables the structure to operate in 3-mode, namely Mode₁, Mode₂ and Mode₃. The power stage can be reconfigured into a single-output configuration (as shown in Fig. 5.3) in order to regulate each output alternatively. The regulation scheme utilized is pulse skipping modulation. It is done by modulating the charging and discharging rate of the outputs. Each output is regulated in each half-period. Mode₁ and Mode₂ represent the charging operation for outputs V_{o1} and V_{o2} respectively while Mode₃ is the discharging operation.

The enabled signals EN1 and EN2 are utilized to activate both outputs on alternate cycles. Two feedback comparators C_{FB1} and C_{FB2} are used to compare a fraction of the output voltages V_{o1} and V_{o2} with their reference voltages V_{REF1} and V_{REF2} respectively. The comparison results are stored in the flip-flops which are updated according to the system clock E_{clk1} and E_{clk2} in even and odd cycles respectively. The tri-mode control scheme is realized by the mode selection blocks which produce the selection signals S_1 and S_2 to control the switches P_1 to P_4 based on the load conditions information $Q_{A,B}$. The load conditions information is obtained from the outputs of the feedback comparators (C_{FB1} and C_{FB2}) periodically. The implementation concept is extendable to more number of outputs by having more bits of signals selection.

(a)

EN_i	$V_{o,i} > V_{ref,i}$ (Q_i)	S_i
0	0	1
0	1	1
1	0	0
1	1	1

$i = 1, 2$ (dual-output)

Fig. 5.11 Mode Selection block: (a) Logic implementation and (b) Circuit implementation.

Fig. 5.11 shows the logic and circuit implementation of the mode selection block. If EN_i is '1', it denotes the output is enabled and the signal S_i will decide whether it is in the charging mode (Mode₁ or Mode₂) or the discharging mode (Mode₃) based on the loads condition information Q_i . A logic '0' of S_i represents a charging operation will be implemented while a logic '1' implies that

discharging operation will be executed. As illustrated in the truth table in Fig. 5.11, if EN_i is '1' and Q_i is '0', it represents charging operation is required while a logic '1' of Q_i denotes discharging operation. On the other hand, the output is disabled when EN_i is '0' and the S_i signal will remain at '1' to skip the switching activity. Hence, by modulating the charging and discharging modes of the outputs, the voltage regulations are achieved successfully.

5.3 Measurement Results and Discussion

Fig. 5.12 Chip micrograph photo of the proposed SSDO tri-mode AC-DC regulator.

The proposed SSDO tri-mode AC-DC regulator has been implemented and fabricated in a standard $0.18\ \mu\text{m}$ CMOS process. The chip micrograph photo of the design is shown in Fig. 5.12. The total active area of the design is $0.63\ \text{mm}^2$, in which the high-side power switches (P_1 - P_4) and low-side power switches (N_1 - N_2) occupy an area of $0.39\ \text{mm}^2$ while the proposed time-sharing tri-mode controller, active diode comparators and gate drivers use up an area of $0.24\ \text{mm}^2$. The chip is packaged in a 64-pin QFN package. The proposed design is tested at the ISM frequency band of 125 kHz and the test setup is illustrated in Fig. 5.13. The primary and secondary coils of 4.3 cm diameter are used for power

transmission. A power amplifier of 1 MHz bandwidth is used to drive the primary side and the secondary side provides the input to the chip through inductive coupling. Each of the output utilizes an off-chip dc filtering capacitor of 10 μ F. For input current measurement, a sense resistor R_{sense} is inserted in the input path. The total input AC power is calculated by taking the average of the product of the input voltage and input current over several period cycles. The detailed calculation for AC power is shown in Appendix B. For safety purpose, zener diodes are used at the input to avoid the induced AC voltage from going higher than the breakdown voltage of the 5.5 V devices. The power conversion efficiency (PCE) of the design can be obtained by taking the ratio of the total dc output power to the total input AC power, as expressed in Eq. (5.3.1), where $V_{AC}(t) = V_{in+} - V_{in-}$.

$$\eta_{SSDO (regulator)} = \frac{\sum_{i=1}^2 \frac{V_{oi}^2}{RL_i}}{\frac{1}{nT} \int_{t_0}^{t_0+nT} V_{AC}(t) \cdot I_{AC}(t) dt} \times 100 \quad (5.3.1)$$

Fig. 5.13 Test measurement setup for the proposed design.

Fig. 5.14 Measured steady-state waveforms of output voltages V_{o1} and V_{o2} at 2 V and 1.8 V and their respective mode selection signals S_1 and S_2 with: (a) Both output currents at 1 mA ($P_{OUT}=3.8$ mW). (b) V_{o1} at 10 mA and V_{o2} at 20 mA ($P_{OUT}=56$ mW). (c) Both outputs at 30 mA ($P_{OUT}=114$ mW).

Fig. 5.15 Measured steady-state waveforms of input voltage, selection signals, input current and dual-output voltages at 2 V and 1.8 V respectively with total output power of (a) 28 mW. (b) 3.8 mW. (c) 114 mW.

Fig. 5.14 shows the measured transient waveforms of the dual-output V_{o1} and V_{o2} their respective selection signals S_1 and S_2 . The selection signals indicate the modulation of the charging and discharging operations of the outputs. As discussed before, a logic '0' of S_1 represents the charging operation for output V_{o1} and a logic '0' of S_2 denotes the charging operation for output V_{o2} . The discharging operation is indicated by a logic '1' of S_1 or S_2 . The tri-mode operations can be identified from the selection signals S_1S_2 , in which a '01' denotes Mode₁, '10' represents Mode₂ and '11' indicates Mode₃ (listed in Fig. 5.3). As illustrated in Fig. 5.14, when the output power increases gradually from 3.8 mW in (a) to 114 mW in (c), the charging operation (Mode₁ or Mode₂) is increased gradually as well in order to cater for the increasing load requirements.

Fig. 5.15(a) shows that I_{AC} flows only during charging occurrence (either Mode₁ or Mode₂) and each time only one output is enabled, which is in agreement with the proposed time-sharing concept. During Mode₃ when both outputs are in the discharging operation, there is no electrical connecting path for the input source to flow to the outputs and therefore the I_{AC} is almost zero under this mode. Fig. 5.15 (b) and (c) show the measured steady-state waveforms of the input voltage V_{AC} , input current I_{AC} and the dual-output voltages V_{o1} and V_{o2} at 2 V and 1.8 V respectively under light-load and heavy load respectively. When both of the outputs are in light-load conditions with a total output power of 3.8 mW, as illustrated in Fig. 5.15 (b), it can be observed that I_{AC} is equal to zero most of the time. It implies that switching activity is skipped frequently under this condition. However, as the output power increases from light-load to heavy-load conditions, as shown in Fig. 5.15(c), I_{AC} flows to charge up the outputs more often in order to cater for the heavy-load requirements.

Fig. 5.16 and Fig. 5.17 show the selection signals and the output voltages waveforms during the transition of output power from 3.8 mW to 114 mW and from 114 mW to 3.8 mW respectively.

Fig. 5.16 The measured waveforms when the output power is changing 3.8 mW (both outputs at 1 mA) to 114 mW (both outputs at 30 mA) with $V_{o1}=2$ V and $V_{o2}=1.8$ V.

Fig. 5.17 The measured waveforms when the output power is changing from 114 mW (both outputs at 30 mA) to 3.8 mW (both outputs at 30 mA) with $V_{o1}=2$ V and $V_{o2}=1.8$ V.

Fig. 5.18 The measured input and output waveforms when during the transition of output power from 3.8 mW (both outputs at 1 mA) to 114 mW (both outputs at 30 mA) with $V_{o1}=2$ V and $V_{o2}=1.8$ V.

Fig. 5.19 The measured input and output waveforms when during the transition of output power from 114 mW (both outputs at 30 mA) to 3.8 mW (both outputs at 1 mA) with $V_{o1}=2$ V and $V_{o2}=1.8$ V.

As expected, the switching activity increases when the output power is increased from light-load (3.8 mW) to heavy-load (114 mW) as shown in Fig. 5.16 and the switching activity is reduced with the discharging operation implemented more frequently when the output power is decreased from 114 mW to 3.8 mW as shown in Fig. 5.17. Fig. 5.18 and Fig. 5.19 show the input and output waveforms during the load transition. As can be seen, during light-load (3.8 mW), there is no input current I_{AC} flowing most of the time. I_{AC} flows more often when the output power increased to 114 mW, implying that charging operation is implemented more frequently to cater for the heavy-load requirement.

In order to investigate the regulation capability of the SSDO tri-mode AC-DC regulator, the load-steps are applied to the design. Fig. 5.20 shows the waveform when both V_{o1} and V_{o2} are stepped from 1 mA to 30 mA (from light to heavy) simultaneously. The undershoot voltages for V_{o1} and V_{o2} are approximately 140 mV and 160 mV respectively. When both loads are stepped together, the switching operation for both outputs increases in order to cater for the loads' requirement and hence it causes more ripples compared to the time when only single load step occurs. Fig. 5.21 and Fig. 5.22 show the waveforms when one output is under load-step transient of 1 mA - 30 mA, the other output is under a constant load current of 1 mA. Fig. 5.21 shows the load transient waveforms when the load of V_{o2} is fixed at 1mA and the load of V_{o1} is stepped up from 1 mA to 30 mA in (a) and in (b) the load is stepped down from 30 mA to 1mA. It takes 65 μ s to recover from the undershoot voltage of 140 mV and it takes 395 μ s to recover from the overshoot voltage of 90 mV. Fig. 5.22 shows the load transient waveforms when the load of V_{o1} is fixed at 1 mA and the load of V_{o2} is stepped up from 1 mA to 30 mA in (a) and it is stepped down from 30 mA to 1 mA in (b). The output V_{o2} takes 64 μ s to recover from the undershoot voltage of 140 mV and it takes 540 μ s to recover from the overshoot voltage of 100 mV. From both cases, it can be seen that the load-step transient of one output does not affect the steady-state operation of the other output. The load-step transient only causes the expected undershoot voltage in the corresponding output and it does not interfere

with the steady-state operation of another output. Therefore, it is still considered to have no cross regulation although the increased of switching operation causes more ripples during the time when both load-step happen together. Both of the output voltages are able to track their respective reference value despite a load-step of 30 times is applied to them.

Fig. 5.20 Both V_{o1} and V_{o2} are stepped from light to heavy (1 mA to 30 mA) simultaneously.

Fig. 5.21 The measured load transient response at zoom-in view for V_{o1} at 2 V and V_{o2} at 1.8 V with V_{o2} at 1 mA when (a) the load of V_{o1} is stepped 1 mA - 3 mA, (b) the load of V_{o1} is stepped 30 mA - 1 mA.

Fig. 5.22 The measured load transient response at zoom-in view for V_{o1} at 2 V and V_{o2} at 1.8 V with V_{o1} at 1 mA when (a) the load of V_{o2} is stepped 1 mA – 30 mA, (b) the load of V_{o2} is stepped 30 mA – 1 mA.

The measured power conversion efficiency against the total output power for $V_{o1}=2$ V, $V_{o2}=1.8$ V and $V_{o1}=2$ V, $V_{o2}=1.6$ V is plotted as shown in Fig. 5.23. The simulated PCE is included as reference. The simulated PCE is based on ideal cases without the layout parasitic extraction. The measured PCE is lower than the simulated PCE due to power losses incurred from process variation, layout parasitic, the package bonding wires, PCB traces, etc. A measured peak power

efficiency of 91.68% is achieved in an output power range of 3.8 mW - 114 mW for dual-output voltages at 2 V and 1.8 V while a measured peak power efficiency of 80.40% is obtained in an output power range of 3.6 mW – 108 mW for dual-output voltages at 2 V and 1.6 V. The efficiency decreases for 2 V and 1.6 V outputs as the on-resistance increases due to decreased gate overdrive voltage. The performance summary is shown in Table 5.5. The link efficiency is measured to be 27.17% and it still hasn't been optimized as the aim focus of the work is to improve the receiver efficiency with multiple-output functions. Table 5.6 shows the comparison between the proposed work and the state-of-the-art work. The proposed work is compared with the reference works that have the nearest possible output power or the same frequency. The designs in [170-171] operate at the same frequency as the proposed work while the works in [3, 100, 113 and 115] have the nearest output power as the proposed work. As they are designed for different maximum output power, their optimal efficiency point is different from the proposed work. Compared to the state-of-the-art works, the proposed SSDO AC-DC converter is able to regulate dual-output voltages in a single-stage with a peak efficiency of 91.68%. The proposed design regulates dual-output in a single-stage instead of two-stage. For instance, compared to the 2-stage work in [3,100 and 115], the proposed work transfers AC power to DC power in a single-stage and therefore the power losses are reduced from 2-stage to one-stage. Thus, the power efficiency can be improved greatly. The switched-mode operation and the single-stage feature are the main contributors for the superior power efficiency.

Fig. 5.23 The measured PCE versus output power for dual-output at $V_{o1}=2$ V, $V_{o2}=1.8$ V and $V_{o1}=2$ V, $V_{o2}=1.6$ V.

Table 5.5 Performance summary of the proposed SSDO Tri-mode AC-DC converter.

Transmitter and Receiver Coil	24 μ H/0.1 Ω @ 125 kHz
Distance between Transmitter/Receiver	0.5 cm
Output Capacitor C_{L1}	10 μ F
Output Capacitor C_{L2}	10 μ F
Active area	0.63 mm ²
Load regulation ₁ ($\Delta V_{o1}/\Delta I_{LOAD1}$)	2.41 mV/mA
Load regulation ₂ ($\Delta V_{o2}/\Delta I_{LOAD2}$)	2.75 mV/mA
Max. link efficiency (η_{LINK})	27.17%
Max. receiver efficiency ($\eta_{RECEIVER}$)	91.68%
Total efficiency ($\eta_{TOTAL}=\eta_{LINK}\times\eta_{RECEIVER}$)	24.91%

Table 5.6 Performance comparison with state-of-the-art work.

	JSSC [170] 2013	ETPEL [171] 2015	Proposed Work	ISSCC [100] 2013	TPEL [3] 2011	JSSC [113] 2013	TVLSI [115] 2016
Technology	0.18 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.35 μ m CMOS	Discrete TLV3702	0.5 μ m CMOS	0.35 μ m CMOS
Structure	Inductor- based current rectifier	Inductor- based current rectifier	SSDO Tri- mode AC-DC Regulator	1X/2X Active rectifier	Active voltage doubler	Adaptive Output Active Rectifier	2 $\times$ /4 $\times$ AC-DC regulator
No. of regulated outputs	0	0	2	1	0	1	1
No. of power conversion stage	1	1	1	1	1	1	2
Active area (mm ²)	0.26	0.26	0.63	0.11	N/A	0.30	*2.72
Operating Frequency	125 kHz	125 kHz	125 kHz	13.56 MHz	20 Hz	2 MHz	1 MHz
Maximum P _{OUT} (mW)	0.224	0.557	114	32	49	13	20
Output Voltage (V)	1 - 1.5	1 - 1.8	1.6 - 2	1.27 - 4	2.24	2.5 - 4.6	4.4
Measured PCE (%)	82.00 @ 224 μ W	84.00 @ 450 μ W	75.98 @ 11.80 mW 83.61 @ 21.80 mW 88.90 @ 29.00 mW, 91.00 @ 35.40 mW, 91.68 @ 41.80 mW, 87.10 @ 49.00 mW	84.20 @ 32 mW	83.00 @ 49 mW	87.00 @ 13 mW	88.50 @ 6.6 mW

*Including stimulating system.

5.4 Power Losses Analysis

The single-stage dual-output converter utilizes a tri-mode controller to regulate the two output voltages. During the conduction mode (Mode₁ and Mode₂), the power losses are the conduction loss, switching loss and leakage power loss. On the other hand, during OFF-mode (Mode₃), the power losses are the switching loss and leakage power loss. The power loss of the tri-mode (which are Mode₁, Mode₂ and Mode₃) can be summarized as shown from Eq. (5.4.1) to Eq. (5.4.7).

$$P_{loss(Mode1)} = P_{conduction\ loss(Mp\&Mn)} + P_{switching\ loss(Mp\&Mn)} + P_{leakage} \quad (5.4.1)$$

$$P_{loss(Mode2)} = P_{conduction\ loss(Mp\&Mn)} + P_{switching\ loss(Mp\&Mn)} + P_{leakage} \quad (5.4.2)$$

$$P_{conduction\ loss(Mp\&Mn)} = I_p \cdot V_{SD(sat)} \cdot D_{eff} + I_n \cdot V_{DS(sat)} \cdot D_{eff} \quad (5.4.3)$$

$$P_{switching\ loss(Mp\&Mn)} = (C_{gp} + C_{gn}) \cdot V_{DC}^2 \cdot f \quad (5.4.4)$$

$$P_{loss(OFF-mode)} = P_{switching\ loss(Mn)} + P_{leakage} \quad (5.4.5)$$

$$P_{losses} = P_{conduction} * (n \cdot T) + P_{switching} + P_{leakage} + P_{others}, n \geq 0 \quad (5.4.6)$$

$$P_{total_losses} = P_{losses} + P_{controller} \quad (5.4.7)$$

D_{eff} is the effective duty cycle of the regulator, which is the conduction time over period. Similar to the single-stage design in Chapter 4, the regulator operates in OFF-mode when necessary when to reduce the conduction power loss. The

power losses estimation for the dual-output of $V_{o1}=2\text{ V}$, $V_{o2}=1.8\text{ V}$ and $V_{o1}=2\text{ V}$, $V_{o2}=1.6\text{ V}$ at a same output power of 40mW are shown in Fig. 5.23.

Fig. 5.24 Power losses estimation for the dual-output of (a) $V_{o1}=2\text{ V}$, $V_{o2}=1.8\text{ V}$ and (b) $V_{o1}=2\text{ V}$, $V_{o2}=1.6\text{ V}$.

As shown in Fig. 5.23, the power losses for the dual-output of 2 V and 1.6 V are higher compared to the dual-output of 2 V and 1.8 V. It is due to higher $V_{SD(sat)}$ drop across the high-side switch and results in higher conduction loss and thus the overall power losses are higher.

5.5 Discussion and Conclusion

This chapter presents a novel single-stage dual-output tri-mode AC-DC regulator for RFID or IMD applications. The benefit of the design is that it enables dual-output voltages to be regulated simultaneously while executing the power conversion in a single-stage. Thanks to the proposed work, the power efficiency has been improved significantly and it makes the integration of a SoC becomes a lot easier by eliminating the use of inductor. The design has been fabricated in 0.18 μm CMOS process. The 2 V output voltage can be used for rechargeable battery and the lower output voltage of 1.8 V or 1.6 V can be used

to supply functional blocks such as for analog/digital/RF modules. The proposed design maximizes the performances of embedded applications that require more than one supply voltage.

However, the designs from Chapter 3 to Chapter 5 require the input voltage amplitude to be greater than the regulated output voltage in order for them to work well. To solve the restriction, the single-stage design concept can be applied to a voltage doubler structure as well. Hence, Chapter 6 will present the single-stage voltage doubler design that enables the output voltage to be greater than the input voltage. It is suitable for applications that require large power transmission range.

Chapter 6 Design of Single-Stage Voltage Doubler Regulator

In this chapter, the single-stage voltage doubler design will be presented. The architecture and working principle of the design will be explained. The implementation of the controller as well as the key circuit blocks will be discussed. Lastly, the simulation waveforms and results will be presented at the end of the chapter.

6.1 Introduction

In this chapter, we propose a single-stage voltage doubler design with embedded regulation capability. It solves the limitation of the previous designs which require the input voltage amplitude to be greater than the output voltage. With the voltage doubler structure, an output voltage value of approximately twice of the input voltage amplitude can be obtained. This helps to extend the power transmission range as well. In [115], the work improves the link efficiency by reconfiguring into either doubler or quadrupler topology. Nonetheless, it needs a LDO in second stage for regulation function.

6.2 Working Principle/Operation

Fig. 6.1 shows the proposed full-wave voltage doubler structure with the proposed tri-mode controller. The single-stage structure is embedded with the regulation capability. It is able to work in tri-mode, which are the P-mode, N-mode and OFF-mode. The output voltage is feedback periodically to the controller to decide the mode operation. The tri-mode operation is shown in Fig. 6.2.

The pulse skipping modulation (PSM) control in Chapter 3 is applicable to the voltage doubler structure as well. By utilizing the PSM control, the proposed structure can be reconfigured into three different modes as shown in Fig. 6.2. For

the P-mode operation in Fig. 6.2(a), only high-side switch MP is turned-on to charge up the output capacitor C_1 and the low-side switch MN is turned-off. The P-mode operation is executed if the output voltage is below the reference voltage V_{ref} and the input node V_{INP} is greater than the output voltage V_{DB} . On the other hand, if the output voltage falls below the reference voltage and the input node V_{INP} is lower than ground (GND), then the low-side switch MN is turned on to charge up the output capacitor C_2 as illustrated in Fig. 6.2 (b). Under N-mode, the high-side switch MP is turned-off. If the output voltage is detected to be above the reference voltage, then both of the high-side and low-side switch (MP and MN) are turned-off and there is no electrical connecting path between the input source and the output as shown in Fig. 6.2 (c). Hence, the output voltage V_{DB} is sustained by the charge in the output capacitors C_1 and C_2 .

Fig. 6.1 Proposed full-wave single-stage voltage doubler regulator.

Fig. 6.2 The tri-mode operation: (a) P-mode, (b) N-mode and (c) OFF-mode.

In short, if the output voltage V_{DB} falls below the reference voltage V_{ref} , implying that charging operation is required and hence it will operate in either P-mode or N-mode, depending on whether the input node V_{INP} is greater than V_{DB} or lower than GND . In contrast, if V_{DB} is above V_{ref} , then it will operate in OFF-mode to skip the switching activity by turning off the switches MP and MN and the output is sustained by the charge in the output capacitors.

6.3 Implementation of key circuit blocks

Fig. 6.3 Block diagram of the proposed voltage doubler structure with its controller.

Fig. 6.3 shows the proposed voltage doubler design and its controller. A fraction of the output voltage is feedback to a comparator and it is compared to a reference voltage periodically. A system clock of twice the input frequency is generated from the input voltages. The system clock will activate the comparator periodically to check on the output voltage. The output of the feedback comparator is fed to a flip-flop to determine the mode operation. The proposed controller is shown in Fig. 6.4. Based on the load conditions, the ‘Select’ signal will determine the whether the doubler structure is in ON-mode or OFF-mode. If it is in ON-mode, it can be in P-mode or N-mode, depending on the input node VINP. In OFF-mode, both of the switches MP and MN are turned off whereas during ON-mode, the outputs of the active diode comparators CMP_P and CMP_N will be passed through to drive the gates of MP and MN respectively.

Fig. 6.4 The proposed controller.

Fig. 6.5 shows the simulated waveforms of the input voltage (VINP and VINN), input current I_{AC}, output voltage VDB, ‘Select’ signal, system clock and the gate driver voltages (VGP and VGN). The simulation is done at an output voltage of 2.2 V and a load current of 10 mA. The load condition is checked

periodically by comparing the output voltage with a reference voltage. The ‘Select’ signal of logic ‘0’ represents ON-mode. In ON-mode, it will operate in N-mode if the input V_{INP} is less than GND and it will be in P-mode if the input V_{INP} is greater than the output V_{DB} . In OFF-mode, the switches are turned off and the input current I_{AC} is zero as there is no electrical connecting path between the input source and the output. The mode transition happens only when the input current is zero to avoid efficiency degradation.

Fig. 6.5 Simulated waveforms of the proposed doubler design.

The active diode comparator CMP_P of the switch MP has been discussed in Chapter 3 and the active diode comparator CMP_N of the switch MN is shown in Fig. 6.6.

Fig. 6.6 The active diode comparator CMP_N of the switch MN.

The non-inverting terminal (V_+) of the comparator is connected to GND while the inverting terminal (V_-) of the comparator is connected to the input node V_{INP} . When the node V_{INP} is more negative than GND, the V_{GS} of the transistor Mn6 increases as node B is fixed. Hence, a larger current I_1 is mirrored to I_{UP} . When the node V_- is lower, node A reduces as well in order to track the fixed biasing current and hence limit the current I_{DN} . As a result, I_{UP} is larger than I_{DN} and the output node $VCMP$ will be pulled 'high' to turn-on the low-side switch MN. In contrast, when the node V_- is greater than GND, the V_{GS} of Mn6 reduces and therefore a lesser I_1 is mirrored to I_{UP} . When node V_- increases, node A increases as well and hence a larger I_{DN} will flow. As a result, I_{DN} is larger than I_{UP} and the

output node VCMP will be pulled ‘low’ to turn-off the low-side switch MN. In order to speed up the turn-off response of the comparator to prevent any reverse leakage current from flowing, the current I_2 is designed to be greater than I_1 so that the pull down current I_{DN} is greater than the pull-up current I_{UP} during equilibrium state. The offset voltage can be estimated from Eq. (6.3.1).

$$V_{offset} = V_{sg(Mp6)} - V_{sg(Mp2)}$$

$$= \sqrt{\frac{2(I_2)}{\alpha}} - \sqrt{\frac{2(I_1)}{\beta}} \quad (6.3.1)$$

$$\text{Where } \alpha = \mu_p C_{ox} \left(\frac{W}{L} \right)_{Mp6}, \quad \beta = \mu_p C_{ox} \left(\frac{W}{L} \right)_{Mp2}$$

Fig. 6.7 Self-start-up waveforms of the proposed design.

The start-up waveforms of the proposed doubler design are shown in Fig. 6.7. The voltage doubler has self-startup capability. A reset pulse RST is used to force

the Select signal to zero, enabling it to start-up with passive rectification. When the gate-to-source voltage (VGS) of low-side switch MN is greater than its threshold voltage V_{thn} , the current flows to charge up the output capacitor C_2 . The current flows to charge up the output capacitor C_1 when the VSG of high-side switch MP is greater than its threshold voltage $|V_{thp}|$. The process repeats until the output voltage VDB reaches the minimum supply of the tri-mode controller. Then, it starts to work in the tri-mode operation as discussed earlier.

6.4 Simulation Results and Discussions

Fig. 6.8 Layout of the proposed voltage doubler structure with its controller.

The layout of the proposed voltage doubler design is shown in Fig. 6.8. It has been fabricated in 0.18 μm standard CMOS process. The off-chip output capacitors (C_1 and C_2) of 10 μF are used. To verify the regulation capability of the proposed design, the load is stepped-up and stepped-down from 1 mA to 40

mA and from 40 mA to 1 mA respectively. Fig. 6.9 shows the dynamic load transient response of the proposed single-stage voltage doubler. It has been shown that the output voltage VDB is able to track the reference voltage at 2 V despite a load-step of 40 times is applied to it.

Fig. 6.9 Simulated load-step transient response of the proposed design.

Fig. 6.10 The simulated power efficiency versus output power for the proposed single-stage voltage doubler design.

Fig. 6.10 shows the simulated power efficiency against the output power for the proposed single-stage voltage doubler design at 2V output voltage and 1.2V input voltage amplitude at 125 kHz. A peak efficiency of 94.40% is achieved for an output power range of 2 to 80 mW.

6.5 Power Losses Analysis

The single-stage voltage doubler design regulates the output by operating in 3 different modes, namely P-mode, N-mode and OFF-mode. The power loss estimation for the design is shown in Fig. 6.11. With an output power of 20 mW, the total power loss is approximately 1.19 mW and the controller consumes around 163 μ W of power. The power losses for each mode can be summarized as shown from Eq. (6.5.1) to Eq. (6.5.5). During OFF-mode, the switching activity is skipped and none of the switches conducts. Hence, the conduction loss and switching loss can be minimized.

$$P_{loss(P-Mode)} = P_{conduction\ loss(Mp)} + P_{switching\ loss(Mp)} + P_{leakage} \quad (6.5.1)$$

$$P_{loss(N-Mode)} = P_{conduction\ loss(Mn)} + P_{switching\ loss(Mn)} + P_{leakage} \quad (6.5.2)$$

$$P_{loss(OFF-mode)} = P_{leakage} \quad (6.5.3)$$

$$P_{losses} = P_{conduction} * (n \cdot T) + P_{switching} * (n \cdot T) + P_{leakage} + P_{others}, n \geq 0 \quad (6.5.4)$$

$$P_{total_losses} = P_{losses} + P_{controller} \quad (6.5.5)$$

Fig. 6.11 Power losses estimation for single-stage voltage doubler.

6.6 Discussion and Conclusion

The proposed single-stage voltage doubler regulator has enabled a regulated output voltage to be obtained at a value higher than the input amplitude. This helps to extend the power transmission range. It is an energy-efficiency solution for applications that require large power transmission range. The design has been tapeout in 0.18 μm standard CMOS process.

Even though the single-stage voltage doubler design enables the regulated output voltage to be higher than the input voltage, it is not able to regulate an output voltage that is required to be lower than the input voltage. Therefore, in future work, it worth combining the features of the work from Chapter 4 to Chapter 6 so that a single-stage AC-DC converter which has both buck and boost characteristic can be realized.

Chapter 7 Conclusions and Future Work

In this chapter, the proposed works and contributions to the research project are summarized and concluded in Section 7.1. The recommendations for the future work of the research project are presented in Section 7.2.

7.1 Conclusions

In recent years, wireless power transfer technology (WPT) has become a prominent solution for industrial applications, such as for wireless charging, radio frequency identification (RFID) tag, biomedical implants, etc.

The main focus of the research work is to improve the performance of the wireless power receiver. The power management unit (PMU) of a receiver consists of a rectifier block for AC-DC conversion and a voltage regulator for DC-DC regulation. In the early stage, a two-stage receiver has been proposed in Chapter 3 with an improved rectifier design and an energy-efficient buck regulator. The two-stage design has been fabricated in 0.18 μm standard CMOS process and it has achieved a measured peak efficiency of 75.35%.

Next, a novel single-stage AC-DC converter has been proposed in Chapter 4 to replace the typical two-stage receiver. The voltage regulation is accomplished without a second stage voltage regulator. The dual-mode concept is introduced to regulate the output voltage and the complexity of the entire system has been reduced as well. The single-stage design has been fabricated in 0.18 μm standard CMOS process. Compared to the two-stage design, the one-stage design can improve the efficiency by as much as 23.10%.

In order to optimize the circuit performance of a system, the concept of the single-stage topology in Chapter 4 can be extended for multiple-output function. The proposed extended multiple-output architecture is presented in Chapter 5. As a proof of concept, the single-stage dual-output tri-mode AC-DC converter has been implemented and fabricated in 0.18 μm standard CMOS process. It achieves a peak efficiency of 91.68% in an output power range of 3.8 mW - 114 mW.

Lastly, a single-stage voltage doubler design is presented in Chapter 6 to solve the limitations faced by the previous works which require the input voltage amplitude to be greater than the output voltage. With a voltage doubler structure, the output voltage which is greater than the input voltage can be obtained. This helps to extend the power transmission range as well. The proposed work has been tapeout in 0.18 μm standard CMOS process. The simulation results show that a peak efficiency of 94.40% is achieved at a regulated output voltage of 2 V with an input voltage amplitude of 1.2 V.

7.2 Future Work

Firstly, the active diode comparator for the proposed work still has room for improvement. The fixed unbalanced biasing comparator was proposed to speed up the transient response of the comparator. However, an adaptive offset method can be used to improve the fixed offset voltage method in order to optimize the efficiency under varying operating conditions.

Next, the proposed single-stage AC-DC converter in Chapter 4 has a buck characteristic, which is able to produce a regulated output voltage that is lower than the input voltage. On the other hand, the proposed single-stage voltage doubler design in Chapter 6 has a boost characteristic, which is able to produce a regulated output voltage that is higher than the input voltage. Hence, it is worth combining both of the proposed works to have a single-stage AC-DC converter that has both buck and boost characteristic. It will be very useful for application systems that require different supply voltages with high power conversion efficiency.

Finally, the link efficiency of the WPT system has not been optimized as the main focus of the work is the receiver efficiency. However, the link efficiency can still be improved for a better efficiency of the whole WPT system.

Appendix A Transfer Function Derivation of a Buck Regulator

In this appendix, state-space averaging approach is described based on a buck DC-DC converter. The AC equivalent circuit model of a voltage-mode DC-DC converter with pulse-width modulation controller is shown in Fig. A.1 [46].

Fig. A.1 The AC equivalent circuit model of voltage-mode DC-DC converter with PWM controller.

Fig. A.2 Buck converter with ESR.

State-space averaging is a technique that allows switching regulators to be represented as linear systems. It is a mathematical model of a physical system as a set of input, output and state variables related by the first order differential equations. The buck converter with ESR in Fig. A.2 is used to describe the state-space averaging approach. In Fig. A.2, r represents the ESR while R is the load. U_1 is the ac current source while X_1 and X_2 are the inductor current and the output capacitor voltage respectively. U_2 is put in parallel with the load to simulate load modulation. The switched buck converter can be approximated from a discontinuous system to a continuous system. The analysis can be done as below [47].

i) S1 on and S2 off:

$$U_1 = L\dot{X}_1 + X_2 + rC\dot{X}_2 \text{ and } X_1 - C\dot{X}_2 - \frac{X_2 + rC\dot{X}_2}{R} = -U_2$$

$$\therefore \dot{X}_1 = -\frac{rR}{L(R+r)}X_1 - \frac{R}{L(R+r)}X_2 + \frac{U_1}{L} - \frac{rR}{L(R+r)}U_2 \text{ and}$$

$$\dot{X}_2 = \frac{R}{C(R+r)}X_1 - \frac{1}{C(R+r)}X_2 + \frac{R}{C(R+r)}U_2$$

As $\dot{X} = AX + BU$,

$$\therefore A1 = \begin{bmatrix} -\frac{rR}{L(R+r)} & -\frac{R}{L(R+r)} \\ \frac{R}{C(R+r)} & -\frac{1}{C(R+r)} \end{bmatrix} \text{ and } B1 = \begin{bmatrix} \frac{1}{L} & -\frac{rR}{L(R+r)} \\ 0 & \frac{R}{C(R+r)} \end{bmatrix}$$

ii) S1 off and S2 on:

$$0 = L\dot{X}_1 + X_2 + rC\dot{X}_2 \text{ and } X_1 - C\dot{X}_2 - \frac{X_2 + rC\dot{X}_2}{R} = -U_2$$

$$\therefore \dot{X}_1 = -\frac{rR}{L(R+r)}X_1 - \frac{R}{L(R+r)}X_2 - \frac{rR}{L(R+r)}U_2 \text{ and}$$

$$\dot{X}_2 = \frac{R}{C(R+r)}X_1 - \frac{1}{C(R+r)}X_2 + \frac{R}{C(R+r)}U_2$$

Rearranging the above equations, we can get:

$$\therefore A2 = \begin{bmatrix} -\frac{rR}{L(R+r)} & -\frac{R}{L(R+r)} \\ \frac{R}{C(R+r)} & -\frac{1}{C(R+r)} \end{bmatrix} \text{ and } B2 = \begin{bmatrix} 0 & -\frac{rR}{L(R+r)} \\ 0 & \frac{R}{C(R+r)} \end{bmatrix}$$

By applying: $A = A1 \times d + A2 \times (1-d)$ and $B = B1 \times d + B2 \times (1-d)$, we can get:

$$A = \begin{bmatrix} -\frac{rR}{L(R+r)} & -\frac{R}{L(R+r)} \\ \frac{R}{C(R+r)} & -\frac{1}{C(R+r)} \end{bmatrix} \text{ and } B = \begin{bmatrix} \frac{d}{L} & -\frac{rR}{L(R+r)} \\ 0 & \frac{R}{C(R+r)} \end{bmatrix}$$

This, in turn, leads to:

$$\begin{aligned} \dot{X}_1 &= -\frac{rR}{L(R+r)}X_1 - \frac{R}{L(R+r)}X_2 + \frac{d}{L}U_1 - \frac{rR}{L(R+r)}U_2 \text{ and} \\ \dot{X}_2 &= \frac{R}{C(R+r)}X_1 - \frac{1}{C(R+r)}X_2 + \frac{R}{C(R+r)}U_2 \end{aligned}$$

The DC term of X , U and d can be separated from the signal frequency AC terms as below, with the parameter with a caret (hat) represents the perturbed small AC quantities.

$$X = X_0 + \hat{X}$$

$$U = U_0 + \hat{U}$$

$$d = D + \hat{d}$$

Based on the state-space averaging concept, the buck converter is modelled as a continuous but non-linear system with the state-space equations above. However, the non-linear equations above can be linearized by using the small signal approximation technique as shown in [47]. By applying the Laplace transform and the generalized control law equation to the linearized equations, the voltage loop gain of the buck converter eventually can be derived as below with the other parameters have the same meaning as in the Fig. A.1 and A.2:

$$T(s) = \frac{\frac{U_{10}G_c(s)r}{V_m L} (s + \frac{1}{rC})}{s^2 + s(\frac{1}{RC} + \frac{r}{L}) + \frac{1}{LC}}$$

Appendix B AC Power Calculation

Fig. B.1 The test measurement setup for AC power measurement.

The measurement is done at 125 kHz of frequency. For input AC current measurement, a sense resistor R_{sense} is inserted in the input path as shown in Fig. B.1. The AC current is obtained by taking the ratio of the voltage drop across the R_{sense} to the R_{sense} value. The voltage drop across the R_{sense} is sensed and amplified by an instrumental amplifier (IA₁). In order to increase the accuracy of

the current measurement, a low offset voltage (50 μ V) instrumental amplifier (INA129) is utilized [169]. Instrumental amplifier is used as it consists of input buffer amplifiers which help to eliminate the need for input impedance matching and hence it is ready for use in measurement or test equipment.

As shown in Fig. B.1, the input AC voltage can be obtained by taking the difference between the voltage node B and C with an instrumental amplifier (IA₂) of gain of 1. The input current is obtained by taking the difference between the voltage node A and B and it is divided by the Rsense value and the gain of the IA₁. The equations for input AC voltage and the current can be expressed in Eq. (B.1) and (B.2) respectively.

$$V_{AC}(t) = V_B(t) - V_C(t) = V_{BC}(t) \quad (B.1)$$

$$I_{in}(t) = \frac{V_A(t) - V_B(t)}{R_{sense} \times G} = \frac{V_{AB}(t)}{R_{sense} \times G} \quad (B.2)$$

Subsequently, the input AC power can be expressed as in the equation B.3.

$$\begin{aligned} P_{AC(t)} &= \frac{1}{T} \int_{t_0}^{t_0+T} V_{AC}(t) \cdot I_{in}(t) dt \\ &= \left(\frac{1}{R_{sense} \times G} \right) \cdot \frac{1}{T} \int_{t_0}^{t_0+T} V_{AB}(t) \cdot V_{BC}(t) dt \quad (B.3) \end{aligned}$$

The input AC power can be calculated from Eq. (B.3). Alternatively, a current probe can be used for the input current measurement. The average of the multiplication of the input voltage and input current for several period cycles can be obtained for the input power.

Appendix C Analog Blocks Design

This appendix shows the sizing of the analog blocks, such as biasing circuit, comparator as well as the bandgap reference used from Chapter 3 to 6. The rating of the transistors is 5.5 V. The wide-swing cascode biasing circuit is shown in Fig. C.1. It is designed for 1.5 μA of biasing current. The transistor sizing and the bias voltage condition are shown in Table C.1 and C.2 respectively.

Fig. C.1 Wide-swing cascode biasing circuit.

Table C.1 Transistor sizing of the biasing circuit.

Transistors	Size (W/L)
Mp1	8/1.2
Mp2	8/1.2
Mp3	8/1.2
Mp4	1/1
Mp5	8/1.2
Mp6	8/1.2
Mp7	8/1.2
Mp8	1/1.7

The active diode comparator design is shown in Fig. C.2. The sizing and bias voltage condition are shown in Table C.3 and C.4 respectively.

Fig. C.2 Active diode comparator.

Table C.3 Transistor sizing of the comparator.

Transistors	Size (W/L)
Mp1 to Mp10	10/0.5
Mn1 to Mn7	4/0.7
Mn8	6/0.7

Table C.4 Bias voltage condition of the comparator.

Bias node Resistor	Value
Vdd	2V
VBP	1.37 V
VCP	1.05 V
VCN	0.97 V
VBN	0.63 V
RB1	46.97 k Ω
RB2	150 k Ω

The bandgap reference design is shown in Fig. C.3 and Table C.5 show values of the transistors and the resistors.

Fig. C.3 Bandgap reference design.

Table C.5 Transistors' sizing of the bandgap reference.

Transistors	Size (W/L)
Mp1	2/1
Mp2 to Mp4	3/1.5
Mn1 to Mn3	5/1
Mn4 to Mn5	1.8/1.2
RB1	891.36 k Ω
RB2	36.01 k Ω
RB3	444.43 k Ω

Publication List

Journals:

1. **Qiong Wei Low**, Mi Zhou, Liter Siek, “A Single-Stage Direct-Conversion AC-DC Converter for Inductively Powered Application,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 26, No. 5, pp. 892-902, 2018.
2. Mi Zhou, Zhuochao Sun, **Qiong Wei Low**, Liter Siek, “Multi-loop Control for Fast Transient DC-DC Converter,” accepted by IEEE Transactions on Very Large Scale Integration (VLSI) Systems in Sep 2018.
3. Mi Zhou, Zhuochao Sun, **Qiong Wei Low**, Liter Siek, “Fast transient response DC-DC converter with start-up in-rush current control,” IET Electronics Letter 2016.

Conferences:

1. **Qiong Wei Low**, Liter Siek, Mi Zhou, “A high efficiency rectifier for inductively power transfer application,” IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Oct 2015.
2. **Qiong Wei Low**, Mi Zhou, Liter Siek, “Performance analysis on active rectifier structures for inductively powered application,” International Symposium on Integrated Circuits (ISIC) 2016.
3. Mi Zhou, **Qiong Wei Low**, Liter Siek, “A high efficiency synchronous buck converter with adaptive dead-time control,” International Symposium on Integrated Circuits (ISIC) 2016.
4. Mi Zhou, Zhuochao Sun, Zhekai Xiao, **Qiong Wei Low**, Liter Siek, “A fast transient response DC-DC converter with an active compensation capacitor module,” IEEE International Symposium on Circuits and Systems (ISCAS) 2018.

Technical Disclosure:

1. **Qiong Wei Low**, Liter Siek, “A Single-stage multiple-output AC-DC regulator for inductively powered application,” has been filed as technical disclosure under reference number: PAT/219/17.

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