Thermal failure of carbon nanostructures

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2018

Maurice, A. (2019). Thermal failure of carbon nanostructures. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/89749>

<https://doi.org/10.32657/10220/48047>

Thermal failure of carbon nanostructures

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University in
partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2018

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*(B) This thesis contains material from 1 paper published in the following peer-reviewed journal(s) / from papers accepted at conferences in which I am listed as an author.

Chapter 4 is published as Maurice, Ange, Laurence Bodelot, Beng Kang Tay, and Bérengère Lebental. "Controlled, Low-Temperature Nanogap Propagation in Graphene Using Femtosecond Laser Patterning." Small 14, no. 31 (2018): 1801348.

The contributions of the co-authors are as follows:

- Bérengère Lebental hosted me in Ecole Polytechnique where I carried out the thermal infrared experiments. She also helped me with the manuscript corrections.
- Laurence Bodelot helped me perform the thermal infrared experiments in Ecole Polytechnique. She also helped me with the manuscript corrections.
- As my NTU supervisor, Tay Beng Kang supervised me throughout the study by providing valuable advices and guidance.
- All work, including data processing, sample preparation and manuscript writing was done by me.

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Acknowledgement

First and foremost, I would like to express my sincere gratitude to Dr Berengère Lebental and Professor Tay Beng Kang, my research supervisors for their patient guidance, encouragement and useful critiques.

I would like to express my great appreciation to Dr Liang Kun for her assistance in the handling of the administrative paperwork. I am also very grateful to Dr Tan Chong Wei and Dr Wang Xingli for their guidance.

A very special thank to Loïc Loisel, who is the best teammate I have ever worked with. By acting as my mentor for my first 2 years of PhD, he helped me to initiate my research. He is also a terrific friend with great humour and spirit.

Speaking of friends, I especially thank my fellow doctoral student and friend Etienne Rodriguez who is the best buddy for trekking, squash (even though I win) and climbing. Of course, I do not forget all the fantastic friends that I met in CINTRA: Aliénor, Charles, Mathieu, Umar, Olivier, Nicolas, Théo, Holger and David. I would also like to extend my thanks to Hasman Bin Hassan from Nanoelectronics 1 for providing me with the necessary tools whenever I needed.

Throughout my PhD, I did a research attachment at the University of Rochester, USA. Therefore, I am incredibly grateful to Professor Eby. G Friedman for welcoming me into his lab. I also thank Boris Vaisband who was a great teammate during my time in Rochester. I also would like to thank the whole team of students working under Prof. Friedman for their

assistance during my stay: Alexander, Gleb, Albert, Kan and Muhammad.

I was also invited to work in École Polytechnique multiple times. I would like to express my sincere gratitude to Associate Professor Laurence Bodelot for her help in performing thermography experiments. I would also like to thank Boris Gusarov for his perfect technical assistance. I also wish to acknowledge Emilliano Palecchi for the in-situ SEM experiments.

Finally, even though France is far, I wish to thank my parents for their support and encouragement throughout my 4 years in Singapore.

Speaking of France, I especially thank my two amazing friends Fabien and Quentin who made my holidays in France so particular every time I was visiting.

Last but not the least, I would like to thank Antonia for her continuous emotional support. She helped me overcome several stressful situations. She is an awesome girlfriend who genuinely laughs at almost all my jokes.

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Summary

The greatest weakness of integrated circuits is thermal. Localized temperature increase can significantly degrade circuit performances, sometimes irreversibly. To tackle this issue, carbon-based materials are envisioned as potential candidates to replace metals like copper, tungsten and aluminium. However, little is known about their failure mechanisms. In this thesis, we studied the thermal degradation mechanisms of graphitic materials (Carbon nanotubes, graphite and graphene). To do so, we first examined the joule-heating induced electrical failure of graphene based devices (electro-burning). From our observations, we identified a thermally heterogeneous electro-burning process driven by localised Joule-heating leading to the propagation of a nanometre-spaced gap. To gain more insight into this degradation, we used a femtosecond laser to induce thermal damage to the graphene locally. Our interpretation reveals that heating a graphitic layer leads to the formation of vacancies resulting in an unstable carbon lattice. Finally, we showed how electro-burning, when controlled, can be an advantage. We use a tightly focused femtosecond laser beam to induce defects in graphene according to selected patterns. We show that the nanogaps in pre-patterned devices propagate along the defect line created by the femtosecond laser with a 92% success rate. Finally, we performed electrical and thermal simulations of an alternative 3D architecture: carbon nanotubes through-substrate vias covalently bonded to graphene/graphite horizontal interconnects. The structure is highly conductive both thermally and electrically and can sustain higher

current densities than currently used copper interconnects. However, our results also indicate that graphite anisotropy could worsen the reliability of the architecture due to higher current crowding.

Keywords: Thermal failure, graphene, carbon nanotubes, electro-burning, laser irradiation

Acronyms

IC	Integrated circuits
TSV	Through-substrate via
MTF	Mean time to failure
CNT	Carbon nanotubes
SWCNT	Single-wall carbon nanotubes
MWCNT	Multi-wall carbon nanotubes
IR	Infrared
I-V	Current-Voltage
3D	Three dimensional
2D	Two-dimensional
1D	One-dimensional
SEM	Scanning electron microscope/microscopy
AFM	Atomic Force microscope/microscopy
CVD	Chemical-Vapour-Deposition
TEM	Transmission electron microscope/microscopy
CCD	Charge coupled device
RF	Radio-frequency
PL	Photoluminescence

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Chapter 1

Introduction

In integrated circuits (ICs), binary information travels between devices through interconnects. Unfortunately, these connections are lossy, dissipating this energy into heat. With low packing densities of transistors, heat easily escapes out of the circuit. However, following Moore's law, the packing density has been increasing exponentially. Consequently, current ICs concentrate tremendous amounts of devices. For instance, a silicon chip can contain more than a hundred metres of total wire length per square metre [15]. The denser a circuit is, the more heat it generates. If improperly managed, this thermal dissipation leads to performance degradations. In extreme cases, the process is irreversible resulting in circuit failure.

To extract heat, industries have adopted efficient architectures where compromises are made to optimise the distances between heat-sensitive and heat-emanating blocks. Furthermore, the chips are often combined with efficient heat sinks. Another solution involves replacing conventional materials with heat-resistant materials.

Among the candidates, carbon allotropes are the most promising. Indeed, some crystalline allotropes outperform most of the existing materials in terms of thermal and electrical conduction. For example, graphene and carbon nanotubes have the highest thermal and electrical conductivity. Also,

they can withstand very high current densities, up to several orders of magnitude higher than copper.

In the next sections, we first describe the most relevant carbon allotropes. Then, we review the principle, consequences and solutions of heating in ICs. Next, we describe various current-induced failures that can potentially occur in extreme cases. Finally, we summarise the properties of carbon-based materials by comparing them with copper, aluminium and silicon.

1.1 Carbon allotropes

Carbon has eight allotropes, namely: Graphite, graphene, carbon nanotube(CNT), diamond, lonsdaleite (hexagonal diamond), amorphous carbon and fullerenes(C_{60} , C_{540} and C_{70}). In this section, we describe the allotropes that are viewed as potential replacement materials to alleviate thermal issues.

1.1.1 Diamond

Diamond is a metastable, high-pressure carbon allotrope with a face-centred cubic crystal structure (Figure 1.1). To form diamond, pressures as high as 5-6 GPa and temperatures higher than 900-1400°C are necessary [16]. In the past, such conditions were only met within the earth mantle. However, with new technologies, it is now possible to synthesise diamond using chemical vapour deposition (CVD).

Diamond is either valued as a precious stone for jewellery or widely used in industry for its outstanding properties: excellent heat conduction and electrical insulation. Also, diamond is one of the hardest materials (Maximum Mohs hardness: 10). Thanks to these properties, diamond is viewed as a potential substitute to silicon dioxide. It would prevent any short circuits while efficiently driving heat out of any localised hotspot. Table 1.1 summarises the properties of pure diamond extracted from experiments.

Figure 1.1: Diamond crystal lattice (Anton, German Wikipedia)

Thermal conductivity	2200 W/m/K	[17]
Electrical resistivity	$10^{11} - 10^{18} \Omega \cdot m$	[18]
Young modulus	$\approx 1 TPa$	[19]
Tensile strength	$4.3 - 14 MPa \sqrt{m}$	[20] [21]
Thermal expansion coefficient	$0.8 - 1.2 \times 10^{-6} / K$	[22]

Table 1.1: Properties of pure diamond, experimental data

1.1.2 Graphite

Like diamond, graphite is a crystalline carbon allotrope. However, it is a layered crystal with atomic regularity in two dimensions (planar). Therefore, bulk graphite is a stacking of two-dimensional carbon crystals. The atomic structure is hexagonal with an sp^2 hybridisation. Each atom is linked to three other atoms within the same plane (Figure 1.2).

Figure 1.2: Graphitic hexagonal atomic structure

Electrical resistivity $\parallel$	$7 - 10 \times 10^{-6} \Omega.m$	[23][24]
Electrical resistivity $\perp$	$2 \times 10^{-4} \Omega.m$	[24][25]
Young modulus $\parallel$	$20 GPa$	[26]
Tensile strength $\parallel$	$137 MPa$	[26]
Thermal conductivity $\parallel$	$1950 m/K$	[27]
Thermal conductivity $\perp$	$5 m/K$	[27]
Thermal expansion coefficient $\parallel$	$7.8 \times 10^{-6} /K$	[28]
Thermal expansion coefficient $\perp$	$26 \times 10^{-6} /K$	[28]

Table 1.2: Properties of pure graphite $\parallel$: In-plane $\perp$: Out of plane. The given values arise from experimental data

The properties of pure graphite are summarised in Table [1.2]. Contrary to diamond, graphite is both an excellent electrical and thermal conductor. In addition, it is a highly anisotropic material with properties defined parallelly or perpendicularly ($\parallel$ or $\perp$) to the basal plane.

1.1.3 Graphene

Graphene is an atom-thick (0.34nm) layer of pure graphite. Since its discovery in 2004 by Novoselov & Geim [29], it has led to a tremendous amount of research.

In this two-dimensional(2D) material, the electrons do not behave like in bulk graphite. They are described as Dirac massless fermions [30]. They can move at very high speed ($10^6 m/s$) and 150 times faster than the carriers in doped silicon. Furthermore, graphene exhibit strong electric field effect. Indeed, by applying a back gate voltage, one can tune its carrier density and thereby modify its ability to conduct electricity. This kind of feature makes graphene a potential candidate for the next generation of transistors.

The properties of graphene (Table [1.3]) outperform most of the existing bulk materials. Therefore, graphene based innovation is expected to be the next disruptive technology. Researchers see possibilities in optoelectronics, photo-voltaic, energy storage, composite materials or next-generation electronics devices [31].

Electron mobility	$40000 - 200000 \text{ cm}^2/\text{V}/\text{s}$	[32], [33]
Electrical resistivity	$10^{-8} - 10^{-5} \Omega.m$	[34]
Young modulus	$\approx 1 \text{ TPa}$	[35]
Tensile strength	130 GPa	[35]
Thermal conductivity	$600 - 5000 \text{ W}/\text{m}/\text{K}$	[36]
Thermal expansion coefficient	$-8 \times 10^{-7}/\text{K}$	[37]

Table 1.3: Properties of monolayer graphene, experimental values

1.1.4 Carbon nanotubes

A single sheet of graphene seamlessly rolled up makes a carbon nanotube (CNT) (Figure 1.3(a)). Multiple SWCNTs of various diameters may also be inserted inside each other to form multi-wall CNTs (MWCNT) as opposed to single wall CNTs (SWCNT). Usually, the electrical and thermal properties of MWCNTs are inferior compared to SWCNTs. Similarly and because it is made of a graphene sheet, carbon nanotubes also possess exceptional properties (summarised in Table 1.4). However, compared with graphene, the properties of CNTs are defined along its axis (1D material). The chirality of the CNT determines whether it is semiconducting or metallic. For a transistor, a semiconducting CNT would be preferred while a metallic CNT would be required for pure electrical conduction. Typically, CNTs are grown in forests or bundles in CVD chambers (Figure 1.3(b)) and exhibit random chiralities. For example, we usually assume that statistically 1/3 of the nanotubes in a bundle are metallic while the rest are semiconducting. It is worth mentioning that it is possible to tune the chirality of a CNT bundle to yield 90% of metallic CNTs [38]. Interestingly, the electrical conductivity of a SWCNT is independent of its diameter and length. This is why its resistance is usually calculated without taking into account its diameter. We define it as a quantized resistance. It means that its effective electrical of thermal conductivity is greatly improved by reducing the diameter of the CNT since the cross section is reduced. The quantum resistance of a CNT is $h/4e^2$ (6.45k Ω) [39] and has been remarkably measured by dipping a

Figure 1.3: (a) Atomic structure of a single wall carbon nanotube (SWCNT) and a multi-wall carbon nanotube (MWCNT) (b) SEM image of a carbon nanotube forest

single nanotube into mercury [40]. However, it is worth mentioning that, in practical cases, scattering of electrons may occur through defects, especially for large nanotubes resulting in a higher resistance [41].

1.2 Heat in integrated circuits

1.2.1 Limits of Moore's Law

Figure 1.4 shows the evolution of transistor count per chip and central processing (CPU) unit clock frequency. In the past 42 years, the transistor count has been following Gordon Moore's predictions that the number would double every two years [46]. Recently, this prognostic has started to erode [47].

Quantized resistance	$6.45k\Omega$	[39]
Young modulus	$\approx 1TPa$	[42]
Tensile strength	$2 - 22GPa$	[43]
Thermal conductivity	$3500W/m/K$	[44]
Thermal expansion coefficient	$7.5 \times 10^{-6}/K$	[45]

Table 1.4: Properties of a single wall carbon nanotube (SWCNT), experimental values

Indeed, as transistors get miniaturised, we are reaching the atomic boundaries with transistors as small as 9nm. At this scale, the laws of physics are changed. Reducing further the transistor size is very challenging regarding fabrication feasibility and also requires to take quantum phenomena into account.

Observing the clock frequency evolution, the plateau started much earlier from the beginning of the 21st century to reach a maximum around 3-4 GHz in 2008. What prevents us from increasing the clock frequency? First, doing so would result in very high power consumption. Indeed, the dynamic power consumed by a chip is roughly equal to :

$$P = CV^2f, \quad (1.1)$$

where C is the thermal capacitance of the chip (fixed), V is the core voltage, and f is the clock frequency [48].

Here, the power scales linearly with the frequency. However, when increasing the frequency, the voltage has to be increased accordingly to maintain the stability of the computation. As shown in Figure 1.4(b), the average power grows faster than the frequency.

With current CPUs being implemented in mobile devices such as tablets and smartphones, it is essential to save battery life and therefore limit the clock frequency. In cases where battery life does not matter (Desktop computers), saving energy is not the only problem. Indeed, the power consumed within the chip dissipates thermally. In other words, significant amounts of

heat are generated within small volumes. Therefore, manufacturers warn consumers who are overclocking their central or graphical processing units (CPU, GPU) by forcing a higher clock frequency above the recommended values.

Figure 1.4: (a) Evolution of the transistor count per chip and the clock frequency in the past 42 years (Data from Karl Rupp) (b) Average power consumption of CPUs as a function of the frequency [1]

1.2.2 Heat-induced degradations of device performances

Temperature variations significantly alter the physics of semiconductors, it impacts the bandgap [49], the carrier concentration, the mobility [50] and the saturation velocity [51]. Increasing the temperature result in performance degradations. The changes can lead to timing failures, causing systems to exceed power or energy budgets. Additionally, the increase in thermal energy leads to more collisions between the electrons hence decreasing the signal/noise ratio (increase of kT). Figure 1.5 shows the threshold voltage of a CMOS transistor as a function of the temperature. It can vary from about 1.4V at 20°C to 1V at 180°C. Because circuits are specifically designed to work with a specific threshold voltage, large temperature rises may significantly disturb the normal operation of a circuit. Leakage currents also increase exponentially with temperatures. As shown in Figure 1.5 the power consumption of a circuit increases significantly with temperature [3]. At 30°C, the leakage current accounts for only 6% of the total power, while at 110°C, the total power consumption doubles with half of that power arising from leakage.

Figure 1.5: (a) Threshold voltage vs temperature for Si-gate CMOS transistors. [2] (b) Power consumption of a die as a function of temperature [3]

1.2.3 Heat extraction solutions

To tackle the thermal issue, heat must be efficiently extracted out of the circuit. Thus, a heat sink is necessary. As shown in Figure 1.6, a high thermal conductivity structure (usually copper or aluminium) is bonded to the chip with a thermal interface material (TIM). The TIM is generally a viscous grease that enables maximum contact at the interface by eliminating air gaps or spaces. The heat sink is usually designed with fins or pins to increase the exposed surface and thus improve convection. In addition, forced convection is normally added by implementing one or several fans (Figure 1.6(b)).

Figure 1.6: (a) Schematic of a chip in contact with a heat sink through a thermal interface material (TIM) [4] (b) Photograph of a heat sink combined with a fan

Another way to manage heat is to optimise the architecture of the integrated circuit. This process is called thermal-aware floorplanning. The idea is to optimize the placements of the different circuits blocks depending on their power density. Ideally, the heat emanating structures would be placed far from each other to prevent localised heating within the chip [52, 53].

1.3 Thermal failure

As described in section [1.2.2](#) high temperatures can significantly lower the performances of transistors. Fortunately, for most cases, these degradations are reversible and do not alter the integrity of the circuit. In more extreme cases, irreversible destruction of the component may occur. To improve a circuit reliability, it is essential to understand such phenomena. In this section, we review the thermally-driven failure mechanisms of conductors.

1.3.1 Thermal stress

Because integrated circuits are composite structures made of several different materials, thermal expansion may be a reliability issue. Indeed, the mismatches in coefficients of thermal expansion (CTE) and Young moduli between the different materials can lead to failure mechanisms such as delamination, de-adhesion or fracture [\[5, 54–56\]](#). We note that such mechanisms can occur at every level of packaging, from transistors to solder joints [\[57\]](#). Often, thermal stress-induced failure goes hand in hand with other failure mechanisms [\[58\]](#). For example, delamination may prevent heat extraction resulting in significant temperature increases that can accelerate electro-migration or electro-burning (see section [1.3.2](#) and [1.3.3](#)).

Usually, silicon has the lowest CTE of $5 \times 10^{-6}/K$ while copper and aluminium have a higher CTE of about $20 \times 10^{-6}/K$. Thermal cycling over a long period of time results in fatigue and void formation. Figure [1.7](#) shows an example of voids appearing after thermal cycling in an aluminium interconnect.

To prevent and diminish the impact of thermal stresses within circuits, several solutions can be employed. First, the thermal loading can just be lowered. Lower temperature differences will result in lower stresses. However, due to the recent trend in IC packaging density, this would generally

Figure 1.7: SEM image showing voids in an aluminium line after 3000 cycles from 25°C to 125°C [5].

result in lower performances. Second, the Young moduli of the components could also be lowered, this reduces the thermal stresses and increases the reliability [58]. For instance, this can be done by making stretchable integrated circuits with flexible polymer-based substrates [59]. For example, a stiff material can be used in conjunction with a compliant material with a low modulus.

Lastly, the impact of thermal stresses could be attenuated by simply choosing materials with matching CTE. Looking at carbon based-materials, the literature mainly focuses on thermal stresses in composite materials containing a both carbon and non-carbon elements [60-62]. However, to the best of our knowledge, there is no research dealing with the thermal stresses within a carbon-based circuit. Nonetheless, they could be interesting candidates because they have similar CTE. However, they also have very large Young Moduli than could significantly heighten the thermal stresses. Even

though they are more robust thanks to their high tensile strength, they could still experience delamination at their interfaces.

1.3.2 Electro-migration

Electro-migration is a failure mechanism caused by moving electrons impacting the atoms and ejecting them out of their equilibrium position. Over time, this leads to the creations of voids, porosities, loss of integrity and ultimately failure (Figure 1.8(a)). The equation of Black provides a model to predict the mean time to failure (MTF) of a metallic conductor [63]:

$$\frac{1}{MTF} = AJ^n e^{-\frac{E_a}{kT}}, \quad (1.2)$$

where A is a factor involving the cross-sectional area of the conductor, J is the current density, n is a constant that depends on the electro-migration mechanism E_a is the activation energy, k is the Boltzmann constant and T is the temperature of the conductor. Figure 1.8(b) shows a plot of the MTF as a function of the temperature for an aluminium interconnect. The MTF at 50°C is about 1300 hours while at 70°C, the MTF is only 200 hours. Above 150°C, the MTF is expected to be less than one hour. Interestingly, even though the melting point of aluminium far from being reached (660°C), the interconnect would break within minutes at 300°C. Therefore, to increase the reliability of interconnects, the temperature needs to be as low as possible. This highlights the need to either lower the temperature within ICs or use new materials resistant to electro-migration instead of copper or aluminium.

Carbon-based materials, for instance, are particularly interesting to look at: They can withstand much higher current densities than metals. For instance, the maximum current density for a CNT is about $10^7 - 10^9 A/cm^2$ [64,65]. For graphene, the value is $10^8 A/cm^2$ [66,67]. These values are several orders of magnitude higher than those of copper or aluminium. It

Figure 1.8: (a)SEM image showing voids and hillocks formed due to electro-migration [6] (b)Mean time to failure as a function of the conductor temperature plotted for an aluminium wire with equation 1.2 and parameters from ref [7]

is particularly interesting to note that carbon materials are not affected by electro-migration and that making composite materials such as copper combined with CNTs significantly improve the resistance against electro-migration [68]. Regarding endurance, Wei et al. have demonstrated that CNTs could withstand current densities up to $10^9 - 10^{10} \text{ A/cm}^2$ for more than two weeks at 250°C [69]. A metallic wire under this kind of loading would fail within seconds.

1.3.3 Electro-burning

If electro-migration does not occur in carbon materials, one may wonder what happens when the maximum current density of carbon materials is reached. The general term used for any material is "electrical breakdown", but for graphene and CNTs, the specific term has become "electro-burning".

Electro-burning systematically leads to the formation of nanometre-spaced gaps (nanogap). In the case of graphene, the nanogap extends as a one-dimensional crack [8, 67, 70, 70-77]. For CNTs, the nanogap is a highly localised constriction [9, 78-80].

In Chapter 2, we perform a comprehensive study aiming at understanding the failure mechanisms of graphene devices during electro-burning.

Figure 1.9: SEM image of a nanogap formed after electro-burning of graphene(a) [8] and CNT(b) [9]

1.4 Advantages of a carbon-based integrated circuit

Table 1.5 lists the properties of carbon-based materials compared with those of elements commonly found in integrated circuits such as copper and silicon.

Summarising the table, carbon based materials, are similar to IC materials regarding electrical resistivity and thermal expansion coefficient. In terms of thermal transport, carbon materials show the best performances with a thermal conductivity 5-10 times better than their metallic counterpart. All conductive carbon materials can withstand up to 1000 times more current density than copper and aluminium lines. Within the scope of fabricating a carbon-based integrated circuit, this shows, on the one hand, that carbon materials would allow better heat extraction hence lowering the maximum temperature of the circuit. On the other hand, they would withstand higher current densities and possibly greater temperatures. In conclusion, using carbon-based materials could significantly improve the reliability of the ICs. We note, however, that cost could be a determining factor enabling the breakthrough of this technology since current ICs are undoubtedly cheaper.

	CNTs	Graphene	Graphite	Diamond	Silicon	Copper	Aluminium
Electro-migration	-	-	-	-	Yes	Yes	Yes
Maximum current density ¹ (A/cm^2)	10^8	10^8	-	-		10^5	10^5
Thermal conductivity (W/m/K)	3500	5000	$1700^{\parallel}/8^{\perp}$	2200	150	400	237
Electrical resistivity ($10^{-8}\Omega.m$)	1.5^2	1.5	$47^{\parallel}/10^{5\perp}$	-	-	1.68	2.82
Thermal expansion coefficient ($10^{-6}K^{-1}$)	7.5	-0.8	$7.8^{\parallel}/26^{\perp}$	0.8	5	16	21
Young Modulus (GPa)	1000	1000	$20^{\parallel}$	1000	150	130	
Tensile strength (MPa)	63 000	130 000	137	60 000	200	262	40

Table 1.5: Properties of current IC materials compared to carbon-based materials. To improve clarity, the references were removed. The same table with the corresponding references are found in Appendix A

¹ For a micrometer-sized interconnect

² CNT dimensions: 1 nm wide, 1 μ m long

Nonetheless, thanks to their robustness, carbon materials could also be applied in harsh environments (corrosive, space, etc...) where the cost would be more balanced.

1.5 Objectives

In this thesis, we explore the use of carbon-based materials as potential candidates to replace conventional materials in integrated circuits. However, although the outstanding properties of carbon allotropes are thoroughly documented, the existing literature lacks information about their failure mechanisms. Therefore, the primary objective is to study the thermal failure of carbon-based conductors at high current densities. First, we aim at identifying the potential thermal weaknesses of a carbon-based circuit through numerical simulations. Second, the objective is to recreate experimentally current-induced failures to study the phenomenon exhaustively. Finally, this work aims at assessing whether thermal failures could be turned into our advantage by controlling electro-burning.

1.6 Organisation of the thesis

In Chapter [2](#) we perform a systematic study of the electro-burning. Electro-burnt graphene is exhaustively characterised using SEM, AFM and Raman spectroscopy. Furthermore, we report two in-situ electro-burning experiments, using SEM and infrared thermography.

In Chapter [3](#) we introduce destructive localised heating by femtosecond laser annealing to recreate a scenario where heat is trapped locally within a circuit. Also, we report additional works on laser irradiation of hexagonal Boron nitride or gallium nitride.

In Chapter [4](#) we investigate the effects of localised laser-induced defects on the electro-burning phenomenon. In particular, we show that the nanogap

formed during electro-burning can be spatially controlled by patterning a defect line on the graphene. We also support our study by showing, via IR thermography and numerical simulation, that electro-burning can occur at room temperature.

In Chapter [5](#) we report the simulation of a hybrid carbon-based 3D IC structure: a CNT through substrate via (TSV) connected to a graphite interconnect. We study how heat and electricity crowds at the interface. In addition, we examine the influence of frequency and anisotropy of graphite on the total resistance.

Chapter 2

Electro-burning graphene

As shown in section [1.3.3](#) although carbon materials are unaffected by electro-migration, they can still fail through a process called electro-burning. Therefore, in order to properly assess the reliability of a carbon-based circuit, we aim at understanding the physical mechanisms leading to a Joule-heating induced failure.

In this chapter, we study the electro-burning of resistive graphene devices. In the first part, we describe and characterise the graphene devices used in this study. Then, we present an exhaustive electrical and morphological characterisation of electro-burnt devices including two in-situ experiments. Finally, we discuss the combined observations to propose a thermally-driven failure mechanism.

2.1 Device structure

2.1.1 Fabrication

Figure [2.1](#) shows the device structure of the two-terminal graphene devices used in this work. We started the fabrication process from chemical-vapor-deposited monolayer graphene (Graphene Supermarket). After a first optical lithography step (photoresist AZ5214), graphene stripes were patterned

on SiO_2 (90nm thick) by O_2 plasma etching for 30s at 60W. After a second lithography step, $\text{Ti}(10\text{nm})/\text{Au}(100\text{nm})$ electrodes were deposited by electron beam evaporation. To study the impact of the device dimensions, distances between the electrodes vary from 5 to 60 μm and so do the graphene stripe widths (5 to 100 μm).

Figure 2.1: (a) Schematic view of a fabricated graphene device (b) Optical microscope image of a block of devices

2.1.2 Presence of polymer residue after device fabrication

Because of the transfer and lithography processes, polymer residues are almost always present at the surface of the graphene, as reported in various works [81–85]. We observe similar graphene residue in our case. Figure 2.2(a) shows the 2D band Raman mapping of a graphene device containing a graphene-free area as there is no 2D peak (dark area). The corresponding AFM image of the dashed blue frame is shown in Figure 2.2(b).

Using the height of the graphene-free area (likely the SiO_2 surface) as a reference, the cross-section plot in Figure 2.2(c) reveals a step height between the graphene-free and the graphene covered areas of $\approx 3\text{nm}$. Since clean monolayer graphene is usually observed to have a thickness of about 0.4 to 1.7nm [86] on AFM, the only possibility is that additional material must be

present to account for this discrepancy. This strongly suggests that graphene is contaminated with polymer residues at the surface of our devices. This finding will be taken into account in the next sections.

We note that metallic contaminants such as copper or iron can also be present. Since the graphene was transferred from a copper substrate to a Si/SiO₂ substrate, some copper contaminants may remain at the surface. This is shown in the work of Lupina et al. [87] where copper atom concentrations of $10^{13} - 10^{14} \text{ cm}^{-2}$ were found. However, its concentration is too small compared to that of a 2nm-thick pure copper layer ($1.71 \times 10^{16} \text{ cm}^{-2}$). Therefore, this suggests that most of the residue is polymer-based with metallic contaminants in small concentration.

Figure 2.2: (a) 2D band raman mapping of the area where graphene is damaged. The corresponding AFM image of the dashed blue frame is shown in (b). (c) Cross-section plot extracted from the AFM image (dotted yellow line)

2.1.3 Electrical characterisation of the graphene devices

We measured the resistance of a large number of devices in order to extract both the graphene sheet resistance ρ_g and the contact resistivity ρ_c between the gold electrodes and the graphene.

The resistance R of the device is :

$$R = \rho_g \frac{L}{W} + 2\rho_c \frac{1}{W}, \quad (2.1)$$

where L is the distance between the electrodes and W is the graphene band width (as indicated in Figure 2.1(a)).

To determine both ρ_g and ρ_c , we plotted $R \times W$ vs L . The corresponding equation is:

$$R \times W = \rho_g L + 2\rho_c \quad (2.2)$$

By measuring the resistance of 68 devices, we plotted the data in Figure 2.3. Using equation 2.2, the slope and the intercept are, respectively, ρ_g and $2\rho_c$. The results are summarised in Table 2.1. Our linear fits reveal a high standard deviation for the fitting parameters. Assuming that the model (Ohm's law 2.2) is valid, other factors such as graphene quality, polymer presence, defects or instruments errors may yield individual variations that affect the correlation coefficient and, in turn, the error. For instance, a high ρ_c often arises from photoresist residues present between gold and graphene. Some areas of the wafer may have more polymer residues than other areas. Comparing the sheet resistance of graphene, the manufacturer specifications predict ρ_g ranging from 660 to 1500 $\Omega/\square$ which is more than twice as low as our value. This suggests that graphene may have been damaged during the fabrication process.

Figure 2.3: $R \times W$ as a function of L for 16 devices. The red dashed line is the linear fit. Its equation is also displayed.

	$\rho_g(\Omega/\square)$	$\rho_c(\Omega.m)$	Device count	R^2
Chip D	2941 ± 494	2526 ± 1042	16	0.73

Table 2.1: Fitted values following equation [2.2](#)

2.2 Inducing electro-burning

Figure [2.4](#) shows the typical electro-burning curve of a graphene device. The voltage is increased gradually until an abrupt total loss of conduction is observed. In some cases, we detect a tunnelling current. Figure [2.4\(b\)](#) shows the I-V curve of a device after electro-burning. It can be fitted with high accuracy by the Simmons model for tunnelling [\[71,88\]](#) (red dashed line). Barrier width estimated by fitting the I-V curves range from ≈ 1 nm to 2 nm. Above ≈ 2 nm, the tunnelling current levels are below the detection limit of our equipment.

We note that in some cases, electro-burning occurs in steps. Several current drops may be needed to reach the minimum conduction (Figure [2.5](#)). As seen later in section [2.4](#), each drop correspond to a specific part of

Figure 2.4: (a) I-V curve showing the electro-burning of a graphene device (b) I-V curve of a device after electro-burning (black) and its fitting with the Simmons model for tunnelling (red dashed)

the graphene that is electro-burnt.

Figure 2.5: I-V curve showing the electro-burning of a graphene device occurring step by step

To analyse the process from a statistical standpoint, we performed electro-burning over a large number of devices both in vacuum and air environment. In the graphene devices studied here, vacuum electro-burning occurs at an average power density of $\approx 280 \pm 140 \text{ kW/cm}^2$ corresponding to temperatures around $1300 \pm 750 \text{ K}$ as estimated from the linear relationship between absorbed power and temperature uncovered in graphene transistors [89]; these values are consistent with reported sublimation temperatures of graphene on

$\text{SiO}_2 \approx 1050 \text{ K}$ [89] In air, electro-burning occurs at a lower average power density of $\approx 80 \pm 30 \text{ kW/cm}^2$. The estimated corresponding temperature is $\approx 616 \pm 100 \text{ K}$. It is consistent with Liu et al. reporting on Joule-heating induced air oxidation of monolayer graphene (oxidation temperatures $\approx 720 \text{ K}$ [90]). For the rest of the manuscript, except for section 2.4, electro-burning is only performed and studied in air environment.

2.3 Characterisation after electro-burning

2.3.1 Raman spectroscopy

Figure 2.6(a,b) show a raman map of a device after electro-burning (spatial resolution: $\approx 500 \text{ nm}$). A crack-like feature systematically appears: a darker region crossing from one edge of the graphene band to the other (lower 2D peak intensity). Aside from seeing a drop in the 2D and G band intensity, the raman spectrum corresponding to this darker region (Black spectrum in Figure 2.6(c)) displays wider peaks and a higher D peak intensity than the rest of the graphene layer. This is consistent with the formation of a physical gap as graphene edges are known to activate the D band [91], hence indicating the presence of edge defects. However, the disorder does

Figure 2.6: Graphene device after electro-burning : (a) D and 2D (b) peak raman maps, (c) Raman spectra of the graphene far from the crack and at the location of the crack.

not entirely explain the peculiar shape of the D and G peaks (very wide at its base). We attribute this broadening to the presence of amorphous carbon arising from the pyrolysis of the photoresist residues. Indeed as shown in Figure 2.7(a), the D and G peaks can only be fitted with 4 Lorentz functions instead of 2. These findings suggest that a certain amount of amorphous carbon is present over the graphene at the crack location. This compares well with the work of Hong et al. [92] who observed a similar Raman signature on annealed graphene. In support of this claim, we also find, in some cases, amorphous carbon far from the crack where only 3 Lorentz functions are used to fit the spectrum (Figure 2.7(b)). Indeed, in this case the graphene D peak is absent since there is no edge.

Figure 2.7: (a) Lorentzian fits at the location of the crack (b) Lorentzian fits far from the crack where amorphous carbon was found

2.3.2 Atomic Force Microscopy

Atomic force microscopy (AFM), is a powerful tool to characterise the graphene devices after electro-burning. The crack is easily visible as a trench linking both edges of the graphene device (Figure 2.8).

It is challenging, however, to determine the real topography of the nanogap. Indeed, the AFM does not give information on the nature of the material. Therefore, it is impossible to confirm that the edge of the trench corresponds to the graphene edge.

To perform consistent measurements of the nanogap width, we high-

Figure 2.8: AFM image of a graphene device after electro-burning

lighted in blue the areas with a height below a certain threshold (Figure 2.9). This threshold was chosen arbitrarily slightly below the graphene surface so that the blue area clearly outlines a crack-like feature. In doing so, we aim at matching, if possible, the edges of the blue area and the real graphene edges. Therefore, we estimate the nanogap width by measuring the distance between these edges.

Figure 2.9: AFM image of the nanogap region, areas below a chosen threshold are highlighted in blue to define the nanogap edges.

Table 2.2 summarises the statistics obtained for four different devices. First, we observe that the nanogap width varies greatly along the nanogap

Device		1	2	3	4
Electro-burning voltage (V)		42.3	52.7	12.3	10.0
Current density ($10^8 A/cm^2$)		3.4	3.2	1.0	0.3
Width (nm)	Average	52.5 ± 31.3	76.8 ± 33.4	13.6 ± 4.8	13.2 ± 5.9
	Max	139.7	164.9	21.8	27.6
	Min	14.9	10.7	5.0	6.3
	# values	42	44	29	13
Depth(nm)	Average	3.3 ± 1.6	7.0 ± 2.7	4.8 ± 0.8	2.5 ± 0.7
	Max	9.3	17.5	8.0	5.4

Table 2.2: Statistics of the nanogap morphology obtained for 4 different devices.

path. Indeed, in all four devices, the standard deviations of the width account for more than 35% of their average. Second, the average width varies greatly from one device to the other. However, the minimum width values are similar for all devices. This suggests that, even when the average nanogap width is large (e.g. device 2), it may remain narrow at isolated locations. This is consistent with the AFM observations of Prins et al. [71] where an isolated narrow constriction is observed along a wide nanogap. Interestingly, the average width is significantly lower when the device breaks at lower voltage and current density. This finding suggests that the observed differences in average width could arise from a different voltage/current when electro-burning occurs.

Analysing the nanogap depth, for 3 devices we find an average depth of 2 to 4nm. These values are consistent with the thickness of graphene covered with a thin layer of photoresist. We note that, for device 3, the average depth is higher (7.0 ± 2.7). Additionally, the maximum depth is 17.5 nm (device 3). Because graphene + photoresist were measured to be about 3nm thick(section 2.1.2), this suggests that the underlying SiO_2 was possibly damaged during electro-burning, also observed in previous works [80,93].

2.4 In-situ SEM

To gain more insight into the electro-burning process of graphene, we performed in-situ electro-burning of graphene inside a scanning electron microscope (SEM). The experiment was conducted at the Institut d'électronique de microélectronique et de nanotechnologie (IEMN) in Lille. The institute has an SEM with micro-probes inside the chamber for electrical contacts (Figure 2.10). The voltage was controlled using a LabVIEW program which

Figure 2.10: SEM image of the chip along with two micro-probes that were used to contact the devices

allowed to apply voltage biases and sweeps. The SEM accelerating voltage was 5kV. The typical radius of the contacting probe was 12μm, compatible with our design.

2.4.1 Active voltage contrast

When a voltage is applied, a strong contrast appears between the two electrodes (Figure 2.11(a)). This is due to a phenomenon called active voltage contrast [94]. The positive side of the device appears darker because the scattered secondary electrons (negatively charged) are attracted back to the

electrode. On the opposite side, the other electrode is negatively or not charged. Thus, the detector receives more signal resulting in a brighter area. This principle is similar for passive voltage contrast where no voltage is applied to the device (see section 4.6.1). Within the graphene, the contrast appears as a brightness gradient going from dark to light grey which roughly yields a spatial mapping of the electric potential. Therefore, by observing gradients, it is possible to approximately locate the current paths. As sketched in Figure 2.11(b), the technique also highlights the areas where graphene is absent.

Figure 2.11: SEM image of a graphene device showing the active voltage contrast under a 10V bias. The positive electrode is darker than the negative one

2.4.2 Broken devices under a constant bias

Figure 2.12 shows a graphene device under a 10V bias before and after electro-burning. As shown in Figure 2.12(b), the brightness gradient within the graphene is replaced by a clear contrasting line stretching across the de-

Figure 2.12: SEM image of a graphene device under a 10V bias before(a) and after(b) electro-burning

vice. This contrast highlights the disconnection path created during electro-burning.

Zooming at the cracked location, Figure 2.13(a,b) shows zoomed views of the nanogap, respectively, at 0V and 10V bias. In (a), a morphological trench is observed. It is very interesting to note that the path of the trench observed in (a), corresponds to the disconnection line highlighted in (b). Moreover, the trench resembles those observed with the AFM (Figure 2.14). This is consistent with the assumption that the topographic trenches observed both with AFM and SEM are precisely positioned where graphene has opened during electro-burning. This finding improves the accuracy of the AFM results.

Figure 2.13: SEM images of a graphene device after electro-burning under 0V(a) and 10V(b) bias. In(b), the nanogap path is highlighted with a yellow dotted line.

Figure 2.14: Zoomed view of the nanogap at 0V bias

We note that resolving the crack morphology is very challenging with the SEM. For instance in Figure 2.14 the scanning speed had to be significantly lowered. As shown in the next section, for video recording, we had to increase the scanning speed at the expense of the resolution.

2.4.3 In-situ electro-burning observation

In this section, we aimed at observing the graphene device while applying an increasing voltage ramp in order to induce electro-burning. Simultaneously, we recorded a video by taking images every 4 seconds.

Figure 2.15(a,b,c,d) shows frames recorded at different timings. The timings of each image is reported in Figure 2.15(e) showing the I-V curve of the experiment. We observe two current drops suggesting that electro-burning occurred in two steps. However, the second current drop at 52s did not result in any change in the video. We listed below a chronological description of the images :

- (a)1.7V 4s** The image shows the initial state of the device.
- (b)13.2V 31s** The device is strongly biased. The voltage contrast is intense. A slight brightness gradient can be observed on the graphene suggesting that electrons are flowing freely across the device.
- (c)15V 35s** A sharp disconnection line has appeared, suggesting that electro-burning has occurred between 31 and 35s. This is consistent the sudden loss of conductivity shown in (e)
- (d)0V 65s** The device is broken and has an infinite resistance. Interestingly, although the voltage is 0V, a slight residual voltage contrast can still be observed.

This experiment shows that the appearance of the disconnection line (nanogap) is synchronised with the loss of conductance. The nanogap is

formed during the 4 seconds interval between (b) and (c). Assuming a propagative process, it is challenging to conclude on a specific nanogap propagation speed. For example, the nanogap formation could have very well initiated anytime during the interval. Also, because of the dynamic nature of crack propagation, the propagation speed is probably not constant. This is very well shown in the in-situ TEM videos from Barreiro et al. [70]. The nanogap first propagates slowly, then suddenly accelerates.

Figure 2.15: (a,b,c,d) SEM images of a graphene device taken at different timings during electro-burning. (e) I-V curve of the experiment, the timings of each SEM image are highlighted in red.

2.5 In-situ infrared thermography

In view of these conclusions, we now aim at complementing our study from a thermal perspective. Consequently, we performed another in-situ experi-

ment with an infrared (IR) thermal camera.

2.5.1 Equipment

We performed infrared thermography with a TELOPS high-definition mid-wave camera yielding a spatial resolution of $4.75\text{ }\mu\text{m}$. The acquisition wavelength ranges from 3 to $5\mu\text{m}$. The silicon chip containing the graphene device was glued to a larger chip (Figure 2.16) to allow gold micro-wire bonding.

Figure 2.16: Photograph of the silicon chip attached within a larger chip

2.5.2 In-band radiance of a silicon chip

For a material with an emissivity ϵ independent of the wavelength λ (grey body), the in-band radiance P emitted by this material is essentially the integration of Planck's law over a specific wavelength interval $[\lambda_{max}; \lambda_{min}]$:

$$P = \epsilon \int_{\lambda_{min}}^{\lambda_{max}} \frac{2hc^2}{\lambda^5} \frac{1}{e^{hc/(\lambda kT)} - 1} d\lambda \quad (2.3)$$

Where h is the Planck constant, λ is the wavelength, c is the speed of light, k is the Boltzmann constant and T is the temperature.

However, this equation is valid for a single emitting material. In our case, silicon and graphene are both grey bodies emitting in the IR region. The

emissivity of highly doped silicon is 0.6 [95]. Graphene has a much lower emissivity of 0.02 [96]. We neglect the SiO₂ layer (transparent at 90nm thickness). Therefore, the total radiance of the device is $P_{tot} = P_g + P_{Si}$.

Additionally, because graphene itself is the only source of heat, its temperature T_g is slightly higher than the underlying silicon temperature T_{Si} . It is usually assumed that $T_g = A \times T_{Si}$ where A is constant [72][97]. We assume, as estimated in the simulation results taken from section 4.8.1 that $T_g = 1.2 \times T_{Si}$.

Figure 2.17 shows a theoretical plot of the emitted radiance as a function of the silicon temperature plotted using equation 2.3. As indicated in the legend, the black, red and blue lines are, respectively, P_{Si} , P_g and P_{tot} .

Because graphene has a very low emissivity, it only accounts for a very small fraction of the emitted radiance P_{tot} . Therefore, we assume that $P_{tot} = P_{Si}$. The relevance of this assumption can be assessed by taking the temperature difference between P_{tot} and P_{Si} . As shown in Figure 2.17(b), for a given radiance of 64 W/m²/sr, T_{Si} is overestimated by 7.1 °C because of the graphene contribution to the total radiance. This difference is not negligible but only accounts for a few % of the absolute temperature values reported in the next sections. This does not impact the interpretation of the results. Therefore, we assume that the thermal image displays the temperature of the silicon substrate.

2.5.3 Temperature estimation

The thermal camera provides a value of radiance P_{cam} for each pixel :

$$P_{cam} = P_{Si} + P_{bg}, \quad (2.4)$$

Figure 2.17: (a) Theoretical in-band radiance of graphene, silicon and silicon + graphene as a function of the temperature. (b) Zoomed view showing the error in estimating T_{Si}

where P_{bg} is the radiance received from the background. Using equation 2.3 this yields:

$$P_{cam} = \epsilon \int_{\lambda_{min}}^{\lambda_{max}} \frac{2hc^2}{\lambda^5} \frac{1}{e^{hc/(\lambda k T_{Si})} - 1} d\lambda + (1 - \epsilon) \int_{\lambda_{min}}^{\lambda_{max}} \frac{2hc^2}{\lambda^5} \frac{1}{e^{hc/(\lambda k T_{bg})} - 1} d\lambda, \quad (2.5)$$

where T_{bg} is the background temperature. By numerically solving equation 2.5 with MATLAB, we can estimate the silicon temperature T_{Si} and obtain a thermal photograph of the chip (Figure 2.18). Because of their almost negligible emissivity, the temperature readings of the gold electrodes are not relevant; these areas appear black in the IR images.

2.5.4 In-situ electro-burning

Similarly to the previous in-situ study (section 2.4), we recorded videos while applying a voltage ramp to observe electro-burning. Figure 2.19(a,b,c,d) shows the thermal images of a graphene device taken at different timings. The timings are indicated in the I-V curve below (Figure 2.19(e)). We listed below a chronological description of the images :

(a) 21V 0.5s The image shows the initial state of the device. The silicon temperature is about 22°C.

(b) 49V 18.5s The device is strongly biased. The maximum temperature

Figure 2.18: Thermal image of the idle chip surface. The gold electrodes appear black because of their negligible emissivity.

of the silicon is 178°C . A large hot spot is present at the centre along with a smaller one at the top left.

(c) 54V 22.5s This is the last frame before electro-burning occurs. The two hot spots are now easy to distinguish. The maximum temperature is 213°C .

54V 22.525s The device is broken. The temperature has dropped suddenly from 200°C to 70°C in 25ms. Due to another device being biased in the vicinity of this device. The temperature remains high.

2.5.5 Analysis of the heating rate

Investigating the dynamics of electro-burning, we plotted the temperature vs time for two pixels located on the graphene device (Figure 2.20). Interestingly, we noticed a sudden increase of the temperature just before

Figure 2.19: (a,b,c,d) Thermal images of a graphene device taken at different timings during electro-burning. (e) I-V curve of the experiment, the timings of each image are highlighted in red.

electro-burning occurs for T1. For T2, we can observe a slight temperature drop.

To clarify this peculiar phenomenon, we plotted spatial mappings of the heating rate $\Delta T/\Delta t$ extracted a few frames before electro-burning in Figure

[2.21](#)

(a) 75ms to electro-burning Most of the device heats up at a steady rate of 10-20°C/s. Interestingly, a small region at the top centre starts to cool down at a rate of -30°C/s. Also, the immediate sides of this cooling region are heating up faster than the rest of the device (up to

Figure 2.20: (a) Temperatures T1 and T2 as a function of time for two pixels. The pixel locations are shown in the thermal image(b)

Figure 2.21: Spatial mappings of the heating rate $\Delta T/\Delta t$ extracted during electro-burning.

80°C/s)

(b)50ms to electro-burning The cooling region has shrunk (-30°C/s).

However, on the sides of this region, the heating rate has suddenly accelerated (150-230°C/s.)

(c)25ms to electro-burning The cooling region has considerably expanded over the whole width of the device. The cooling rate has also accelerated to -110°C/s. Despite its smaller size, the heating region still heats up at a rate of 230°C/s.

(d)54V Electro-burning The device breaks. The temperature drops sud-

denly at an impressive rate of several thousand degrees per second.

The above results are strong evidence of the heterogeneity of the electro-burning process. Not only we observed spatial heterogeneities in temperature (section 2.5.4), but we observed important spatial variations in heating rates a few hundreds of milliseconds before electro-burning. More importantly, the peculiar presence of this cooling region is fascinating. This lack of heating source could be explained by a localised loss of conduction which, in turn, could be caused by the propagation of a nanogap initiating at the centre and expanding in two directions towards the edges of the graphene flake. Therefore, with a nanogap halfway propagated at the centre, the current would be forced to crowd at the sides thus consistently increasing the heating rate. Assuming that this scenario is valid, we estimate the propagation speed of the nanogap to be roughly about 10-40 $\mu\text{m/s}$.

2.5.6 Heating of the chip

In this section, we examine the heating of the silicon chip at a larger scale. Figure 2.22, shows a thermal image of a large portion of the chip at the electro-burning point. Interestingly, the amount of heat generated is such that substrate temperatures of $\approx 80^\circ\text{C}$ spread over more than one millimetre around the device. Even 3 mm from the heated device, the chip is still at 55°C . Therefore, electro-burning a graphene device may also thermally damage adjacent devices. After electro-burning, We have sometimes observed burnt photoresist residues around the device.

2.6 Interpretation

Based on the experiments shown above, we aim at understanding the physical mechanisms of the electro-burning process.

Figure 2.22: Thermal image of the chip before electro-burning occurs.

2.6.1 Summary of the observations

Electrical characterisation: When the voltage is sufficiently high, one or several current drops occur until a complete loss of conduction. The loss of conduction is sudden and usually occurs in less than 100ms. In vacuum, electro-burning requires more energy than in air (oxidation vs sublimation).

Raman spectroscopy: On the mapping, a crack-like feature systematically appears. Remains of amorphous carbon (burnt photoresist) is systematically found at the crack vicinity. Interestingly, amorphous carbon is not usually found far from the crack. This suggests that heat concentrated specifically along the crack.

AFM: The topography of the crack is a nanometre-spaced gap (nanogap). The width of the nanogap varies greatly along its path. Higher electro-burning current densities and voltages seem to induce larger nanogap width. Nonetheless, it always has very narrow constrictions less than 10nm in width. The damaging of the underlying SiO_2 confirms the Raman spectroscopy observations: Highly localised heating is present along the crack.

In-situ SEM: The path of the nanogap coincides with a loss of conduction

across of the device.

In-situ Thermography: Significant joule-heating is observed with silicon temperatures rising to 213 °C. This means that T_g may reach at least 255°C if not more. Also, the temperatures are spatially heterogeneous with clear circular hot spots.

2.6.2 Discussion

Based on our observations, all evidence point towards a highly heterogeneous process: First, graphene only breaks along the nanogap as confirmed with Raman, SEM, and AFM. Second, the thermal images show the formation of hot spots forming several seconds before electro-burning Third, less than 100ms before the loss of conduction, the heating rate becomes spatially heterogeneous(section 2.5.5). We attributed this observation to a nanogap initiating at the centre of the flake and propagating towards the edges. The assumption of a propagative process is consistent with the in-situ TEM (Transmission electron microscope) observations from Barreiro et al. [70]. Additionally, since we consistently observe a single nanogap path with no additional ramifications, the whole crack likely originates from a single starting point propagating either in both directions or from one graphene edge to the other.

This heterogeneity may be attributed to two factors: first, the heterogeneity of resistivity which causes differentiated Joule heating and thus hot spots at locations with higher resistivities. For instance, when graphene of CNTs are under high bias, the carrier concentration (hence the resistivity) becomes spatially heterogeneous due to electrostatic effects [72][80]. As a consequence, a localised polarised heating with a hot spot appears. Additionally, the heterogeneity of resistivity may be caused by defects, either punctual (e.g vacancies) or extensive (holes, tearing, defect line) [98][99] also leading to heterogeneous heating.

Second, the heterogeneity of the lattice itself: indeed, at the atomic scale, thermal oxidation of a graphitic layer has been shown to initiate from point defects (e.g monovacancies, divacancies) [100][101] which is consistent with the fact that carbon atoms in defect sites require less energy to break free than in perfect lattice sites (7eV vs 30 eV) [102]. Indeed, there is a strong enhancement of current densities, and thus of Joule heating, around sharp features, notably crack tips [73]. Therefore, we propose that defects are used as seeds to initiate the propagation. As the defect expands, it could locally create a dynamic hotspot further facilitating the graphene destruction by propagating a nanogap. Naturally, as the crack propagates, current crowding is heightened hence accelerating the propagation until a loss of conduction is reached. This concept of hot nanogap propagation is consistent with our Raman and AFM observations: Carbonisation of the photoresist and damaging of the SiO₂ specifically along the nanogap.

To explain the peculiar damaging of the oxide, another possible mechanism could be electric-field driven, occurring by electrical breakdown of the oxide. Indeed, SiO₂ has a dielectric strength of 500MV/m [103]. Therefore, considering a 20nm wide graphene nanogap, it only requires a voltage of 10V to induce electrical breakdown of the oxide. A typical electro-burning voltage is usually above 20V. This hypothesis is supported by several works dealing with the resistive switching of SiO₂ in nanogap systems [93][104][108]. These reports show that the underlying oxide undergoes important structural changes during electro-burning and suggest the presence of a filamentary conduction within the oxide. This concept of filament is consistent with an electric-field induced damaging of the SiO₂.

Multiple observations also show that, after the loss of conduction, the system is still active if the voltage remains applied. Indeed, the duration at which the voltage remains applied just after the loss of conduction is a critical factor conditioning the gap size. In order to narrow down the gap size,

researchers use feedback controlled electroburning where the variations of conductance are monitored during the voltage ramp. When the conductance drops of more than 10%, a feedback condition is triggered and the voltage is swept back to zero instantly. Afterwards, a new voltage ramp starts again etc. This process allows to obtain a much higher yield of nanogaps widths between 1-3nm [8,71,73,109-112].

2.7 Conclusion

To conclude this chapter, we have successfully provided a comprehensive study of graphene electro-burning. By applying voltage ramps to newly fabricated resistive graphene devices, we performed electro-burning on a large number of devices. Raman spectroscopy combined with AFM revealed the formation of a crack-like feature splitting the graphene device into two parts. Analysing its morphology, we concluded that the nature of the crack was a nanometre spaced physical gap (nanogap). Eventually, we carried out two in-situ experiments with an SEM and a thermal infrared camera.

By interpreting our observations, we speculated that electro-burning of graphene is a thermally driven mechanism occurring through oxidative burning in air environment. Particularly, it is a highly heterogeneous propagative process. Indeed, current crowding creates local hot spots that are likely to host crack initiation. We proposed that defects are the key enabler of the propagation acting both as seeds to initiate the crack but also as guides to direct the nanogap through its propagation. Although only graphene is studied here, the logic could be applied to both graphite and CNTs as they essentially have the same lattice structure. They only vary in morphology. Overall, if we employ such materials in a carbon-based circuit, our results suggest that localised heating caused by current crowding may lead to early failure. As seen in Chapter [5], an anisotropic interconnect combined with a

high frequency tends to increase current crowding. Therefore, steps must be taken to limit crowding to improve the reliability.

Chapter 3

Defect engineering using femtosecond laser annealing

In Chapter [2](#) we have seen that thermal failure through dynamic current heterogeneities. Indeed, this involves the formation of hot spots that could lead to the irreversible thermal failure of the circuit. To avoid this phenomenon, we aim at studying the mechanisms of localised heating in monolayer graphene.

This intense localised heating can be reproduced and controlled using femtosecond laser irradiation. In terms of spatial profile, reported simulations show that the Joule-heating induced hot spot is as sharp as 1-2 μm thus consistent with our laser spot size [\[97\]](#). The thermal profiles are expected to be similar. Furthermore, since we established that oxidative burning occurs in both cases, the temperatures levels should be similar. Overall, by performing laser irradiation, we are introducing localised thermal loading without nanogap formation.

This Chapter presents, in the first part, a detailed description of the femtosecond laser apparatus that we constructed. Then, we took advantage of this newly built optical setup to carry out systematic studies on the laser annealing of monolayer graphene. Finally, we also present other results

obtained by annealing other nanostructures similar to graphene and CNTs such as monolayer boron nitride and gallium nitride nanowires.

3.1 Femtosecond laser

3.1.1 Description of the laser

Table 3.1 lists the specifications of the femtosecond laser used in our experiments.

Nominal Power (800nm)	4W
Wavelength range	670 to 1080nm
Pulse width	140 ± 20 fs
Spatial mode	TEM ₀₀
Beam diameter	1.2 ± 0.2 mm
Beam ellipticity	0.9 to 1.1
Repetition rate	80 MHz

Table 3.1: Specifications of the Coherent Chameleon Ultra II Titanium-Sapphire femtosecond laser

Pulse width It is the duration of a single pulse. The pulse duration is related to the width of the gain profile. In our case, it is very wide ranging from 680nm to 1080nm. This allows very short pulse duration from 5 fs to 100fs [113].

Spatial mode TEM₀₀ It is the main mode which results in a Gaussian beam profile (Figure 3.1)

Beam ellipticity Beam ellipticity: Ratio of greater over lesser beam diameter. In Figure 3.1, we can see that the beam is not perfectly circular thus slightly elliptic.

Repetition rate Number of pulses per second. Here, our laser has a repetition rate of 80MHz. This is a typical value for mode-locked solid-state lasers (from 50MHz to 1GHz).

The laser fluence (energy per pulse) Φ_0 is:

$$\Phi_0 = \frac{2P}{\tau\pi w^2}, \quad (3.1)$$

where P is the incident power, τ is the repetition rate, and w is the distance from the centre of the beam when $\Phi = \Phi_0/e^2$ as sketched in Figure 3.1(b). In other words, it is defined as the $1/e^2$ beam radius.

Figure 3.1: (a) 2D beam profile of the pristine laser beam (b) Plot of the spatial distribution of the fluence. The beam radius w is defined at $\Phi = \Phi_0/e^2$ (c) Spectrum of the laser when it is tuned at 800nm (4W power)

Along with the laser head (Photograph in Figure 3.2), the laser is equipped with:

- A power supply: Its functions are to supply DC power for the laser diode system that pumps the gain medium in the Verdi laser head, control the servo loops, provide cooling for the laser diode assemblies, control and monitoring, data storage and a user interface.
- A miniature recirculating unit: A separate unit that is connected directly to the laser head. It performs the task of cleaning, conditioning and dehumidifying the air inside the laser head to maintain stability and long-term operation.
- A chiller that is constantly maintaining the baseplate within the laser head at 20°C.

Figure 3.2: Optical block of the laser

3.1.2 Lasing of Ti-Sapphire

The mechanism of lasing relies on multiple reflections occurring inside a semi-reflecting cavity. The cavity is filled with a medium (gas or solid). The feeding of energy (pumping) into this cavity induces population inversion producing more excited electrons at higher energy levels. These excited electrons may decay to a lower energy level by emitting photons. In a process called stimulated emission, all the produced photons are in phase and of the same wavelength. This results in a phase coherent directional ray commonly called laser (Light Amplification by Stimulated Emission). In our laser, the cavity medium is made of a solid crystal of Al_2O_3 doped with Titanium ions (Ti^{3+}). The doping is usually $10^{25}m^{-3}$ which represents 0.03% of its weight. Figure 3.3 shows us that this is a 4 level laser where the light emission occurs from the decay of level 2 to level 1. The lifetime at level 2 is much longer (3.2 us) than at level 1 (0.1ps). These are important parameters to achieve population inversion easily. The more populated the level 2 is compared to level 1, the higher the gain is.

In contrast with continuous lasers, the laser output is pulsed. It is

Figure 3.3: Band diagram of Ti-Sapphire laser (b)The

composed of regular bursts or pulses of light. This pulsating behaviour is achieved through a process called mode-locking. The technique consists of introducing a fixed phase relationship between the longitudinal modes. Constructive and destructive interferences between these modes produce a train of short pulses (Figure 3.4). The duration of the pulse depends on the wavelength range emitted by the gain medium. The wider the range is, the shorter the pulse is. A Ti-Sapphire crystal emits from 680 to 1080nm, which results in an ultra-short pulse of 140 femtoseconds.

Figure 3.4: Band diagram of Ti-Sapphire laser (b)The

3.1.3 Physics of femtosecond laser annealing

Femtosecond lasers have been shown to provide high precision capabilities at the sub-micron scale with minimum damage. Indeed, the ablation threshold

of a material is lower for femtosecond pulses [114][115]. Therefore, it reduces the damage outside the target region and improves the contour sharpness of the structure. Such behaviour was first believed to arise from non-thermal effects in the material during irradiation.

Furzikov et al. claimed that the irradiation mechanisms vary depending on the pulse duration τ compared with the phonon-electron relaxation time t_{e-ph} (≈ 1 ps) [116]. In order to explain these phenomena, we distinguish the temperature of the electrons and the temperature of the lattice (two-temperature model). The temperature of the lattice arises from the phonons (atom vibrations) and is the one related to heat while the temperature of the electrons is derived from the free electron density.

Figure 3.5: Temporal evolution after irradiation of the laser pulse (dotted line), the electron temperature T_e (red) and the lattice temperature T_L (blue). The electron and lattice temperatures are out of equilibrium until t_{e-ph} [10]

During the few femtoseconds following irradiation, the electron temperature rises while the lattice remains cold (Figure 3.5) with no atom vibration. This creates a free carrier plasma where about 10% of the valence electrons are removed from their orbitals [117]. As a consequence, the lattice is electronically weakened and structural changes may occur although the phonon temperature stays low (cold). If this occurs, it prevents any thermal diffusion

and thus results in a clean ablation area. However, the literature is not clear whether this type of mechanism really occurs. Recent papers suggest that non-thermal effect would only occur if the pulse intensity is high enough. In other words, the peak power would have to reach a given threshold. A too low pulse intensity would not sufficiently heat up the electrons to destroy the lattice so they would transfer their energy to the lattice in a process called thermalisation where melting and evaporation may occur afterwards [118]. As a suggestion, it would be more relevant to assume that both thermal and non-thermal effects occur simultaneously [119]. This would explain the discrepancies found in the literature when comparing different papers. The phenomena described above are only valid for single shot exposures. Indeed, our femtosecond laser has a repetition rate of 80MHz which lies at the highest range of values reported in the literature. Such a high repetition rate corresponds to an interval of about 10ns between each pulse. This may lead to coupling between successive pulses and accumulation of energy (incubation effect). According to Gamaly et al. [10], the presence of a "pre-pulse" or a "post-pulse" changes the rules since they contain energy influencing the irradiation effects of the main pulse. As a consequence, this could result in a reduction of the ablation threshold ϕ_{th} when the repetition rate is above a certain value. As mentioned earlier, low pulse intensities imply thermal effects. In our case, obtaining non-thermal effects would require reducing the repetition rate of the laser which can be done by purchasing additional tools (see section 6.1 about Pulse picker).

3.2 Apparatus

To perform controlled experiments, the output of the laser must be adjusted spatially and energetically with a set of optical components. Figure 3.6 shows a schematic view of the entire apparatus.

Figure 3.6: Apparatus of the setup

3.2.1 Exposure Control

- Laser power adjustment: The high 4W output power of the laser is attenuated by cross polarisation. Two linear polarisers (P1 and P2) sandwiching a half-wave plate are assembled at an angle of 90°. Depending on the angle ϕ of the half-wave plate, the laser power can be adjusted following Malus law:

$$I_{out} = I_{in} \cos^2 \phi.$$

, where ϕ is the angle between the polarisers.

- Exposure time control: A mechanical shutter is used to block or release the laser beam for specific durations. It can yield exposure times down to 50ms. Afterwards, the beam is fed towards 3 mirrors (M1 to M3) mainly used for alignment.

3.2.2 Focusing

- Beam broadening: The two lenses L1 and L2 are positioned with their focal points coinciding. They work as a telescope thus broadening the beam width. This increased the beam width to achieve better focusing through the microscope objective later on.
- The objective lens of 40x or 10x concentrates the laser beam on the sample surface yielding a spot diameter of 1.5 μ m minimum.

3.2.3 Imaging system

To display the sample surface, we implemented an imaging system with two removable beam splitters (BS1 and BS2), one lamp, one CCD camera and one lens (L3). The light from the lamp is reflected by BS2 and goes through BS1 and the objective to be focused onto the sample surface. The surface

reflects an image that goes back through the objective and is reflected by BS1 to be focused by L3 onto the CCD. Figure 3.7 shows two images obtained with the imaging system with the 10x and 40x objective. The quality of the image is lowered with the 40x objective mainly because of chromatic aberrations at L3 and the beam splitters.

Figure 3.7: Images of a sample taken with the 10x(a) and 40x(b) objective

3.2.4 Sample holder

We have implemented, in January 2016, a pico-motor translation stage (Figure 3.8). It has a 30 nm resolution increment and can move in two directions for 25mm. This allows to precisely aim and scan over samples at a wide range of different speeds in order to carry out dynamic exposures. The picomotor

Figure 3.8: (a)XY Newport pico-motor translation station (b) Photograph of the stage mounted within the optical setup

stage is remotely controlled with a computer. We have designed a Lab-View program to make the controls more user friendly. Figure 3.9 shows a

screenshot of the user interface. The program includes various features such as:

- Arrow buttons pointing in all 4 directions to manually control the position.
- Real-time display of the stage position coordinates
- Relative movement with a given number of steps
- Absolute movement with a given target position to reach.
- Control of the scanning speed and acceleration
- Set the origin (0,0) of the movement
- Command a zigzag motion to draw crenellated patterns (see section 4.6.1)

Figure 3.9: Screenshot of the user interface of the LabView program designed to control the motorised stage

The input commands of the motors are required in steps. Therefore, we carried out a calibration study to determine the step size. According to the manufacturer, the step size is around 30 nm, but each motor still has different step size that arise from manufacturing fluctuations. It is important to note

that the step size also changes between forward and backward movements (positive and negative voltage in the pico-motor). The calculated step sizes range from 15 nm to 27nm and are consistent with the specifications.

3.3 Laser annealing of monolayer graphene

3.3.1 Single exposure

Figure 3.10 shows a Raman spectroscopy characterisation of graphene after laser annealing with a fluence of 0.1 J/cm^2 during 5s. At this energy, there is no damage of the underlying substrate after irradiation since its modification threshold is higher [120][121] and we do not observe any change of Raman spectra of silicon after irradiation.

The mappings of the 2D, G, and D band are shown in (a,b,c), respectively. For all mappings, a clear circular pattern is visible at the centre corresponding to the irradiated area. No Raman signature of graphene is found within these areas. Spectrum 1 from Figure 3.10(d) confirms the total absence of graphene within the circular pattern. Indeed, the blue spectrum does not display any of the three typical graphene peaks. Therefore, laser annealing ablated graphene over a circular region of about $2.6\mu\text{m}$ in diameter. Interestingly, the D band mapping shows a high-intensity ring around the graphene edges. Since the D peak is activated when structurally defective hexagons are present, this suggests that the laser also created defects around the ablated area. Looking at spectrum 2, we can confirm the significant rise of the D peak within the defective ring as compared to the pristine graphene (spectrum 3).

The peculiar presence of this defective ring suggests that the sides of the laser spot might have damaged the graphene without complete ablation. This hypothesis is supported by the fact that the spatial distribution of the incident beam is Gaussian. Figure 3.11(a) shows a D band raman mapping

Figure 3.10: Raman spectroscopy of graphene after laser annealing with a fluence of 100 mJ/cm^2 during 5s 2D(a) G(b) and D(c) band Raman mappings, (d) Raman spectra of the corresponding locations shown in (c)

of graphene after annealing at a much lower fluence ($\Phi_0 = 11 \text{ mJ/cm}^2$). We observe a much larger defective ring. This suggests that graphene has two fluence thresholds. As displayed in Figure 3.11(b), Φ_a is the ablation threshold and, Φ_d is the damage threshold. For a beam with an incident fluence Φ_0 , ablation occurs around the central part of the beam since $\Phi > \Phi_a$. For the beam tails, we have, $\Phi_a > \Phi > \Phi_d$, resulting in damage leading to the formation of defects. Finally, outside the beam, $\Phi_a > \Phi_d > \Phi$, no changes occur within the graphene.

Starting from the Gaussian beam distribution shown in Figure 3.11(b), we have:

$$\Phi = \Phi_0 \exp\left(-\frac{2r^2}{w^2}\right), \quad (3.2)$$

where w is the beam radius, and r is the distance from the centre of the beam.

Following our previous logic, if $\Phi = \Phi_{th}$, where Φ_{th} is a modification

Figure 3.11: (a) D band Raman mapping of graphene after annealing at 11 mJ/cm^2 (b) Schematic plot of the Gaussian distribution of the incident fluence Φ_0 . A schematic of the graphene surface is shown at the bottom.

threshold, equation 3.2 becomes :

$$\Phi_{th} = \Phi_0 \exp\left(-\frac{4D^2}{w^2}\right), \quad (3.3)$$

where D is the affected diameter.

Isolating D this yields:

$$D = 2w \sqrt{\frac{1}{2} \ln \frac{\Phi_0}{\Phi_{th}}}. \quad (3.4)$$

Therefore, by fitting D vs Φ_0 , we should be able to determine both D and Φ_{th} .

3.3.2 Estimation of the fluence thresholds

To control the process of graphene annealing, we carried out a systematic study. We performed 30 static exposures of 5s in air with optical powers ranging from 500mW to 3mW. Figure 3.12 shows the Raman mappings of graphene after exposures from 188 to 62 mW (left to right). As expected, as we lower the incident power, the ablated diameter D_a and the damaged diameter D_d shrink.

Figure 3.12: ((a)2D and D(b) band Raman mapping of graphene after several exposures from 188 to 62 mW

To precisely measure the diameters on the Raman mappings, we adopted a methodology based on a fixed threshold (similar to section 2.3.2). Indeed, since graphene goes progressively from pristine to defective and then fully ablated, we need to define arbitrary limits using Raman quantities that are consistent with physical realities.

To estimate D_a , we used the 2D peak intensity which arises from the circular breathing of the hexagonal graphene lattice [122]. Therefore, if less complete hexagons are present, this directly lowers the intensity of the 2D peak. Thus, it is a good measure of the graphene integrity. Ablation occurs when the intensity of the 2D peak decreases to only 10% of its original value. This assumption is consistent with the work of Casiraghi et al. who investigated the Raman response of graphene at the edges [91].

For D_d , we used the ratio $I(D)/I(G)$ that is commonly used to quantify defects in graphene [123]. Graphene starts to be damaged when $I(D)/I(G) > 0.2$ which is considered to be a very low defect density [12][123][124]. We note that, after several Lorentz fits performed with the Origin software, the standard error of the Raman peak intensities are consistently below 2%.

Using the software Gwyddion, we can apply a mask based on a defined thresholds (3.13(a,b)). As indicated in (b), the diameter was measured by averaging the vertical and horizontal diameter. Figure 3.13(c) shows D_a and D_d as a function of the incident power. The data can be very well fitted using equation 3.4 ($R^2 > 0.9$). Table 3.2 summarises the result of the fitting. The beam radius ranges from 1.5 to 1.8 μm . The ablation threshold Φ_a is

Figure 3.13: (a) 2D and I(D)/I(G) Raman mappings after laser annealing at 57mW. A yellow and blue mask is applied to measure precisely the diameters. (c) Affected diameter as a function of the incident power. The fitted curves are shown in red.

11.8 mJ/cm^2 . As a matter of comparison, and for the same laser, Li et al. [125] find a much higher ablation threshold of 125 mJ/cm^2 while Beltaos et al. report a lower value of 4 mJ/cm^2 [126]. This discrepancy might come from the method used to calculate the fluence from the optical power. Some papers do not consider the beam radius by using the $1/e^2$ rule (see Figure 3.1(b)), they might consider a beam radius using the $1/e$ rule. In fact, this common mistake might lead to factor 2 to 4 error in calculating the fluence. Moreover, some papers do not even consider the incident beam as Gaussian. These reasons added to probable measurement uncertainties may lead to significant differences in the literature.

	Ablation	Damage	Comments
w (μm)	1.50 ± 0.04	1.84 ± 0.05	
P (mW)	33.6 ± 1.21	12.0 ± 0.91	
	11.8 ± 0.42	2.95 ± 0.22	Oxide 280nm
$\Phi(mJ/cm^2)$	5	1.8	Oxide 90nm
	125		Ref [125]
	4		Ref [126]

Table 3.2: Fitting results from the plot in Figure 3.13, estimation of the threshold for graphene on 90nm oxide, comparison with literature.

We note that the given thresholds are valid for monolayer graphene on

a 280nm thick SiO₂ layer. We have noticed that the threshold decreased for a 90nm thick oxide layer. This suggests that the annealing process is substrate dependent.

3.3.3 Defect generation

As shown in the diagram, a transition seems to exist between a perfect graphene lattice and a complete ablation. Therefore, as shown in the previous section, when $\Phi_a > \Phi_0 > \Phi_d$, only defects are introduced.

Testing this hypothesis, Figure 3.14(a) shows the I(D)/I(G) band mapping of graphene after annealing at $6mJ/cm^2$. Extracting the Raman spectrum from the centre of the annealed area(Figure 3.14(b)), the D peak rises sharply and also gives birth to the D' peak (related to defects) overlapping with the G peak. The ratio I(D)/I(G) is 3.2, which corresponds to an inter-defect distance L_d of 3.5nm. Since I(2D) is still higher than 10% of the 2D peak intensity of the pristine graphene, we consider that the material is not ablated. Therefore, we prove that we can introduce defects without ablation.

Figure 3.14: (a)I(D)/I(G) Raman mapping after annealing at $6mJ/cm^2$ (b) Raman spectra extracted from location 1 and 2 indicated in (a)

3.3.4 Dynamic exposures

Until now, we have only performed laser annealing at a single location at a time (static exposure). In this section, we take advantage of our automated

motorised stage to perform dynamic exposures by annealing graphene while moving the stage in order to pattern defect lines. Figure 3.15 shows a Raman mapping of the $I(D)/I(G)$ ratio after the first test with a scanning speed of $3\mu\text{m/s}$ at various fluences. The image clearly shows defined lines with a higher $I(D)/I(G)$. Counter-intuitively, the amount of defect does not seem to vary with the fluence. Although we applied fluences that are greater than the ablation threshold of graphene, $\Phi_a = 11.8\text{mJ/cm}^2$, ablation does not occur. Indeed, as shown previously, a steady state with ablation is reached after 5s of static exposure. As a matter of comparison, a scanning speed of $3\mu\text{m/s}$ is roughly equivalent to a static exposure of 0.6s. This evidence shows that laser annealing of graphene is a time-dependent process occurring in a few seconds.

Figure 3.15: (a) $I(D)/I(G)$ Raman mapping after dynamic exposures at a scanning speed of $3\mu\text{m/s}$ at different fluences

To gain more insights, we carried out a systematic study by scanning with 3 different speeds and fluences. For each defect line, we performed a Raman spectroscopy mapping. Then, we extracted the average value of $I(D)/I(G)$ over the irradiated area. Table 3.3 summarises the extracted values. Interestingly, the variation of fluence has almost no impact on the value of $I(D)/I(G)$ whereas the scanning speed is the determining factor. From a speed of $15\mu\text{m/s}$ to $1.5\mu\text{m/s}$, the ratio $I(D)/I(G)$ triples from 0.1 (no defects $L_d > 30\text{nm}$) to 0.3 (low defect density $L_d = 19\text{nm}$).

The fluences that are used for dynamic exposures are significantly higher than for static exposures. For instance, we use fluences ranging higher

than 28 mJ/cm^2 while the ablation threshold of graphene is $\Phi_a=11\text{mJ/cm}^2$. Therefore, we show that, in the dynamic regime, the scanning speed is a more important factor than the fluence. Following this logic, the results suggest that the generation of defects in graphene is time-dependant. By further reducing the scanning speed, we would tend towards a more static regime where the fluence would be the dominant factor.

		Speed		
		15 $\mu\text{m/s}$	3 $\mu\text{m/s}$	1.5 $\mu\text{m/s}$
Fluence	49 mJ/cm^2	0.1	0.22	0.344
	39 mJ/cm^2	0.112	0.234	0.314
	28 mJ/cm^2	0.098	0.217	0.238

Table 3.3: Table listing the average ratio $I(D)/I(G)$ for different fluences and scanning speeds

3.3.5 Sensitivity of defects to a subsequent exposure

By using the motorised stage, we can perform dynamic laser exposures to draw specific patterns on the graphene. Figure 3.16(a) shows a micrograph of graphene after scanning with 6.4, 7.5 and 8.7 mJ/cm^2 . The exposures were carried out from right to left at a speed of 120 step/s at three different fluences. As indicated, marking holes were drilled in the silicon to locate the starting and finishing point by annealing at very high fluence. The corresponding $I(D)/I(G)$ Raman mapping in Figure 3.16(b) shows the coil shape pattern of the annealing.

First, the mapping clearly shows that we can successfully control the irradiation of defect spatially, with a consistent defective line width of about 1 to 1.5 μm . However, Figure 3.16 shows that the defect density varies greatly along the defect lines. In particular, we notice a localised increase around the first marking hole which contains defects. The phenomenon does not appear around the "finish" marking holes located on the left of each coil. It seems that the initial defects introduced initially by the "start" marking

holes tend to spread around when the femtosecond laser scans over them a second time. This observation highlights the sensitivity of defects to a subsequent laser exposure (or source of energy) and their ability to spread along that dynamic exposure. This finding is crucial because it suggests that graphene becomes unstable when containing defects. We note that this phenomenon was repeatedly observed with other exposures.

Figure 3.16: (a) Micrograph of the mapped area after annealing at 6.4, 7.5 and 8.7 mJ/cm². (b) I(D)/I(G) Raman mapping of the scanned area. The bright spots are marking holes drilled on the silicon to locate the area after annealing. The exposures were carried out from right to left

3.3.6 Type of defect

In this section, we investigate the type of defect that is generated. To do so, we used the ratio $I(D)/I(D')$, which, according to Eckmann et al. gives information about the defect type [127]:

$I(D)/I(D')=13$ sp^3 -type Impurities are attached at the surface of graphene.

They change the hybridisation of the graphene bonds [128].

$I(D)/I(D')=7$ Vacancy type One, or several atoms are removed from the lattice. [129]

I(D)/I(D')=3.5 Grain boundary One-dimensional defects marking the limit between two grains, usually a combination of vacancies and Stone-Wales defects (bond rotations) [130,131]

By fitting the Raman peaks with 4 Lorentz functions using SCILAB, we can extract the intensity of the D' peak that overlaps the G peak (Figure 3.17(a)). Figure 3.17(b) shows a Raman mapping of graphene after annealing at $13\text{mJ}/\text{cm}^2$ with a speed of $3.6\mu\text{m}/\text{s}$. The scanning was performed in a crenellated pattern to introduce defects over a squared shape area. From this mapping, we wrote a program to fit the peaks within all the Raman spectra. Finally, we extracted the ratio $I(D)/I(D')$ for the spectra with a detectable D' peak. Figure 3.17(c) shows the histogram of the $I(D)/I(D')$ values. The values range from 3 to 10. According to the literature, this suggests that sp_3 and vacancies defects are present. However, it is challenging to quantify their relative concentrations.

3.3.7 Discussion

Summary of the observations

- Graphene has two modification thresholds : Ablation $\Phi_a = 11.8\text{mJ}/\text{cm}^2$ and damage $\Phi_d = 2.95\text{mJ}/\text{cm}^2$
- The thresholds are lowered with a thinner oxide layer.
- By tuning the laser fluence, we can introduce only defects without ablation
- Defect creation with the laser is time-dependent, possibly occurring in a few seconds.
- If $\Phi_0 > \Phi_a$, ablation might not occur if the scanning speed is high enough.
- The defects are highly sensitive to a subsequent laser exposure.

Figure 3.17: (a) Raman spectra of defective graphene fitted with 4 Lorentz functions (b) $I(D)/I(G)$ Raman mapping of an area annealed at 13 mJ/cm^2 and scanned with a speed of $3.6 \mu\text{m/s}$. (c) Histogram plot of $I(D)/I(D')$ extracted from 39 Raman spectra

- The defects are likely to be vacancies and sp^3 .

Interpretation

As explained previously in section [3.1.3](#), the physics of annealing with ultra-short laser pulses is complex. Both thermal and non-thermal effects might be at play. However, the theory states that non-thermal effects usually lead to extremely fast lattice destruction occurring at the picosecond scale, virtually instantaneously.

From our experiments, we have seen that both ablation and damage are time-dependent mechanisms occurring within seconds. Therefore, these observations would not be compatible with a non-thermal effect. Instead of breaking the lattice, the femtosecond pulses would transfer their energy into heat. We note, nonetheless, that ablation of graphene might still occur partly

with non-thermal effects. This would be especially true at high fluences when electrons are more likely to be instantly knocked off from their orbitals instead of transferring their energy into heat.

The hypothesis that graphene laser annealing is mostly thermally-driven is supported by the fact that the mechanism is substrate dependent. Indeed, this is consistent with our observations and the literature [132][135]. The reasons of this dependence arise from the fact that graphene only absorbs 2.3% of the light [96] while a bulk silicon wafer absorbs 70% of it. Therefore, under laser annealing, heat is probably mostly generated at the silicon surface then travels towards the graphene through the oxide. As a matter of comparison, suspended monolayer graphene has a higher ablation threshold [134] since optical absorption of silicon does not occur. Moreover, heat is likely to be highly localised within the irradiated area. The high conductivity of graphene is eclipsed by the large cross-section area of the SiO₂ layer despite having a lower thermal conductivity (1.4 W/m/K). In other words, the heat generated directly flows towards the substrate without travelling across the flake.

In air environment, following the logic of a thermal effect, graphene is likely damaged through oxidative burning as suggested by several reports [132][135][135][136]. Additionally, the gradual formation of defects in the presence of oxygen at high temperatures is widely reported for CNTs [137], graphite [100][138] and graphene [90][101][139]. It is also fully consistent with our observations. Interestingly, the formation of vacancies is frequently reported in very good agreement with the Raman results [90][101][137][139].

Regarding the thermal stability of defects, disordered graphene is shown to have a lower oxidation temperature than its pristine counterpart [140][141]. This is consistent with the fact that carbon atoms in defect sites require less energy to break free than in perfect lattice sites (7eV vs 30 eV) [102]. Thus, irradiating defective graphene could increase the amount of defects even if

$\Phi_0 < \Phi_d$, in agreement with our observations.

To summarise, our interpretations suggest that femtosecond annealing of graphene is a thermally-driven phenomenon resulting in total or partial oxidation of graphene in air environment. This results in the formation of defects that significantly impact the thermal stability of the lattice.

To obtain solid evidence on the nature of the mechanism, a thermal camera could be implemented to the femtosecond laser setup. This would allow an in-situ temperature monitoring during laser annealing. However, extracting the exact graphene temperature might be challenging since the thermal camera sees mainly the temperature of the silicon substrate. For this experiment, it would be useful to consider using a transparent substrate (e.g. Sapphire) to avoid any parasitic radiation. A more precise approach would be to use Raman spectroscopy, to monitor the exact temperature of the graphene. As shown in refs [96, 142], it is possible to accurately probe the graphene temperature using the G band shift position. Such experiments would provide extremely valuable information on the nature of the irradiation mechanism.

3.4 Annealing of other nanomaterials

This section summarises the results obtained when annealing other nanostructure such as monolayer hexagonal boron nitride or gallium nitride nanowires.

3.4.1 Hexagonal boron nitride

In this section, we demonstrate the defect engineering of hexagonal boron nitride (h-BN) using laser annealing. We created optically active defects (colour centres) in h-BN monolayers via laser irradiation. We irradiated the area with the 40X objective at a laser power of 1.93W (fluence $2.11 J/cm^2$). Figure 3.18(a,b) shows a photoluminescence(PL) mapping of a laser-annealed

area. As seen in the micrograph (Figure 3.18(c)), the underlying silicon substrate was severely damaged. Hence, neither PL nor h-BN is found within the circular area inside the hole made in the substrate. However, the areas surrounding the hole exhibit high PL intensity. Figure 3.19(a), shows the

Figure 3.18: (a,b) PL mappings around the region annealed by the laser. (c) Corresponding micrograph of the irradiated region. The mapping areas are framed in blue(a) and red(b).

PL spectra of the h-BN annealed region. From the PL spectra, the main narrow peak at 624nm corresponds to an anti site complex $N_B V_N$ in which the nitrogen atom occupies the boron site while the nitrogen site is a vacancy nitrogen boron vacancy (Figure 3.19(b) [11]). The broad smaller peak centred at 640nm is attributed to cubic-BN vacancy defects [143]

By lowering the fluence, we demonstrate that colour centres can be introduced without damaging the substrate. Moreover, we showed that these defects can be used as potential single-photon sources. Hanbury-Brown-Twiss (HBT) interferometry was carried out to determine the second-order autocorrelation function $g^2(\tau)$. In short, this function assesses the coherence of a photon flow passing through a 50/50 beam splitter. Two detectors are placed at each exit of the beam splitter. For a single-photon source, a photon coming through one side of the beam splitter will not coincide with another photon at the same time. Therefore $g^2(0) = 0$ Figure 3.20

Figure 3.19: (a) PL spectra of laser annealed h-BN (b) Schematic view of a $N_B V_N$ defect reproduced from [11]

shows $g^2(\tau)$ for a colour centre created by laser annealing. We have a good single-photon source with $g^2(0) \approx 0.2$. This result indicates that single-photon

Figure 3.20: (a) Second-order autocorrelation function $g^2(\tau)$ as a function of the time delay τ for colour centres in h-BN flakes created with femtosecond laser annealing. (b) PL mapping of the corresponding area.

sources can be selectively engineered in h-BN by femtosecond laser annealing without damaging the substrate. These findings provide useful insights into the defect properties of 2D materials. We provide more details in our work published in the journal 2D Materials [144].

3.4.2 Gallium nitride

We performed a similar experiment on Gallium Nitride (GaN). We carried out femtosecond laser annealing on three configurations of GaN: First, a $1 \mu m$

thick GaN thin film grown by Metal-Organic-Chemical-Vapour-Deposition (MOCVD) on a sapphire substrate. Additionally, two types of GaN nanowires were grown on silicon by Molecular Beam Epitaxy (MBE): Mg-doped and intrinsic. The diameter of the nanowires was 40-50nm.

Figure 3.21 shows a comparative study of the three configurations after laser annealing at a fluence of $325\text{mJ}/\text{cm}^2$. Micrographs, Raman mappings of the E_2^H band and PL mappings are shown from left to right. The rows correspond to (a)GaN thin film (b)GaN nanowires and (c)Mg-doped GaN nanowires.

For all three configurations, the raman mappings show that the fundamental GaN E_2^H mode is removed after laser irradiation at the centre of the craters. This indicate either strong destruction of the crystal integrity or very low reflectivity of the sample caused by the crater topography. All PL mappings show the craters to be optically active. This confirms that femtosecond laser annealing is successful in introducing point defects that we can use as nano-sized light sources. Figure 3.22 shows the PL spectra of the GaN thin film, GaN nanowires and Mg-doped GaN nanowires with a peak emission at 626, 653 and 680 nm, respectively. Also, we have measured the lifetime decays to be 0.8 ± 0.01 ns for the GaN thin film, 1.1 ± 0.03 ns and for the GaN nanowires, 0.95 ± 0.01 ns. Summarising the results, we demonstrate the engineering of nano-emitters via femtosecond laser annealing of GaN. The emission arises from optically active defects. Depending on the configuration, the peak emission wavelength can be tuned from 626 to 680nm. Such tunable light sources could be useful in designing new lighting applications in optical devices within photonic circuits. We provide more details in our work accepted in the journal "Optical Materials Express".

Figure 3.21: From left to right: micrographs, GaN E_2^H Raman mappings and PL mappings of (a) GaN thin film (b) GaN nanowires and (c) Mg-doped GaN nanowires. The Raman and PL spectra are shown in the insets. The fluence of the femtosecond laser was 325 mJ/cm^2

Figure 3.22: PL spectra of GaN thin film, GaN nanowires and Mg-doped GaN nanowires.

3.5 Conclusion

This Chapter described, in the first part, the implementation of a new femtosecond laser annealing apparatus. The setup includes features such as an imaging system, a motorised sample holder and a set of polarising components to tune the laser power. We have also developed a LabView program for complete monitoring of the experiment with the computer. This allows to carry out safer and more reproducible experiments.

In the second part, we presented a comprehensive study on the femtosecond annealing of graphene. We demonstrated that laser irradiation leads to the formation of defects (mainly vacancies). At sufficiently, high power, graphene can be neatly ablated. Next, by using the motorised stage, we carried out dynamic exposures by using the motorised stage. By doing so, we presented a controlled method of engineering defects via ablation/modification at the micrometre scale.

Combining our observations with the literature, we ruled out the presence of non-thermal mechanisms because of the time-dependent nature of the defect formation. Therefore, we speculated that the observed substrate dependence is linked to heat extraction by the silicon wafer itself thus suggesting a thermally driven mechanism led by oxidative burning. Finally, we shed light on the instability of a disordered carbon lattice. From a reliability standpoint, this finding highlights the importance of keeping a low defect density when fabricating carbon-based circuits.

In the last part, we summarised the results of two laser annealing experiments performed using other nanostructures: monolayer hexagonal boron nitride and gallium nitride nanowires. The defects introduced via laser annealing are shown to be optically active, displaying strong photoluminescence responses. For boron nitride, we unveiled the single-photon generation potential of these nano-sized light sources. For gallium nitride, we showed that the photoluminescence mechanism is tunable from 626 to 680nm.

Chapter 4

Controlling electro-burning using laser patterning

In Chapter [3](#) we have observed that, after introducing defects with the laser, they were very sensitive to subsequent laser exposure. Notably, they would tend to spread quickly around. In this chapter, we study the worst case scenario for a carbon circuit: we combine laser annealing with electro-burning. In the meantime, a defect-induced weakening could also become an advantage.

4.1 Motivation

Indeed, nanogap systems have recently captured widespread attention for their numerous applications promoting the use of graphene nano-electrodes in integrated circuits. A trending approach is to use the nanogap as a receptacle to host external compounds bound to be the functional units of the device while the separated graphene flakes act as the electrodes. For instance, phase change materials can be introduced in the nanogap to make electronic switches [\[145\]](#). Because the nanogaps can be a few nanometers wide, single molecules can also be inserted to make transistors [\[71\]](#)[\[109\]](#)[\[146\]](#)–[\[154\]](#), DNA sequencers [\[155\]](#)[\[156\]](#) or quantum dots [\[74\]](#)[\[157\]](#) hence making

graphene nanogap systems extremely important in the field of molecular electronics.

In addition, after electro-burning, researchers have shown that conduction within the gap can be reversibly switched ON and OFF to make non-volatile memories [93][108][158][160]. Similarly to electro-burning, the devices are subjected to an increasing current sweep (0-20V) in order to induce an electro-forming (EF) of the underlying SiO_x . The aim is to enable conduction by triggering a dielectric breakdown within the oxide (Figure 4.1(a)). Figure 4.1(b) shows the SET process by which a device is turned ON (red line). Starting from the OFF state, during the downward voltage sweep (from 20 V to 0 V), the current increases noisily, then from 11 V downward, it decreases smoothly. The increasing voltage sweep shows the RESET process by which the device is turned OFF, an abrupt current drops occurs at 16V. The inset of Figure 4.1(b) shows that, when reading the current at 1V, I_{ON} is significantly greater than I_{OFF} . As shown in Figure 4.1(c), the endurance of the devices is also assessed. Some devices can switch for more than 125 cycles with a $I_{\text{ON}}/I_{\text{OFF}}$ as high as 10^4 , while others can switch up to 500 cycles with $I_{\text{ON}}/I_{\text{OFF}} \approx 450$. Much larger $I_{\text{ON}}/I_{\text{OFF}}$ ratio values can be achieved ($\approx 10^6$), though not yet with satisfactory endurance. However, less than 1 device out of 10 would show such high performances thus resulting in a very poor reproducibility. The results shown in Figure 4.1

Figure 4.1: (a) I-V curve showing the electroforming process of the device after electroburning, an unstable behaviour is observed along with large current fluctuations (b) I-V graph showing the RESET process achieved by sweeping the voltage up (dark line) and the SET process by sweeping down (red line). The inset shows an I-V curve at the ON (dark line) and OFF (blue line) from 0 to 1V (c) Endurance test of the device

were obtained in the early phases of the project in order to achieve reproducible switching. However, these performances are comparable with prior works found in the literature [93][104][158]. Because of a poor endurance and reproducibility, they are insufficient to compete with existing non-volatile memories. We speculate that improving the control of the nanogap path could increase the reproducibility of such memories.

It is worth mentioning that He et al. have shown that the nanogap systems on SiO_2 can host a tunable electroluminescence source.

To conclude, the existing literature describes several types of nanogap-based devices with a wide range of applications. However, because of the erratic nature of the electro-burning process, improving the reproducibility and reliability of such devices is a significant challenge for future applications. To address this issue, researchers have first shown that the nano-gap width could be tuned by varying the air pressure [75] or by feedback controlled electro-burning [8][71][73][109][112][161]. The path taken by the crack is a second aspect to consider. To tackle this issue, researchers generally use an "hourglass" design to create a constriction in the graphene flake where the current density is higher [73][75][162]. Despite successfully triggering the crack formation at the constriction, this method requires to adapt the layout. Moreover, uncertainties remain on the crack features (within the constriction).

4.2 Using ablation

Here, we perform selective ablation to direct the propagation of the crack during electrical breakdown. Thus, the idea is to ablate the graphene by forming a line of regularly spaced holes parallel to the electrodes. These defects should induce crowding and increase the current density to force the nanogap to propagate between the holes.

Remarkably, the Raman maps in Figure 4.3(a) shows that the nanogap consistently propagates across the holes. As expected, the electrical breakdown occurs step by step (Figure 4.2). In the Raman spectra, we count 20 pieces of crack compared to 21 current drops observed in the electrical data. This finding supports the hypothesis that the nanogaps gradually form one by one between each hole during electro-burning.

Figure 4.2: Ablation spots linked by the nanogap after electro-burning (a)SEM image (b)2D Raman mapping and (c)AFM image of the yellow framed area shown in (a)

The SEM picture 4.3(a) shows a strong brightness contrast between the laser ablated areas, the nanogap and the graphene. Figure 4.3(b,c) shows a 2D Raman mapping and an AFM image of the area framed in yellow in the SEM image. The AFM image reveals a rough topography with probably large quantities of polymer residues. Nonetheless, we can clearly distinguish the crack and the laser ablated areas, where both the graphene and the polymer are removed.

To summarise, the results show that we can successfully steer the nanogap path by ablating a line of regularly spaced holes. However, several drawbacks can be pointed out:

Figure 4.3: Ablation spots linked by the nanogap after electro-burning (a)SEM image (b)2D Raman mapping and (c)AFM image of the yellow framed area shown in (a)

- The nanogap path is not controlled between the ablated holes. As shown in Figure 4.3, the paths are not perfectly straight between the holes. Also, they are not repeatable.
- Because of ablated holes, the graphene integrity is altered.
- The devices break step by step, at high voltages, which may results in large nanogap widths (as explained in 2.6.2), unsuited for molecular electronics applications.

4.3 Using a defect line

An alternative way to control the nanogap path is to locally weaken the graphene layer within a chosen pattern(Figure 4.4(a,b)). As opposed to previous studies, the proposed method would allow to reliably control the nanogap geometry and path over distances greater than 60 μm without constraints on the device shape.

Figure 4.4: Principle of the laser-based pre-patterning method (a) A line of defects is patterned across the graphene device via femtosecond laser irradiation.(b) During electro-burning, a nanogap forms along the defective region.

4.4 Characterization of the defect line

Figure 4.5(a) shows a typical SEM image of a graphene device after laser patterning. The defect line appears as a slightly brighter band in the middle of the device. Figure 4.5(b,c) show the 2D and D Raman maps of a graphene device after laser pre-patterning. Figure 4.5(d) shows a typical Raman spectrum taken in the middle of the defect line. The D peak rises sharply along the defect line, indicating the presence of structurally defective carbon hexagons. In agreement with a high level of disorder, the 2D band also decreases [163].

We also calculated the average distance between defects L_d for 15 pre-patterned devices using the $I(D)/I(G)$ ratio(Figure 4.5(e)). Following the 2-stage model introduced by Ferrari [122], the amount of disorder within the defect line can be quantified. Figure 2(e) shows the theoretical curve of the $I(D)/I(G)$ ratio vs the average distance between defect L_d plotted using

equation 4.1 from ref 12:

$$\frac{I_D}{I_G} = C_A \frac{r_A^2 - r_S^2}{r_A^2 - 2r_S^2} [e^{(-\pi r_S^2/L_d^2)} - e^{(-\pi((r_A^2 - r_S^2)/L_d^2)}], \quad (4.1)$$

where r_S is the radius of disordered region around a defect(1nm), r_A is the radius of the activated region where the D band is activated(3.1nm). C_A is an empirical value related to the scattering efficiency of the optical phonons(4.5). With increasing disorder, the ratio $I(D)/I(G)$ first increase in stage 1 until reaching a maximum and dropping abruptly in stage 2. It should be noted that a given value of $I(D)/I(G)$ could belong to either stage 1 or 2. This problem is solved by using the full width at half maximum of the G peak (always larger in stage 2 123,124). Our data indicate that L_d ranges from 2 to 7nm. Even though the same irradiation conditions are carried out for all devices, some differences still occur due to slight fluctuations in focus. Note that stronger levels of disorder ($L_d < 2nm$) result in an electrically broken device, hence not relevant to our study.

4.5 Electro-burning of pre-patterned graphene

After laser patterning, we electro-burn the devices by ramping up the voltage at 0.5V/s until the current drops sharply. Figure 4.6(a) shows the electro-burning I-V curve for a pre-patterned and a pristine device (without defect line). The breakdown current density of pre-patterned devices is found to be lower on average than for pristine devices. With laser pre-patterning, we estimate an average breakdown current density of $1.7 \pm 1.7 \times 10^7 \text{ A/cm}^2$ over 13 devices), one order of magnitude lower than for pristine devices ($1.0 \pm 0.3 \times 10^8 \text{ A/cm}^2$ over 13 devices), in agreement with 67,73,158). As expected, this difference suggests that graphene was weakened by the laser.

Figure 4.5: (a) SEM image of a device showing the defect line, the brighter area between the two dashed yellow lines. 2D(b) and D(c) Raman maps of a graphene device after laser pre-patterning. (d) Raman spectrum extracted within the defect line (e) Theoretical relationship between $I(D)/I(G)$ L_d for monolayer graphene [12]. The two dotted red lines highlight the range of defect densities which enables the controlled nanogap propagation. The inset shows the estimated values of L_d for 15 devices.

Figure 4.6: electro-burning curve of a pristine device (blue line) and a laser pre-patterned device (red line) with identical size.

4.6 Morphology of the nanogap

4.6.1 Passive voltage contrast

As nanogaps are too small to be resolved on SEM, we establish the path of the nanogap with a passive voltage contrast technique by connecting one of the gold pads to an electrical ground [94][164]. Before electro-burning, no brightness contrast is observed on the SEM image as charges flow freely through the graphene and both electrodes have the same electric potential. However, a nanogap isolates one side of the device from the other. Charge build-up at the floating electrode leads to a different electric potential compared to the grounded electrode. A charged floating structure appears much darker on the SEM because secondary electrons are pulled back towards the positively charged structure, as sketched in Figure 4.7(a). As shown in Figure 4.7(b), the right side (isolated) appears darker than the left side. The sharp brightness change in the middle of the device highlights the disconnection line, therefore, the nanogap path. Thus, we confirm that the nanogap path follows the defect line.

Using passive voltage contrast, we characterized 26 pre-patterned devices to verify the reproducibility of our method. Out of 26 devices with L_d between 2 to 7nm, only 2 devices failed to form a crack along the defect line, hence yielding a 92% success rate. We note that homogeneous graphene coverage is critical since any tear or hole in the graphene may trigger the crack formation outside of the defect line. To further test the robustness of our technique, we also modified the defect line pattern by drawing crenelated lines of defects (Figure 4.7(c,d)). **The SEM images confirm that the crack propagation still follows the defects even when the line is not perpendicular to the current flow.**

In some cases, the crack might deviate from the defect line: Figure 4.8 shows a passive voltage contrast image of a device after electro-burning

Figure 4.7: (a) Sketch of the passive voltage contrast principle, the positively charged side appears darker, as less secondary electrons may reach the detector due to electrostatic attraction. SEM images showing passive voltage contrast for a straight (b) and crenelated (c,d) pattern. In (b) the defect line is highlighted between the two dotted yellow lines

(Figure 4.8(a) at 10kV and (b) at 1.5kV). Here, the density of defects is too low to control the nanogap propagation. Indeed, the average distance between defects, L_d is about 10 nm compared to the maximum limit of 7nm. Consequently, the nanogap path deviates from the defect line. Interestingly, the path still follows partially the defect line in some regions, suggesting that a lower defect density still slightly influences the nanogap propagation.

4.6.2 Atomic Force Microscopy

AFM height and phase images of an area where pre-patterning and electro-burning were performed are shown in Figure 4.9(a) and (b) respectively. The nanogap and the defect line appear remarkably clear in the phase AFM

Figure 4.8: SEM image of a pre-patterned graphene device after electro-burning at 10kV(a) and at 1.5kV(b) The nanogap deviated from the defect line. The defect line is highlighted between two yellow dotted lines in (a)

image. Interestingly, it is not perfectly straight but still remains within the defective region. This finding suggests that a reduction of the defect line width below 700nm could yield an even straighter nanogap. Analyzing the topography in Figure 4.9(c), the defect line appears as a 4nm-deep and 700nm-wide trench. The measured depth of the defect line, is attributed to the partial removal of polymer residues during laser irradiation. The nanogap is visible at the center of the defect line as a 2nm-deep trench. Using AFM, clean monolayer graphene is usually measured to have a lower thickness ranging from 0.4 to 1.7nm (actual thickness is 0.34nm) [86]. This discrepancy might simply arise from remaining polymer residues that withstood the laser irradiation. Using the method described in section 2.3.2 we measured a nanogap width of $36.4 \pm 18.5\text{nm}$ over 16 values taken every 100nm along the nanogap path. The maximum width is found to be 94nm and the minimum is 17nm. These values are based on the assumption that the graphene edges are positioned at the same location as the topographic edges.

4.7 Discussion

The observation of the nanogaps systematically located within the defect line in pre-patterned graphene is completely consistent with the interpretation

Figure 4.9: AFM height(a) and phase(b) image of a graphene device after laser pre-patterning and electro-burning. The defect line is highlighted between the two yellow dashed lines. The nanogap corresponds to the dark brown zigzagged line in the height image and to the black zigzagged line in the phase image. The blue dashed line in (a) shows the profile corresponding to the cross-section plot shown in (c)

that nanogaps initiate in highly resistive or highly defective regions where the temperature is the highest (as explained in section 2.6.2). As seen in Figure 4.9, the nanogap seems to bounce back when reaching the edge of the defect line. On the contrary, if the defect density within the defect line is closer to that of pristine graphene ($L_d > 10nm$), the crack path may deviate from the defect line (Figure 4.8). This further supports the theory of a preferential nanogap propagation through the defective region.

On the contrary, in the case of pristine graphene, defects formed during growth, transfer and fabrication are often scattered randomly over the flake. Moreover, the absence of a defect line should enhance the electrostatic effects observed at high biases thus yielding strong heterogeneous heating. For

pristine graphene, the combination of both electrostatic effects and a random defect arrangement result in an unpredictable nanogap path.

At this stage, the question remains open as to whether the nanogap forms within the defect line only because of a higher resistivity inducing localized Joule heating, or because defects themselves play a role in the electro-burning process. In the first case, the required temperature for electro-burning should be the same for both pristine and pre-patterned graphene. In the second case, the temperature should be reduced in pre-patterned graphene, as oxidation may be facilitated due to a weaker lattice [102]. To clarify this matter, we investigated the thermal aspects of electro-burning in laser pre-patterned graphene via finite element analysis coupled with in-situ infrared thermography.

4.8 Thermal analysis

4.8.1 Numerical simulation

We first performed a finite element analysis (FEA) using COMSOL 5.0. A 2D model (Figure 4.10) was built: it consisted of two 100nm thick, 20 μ m wide gold electrodes contacting a 0.34nm-thick graphene flake with variable dimensions. The distance between the electrodes varied from 5 to 60 μ m depending on the device. Similarly, the graphene flake width varied from 5 to 80 μ m. The contact resistance between the graphene and the electrodes was set at 30 k $\Omega \cdot \mu$ m² as measured for our devices.

In addition, the interfacial thermal resistance between the graphene and the SiO₂ was set at $8 \times 10^{-9} m^2 \cdot K/W$ taken from ref [165]. As this value may decrease when graphene contains defects [166], we have verified that this has a very low impact on the electro-burning temperature (less than 1%). The silicon substrate was made significantly bigger than the graphene device (600 $\times$ 600 μ m). The defect line was modeled by setting a higher

sheet resistance within a $0.7\mu\text{m}$ domain in the middle of the graphene flake. The sheet resistance of the defect line was calculated from the experimental data by subtracting the resistance before and after laser patterning. Indeed, we consistently observe a significant increase of resistance after laser pre-patterning. We obtain values widely ranging from $50\text{k}\Omega/\square$ to $6\text{M}\Omega/\square$ (versus $3\text{k}\Omega/\square$ for pristine graphene). Greater resistances are associated with higher defect densities observed with Raman spectroscopy [98,99,167,168]. Regarding the boundary conditions, a fixed temperature of 20°C was applied to the bottom and sides of the substrate. In addition, the device was biased by applying an electrical power to the electrodes. For each of our device, we applied the power that was measured from its corresponding I-V curve. This allows us to obtain the temperature of each pre-patterned device at the time of electro-burning by simulating their thermal responses. Table 4.1 lists the material properties used in the simulation. We note that the thermal conductivity of graphene does not impact the results. The thermal conductivity of graphene is eclipsed by the large cross section area of the SiO_2 layer despite having a lower thermal conductivity (1.4 W/m/K). In other words, the heat generated within the graphene directly flows towards the substrate without travelling across the flake. We have verified that changing the value of graphene thermal conductivity has no impact on the simulation results.

Figure 4.10: (a) 2D model used for the simulation, dimensions are not to scale (b) Zoomed view of the framed area

	Electrical conductivity (S/m)	Thermal conductivity (W/m/K)
Graphene	10^6	-
Defective graphene	$10^2 - 10^4$	-
Silicon	10^{-12}	100
Silicon dioxide	∞	1.4
Gold	4.1×10^7	315

Table 4.1: Material properties used for the numerical simulation

Figure 4.11: (a)Top and (b,c)side views of the 2D temperature distribution for a pre-patterned device at the electro-burning. A zoomed view of the framed area is shown in (c) (d)Critical electro-burning temperature as a function of the defect line sheet resistance. The red square corresponds to the device shown in (a,b,c)

Figure 4.11(a) shows the top-view 2D temperature plot of a pre-patterned device whose defect line sheet resistance is $86 \text{ k}\Omega/\square$. As expected, the device displays a sharp elongated hot zone at 245°C following the defect line while the rest of the device remains colder ($\approx 70^\circ\text{C}$). This temperature concentration is peculiar since we would expect a high thermal conduction within the graphene (600 W/m/K on SiO_2 [169]). In reality, the plot in Figure 4.11(b) reveals that heat mostly dissipates directly from graphene to substrate. It is consistent with the literature: for instance, Bae et al. have estimated that more than 77% of the heat is dissipated directly through the substrate [72]. We note, however, that the oxide layer has a high thermal resistance(see a

zoomed view of the defect line vicinity in Figure 4.11(c)). As a result, the underlying silicon surface stays substantially colder (90°C vs 240°C for the graphene).

By extracting the maximum temperature in the middle of the defect line, we estimated the electro-burning temperature as a function of the defect line sheet resistance for 12 devices (Figure 4.11(d)). The red square corresponds to the device shown in Figure 4.11(a,b,c).

We observe that the electro-burning temperature decreases as the sheet resistance of the defect line increases. The values range from 245°C to 22°C, lower than the minimum oxidation temperature of pristine graphene (260°C from Yamada et al. [101]). For highly disordered defect lines (above $10^6 \Omega/\square$), electro-burning temperatures are found to be well below 50°C. It is worth mentioning that for a given electrical power, higher defect line sheet resistances yield higher temperatures (Supplementary information Figure S4). However, in our case, this effect is compensated by the fact that the highly defective devices break at much lower electrical powers. This strongly supports the hypothesis that the electro-burning process is not only driven by Joule heating concentration due to a higher resistivity within the defect line, but also by defect-induced weakening of the lattice which enables oxidation at lower temperatures. We note that, despite Raman measurements suggesting that the defect line contains vacancy defects, there is no information on the impact of the defect type on the lattice weakening.

Figure 4.12 shows the maximum temperature of the graphene as a function of the applied electrical power for various defect line sheet resistances. At a given power, we observe that lower sheet resistances result in lower temperatures. This occurs simply because there is less heterogeneity in resistivity across the device and thus less differential joule heating. This results in a more spread out thermal dissipation.

Figure 4.12: Maximum graphene temperature as a function of the electrical power for a defect line sheet resistance of $5 \times 10^5 \Omega/\square$ (black), $5 \times 10^4 \Omega/\square$ (black), $5 \times 10^3 \Omega/\square$ (blue)

4.8.2 Infrared thermography

To verify the results of the simulation, notably the unexpectedly low temperature values, we performed in-situ infrared (IR) thermography of pre-patterned and pristine devices during electro-burning.

Figure 4.13(a,b) show, respectively, the thermal images of a typical large pristine device and a smaller pre-patterned device. Both images were extracted one time frame (131ms) before electro-burning occurs. As expected, the temperature rises significantly between the electrodes where the graphene flake is located. For the pristine device, silicon temperatures rise up to 213°C. As a reminder, the temperature measured here, is that of the Si substrate. Because of the large thermal resistance of the SiO_2 , the actual graphene temperature is expected to be much higher and easily reach temperatures above 300°C, consistent with graphene electro-burning in air [75]. We also notice two large circular hot spots of different sizes. This confirms the interpretation given in the previous section that pristine graphene undergoes very heterogeneous temperature increase during electro-burning which, in

turn, yield an uncontrolled nanogap formation.

Interestingly, the amount of heat generated is such that substrate temperatures of $\approx 100^\circ\text{C}$ spread over more than one millimetre around the device. Therefore, electro-burning a pristine device may substantially damage adjacent devices.

Moving to the pre-patterned device (Figure 4.13(b)), the silicon temperature achieved at electro-burning is drastically lower than for the pristine device, reaching a maximum of 83°C , of the same order of magnitude than the simulated temperature.

Figure 4.13: Infrared images of a pristine(a) and pre-patterned(b) device one time frame before electro-burning occurs (131 ms).

To compare more finely with simulation, we plotted the silicon temperature as a function of the electrical power (Figure 4.14). The black dots are the experimental points averaged from 4 central pixels in the middle of the device. In comparison, the red line shows the simulation results (for the same device tested experimentally with defect line sheet resistance of $86\text{k}\Omega/\square$) extracted by averaging the silicon temperature beneath the graphene. We observe a very good agreement between thermography and simulation. The inset of Figure 4.14 shows the absolute difference $|\Delta T|$ between experiment and simulation as a function of the electrical power. From this distribution, we calculated an average difference of only $2.5 \pm 1.7^\circ\text{C}$.

This strongly supports the outcomes of our thermal simulations showing electro-burning temperatures below 50°C for highly defective lines.

Overall, this shows that nanogaps can be formed while graphene remains

cool. If the technique is used between several fabrication steps, graphene and other sensitive compounds (polymers, adjacent devices etc...) surrounding the device could be spared from potential thermal damage.

Figure 4.14: Average silicon temperature as a function of the electrical power for the pre-patterned device shown in Figure 4.13(b). The black dots are the experimental points averaged from the 4 central pixels within the device. The red line is the simulated temperature. The inset shows the absolute difference $|\Delta T|$ between simulation and experiment vs the electrical power

4.9 Conclusion

To conclude, we first demonstrated, that the nanogap propagation could be controlled by ablating a line of regularly spaced holes to heighten current crowding between them. This result confirms that graphene would preferably break around areas with higher current densities. Within the scope of improving the reliability of a graphene-based circuit, current crowding should be avoided, especially around sharp angles such as bends (see section 5.2.1).

In the second part, we performed electro-burning after the introduction of a defect line. We showed that the nanogap consistently propagates following the chosen pattern with 92% reproducibility. Via infrared thermography,

we discovered that electro-burning occurs at temperatures lower than 50°C for high defect densities. In the context of large-scale fabrication, this suggests that we can control the propagation of the nanogap without thermally damaging any adjacent device.

Unlike previous works, our method leaves a residual defective area around the nanogap (700nm wide). Whether this will undermine or enhance the performances of future nanogap based devices is an open question. Nonetheless, molecular simulations from Bergvall et al. suggest that moderate disorder around the graphene edges would not impact the performances of single molecule transistors [\[152\]](#).

To summarise, during electro-burning, graphene within the defect line is the hottest and has the weakest lattice structure resulting in a preferential nanogap propagation along the defect line in agreement with our experimental results. However, this defect-induced weakening is also double-edged. Indeed, on the one hand, the technique enables a safe electro-burning where the device surroundings (up to 1mm) remain spared from thermal damage. On the other hand, any unwanted defective regions that are not intended for fabricating nanogaps could significantly worsen the reliability of the circuit.

Chapter 5

Numerical simulation of a hybrid CNT/graphite structure for 3D interconnects

As shown in Chapter [2](#) and [3](#), thermal failure of graphitic structures in air occurs through thermally driven heterogeneous oxidation. Highly localised hotspot induced by current crowding can significantly affect the reliability of a circuit.

In this chapter, we explore the possibility of using a novel hybrid CNT/graphite structure to replace conventional metallic interconnects. We perform numerical simulations to assess the reliability of the structure depending on both geometrical and material parameters. We first propose an innovative way to calculate the contact resistivity of a CNT/graphite junction. Then, we performed numerical simulations of a CNT/Graphite structure under thermal and electrical loading. The results allow us to provide design advice for future fabrication to maximise the reliability of the circuit. Also, we aim at identifying potential thermal weaknesses that could yield to failure.

For this study, we chose to focus on three-dimensional integrated circuits (3D ICs) where wafers are stacked and interconnected vertically. This brings

all devices closer to each other resulting in shorter interconnects. 3D chips can achieve higher performance, lower power consumption and a smaller footprint [170][171]. To interconnect the dies vertically, manufacturers can use through substrate vias (TSV). They are seen as useful platforms for heterogeneous integration. The TSVs are short vertical interconnections between layers (typically 20 μm in length and 2 to 4 μm in diameter) that may carry both electrical signals and heat (thermal TSVs) [172]. Within the scope of this PhD work, a 3D IC is interesting because heat extraction is a particular concern. Unlike 2D circuits, the additional material layers trap the heat [173]. Different solutions have therefore been proposed to alleviate thermal congestion, ranging from algorithmic approaches (i.e., thermal floor-planning or thermal TSV placement) [172] to microfluidic channels [174]. In this work, the potential of substituting copper with carbon materials is assessed.

This work was carried out during an overseas research attachment at the University Of Rochester. We have published a paper that proposes an electrical and thermal model of the interface between the CNTs and the graphite [175]. Such models can be implemented in circuit simulation software to simulate entire circuits.

5.1 Description of the structure

5.1.1 Model

A structure consisting of a TSV and two interconnects was numerically built (Figure 5.1). The objective is to simulate electrical and thermal conduction within the structure to optimise the design for reliability improvement. As shown in Figure 5.1, we applied a $\Delta T/\Delta V$ at the end of both interconnects. We calculate the thermal and electrical resistances of the full structure by measuring the thermal flux Φ and the electrical current I at the terminal.

Figure 5.1: Side(a) and top(b) view of the structure used in the COMSOL simulation

We applied the interfacial resistances at the contact area between the TSV and the interconnect.

5.1.2 Intercalated graphite

To compete with copper-based technology, it is preferable to consider a thick interconnect line of highly crystalline graphite to obtain a low effective resistance both thermally and electrically. Also, if only monolayer graphene was connected to carbon nanotubes, the current density would be too high and would result in failure. Although one single carbon layer (graphene) has a high electrical conductivity, increasing the number of layers affects its properties. For instance, monolayer graphene has a resistivity of $1.4 \mu\Omega\cdot\text{cm}$ while graphite has a resistivity of $318 \mu\Omega\cdot\text{cm}$ [34]. As advised by Sarkar et al., this problem can be solved by intercalation doping [176]. Indeed, inserting intercalation compounds, such as pentafluorides (AsF_5 , SbF_5) or pentachlorides (SbCl_5 , CuCl_5), has been shown to significantly improve the electrical

Resistivity (a-axis)	$1.1\mu\Omega.cm$	[177, 180, 181]
Electrical anisotropy	$10^3 - 10^6$	[179, 180]
Thermal conductivity	700 W/m/K	[182, 185]
Thermal anisotropy	$10 - 10^3$	[185, 186]

Table 5.1: Properties of the intercalated AsF₅ graphite

conductivity as compared to pure graphite. The compounds are sandwiched between the graphitic layers and increase the free carrier density (doping). This results in a very low resistivity down to 1 $\mu\Omega.cm$ for AsF₅ [177] or SbF₅ [178] intercalated graphite, one and a half time lower than copper. However, this intercalation affects the c-axis resistivity by physically separating the graphite planes. For example, In the case of AsF₅ graphite, the c-axis electrical resistivity is 10^6 times higher than the a-axis (plane) resistivity [179, 180]. Table 5.1 summarises the properties of intercalated AsF₅ graphite.

Regarding thermal conduction, studies report conductivities up to 700 W/m/K for intercalated graphite [182, 185], which is about twice as high as the conductivity of copper, and even higher when taking into account the negative impact of the interconnect dimensions on copper [187]. The thermal anisotropy ratio is found to be around 10^3 , much lower than for electrical measurements [185, 186, 188]. Regarding feasibility, graphite is usually synthesised at high temperatures through processes such as pyrolysis [189, 190] or carbonisation of polymers [191–193]. For interconnect applications, chemical vapour deposition (CVD) would be preferred [194–198]. Indeed, CVD techniques are already widely used in industry and allow high layout flexibility by patterning using photolithography techniques. We note that the intercalation process is also compatible with CVD processes [199].

5.1.3 CNT bundle

The TSV array is composed of Single Wall carbon nanotubes (SWCNT). To define the material properties of the SWCNT bundle, we start by defining the

properties of an isolated SWCNT. According to the work of Xu et al. [200], the impedance of a SWCNT is given by:

$$Z_{SWCNT} = R_Q + R_S + j\omega L_K \quad (5.1)$$

Where $R_q = h/2q^2$ is the quantum ballistic resistance, $R_S = hH/2q^2\lambda$ is the scattering resistance, $L_K = hH/4q^2v_F$ is the kinetic inductance arising from the inertia of the electron mass. h is the Planck constant, H is the TSV height, q is the electron charge; v_F is the Fermi velocity ($8 \times 10^5 m/s$), and λ is the mean free path of the electrons ($\lambda = 1\mu m$ [200]). Substituting these expressions into equation [5.1] yields:

$$Z_{SWCNT} = \frac{h}{2q^2} \left(1 + \frac{H}{\lambda} + j\omega \frac{H}{2v_F} \right). \quad (5.2)$$

To determine the complex effective impedance of a bundle Z_B , an estimate of the number of SWCNTs within a bundle N_{CNT} is necessary. Thess et al. have experimentally shown that ropes of CNT arrange in two-dimensional triangular packing structure, as illustrated in Figure [5.2] [14]. The number of CNTs within a bundle is, therefore:

$$N_{CNT} = \frac{2\pi r_{TSV}^2}{\sqrt{3}(d + \delta)^2}. \quad (5.3)$$

Where d is the diameter of a SWCNT (1nm), δ is the minimum Van der Waals intertube spacing, and R_{TSV} is the radius of the TSV. From equation [5.3], the impedance of a bundle is:

$$Z_B = \frac{Z_{SWCNT}}{N_{CNT}F_m}, \quad (5.4)$$

where F_m is the metallic fraction of CNTs. In other words, the semi-conducting CNTs are not part of the electrical conduction. Statistically, one-third of CNTs are metallic ($F_m=1/3$) although it is possible to tune

Nanotube diameter d	1nm
Intertube spacing δ	0.34nm [13]
CNT density	$6.43 \times 10^{13} \text{CNTs}/\text{cm}^2$
Electrical resistivity ρ_B	$6.17 \times 10^{-8} \Omega.m$
Thermal conductivity K_B	1770 W/m/K

Table 5.2: Calculated properties of a SWCNT bundle

the chirality and obtain higher metallic fractions ($F_m = 0.91$) [38]. From the impedance Z_B , we can extract the effective conductivity of the CNT bundle. Regarding heat transport, the chirality of the CNTs does not significantly affect the thermal conductance [201-203]. Thus, similarly, the effective thermal conductivity of the CNT bundle K_B is:

$$K_B = K_{CNT} N_{CNT} \left(\frac{d}{2r_{TSV}} \right), \quad (5.5)$$

where K_{CNT} is the thermal conductivity of an isolated SWCNT. Here, $K_{CNT} = 3500 \text{W}/\text{m}/\text{K}$ [44]. The effective resistivity and thermal conductivity (calculated in table 5.2) are strongly dependent on the CNT density. Therefore, we emphasise the importance of maintaining a high density of CNTs in the bundle to compete with Copper-based TSV in terms of electrical and thermal conductivities. To compare with recent experimental values, the highest reported density of vertically aligned nanotubes is $1.5 \times 10^{13} \text{CNTs}/\text{cm}^2$ [204] while we calculated a theoretical maximum at $6.43 \times 10^{13} \text{CNTs}/\text{cm}^2$. Reducing the gap between the experimental and theoretical maximum density of CNTs is a major challenge that could be solved by improving CNT synthesis methods.

5.1.4 Interface CNT/graphite

Theoretical work predicts the covalent bonding between CNTs and a carbon sheet to be thermodynamically stable. Research on this topic was first reported as a 3D architecture called “pillared graphene” consisting of CNTs

Figure 5.2: Top view of a CNT TSV. The diameter of the CNT and TSV is, respectively, 1 nm and 2 μm . $\delta = 0.34$ nm is the minimum Van der Waals spacing between CNTs [13]. The area per CNT is based on a 2-D triangular packing structure [14].

pillars connecting graphene sheets and finding applications in energy storage and supercapacitors [205,206]. Due to the covalent nature of the junction and the material similitude, the scattering of phonons and electrons is greatly reduced hence resulting in higher conduction at the interface. Recently, the growth of a CNT array on top of graphene layers has been remarkably achieved [207]. Furthermore, they showed unequivocally that the CNTs are covalently bonded with graphene. Electrical characterisations of such structure reveal an ohmic electrical contact at the junction [207-209]. However, none of these experimental works specifically focus on studying the properties of the interface itself. The CNT and graphene resistance usually masks the isolated junction resistance.

For the thermal conductance, even though few theoretical studies provide thermal interface resistance values [210-214], there is currently no experimental measurement of the conduction at the interface CNT/Graphite for both thermal and electrical transport. **To overcome this lack of data, we propose an innovative approach by assuming that the junction**

properties are similar to that of a grain boundary (GB) in a planar graphene sheet for which the experimental and theoretical studies are numerous. Indeed, the atoms arrangement at the junction is expected to contain structural defects such as heptagons or pentagons, distorted rings and Stone-Wales defects simply because of crystallographic mismatch, nanotube chirality and multiple attachment possibilities [206,207,213-217]. Indeed, Park et al. equilibrate the pillared graphene structure through molecular dynamic simulation by a regular combination of septagon-hexagon circularly arranged around the junction (Figure 5.3) [214]. Later, they emphasised that these hexagonal and heptagonal rings were also distorted [211]. In such covalent junction, Zhu et al. remarkably showed on TEM the presence of highly distorted rings thus confirming theoretical studies [207]. All these defect types are theoretically predicted [218-221] as well as experimentally observed [222-224] in a grain boundary structure. Therefore, the grain boundary of a planar graphene sheet is in fact structurally similar to a CNT/graphene covalent bonding.

Figure 5.3: Side(a) and top(b) view of the crystalline structure between a (4,4)SWCNT and a graphene sheet, the structure is equilibrated by adding six heptagons highlighted in red. The sketch was done with AVOGADRO software

From these values we aim at calculating the effective surface resistivity ρ_{int} between a CNT bundle and a graphitic sheet. For a single CNT, the

Interfacial thermal conductance G_J (W/m ² /K)			
CNT/graphene	6	211	213
	100	212	
	13	210	
Grain boundary	19-47	225	
	15-47	226	
	10	227	
	4	228	
	14	229	
	3	230	
	20-30	231	
Contact resistivity ρ_{GB} ($\Omega \cdot \mu\text{m}$)			
Grain boundary	42-143	232	
	60	222	
	500-35000	233	

Table 5.3: Interfacial thermal conductance and electrical contact resistivity extracted from the literature for grain boundary and CNT/graphene junction

Table 5.3 reports thermal and electrical values extracted from literature for ρ_{GB} and G_J . We insist that these values are relevant for one single CNT covalently bonded to a graphitic layer.

resistance at the interface is equal to:

$$R_{CNT/G} = \frac{\rho_{GB}}{\pi d}, \quad (5.6)$$

where, πd is the perimeter of the CNT, d is the CNT diameter. Additionally, the effective contact resistivity of the bundle ρ_{int} is equal to:

$$\rho_{int} = \frac{R_{CNT/G}}{D_{CNT}}, \quad (5.7)$$

where D_{CNT} is the density of CNTs in the bundle. Therefore, combining equations 5.6 and 5.7, we have:

$$\rho_{int} = \frac{\rho_{GB}}{\pi d \times D_{CNT}}. \quad (5.8)$$

For the thermal properties of the interface, the effective thermal conductance G_{int} can be calculated either from the grain boundary or from the

direct value of CNT/graphite interface provided in the literature.

Using a similar logic we have:

$$G_{int} = G_J \cdot d \cdot \tau \cdot D_{CNT} \cdot \pi, \quad (5.9)$$

where τ is the thickness of the nanotube wall (0.34 nm). Table 5.4 shows the estimated values of G_{int} and ρ_{int} for a strong sp^2 covalent bonding. According to our estimation, the thermal conductance is ≈ 3000 times higher with a CNT/G interface while the surface electrical conductivity is ≈ 50 times higher compared to a CNT/Cu interface. We note that a recent study has confirmed the calculated value of G_{int} [234] experimentally.

		CNT/graphite	CNT/copper
Thermal	G_{int} (MW/m ² /K)	8930 [210]	2.5 [235]
Electrical	ρ_{int} (10 ⁻¹³ Ω.m ²)	2.47 [233]	100 [236]

Table 5.4: Interfacial thermal conductance and contact resistivity at the junction for CNT/graphite and CNT/copper

5.1.5 Summary of the properties

Table 5.5 summarises the different parameters used for the simulation.

Because CNT TSVs connected to copper interconnects have been the subject of intense research works [237]–[240], the carbon structure is also compared with a CNT/Cu structure where graphite is replaced by copper. In these cases, the interfacial resistances ρ_{int} and G_{int} are also adjusted according to table 5.4

5.2 Numerical Simulation

This part describes the results of the simulation. Apart for section 5.2.5 we present results obtained from electrical simulations. Indeed, as shown in Chapter 2, heterogeneous Joule-heating leads to current crowding and

Parameter	Value
Geometric	
TSV radius r_{TSV}	$0.5 - 2.5\mu m$
TSV height H	$20\mu m$
Graphite thickness t	$0.5\mu m$
Graphite length	$1\ 10\mu m$
Electrical	
CNT bundle resistivity	$6.17 \times 10^{-8}\Omega.m$
Graphite in plane resistivity ρ_{Gr}	$1.1 \times 10^{-8}\Omega.m$
CNT/Graphite surface resistivity ρ_{int}	$10^{-13}\Omega.m^2$
Anisotropy	$10 - 10^6$ [178,179]
Thermal	
CNT bundle conductivity K_B	$1750W/m/K$
Graphite conductivity K_{Gr}	$700W/m/K$
CNT/Graphite surface conductivity G_{int}	$8930MW/m^2/K$
Anisotropy	$10 - 10^3$ [182,185]

Table 5.5: Parameters used in the simulation

ultimately failure. Therefore, we aim at assessing the reliability of such structure.

5.2.1 Crowding at the interface

Naturally, heat or current tend to take the least resistive path. In the case of a 90° bent conductor, the current usually crowds through the shorted path. Figure 5.4(a) shows a 2D plot of J/J_0 at the interface vicinity. J is the current density and J_0 is the base current density injected into the structure. J almost doubles at the bend. Figure 5.4(b) is a contour plot of the blue framed area in (a). The arrow plot shows the path of the current along with its magnitude (arrow size). This confirms that most of the current curve directly towards the TSV underneath without spreading evenly across the interface area.

Ideally, crowding should be avoided to prevent the formation of hot spots at the interconnect bend. To gain more insights into the influence of the geometry, we plotted in Figure 5.5 the maximum J/J_0 as a function of the TSV radius and the interconnect thickness.

Figure 5.4: (a) 2D plot of J/J_0 at the interface location (b) Contour plot of the blue framed area, the orange arrows indicate the direction of the current

Figure 5.5: Plot of J/J_0 as a function of the TSV radius(a) and the interconnect thickness(b)

The results suggest that, to make a reliable design with the least crowding, the TSV radius should be kept as large as possible ideally at $2.5\mu\text{m}$ where it reaches its minimum crowding. As shown in Figure 5.5 increasing the interconnect thickness results in greater crowding up to a J/J_0 of 3 for a $0.9\mu\text{m}$ thick interconnect. The reason for this increase is geometrical: as we increase the thickness, the difference in current densities between the crowded bottom and the top is greater hence increasing the ratio. Practically, this is not a serious concern. Indeed, if we increase the thickness of the interconnect, this would reduce the total resistance and, for a given voltage, the absolute value of the current density would also be reduced thus preventing any damage. However, an incorrect assessment would be to take advantage of a lower interconnect resistance to increase the voltage hence keeping the same current density as the thinner interconnect. This would result in a much higher absolute value of the current density potentially leading to damage. To summarise, a thicker interconnect would be preferred for

lowering the resistance. However, if incorrectly assessed, the structure might undergo thermal failure due to important crowding. This could impact the reliability of the component.

5.2.2 Influence of the anisotropy

So far, we have neglected the graphite anisotropy in the simulation to focus on the crowding at the interface. However, as shown in Table 5.5, anisotropy within the graphite can range from $10 - 10^3$ for both heat and electricity. However, in this regard, the literature is still very scarce. It is difficult to conclude on a precise value. Therefore, we investigated the influence of the horizontal interconnect anisotropy. We applied an anisotropy on the graphite properties by modifying the conductivity tensor. The Y-axis property was lowered by a given factor (anisotropy ratio $\rho^{\parallel}/\rho^{\perp}$).

Figure 5.6 shows a 2D plot of the current crowding J/J_0 at the interconnect bend for an anisotropy ratio of 1000. The current is forced to concentrate at the bottom of the interconnect. Therefore, the top of the conductor is electrically idle.

Figure 5.6: 2D plot of the current crowding J/J_0 at the interconnect bend for an anisotropy ratio of 1000

Figure 5.7(a) shows the resistance of the full carbon-based structure as

a function of the anisotropy ratio. We first note that there is no resistance improvement for increasing the thickness above $0.5\mu\text{m}$. Practically, this suggests that doing so would result in a waste of material. We also observe a steady increase of the electrical resistance with the anisotropy. This is due to the current being forced to travel across the basal planes of graphite. This effect worsens when the thickness is increased. This is consistent with the spatial mapping shown previously in Figure 5.6 where the top of the interconnect is electrically idle.

Figure 5.7 shows a plot of J/J_0 as a function of the anisotropy ratio. Apart from $t=0.1\mu\text{m}$, crowding increases dramatically with anisotropy up to a factor of 45 for $t=1\mu\text{m}$. As a matter of comparison, J/J_0 would only be about 4 for isotropic graphite. Once again, we notice that crowding worsens when working with thicker interconnects. These results are consistent with the recommendations given in the previous section (5.2.1) that t should also be reduced to limit crowding.

Figure 5.7: (a) Resistance of the full carbon structure as a function of the anisotropy ratio $\rho^{\parallel}/\rho^{\perp}$ (b) J/J_0 as a function of the anisotropy ratio. Both plots are for three different interconnect thicknesses t .

5.2.3 Influence of the frequency

Because circuits sometimes operate at very high switching frequencies, we investigated the influence of a high-frequency signal passing through the structure Interconnect-TSV-Interconnect. Figure 5.8(a,b) show that the re-

sistance and the crowding factor J/J_0 increases with frequency. This high-frequency behaviour is a well-known phenomenon commonly called skin effect [241]: An alternating current in a conductor generates a magnetic field. At high enough frequencies, this field acts on the current flow itself and opposes the change in current density due to an electric field called "counter-electromotive force". This force is strongest at the centre of the conductor and pushes the electrons to the outside of the conductor. The effect is well illustrated in the 2D cross-sectional plot in Figure 5.8(c,d) showing the structure under a 200GHz electrical loading. The current density is five times larger near the edges of the conductor.

Figure 5.8: (a) Resistance and (b) crowding factor J/J_0 of the full structure as a function of the frequency. (c,d) Cross-sectional views of the structure under 100GHz electrical loading. (c) shows a side view of the bend vicinity. The cross-sectional plot shown in (d) corresponds to the black dashed line shown in (c)

5.2.4 Influence of the bonding quality between CNT and graphite

Until now, we have considered a perfect covalent bonding between the CNTs and the graphite. The carbon atoms at the interface may not be perfectly bonded partly because of crystallographic mismatch or experimental fluctuations. Thus, to have a realistic approach, we chose to consider, on the one hand, a high-quality interface and on the other hand a low-quality interface. For example, Shi et al. [210] reported G_J values for strong sp² covalent bonding (13 GW/m²/K) and weak Van Der Waals bonding (25 MW/m²/K) where the tip of the CNTs would be only physisorbed on the graphene plane. In a complete study, Tsen et al. [233] measured ρ_{GB} ranging from 500 to 35000 $\Omega.\mu\text{m}$ depending on the quality of the grain boundary. Indeed, using equation [5.8] this gives ρ_{int} ranging from $2.43 \times 10^{-13} \Omega.m^2$ (the value used until now) to $173 \times 10^{-13} \Omega.m^2$ (Van Der Waals bonding). Because CNT TSVs connected to copper interconnects have been the subject of intense research works [237-240], we also compare the CNT/graphite structure with a Cu structure and a CNT/Cu structure using ρ_{int} from Table [5.4] where graphite is replaced by copper. It is worth mentioning that the anisotropy of graphite is set at 10^3 to provide a realistic comparison. The red line in Figure [5.9] shows the electrical resistance of a CNT/Graphite structure as a function of ρ_{int} . For an ideal covalent bonding, the resistance of the carbon structure equals that of a copper structure (3.5Ω). For a Van Der Waals contact (ρ_{int} max), the resistance is 37Ω , 10 times higher than for ideal bonding. It is worth noting that a structure with a CNT/Cu interface would result in a resistance of 23Ω . Thus, if resistivity of the interconnect is the main criterion, a CNT/Cu structure would be unsuitable. Similarly, for a CNT/Graphite structure, we stress the importance of a high-quality bonding at the area in order to compete with Cu based interconnects.

Figure 5.9: Electrical resistances of the structure as a function of the CNT/graphite contact resistivity ρ_{int} set at the junction. The horizontal lines are the resistances for CNT/Cu and full Cu structures

5.2.5 Case of heat conduction

As mentioned previously, we mainly focused on the electrical simulation. Nevertheless, in this section, we briefly review the case of heat conduction. Figure 5.10 shows the thermal resistances of the carbon structure as a function of the interfacial thermal resistivity $1/G_{int}$. Similar to Figure 5.9 we observe a linear increase of the thermal resistance when increasing $1/G_{int}$. However, even at high resistivities (Van Der Waals contact), the thermal resistance of the carbon structure is still slightly lower than a copper structure and greatly lower than a CNT/Cu structure. Thus, using carbon materials could significantly improve heat conduction compared to copper. We stress that the heat simulation is significantly more complex than the electrical case. Although heat is generated within the conducting parts, as opposed to electricity, it can also escape out of the circuit towards the embedding structures (substrate). Therefore, even though the thermal conduction of carbon circuits is better, it does not necessarily guarantee a better heat extraction since other factors are also at play.

Figure 5.10: Thermal resistances of the structure as a function of the CNT/graphite contact resistivity $1/G_{int}$ set at the junction. The horizontal lines are the resistances for CNT/Cu and full Cu structures

5.3 Conclusion

To conclude this chapter, we studied a novel carbon structure composed of horizontal graphite interconnects connected to CNT TSVs. We proposed that the CNTs are covalently bonded to the graphitic plane. By assuming that the defects present at the interface between a CNT and a graphene plane are structurally identical to a grain boundary, we proposed a way to calculate the thermal and electrical interface resistance of a CNT bundle attached to a graphite interconnect. When comparing this resistance to a CNT/copper interface, we found that a CNT/Graphite covalent contact is approximately 3000 and 50 times better regarding heat and electrical conduction, respectively.

Next, we performed simulations of a, interconnect-TSV-interconnect structure by studying the influence of anisotropy, bonding quality and frequency. Our results indicate that current concentrates at the interface because of the 90° geometry of the 3D structure. Furthermore, we found that factors such as a thick interconnect or a high-frequency, can heighten current crowding. This is especially true when working with a high graphite anisotropy which, in turn, appeared to be the most critical factor.

In view of these results, the graphite interconnect should be made as

thin as possible to limit these effects. Therefore, a compromise should be found between interconnect thickness and absolute resistance. Comparing with a CNT/Cu structure, our hybrid carbon structure has a much lower electrical resistance due to its lower interface resistance. However, we found that, when comparing with a copper structure, the carbon one was only competitive with perfectly covalent bondings. This stresses the importance of maintaining a high-quality bonding at the interface in the scope of replacing metallic interconnects with carbon materials.

Chapter 6

Conclusion

In Chapter 2 we directly studied the thermal failure of graphene devices through electro-burning. Using Raman spectroscopy combined with atomic force microscopy, we characterised graphene devices after electro-burning. We show that a nanogap systematically forms across the graphene flake during electro-burning. Via in-situ SEM, we confirmed that the path of this nanogap is the disconnection line that leads to electrical failure. Thermal imaging of graphene during electro-burning reveals strong heterogeneities with the formation of localised hotspots along with a significant temperature increase. Our results highlighted the heterogeneity of the electro-burning mechanism. We proposed that defects trigger nanogap initiation by acting as seeds and potentially as guides to steer the nanogap path.

Moving to Chapter 3 we investigated the effect of localised heating in monolayer graphene. To introduce localised heating, we used femtosecond laser irradiation. During this thesis work, we implemented a new laser apparatus with a set of optical components aiming at controlling the laser exposures. In particular, we included several features such as an imaging system, a motorised stage and rotating polarisers to tune the laser power. Later, we added the possibility of monitoring the setup remotely with a computer. Using the apparatus, we carried out an exhaustive study of the

femtosecond annealing of graphene. We showed that laser irradiation results in either ablation or defect formation (vacancies) depending on the incident fluence. For monolayer graphene, we estimated the ablation and damage thresholds to be 11.8 and 2.95 mJ/cm², respectively. Next, we demonstrated that dynamic exposures allow introducing disorder with spatial control. Interpreting our experimental observations, we proposed that, under laser irradiation, graphene undergoes intense localised heating leading to oxidative burning in air. Additionally, we discovered that laser-induced defects were highly sensitive to subsequent laser exposures. This finding highlights the instability of a defective carbon lattice. At the end of this chapter, we

In Chapter 4 we combined our results from the two previous chapters. Indeed, we performed electro-burning of laser-annealed graphene devices. In other words, we examined the worst case scenario by both heightening current crowding and lattice weakening. First, we introduced a line of regularly spaced holes in the graphene device. By doing so, we showed that the nanogap preferably forms between the holes where current concentrates the most. In the second part, we investigated the influence of the defect density by proposing an efficient and repeatable method to yield controlled nanogaps in graphene devices. We tailor the path of the nanogap during electro-burning by selectively introducing, following a chosen pattern, a high density of defects in the graphene layer thanks to femtosecond laser irradiation. We used SEM based passive voltage contrast to track the nanogap path and verify the reproducibility of our technique. Using high defect densities (L_d from 2 to 7nm), we have a success rate of 92% over 26 samples. We used numerical simulation coupled with real-time infrared thermography to assess the thermal behaviour of the graphene devices during electro-burning. We found that electro-burning may occur at a temperature lower than 50°C for high defect densities.

Finally, in Chapter 5 we examined the possibility of replacing conventional metallic interconnects with carbon-based materials. Notably, we focused on 3D integrated circuits where heat extraction is crucial. We explored the use of a novel hybrid carbon structure composed of horizontal graphite interconnects connected to vertical through-substrate-vias made out of carbon nanotubes bundles. Via numerical simulation, we showed that the carbon structure vastly outperforms a CNT/Copper structure regarding electrical and thermal conduction. However, comparing with current interconnects (only copper), the results only show a slight advantage for the carbon materials. Looking at potential weaknesses, we found that current crowding could significantly increase with our geometry, especially at high frequency. Furthermore, we showed that anisotropy of the graphite interconnects increases current crowding up to a factor 40.

6.1 Perspective

The work presented in this thesis significantly improves our understanding of the mechanisms leading to the thermal failure of graphitic structures. Even though our work focused mainly on graphene, we can apply this reasoning to other graphitic structure such as graphite and CNTs due to the very high similarity of the lattice structure.

Under large current densities, graphene fails through a highly heterogeneous process resulting in the formation of a nanogap (for graphene and CNT). As shown in our experiments, biasing graphene triggers the formation of thermal hot spots that may host the initiation of a nanogap. As the nanogap starts propagating, the hot spot becomes dynamic and follows the crack tip until a complete rupture of the device.

At the atomic scale, we found that defects are critical enablers of the thermal degradation of the lattice. The formation of these defects is transient,

occurring in seconds under localised heating. Their effect is twofold: On the one hand, defects lower the stability of the lattice. On the other hand, they increase the resistivity resulting in greater Joule-heating. Therefore, the defect concentration should be maintained as low as possible.

However, we show an exception in Chapter 4 Selective patterning of defects with femtosecond laser yields a controlled, low-temperature electro-burning. In the future, graphene nanogap systems are seen as the fundamental building blocks of molecular electronics circuits. Therefore, in the perspective of large-scale fabrication, we expect this technique to allow innovative patterning possibilities, paving the way towards the development of nanogap-based molecular electronics circuits.

The use of carbon materials as replacement of metallic interconnects must be done carefully. Indeed, the advantages of carbon do not compensate for the drawbacks of metals depending on the applications. Giving directions for future research, the strength of carbon materials may be its robustness. Therefore, future work should aim at studying in details the reliability of carbon materials in rough conditions (corrosive, vacuum, frost) where they are expected to outperform metals significantly.

Future work should aim at studying the thermal failure of other graphitic structures. Counter-intuitively, the existing literature poorly describes the electro-burning of 3D carbon materials such as graphite and CNT bundles. Indeed, the nanogaps should propagate as 2D structures as opposed to the one-dimensional nature of graphene nanogaps. As a consequence, the propagation mechanisms of a 2D nanogap may be different. Given the lack of data in the literature, this needs to be addressed.

We can apply the same logic to the laser annealing part. Researchers have not studied in depth the irradiation of graphite and CNT bundle. Therefore, future research could examine the ablation and modification under various exposure conditions. Besides, we could perform femtosecond annealing of

other nanomaterials (e.g. MoS_2 , TeS_2) and extract, among others, the ablation and modification thresholds.

In addition, we implemented the possibility of controlling the repetition rate by using a pulse picker which contains an acousto-optic modulator or Bragg cell.

The Bragg cell consists of a SiO_2 optically polished slab, with a piezoelectric transducer bonded on one side. As shown in Figure 6.1 when we apply a radio frequency (RF) excitation to the piezoelectric transducer, this launches an acoustic wave into the slab. This acoustic wave, can be considered, as a plane wave travelling in the direction perpendicular to the PZT bonded slab face. Since the optical index of refraction in the material is coupled to the modulating strain field of the acoustic wave through the photo-elastic effect, the regions of compression and expansion exhibit a different index of refraction. Thus, this acoustic wave creates a dynamic optical grating that can diffract the incident light.

Figure 6.1: Bragg Cell Simplified Functional Diagram

Therefore, by syncing the RF signal at the input of the pulse picker with the laser pulse train, it is possible to select which laser pulse to be diffracted. Indeed, in the absence of any signal, the laser beam entering the pulse picker is stopped via a beam stop. As shown in Figure 6.2 if an RF pulse is sent with a controlled delay, amplitude and width, the incoming laser pulse will be "picked" and deflected out of the pulse picker. By sending RF pulses at specific frequencies, we can control the femtosecond laser repetition rate. As mentioned in section 3.1.3 the pulse picker reduces the repetition rate.

Figure 6.2: Pulse Picker Timing Diagram

This would potentially remove any incubation effect thus leading to non-thermal degradation of matter.

Finally, the work presented in chapter 4 on the low-temperature controlled electro-burning of graphene needs to be continued exhaustively. For instance, future work should aim at assessing the limit of the patterning control. As shown in the Chapter, the nanogap can follow the line of defects even when the pattern is not perpendicular to the current flow (crenellated patterns). It would be of great interest to investigate the limits of this technique by tuning the defect line geometry. Can we draw complex patterns or mainly straight lines?

To further investigate the potential of using CNT/Graphite 3D interconnects presented in Chapter 5 future work should focus on the experimental fabrication and characterisation of this structure. The project is currently undertaken by other members of the research group and some preliminary results have been obtained:

Figure 6.3: (a) Schematic illustration of the fabrication and assembly process of the CNT/graphene structure (b) SEM and optical micrograph (c) of the structure after CNT growth and graphene transfer. The multilayer graphene covers the entire surface. Courtesy of Zhu Ye: Assembly Process and Electrical Property of Top-Transferred Graphene on Carbon Nanotubes for Application as Carbon-Based Three-Dimensional Interconnects

As shown in Figure 6.3(a), CNT/graphene structures were fabricated by first patterning and depositing bottom gold electrodes. Catalyst for CNT growth was patterned onto the gold electrodes and subsequently, CNTs were grown. PET spacer with the same height as the CNTs were placed beside to act as support to prevent the damage of the CNTs during the graphene transfer process. Graphene on PET substrate was placed face down in contact with the CNTs and secured with adhesive. The free-standing CNTs were grown by thermal CVD method with hydrogen and acetylene gas flows. Figure 6.3(b) and (c) show the resulting structure observed with SEM and optical microscope. Although transparent, the graphene can be spotted in (c) thanks to its visible network of grain boundaries.

Next, we compared a CNT/graphene and CNT/Au contact. The electrical characterisation reveals a similar contact resistance for both structures.

However, as shown in section 5.1.4, there needs to be covalent bonding in order to have a good electrical contact between the graphene and the CNTs. Future work will focus on improving the electrical contact between the graphene and the CNTs by using annealing techniques with the hope of fusing graphene and CNTs together.

6.2 Author's publication

6.2.1 Journal papers

1. Ange Maurice, Laurence Bodelot, Beng Kang Tay, and Bérengère Lebental Controlled, low-temperature nanogap propagation in graphene using femtosecond laser patterning. *SMALL*, 2018 [DOI:10.1002/sml.201801348](https://doi.org/10.1002/sml.201801348)
2. Boris Vaisband, Ange Maurice, Chong Wei Tan, Beng Kang Tay, and Eby G Friedman. Electrical and thermal models of CNT TSV and graphite interface. *IEEE Transactions on Electron Devices*, 65(5):1880–1886, 2018. [DOI:10.1109/TED.2018.2812761](https://doi.org/10.1109/TED.2018.2812761)
3. Songyan Hou, Muhammad Danang Birowosuto, Saleem Umar, Maurice Ange Anicet, Roland Yingjie Tay, Philippe Coquet, Beng Kang Tay, Hong Wang, and Edwin Hang Tong Teo. Localized emission from laser-irradiated defects in 2d hexagonal boron nitride. *2D Materials*, 5(1):015010, 2018. [DOI:10.1088/2053-1583/aa8e61](https://doi.org/10.1088/2053-1583/aa8e61)
4. Umar Saleem, Muhammad Danang Birowosuto, Songyan Hou, Ange Maurice, Tay Beng Kang, Edwin Hang Tong Teo, Maria Tchernycheva, Noelle Gogneau, and Hong Wang. Light emission from localised point defects induced in GaN crystal by femtosecond-pulsed laser *Optical Materials Express*, 2018, **Accepted**.

6.2.2 Conference papers

5. Loïc Loisel, Ange Maurice, Bérengère Lebental, Stefano Vezzoli, Costel-Sorin Cojocaru, and Beng Kang Tay. A graphene-based non-volatile memory. In *Carbon Nanotubes, Graphene, and Emerging 2D Materials for Electronic and Photonic Devices VIII*, volume 9552, page 95520R. International Society for Optics and Photonics, 2015. [DOI:10.1117/12.2188110](https://doi.org/10.1117/12.2188110)

6. Loïc Loisel, Ange Maurice, Bérengère Lebental, Stefano Vezzoli, Costel-Sorin Cojocaru, and Beng Kang Tay. A Non-volatile Memory Based on Disordered Graphene In *SPIE Nanoscience and Engineering 2*, 2015 [HAL-ID: hal-01798526](#)

6.2.3 Working papers

7. Ange Maurice, Beng Kang Tay, and Bérengère Lebental. Femtosecond laser irradiation of graphene: A systematic study In *Applied Physics Letters*,
8. Ange Maurice, Laurence Bodelot, Beng Kang Tay, and Bérengère Lebental. Electro-burning of graphene, a highly heterogenous process In *Applied Physics Letters*
9. Boris Vaisband, Ange Maurice, Chong Wei Tan, Beng Kang Tay, and Eby G Friedman. A multi-bit CNT TSV In *Solid state Electronics*

List of changes

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Appendix A

	CNTs	Graphene	Graphite	Diamond	Silicon	Copper	Aluminium
Electro-migration	-	-	-	-	Yes	Yes	Yes
Maximum current density ¹ (A/cm^2)	10^8 [64][65]	10^8 [66][67]	-	-	-	10^5 [242][243]	10^5 [242]
Thermal conductivity (W/m/K)	3500 [44][244]	5000 [245]	$1700^{\parallel}/8^{\perp}$ [246]	2200 [247]	150 [248]	400 [249]	237 [249]
Electrical resistivity ($10^{-8}\Omega.m$)	1.5^2 [39]	1.5 [250]	$47^{\parallel}/10^{5\perp}$ [246]	-	-	1.68 [251]	2.82 [252]
Thermal expansion coefficient ($10^{-6}K^{-1}$)	7.5 [45]	-0.8 [37]	$7.8^{\parallel}/26^{\perp}$ [28]	0.8 [22]	5 [253]	16 [253]	21 [253]
Young Modulus (GPa)	1000 [42]	1000 [35]	$20^{\parallel}$ [26]	1000 [19]	150 [254]	130 [255]	-
Tensile strength (MPa)	63 000 [256]	130 000 [35]	137 [26]	60 000 [257]	200 [258]	262 [259]	40 [260]

Properties of current IC materials compared to carbon-based materials. This table is also shown in section [1.5](#) without the references

¹ For a micrometer-sized interconnect ² CNT dimensions: 1 nm wide, 1 μm long