Fault tolerance and protective schemes for DC power distribution

Yap, Heng Goh

2018

Yap, H. G. (2018). Fault tolerance and protective schemes for DC power distribution.
Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/89768>

<https://doi.org/10.32657/10220/46414>

Fault Tolerance and Protective Schemes for DC Power Distribution

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**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

**A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy**

2018

Acknowledgments

As this PhD research journey comes to an end, it is time to express my sincere gratitude to all the great people who have continuously helped and encouraged me along the way. They have made over a thousand arduous days of study and work into bright memories. This dissertation belongs not only to the author but also to all these people.

First of all, I would like to express my sincere respect for my supervisor, Assistant Professor Xu Yan. I would like to thank him for taking me as his student and his continuous support, guidance, and tolerance for my research. I will never forget the constructive discussions we had during in these few years. His encouragement made me feel brave when confronting the unpredictable challenges of my research life.

I would like to express my gratitude to my former supervisor Professor Tseng King Jet, a man who has devoted his life to the field of Power. I thank him for introducing this research and giving me the opportunity to work on this project. He is erudite, knowledgeable, friendly, and generous and has almost all the virtues a great professor could have.

I am greatly deeply grateful SINBERBEST funding me in the form of research scholarship. I greatly appreciate the School of EEE, Nanyang Technological University for providing me with the financial support in the form of research scholarship.

Last but not the least, I would also like to use this opportunity to thank my parents and friends for their full support and encouragement throughout my research work.

Abstract

The integration of distributed generation such as renewable energy at the distribution is considered as the better option to cope with the rising demand for electrical energy. The storage system is also introduced to act as an additional power buffer to the power system due to the intermittent supply of energy from the distributed generation. With the addition of these 2 DC energy systems, the DC distribution system can achieve a better system efficiency than the AC system. The DC system can reduce the power conversion stages such as the power factor correction and a rectifier circuit. Of the advantages, the fault protection is the major obstacle for the DC system to move forward. Hence, a research topic is brought out with the major aim is to develop an effective fault tolerance solution to increase the resiliency of the DC distribution system. Complete fault tolerance and protection process with the sequence is: 1) fault detection, 2) fault isolation, 3) fault identification, 4) fault recovery.

In the DC system, a fast tripping speed of the circuit breaker can reduce the consequences of high fault current sourcing toward the fault point. A T-source circuit breaker is a device for the fault detection and isolation in the DC system. The T-source circuit breaker is a kind of impedance-network based circuit breakers which provide a high-speed breaking capability, and no sensor is required. It also has the benefit of preserves a common ground, zero reflected source current, and provide a low-pass filter behavior. The achievement low output surge fault current is presented. The T-source circuit breaker is modeled in pre-tripping state and post-tripping state. The circuit breaker capacitance of the T-source circuit breaker is selected using the proposed design flow based on the criteria of the current rating, and the load capacitance. The post-tripping model is used as a reference for the output surge fault current to determine the transformer inductance. A manual tripping circuit modification for the protection of SCR device in the T-source circuit breaker is also presented. The selection of the resistor in the modification circuit is based on the current rating.

A high accuracy fault identification solution can ease the task of inspection, maintenance, and the repair work. High accuracy can also speed up the restoration service and possesses the merit of less maintenance cost. The probe power unit is a kind of signal injection method. The chosen of the probe power unit as the solution for fault location identification is due to the benefit of single end injection which does not require multipoint measurement, no high data acquisition needed. This method can be

used as the fault point tracking in an offline mode whereby the fault current from source has interrupted completely. The logarithm decrement technique is introduced to obtain the damping constant of the damping injection current. The logarithm decrement technique has the advantages of high accuracy, less data reading needed, and fast processing speed. The component selection of the probe power unit with the inductor and capacitor pair value is based on the maximum detectable fault resistance and the peak current deviation tolerance. A wider range of fault resistance can be identified for the fault location identification using the proposed design probe power unit. A modification of the probe power unit circuit associated with the proposed parallel fault identification flow can determine the exact fault segment line with the respective location. This fault identification solution provides information to the fault segment isolation of a complex network such as a meshed network.

Fault recovery is a final step of the fault protection process which recovery the non-faulty system back to normal operation. The DC distribution system has various facilities using a different power converter. The standard facilities in the microgrid include the grid interfacing system, the storage system, and the photovoltaic system. A DC circuit breaker is used as the fault interruption device instead of the AC circuit breaker in the DC distribution system. The different placement of DC circuit breaker needs different reconfiguration step than conventional AC circuit breaker for reconnecting the facilities back to the grid. The reconfiguration step is the order of action between the deblocking the power converter and the reclose of DC circuit breaker. The simultaneous connection and sequential connection is compared for the system recovery of facilities. The sequence of reconnecting each facility back to the DC network is demonstrated. Minimum transient of voltage and current profile is chosen as the system recovery step to achieve a stable fault recovery.

As above mentioned, the main reason for introducing fault tolerance and protection scheme into the DC system can increase overall system reliability. This protection scheme can prevent a harmful high current triggered in a fault event. In the result, the proposed solution can prevent damaging the non-fault device or facilities attached to the DC system and restore back the facilities into normal mode once the fault point is isolated from the system.

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Chapter 1. Introduction

1.1 Background

The distributed energy is one of the methods to cope with the electrical energy rising demand. The integration of renewable energy sources is the distributed generation to the power systems. As renewable energy sources are intermittent, energy storage system is introduced to act as an additional power buffer to the power system. At the last-mile power system, the use of DC loads is increasing in the coming future. Fig 1-1 illustrated a few examples of DC load, distribution generation system, and energy storage system.

Fig 1-1. The examples of DC load, distribution generation system, and energy storage system

With the emergence of DC energy systems and the increasing use of DC loads, the DC distribution system can achieve a higher overall system efficiency. The increase in system efficiency is due to the reduction in power conversion stages such as power factor correction and rectifier circuit[1]. [2] shows the power loss of each energy conversion is about 2.5%. In contrast, the utilization of the DC to the distribution system has lower conversion losses. For example, every single DC load require a power factor correction circuit and a rectifier in the adapter when connecting to the AC system. The introduction of DC distribution systems can eliminate the power factor correction circuit and rectifier with the result of enhancing overall system efficiency, reducing the power converter size, and reducing the power losses at every conversion point.

In fact, the DC system has a benefit of eliminating the low-frequency ripples generated from the loads and the AC grid system. This low-frequency ripples can cause a low-efficiency energy harvesting for the renewable energy system due to difficulty in tracking the maximum power point. Apart, the connection of renewable energy system has to meet the requirement of the AC distribution systems inherent features such as frequency synchronization and reactive power issues whereas these features are immune in the DC distribution system. Several research entities such as Zero Energy Building Consortium and EMerge Alliance show the utilization of the DC system to a building can achieve a significant energy saving[3]. Fig 1-2 shows the summary result of energy savings for each application when applying DC systems to a building.

Building Applications (in priority listing of EMerge Alliance)	Ave % of Building Energy Used	Potential Energy Savings by Going DC	Keys to Maximizing Efficiency in Going DC
Interiors (Lighting)*	28%*	Up to 15%	LED, Renewables
Data/Telecom	17%	Up to 30%	Highervoltage, Renewables
Service/Utility (HVAC)	36%	Up to 10%	Renewables
Outdoor	6%	Up to 10%	LED, DC CPEVs, Renewables
Other (misc equip loads)	13%	Up to 5%	Different voltage conversions

Fig 1-2. Energy Saving for different application in DC Building Distribution System[3]

A 48Vdc voltage is now widely used for switching facilities, servers, and routers in telecommunication building. The exponential increase of DC load causes the load current drawn higher. Eventually, the low voltage and large current will cause more power loss at the transmission line. The system needs bigger size cable for more power transmission and would incur a higher cost for the adoption of DC system at the distribution. For the low voltage power loss problem, the NTT group proposed a voltage level with 380v for the DC distribution systems in the year 2008[4]. The standard communities such as ETSI and EMerge Alliance have formulated a standard that deals with 380V for the DC distribution system[3]. [5] shows the efficiency comparison of several different voltage levels for DC and AC as the system. The result shows 380Vdc has better efficiency in the high load condition.

The introduction of the DC system is an outgrowth concept for the multi-terminal system with different facilities. A meshed network was proposed in [6] and the adoption of the meshed network as the DC distribution system network in this research. The chosen of the meshed network is due to higher reliability in comparison to the radial network in term of fault. The meshed network has the advantage of

recover back entire facilities with the occurrence of a fault in any transmission line segment. Fig 1-3 shows four terminals meshed DC network[7, 8]. The commonly seen facility in the distribution system is grid interfacing system, storage system, renewable energy system. For a country in the tropical zone such as Singapore has rich sunlight. The utilization of solar energy produced DC energy from the photovoltaic cell is the primary choice as the distributed generation source. These facilities are located at different places in the meshed network as shown in Fig 1-3 with a 380Vdc in normal operation.

Fig 1-3.The DC microgrid Meshed Network

Of the introduction of the DC distribution system and the advantages, one of the main challenges of the DC distribution system implementation is the fault protection. The continuous fault current in the DC system has the consequences of destructive arc erosion effect at the fault location, the system-wide collapse of the bus voltage, loss of power, and possibly damage another non-fault application.

The cause of a fault in the DC system is usually a short circuit of at the DC transmission line or the load side. The short-circuit fault is categorized as the line to line fault and the line to ground fault. The line to line fault is generally a short circuit in between positive and negative phase, whereas the line to ground fault occurred when either positive or negative phase is shorted circuit to ground. The characteristic of line to line faults are usually a low fault impedance, and the characteristic of line to ground faults can be high fault impedance and low fault impedance depending on the grounding configuration[9, 10]. The fault with low impedance can cause an overcurrent effect to the DC system, and, propagates to other healthy section of the networks eventually.

Typically, the two sources feed the fault are: 1) the power source through power converters from the grid, renewable energy, and storage system, uninterrupted power service system, etc. 2) the smoothing capacitor in the power converter. The fault withdraws a large magnitude fault current from the power source and discharges the stored energy from the smoothing capacitor toward the fault point in a short time. Consequently, DC system results with a high amplitude fault current in short rise time. The derivation of fault currents from the power source and the capacitor are shown (1-1) and (1-2) respectively[11-13]. The V_{dc} is the line voltage, R is the summation of fault resistance and DC transmission line resistance, L is inductance in the DC transmission system, C is the smoothing capacitor in the power converter, ξ is the damping ratio of the fault current drawn.

$$i_{\text{fault}}(t) = \frac{V_{dc}}{R} \left(1 - e^{-\frac{R}{L}t} \right) \quad (1-1)$$

$$i_{\text{fault}}(t) = \frac{V_{dc}}{L\xi} e^{-\frac{R}{2L}t} \sin(\xi t) \quad (1-2)$$

$$\xi = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$$

The high magnitude fault current flow to the DC system as the fault consequences brings out a research topic with the major aim is to develop an effective fault tolerance solution to increase the resiliency of the DC distribution system. A robust fault tolerance and protection solution can minimize the effect of fault disturbance and recover the DC system back to normal operation. The fault tolerance process consists of fault detection, fault isolation, fault identification, fault recovery with the process sequences as shown in Fig 1-4. Few literature reviews presented in the sequence of the fault identification is taken places before the fault isolation. The reason is due to a fault current limiter is exploited as the device to suppress and limit the fault current before fault isolation[14-17]. For an AC system, the long breaking operation time before the tripping of the mechanical circuit breaker is used as identifying the fault segment and fault location. However, the DC system would like to have a fast speed isolation device in the absence of the fault current limiter device. A shorter tripping time can reduce the magnitude of fault current significantly. Hence, the fault isolation should have taken place before the fault identification for a DC system with a result of reducing the fault current magnitude feeding to the DC system.

Fig 1-4. The Sequence of Fault Tolerance Process

The fault detection is a step that makes a judgment of the presence of a fault in the downstream system. The detection device provides fault information to the fault isolation device and to interrupt the continuous feeding of fault current. The fault identification is a step that determines the fault segment and location in the system and provides the information for further isolates the fault segment for the system recovery purpose. Finally, the fault recovery will take place to reconfigure the system and restore back to normal operation for the non-faulty device in the DC system.

1.2 Motivation

For an AC system, the conventional solution for the protection is the utilization of an AC circuit breaker or a fuse to detect and isolate the fault. The fuse and AC circuit breaker can interrupt the fault current. The AC circuit breaker trips at the zero crossing points which occur at every half period to extinct the arc between the parting contacts. However, the DC fault is not the same as the AC fault. The DC fault does not have a natural zero current crossing so that the arc can be extinguished when the AC breaker opens. One method of using the AC breaker for DC fault protection is to locate the AC breaker at the AC side of the power converter, and a DC switch at the power converter DC end to interrupt the DC fault [18-20]. The AC circuit breaker trips the fault current first, and the DC switch activates once it has fallen smaller than the threshold magnitude. The entire fault isolation process takes a time of around 0.1s. This interruption time is relatively slow for a DC system and might have a chance to damage the equipment attached to the DC end. A fast fault interruption speed can reduce the consequences of high magnitude fault current propagates along the DC system. Hence, an alternative fault isolation solution for the DC system is required instead of the commercially available AC circuit breaker.

Alternatively, the introduction of the hybrid circuit breaker[21-27] and the solid-state circuit breaker[28-31] can resolve the DC fault. Hybrid circuit breaker requires additional auxiliary solid-state device together with a mechanical circuit breaker to isolate the fault. The slow speed mechanical switch in the hybrid circuit breaker is the limiting factor of the circuit breaker tripping speed. Typically, the tripping

process can up to a millisecond time and consequently may result in a high fault current. A solid-state circuit breaker can increase breaking speed, but its disadvantage is in its operating losses.

Moreover, most of the hybrid and solid-state circuit breaker require an additional current sensor to detect a fault which would increase the time of fault isolation process and increase the cost. The SCR device has a relatively low conduction loss than the other solid-state device such as IGBT[32]. In existing literature together with the SCR device, the use of impedance-source network circuit breaker is a kind of SCR solid-state circuit breaker. The impedance-source network circuit breakers in existing literature are cross Z-source[33], parallel Z-source[34], series Z-source[35], and coupled inductor[36].

However, different impedance-source circuit breakers have their disadvantage. The crossed Z-source does not provide common ground between source and load terminal due to the return path inductor placement. There is no common connection at the negative rail for the input and output terminal of the circuit breaker. The parallel and series Z-source has a reflected current at the source after fault clearance. The reflected-source current is due to an inductor is placed at the source side that causes the current across source inductor cannot vanish immediately. A transformer-based impedance source circuit breaker termed as coupled-inductor circuit breaker preserves a common ground connection and zero-reflected current. However, the coupled-inductor circuit breaker has a notch filter behavior with the improper design. A new topology was proposed in [37] terms as T-source circuit breaker can also cope with common ground, zero reflected source current. At high frequency, the T-source circuit breaker is a resonator, and it has an attenuation behavior and negative phase if primary to secondary transformer winding ratio is more than one. Compare to previous Z-source circuit breakers topology, T-source circuit breaker requires only a transformer, and one capacitor, which can reduce the use of one capacitor and one inductor core compare to previous introduced Z-source circuit breakers. The component reduction shows an increase in overall system reliability and a cost reduction. As a result, the fault detection and isolation device in this research is the T-source circuit breaker.

After the tripping process, a fault segment and location are required to identify and isolated before a system restores back to normal operation. Without this action taken, the system recovery will turn into a tripping state again if there is a permanent

fault in the DC system. A high accuracy fault identification solution can ease the task of inspection, maintenance, and the repair work. It can also speed up the restoration service and possesses the merit of less maintenance cost. For an AC system, the adoption of phasor measurement unit is the common method for fault location identification [38-42]. This approach utilized the synchronize positive sequence of voltage and current measurement on each bus to determine the fault branch and fault location. The fault isolation of the AC system has a millisecond range of time before circuit breaker tripping. This feature allows the capture of voltage and current data measurement before tripping. However, the difficulty of phasor measurement unit apply in the DC system is the absence of the voltage and current measurement after tripping. The DC system requires a fast speed tripping to interrupt the fault current to prevent the consequences of high magnitude fault current in the DC system.

The traveling wave method and the injection-based method are the two-major fault location identification approaches that are using for the DC system. The traveling wave method utilizes the propagation wave along the transmission line and the surge arrival time to determine the fault location. A single-end traveling wave method using two consecutive reflected waves to determine the fault location identification [43-48]. Two end traveling wave method captures the waves at both ends of the feeder [49-51]. High dependencies of sampling time, sampling synchronization (for two ended method), and uncertainties of traveling wave propagation velocity determine the accuracy of fault location identification. The injection-based method uses an extra voltage transformer [52, 53] or compensation coil [54, 55] as the injection tool to identify the fault location. These injection methods require multipoint measurement for the fault location identification.

On the contrary, the offline method has a great advantage of localized fault after source-fault isolation. The time-frequency Domain Reflectometry method is an offline method and taking the Euclidean distance as the fault location [56]. The measurement of fault distance is the time differences of time-frequency distribution of injected reference signal to the cable and the reflected signal. Alternatively, the probe power unit as an offline single-ended method was introduced to identify a fault location[13]. The probe power unit injects a resonant current to the transmission line. The injected current decaying with time and this decay factor contains the fault information which allows identifying fault location. The probe power unit has the benefits of high accuracy with low data acquire needed. It has an advantage of no

waiting reflected signal compare to the time-frequency Domain Reflectometry method which results with no sampling time required. The injected signal velocity from the time-frequency domain reflectometry method is dependent on the transmission medium and might be distorted when the injected signal is traveling along the transmission medium. Hence, the probe power unit method is the better option chosen as the offline fault identification device for the fault location identification in this research.

The fault recovery is the final step of the fault protection process. The system recovery can entirely or partially restore the system back to normal operation without waiting for repairing and staying at outage for the whole system. However, the literature of the fault recovery of the power system is rare. The system stability of reconnecting the application back to the DC system is the most concern for system recovery. A stable DC voltage and current in the DC system is the goal of system recovery. In the DC system, various facilities application in the DC distribution system that adopts a different type of power converter. Each facility power converter performs differently toward the DC distribution system.

A system reconfiguration sequence was proposed for an offshore wind farm integration to the grid with the adoption of the modular multilevel converter(MMC) as the common converter in the multi-terminal HVDC(MTDC)[20, 57]. However, the adoption of AC circuit breaker system reconfiguration can have a different result for DC circuit breaker due to the placing of DC circuit breaker is at power converter DC side. The DC circuit breaker that using the same reconfiguration step as AC circuit breaker can result with high transient DC voltage at the initialization stage.

1.3 Problem Description

Of all the listed advantages of the T-source circuit breaker, there are few limitations in existing literature review:

- 1) The transformer inductance and the capacitance selection of the T-source circuit breaker prototype design in [37] are 232mH and 940uF respectively. These components values are oversized and relatively large for 15V input voltage. In contrast, the transformer inductance and the capacitance chosen of the T-source circuit breaker for the simulation in [37] are 240uH and 100uF. These component value might cause tripping to fail when the load capacitor is large.

- 2) The circuit breaker current rating is not stated in the literature which is the important metric for the circuit breaker.
- 3) High output surge fault current may damage the to the downstream attached device. Low output surge fault current to the nominal current ratio indicates good effectiveness design for the impedance-source circuit breaker. TABLE 1-I shows the comparison of different transformer-based impedance source circuit breaker. From the experiment and simulation result, the coupled inductor circuit breaker has a relatively high metric ratio of output fault surge current to the nominal current. The design of T-source circuit breaker in [37] for simulation and experiment is different. The metric ratio of 15 for the simulation result is high whereas the metric ratio for the experimental result is low due to the high-value transformer magnetizing inductance 232mH.

TABLE 1-I: The result of the output surge fault current to the nominal current for various topology

Current Topology	Simulation				Experiment			
	Nominal Current	Output Fault Surge Current	Metric Ratio	Fault resistance	Nominal Current	Output Fault Surge Current	Metric Ratio	Fault resistance
Coupled-Inductor [14]	2A	75A	37.5	0.01ohm	2A	90A	45	0.01ohm
T-source [17]	1000A	15000A	15	0.1ohm	0.44A	3A	6.8	0.5ohm

Of all the listed advantages of the probe power unit, there are few limitations in existing literature review:

- 1) The fault location identification using probe power unit has not considered the damping coefficient, and the natural frequency was assumed the same as the damping frequency [13]. The inconsideration of damping coefficient technique brings a low accuracy at high fault resistance and short fault distance. Another technique in the literature is the probe power unit associated with the least square error method to find out the damping coefficient [58]. The least square error method provides a result with the error reduction for the fault distance measurement. However, this technique requires high numbers of data reading with using pseudo-inverse matrix solution. This technique has the disadvantages of slow computation time and low accuracy for high fault resistance.
- 2) There is no investigation of high fault resistance for the fault location identification. Taking underdamped current into consideration, the selected inductor and

capacitor pair value of the probe power unit design in [13] can only identify the fault location with the maximum fault resistance is 9.866ohm

Of all the listed existing fault recovery sequence, the existing literature review does not show:

- 1) The effect of adopting the DC circuit breaker and the sequence of reconfiguring the power converter and DC circuit breaker.
- 2) The comparison of simultaneous connection and sequence connection
- 3) The comparison of different connection sequence for the facilities to the DC network

1.4 Proposed Solution and Contribution

The design of the T-source circuit breaker for optimum size and achieve a low output fault surge current is presented in this thesis. The introduction of the T-source circuit breaker model to provide a mathematical derivation and design analysis for the components selection of the T-source circuit breaker. The load capacitor and the desired maximum added load/minimum added resistance are the metrics of circuit breaker capacitor selection. The selection of transformer inductance is determined by the current rating of the circuit breaker in which the output surge fault current does not exceed the current rating. Additionally, the T-source circuit breaker is modified to achieve manual tripping capability for device protection. The resistor used for modification circuit is determined based on the current rating to ensure manual tripping work.

The probe power unit is a device for fault location identification. A simpler fault location identification technique to obtain the damping coefficient using logarithm decrement technique is presented in this thesis. The logarithm decrement technique can increase a much better accuracy with the advantages of less data reading needed and fast processing speed. The inductor and capacitor of the probe power unit are reselected to achieve a higher range of fault resistance for fault location identification. The peak current deviation tolerance and the maximum detectable fault resistance are the factor in determining the probe power unit inductor and capacitor pair value. Adding the current probe at each junction terminal to form a parallel probe power unit and the proposed parallel path fault identification flow can accurately identify the fault segment and the fault distance of the multiple parallel path networks.

In the extension from the existing literature, the reconfiguration step of grid interfacing system, storage system, and distributed generation system back to the DC system are shown. The reconfiguration step shows the priority of the reclose of DC circuit breaker and deblock the power converter for each facility. The comparison of simultaneous connection and sequence connection for the facilities to the DC network. Apart, the connecting sequence of all facilities at different timing to the DC system is compared for the system recovery.

1.5 Objective

There are several objectives for the fault protection process of DC distribution systems. The following is the list of scope:

1. Design an optimum size for the T-source circuit breaker and achieve a low output fault surge current.
2. Increase the accuracy of probe power unit solution for the fault location identification in the DC system and widen the fault resistance range for fault location identification.
3. Show a stable system recovery process with least transient for different facilities reconnected back to the DC distribution system

1.6 Organization of the thesis

Chapter 1 introduces the background, motivation, problem description, proposed solution and contribution, the objectives of each section, and the organization of this thesis.

Chapter 2 shows the literature review of solid state, hybrid, impedance-based DC circuit breaker. This chapter also presents the literature review of the previous solution for fault segment and location identification. The fault identification technique includes a traveling wave method and a signal injection method. The last part is the recovery process literature review.

Chapter 3 shows the T-source circuit breaker basic operation, analysis, and the component value determination. The modeling of the T-source circuit breaker is pre-tripping modeling and post-tripping modeling. The pre-tripping model is used as the analysis of the tripping operation, and the post-tripping model is a reference for output fault surge current. Then, a design flow is introduced for the component sizing purpose. Finally, the simulation result verifies the chosen component design. In addition, a

modifying the T-source circuit breaker to achieve the manual breaking capability is shown.

Chapter 4 presents the use of probe power unit with the propose logarithm decrement technique for fault distance calculation. The comparison of the propose logarithm decrement technique with the no decay technique and the least square error technique is shown. Then, the probe power unit is redesign based on a proposed flowchart to widen the range of fault resistance for fault location identification. The comparison of fault distance calculation accuracy is illustrated for a various range of fault resistance for the selected components of the probe power unit design. The introduction of parallel probe power unit for identifying multiple parallel paths. The modification probe power unit associated with the multipath fault identification flow can identify the fault segment and fault distance.

Chapter 5 demonstrates the fault recovery reconfiguration and the reconnection to the facilities in the DC system. The facilities in the DC system consists of grid interfacing system, storage system, and the photovoltaic system. The commonly seen power converter for each facility is selected. The reconfiguration step of reclose the DC circuit breaker and deblock the power converter. A comparison of simultaneous connection and sequences connection to the DC network is compared. Finally, the sequences of reconnecting the facilities back to the DC system is illustrated. The reconnection with the result of least transient in voltage and current is chosen for the system recovery.

Chapter 6 concludes the proposed fault protection solution. Then, a discussion of the future work with the fault tolerance solution that can improve the reliability of the DC distribution system is presented.

Chapter 2. Literature review

2.1 Fault Detection and Isolation - Circuit breaker

Many tripping devices were proposed for the DC system, such as a fuse, mechanical circuit breaker, power converter based circuit breaker, solid-state circuit breaker, hybrid circuit breaker, impedance-source network circuit breaker. The fuse interrupts the fault current by melting the conduction wire when the current over the threshold with generating heat within the device. However, the fuse has a problem with a long time constant and incapable to reuse. For the AC circuit breaker as mentioned in chapter 1, the interruption process takes a long time, and it generates a dangerous arc for a non zero crossing current interruption. Hence, the fuses and AC circuit breaker are not considered to be used as the tripping device in the DC system. Fig 2-1 shows a summary of the literature review of the interruption device for the DC system. The following will discuss the pros and cons of each source interruption device for DC system fault isolation.

Fig 2-1. The circuit Breaker type for the DC system

2.1.1 Mechanical circuit breaker

Fig 2-2a shows a general mechanical DC circuit breaker circuit diagram which consists of a varistor, a mechanical switch, and a commutation path[59]. The modeling and the control logic of mechanical DC circuit breaker were presented in [60]. The current flow through the mechanical switch at normal operation and commutated to the commutation path at the fault state for the current interruption. The DC mechanical circuit breaker tripping process diverts the fault current from the mechanical switch to the commutation path. The commutation path consists a series inductor-capacitor component that generates an oscillation current at the fault event to cause the current zero-crossing. The commonly seen vendors of DC mechanical circuit breaker in the market are ABB, Schneider, Siemens, Carling [61]. The example of mechanical DC circuit breaker is illustrated in Fig 2-2b. The DC mechanical circuit breaker has a drawback of slow speed interruption which the interruption time is about 5ms. [59] show a

mechanical circuit breaker can interrupt 5kA current in 3ms. The slow speed tripping of mechanical DC circuit breaker will cause a high magnitude of fault current drawing to the fault. Consequently, the high magnitude fault current has a chance to damage interval device attached.

Fig 2-2. (a) the common mechanical circuit breaker circuit diagram[59] (b) the commercial available mechanical switch

2.1.2 Power converter-based circuit breaker

A direct power or current control associated with the integration of fault current handling capability within the power converter can shut down the gating of a power converter to transform it into a fast acting current limiting circuit breaker[62].

However, certain power converter such as a single phase-controlled rectifier does not fully interrupt the fault current even the gating is shut down. The replacement of all uncontrollable diodes in the power converter to an active switch can achieve current limiting capability[63]. Fig 2-3 shows a single-phase rectifier as an example of a power converter-based circuit breaker with the replacement of an antiparallel diode to the controllable switches. The modification of power converter to power converter based circuit breaker has the advantage of no additional power loss across the breaking device at the conduction state as compared to the common series circuit breaker. However, a high number of controllable switches in the power converter for the circuit breaker transformation will lower the system reliability, and the original control method require a change.

Fig 2-3. The replacement of antiparallel diode to the controllable switches for power converter based circuit breaker[63]

TABLE 2-1: Summary of Power Converter-based Circuit Breaker

Type of Power Converter Circuit breaker	Auxiliary Controlled method [62]	Replacement of uncontrollable diode to active switch[12, 63]
Circuit diagram		
function	<ul style="list-style-type: none"> Shut down the gating of the power device in the power converter No modification on the original power converter 	<ul style="list-style-type: none"> The controllable switch can interrupt the continuous current flow at the fault event
disadvantage	<ul style="list-style-type: none"> Does not fit all power converter such as switches in the rectifier has an antiparallel diode can bypass the fault current 	<ul style="list-style-type: none"> the high number of controllable switches can lower system reliability require the changes of the control method

However, the smoothing capacitor in the power converter discharges during fault remains is uncontrollable. The high discharging current can cause damage to the attached equipment in the DC system[64]. A modification of the smoothing capacitor by adding switching devices and inductor in series can limit the discharging current during a fault happens. Fig 2-4 shows the modified smoothing capacitor branches with the series inductor is added to limit the fault discharging current. The drawback is an additional power loss in the normal operation due to the charging and discharging of the smoothing capacitor with the current pass by the switching device[12].

Fig 2-4. The capacitor branch as a current limiter[12]

[63] shows the emitter turn off(ETO) thyristor as a current limiting device and can be placed at in series with the smoothing capacitor. The ETO can achieve a low power loss in normal operation. However, the ETO is no adopted as the current limiting device in practical is due to the ETO has an enormous size compared to the size of the power converter[65].

In overall, the transformation of the power converter to a circuit breaker has the concern of auxiliary controlled, uncontrollable diode replacement, and smoothing capacitor modification. All the changes in the power converter can bring the system to a more complex level.

TABLE 2-II: Summary of the current limiter devices of smoothing capacitor for Power Converter-based Circuit Breaker

Smoothing capacitor modification	Current Limiter[12]	ETO[63, 65]
Circuit diagram
function	<ul style="list-style-type: none"> The series inductor is activated in the fault state the series inductor can limit discharging current 	<ul style="list-style-type: none"> The thyristor-based switching has a low power loss in normal operation
disadvantage	<ul style="list-style-type: none"> Additional power loss due to charging and discharging current pass by the switching device in normal operation 	<ul style="list-style-type: none"> Bulky size compares to the power converter

2.1.3 Hybrid DC circuit breaker

The integration of mechanical switch and snubber static branch form a hybrid circuit breaker. The hybrid circuit breaker was introduced in the early literature [21], and the general review of the hybrid circuit breaker is shown in [66]. The hybrid circuit breaker has the benefit of low conduction loss due to the current only pass through the mechanical switch in the normal operation. The hybrid circuit breaker tripping operation relies on the conduction of static branch solid state device with the current across the mechanical circuit breaker initially and commutates to the static branch solid- state device. The solid-state device is turned off for fault current interruption at the time when the mechanical switch is fully opened. The fault current is then transferred to the absorber or varistor with high resistance to dissipate the energy. A sketch as shown in Fig 2-5 illustrates the basic hybrid DC circuit breaker structure which is the same as the solid-state circuit breaker but an additional mechanical switch.

Fig 2-5. The conceptual structure for hybrid circuit breaker

[23] proposed the utilization of a damped resistor as the parallel dissipation circuit that diverted the fault current from a solid-state device for voltage suppression. [22, 24] introduces a hybrid circuit breaker design that utilizes the IGCT as the static solid-state device branch. The IGCT in the chain connection can sustain the high breaking voltage, and the parallel connection of IGCT has a safe interruption of high current. A diode in series to IGCT and the snubber diversion circuit can guarantee the turn-on reliability of the parallels IGCT. [25] presents the hybrid circuit breaker turn off characteristic with the principle of zero voltage and zero current switching to divert the fault current from the mechanical switch to the static switch branch and varistor. An IGBT with a snubber resistor, a Zener diode at the gate for voltage protection, and a MOSFET device in a series arrangement can be used as blocking the fault current flown was proposed in [26]. The modeling and the control logic of hybrid circuit breaker were presented in [27] and can be used as a reference to design the desired current rating and the tripping time.

In overall, the hybrid circuit breaker has relatively slow speed fault clearing. The commutation in between the mechanical switch and static branch prolongs the breaking time. Typically, the tripping process for hybrid circuit breaker requires at least 1milisecond for the complete interruption of fault current. The long breaking time can cause a high fault current surpasses into the DC system.

TABLE 2-III: Summary of Different Type Hybrid DC Circuit Breaker

Hybrid circuit breaker	Parallel Dumped resistor[23]	IGCT chain connection static branch[22, 24]	Zero voltage and zero switching breaking[25]
Circuit diagram
function	<ul style="list-style-type: none"> • Dumped resistor as the varistor to divert the fault current from solid state branch • Reduction of interruption time compare to the mechanical circuit breaker 	<ul style="list-style-type: none"> • Diverted the fault current to the static breaker for fault current interruption • Withstand high transient voltage 	<ul style="list-style-type: none"> • Before being interrupted under forced commutation, the commutation of the static branch to the capacitor and inductor branch form an oscillation and bring the current of a mechanical switch and static branch to zero • Allow high current commutation
disadvantage	<ul style="list-style-type: none"> • 20ms interruption for 400A 	<ul style="list-style-type: none"> • 50ms to 1s interruption time for 1kA to 6kA fault current 	<ul style="list-style-type: none"> • Does not state the interruption time but more than 2ms

2.1.4 Solid-state DC circuit breaker

The integration of solid-state devices such as GTO, IGCT, IGBT with resistor, inductor, and capacitor components stimulates the development of the solid-state circuit breaker. The solid-state circuit breaker has the benefit of no modification of power switches is necessary for a power converter and is relatively breaking faster than a fuse and mechanical protection device. Fig 2-6 shows the common solid-state circuit breaker structure. A detection circuit with the driver and control circuit prompts the solid-state device to turn off at the fault event.

Fig 2-6.The conceptual structure of solid-state circuit breaker

The IGBT solid state circuit breaker can achieve fast speed interruption and withstand a high short circuit current[31]. The IGBT device has the additional advantage of low driving power to the gate, and it is commercially available. In the literature review, the transient voltage when the switch opening and the transient current

triggered from the fault can damage the solid-state device easily. [28] realizes the solid-state circuit breaker with a high blocking voltage capability by connecting multiple series IGBT devices and commutating the fault current to the parallel snubber circuits. [29] upgrades the circuit breaker configuration by adding the freewheeling diode connecting across the output terminal to clear the fault current. This freewheeling diode has the advantage of reducing the surge voltage. The freewheeling diode will turn on at the transient voltage state and bypass fault current when the charging of snubber capacitor is full. The solid-state circuit breaker can increase the tripping speed by a pre-charged capacitor in a passive network to force commute off the main solid state switching device during fault operation[30].

TABLE 2-IV: Summary of different type IGBT solid-state DC circuit breaker

Solid-state circuit breaker	Multiple Series IGBT[28]	Freewheeling diode[29]	Passive Pre-charge capacitor[30]
Circuit diagram
function	<ul style="list-style-type: none"> commutating the fault current to the parallel snubber circuits high blocking voltage capability 	<ul style="list-style-type: none"> turn on at the transient voltage state and bypassing fault current when the charging of snubber capacitor is full suppress the surge voltage the reduction of the absorbed energy in the varistor 	<ul style="list-style-type: none"> pre-charged capacitor force commutates off the main circuit breaker increase the tripping speed
disadvantage	<ul style="list-style-type: none"> High conduction loss 	<ul style="list-style-type: none"> High conduction loss 	<ul style="list-style-type: none"> Require a pre-charging to the capacitor for the tripping operation High conduction loss

An introduction of SiC static induction transistor(SIT) device as shown in [67] can reduce the overvoltage and transient oscillation. The SiC-SIT also has the benefit of extremely low on-state resistance. [68] shows an introduction of a SiC junction gate field effect transistor(JFET) device. The JFET device has a normally on capability and a very low resistance at normal on state. A voltage sensor circuit senses the drain-source

voltage and draws power from the fault condition to turn off the JFET device. The protection signal is driven using a fast-starting isolated dc-dc converter[69]. However, the proposed JFET circuit breaker has a high number of component counts which can lower the reliability of the circuit breaker.

For switching device technology, the SCR/thyristor device has lower conduction loss than IGBT device has higher due to half the on-state voltage. [70] presents an introduction of gate turn-off thyristor(GTO) device as the solid-state circuit breaker. The GTO has a controllable turn on and off capability. It has the benefit of high voltage blocking capability, a low on-state voltage, and a low turn off power loss. However, a slow switching speeds capability for GTO can cause a rise of high current magnitude for switching off in the fault condition. The integrated gate commutated thyristor(IGCT) is another type of gate turn off devices evolve from the thyristor[71]. The behavior of ICGT with a low conduction loss, high voltage rating, and high current rating are the advantages of IGCT can be used as a circuit breaker and presented in [72]. The switching speed of IGCT is considerably slower than IGBT. As a comparison, the IGBT device is appropriate for a downstream low current rated circuit breaker which requires a high-speed fault current interruption, and the IGCT device is a good choice for medium range rated current such as transmission line[32].

TABLE 2-V: Summary of different type SCR based solid-state circuit breaker

Thyristor based Solid-state circuit breaker	GTO circuit breaker[70]	IGCT circuit breaker [71, 72]
Circuit diagram
function	<ul style="list-style-type: none"> • High voltage blocking capability • Low on state voltage • Low turn off loss 	<ul style="list-style-type: none"> • High voltage rating • High current rating • Low conduction loss
disadvantage	<ul style="list-style-type: none"> • Slow switching speed 	<ul style="list-style-type: none"> • Slower than IGBT

In overall, the primary disadvantage of IGBT based solid state circuit breaker is a high-power loss over the semiconductor device in normal operation. The SCR based solid state circuit breaker using GTO and ICGT device can be taken as another trend of the solid-state circuit breaker to lower the conduction loss. The tradeoff for SCR based circuit breaker is a lower turn off speed compare to IGBT based circuit breaker.

2.1.5 Impedance-source DC circuit breaker

Most of the hybrid and solid-state circuit breaker require an additional current sensor to detect a fault which would prolong the fault tolerant time and increase the cost. The introduction of impedance-source network circuit breakers is treated as another trend of solid state circuit breaker. The impedance-source circuit breakers are reconfigured from the impedance source inverter with the introduction of additional zero states for further boost or buck the output by shorting the switches of the similar leg. The impedance-source based circuit breaker can be considered as a type of solid-state circuit breaker with the utilization of resonant current that produced at fault event to trip the circuit breaker at the zero-crossing current. The SCR device is chosen as the solid-state device due to low conduction loss and the natural cut off at zero-crossing. The impedance-source network circuit breaker has the additional benefit of no additional sensor required for the fault detection. Fig 2-8. shows the structure of the impedance-source based DC circuit breaker.

Fig 2-7.The conceptual structure of impedance source circuit breaker

The first impedance-source circuit breaker introduced in [33] is the crossed Z-source circuit breaker. The arrangement of capacitors pair is in a cross in between positive and negative rail. The inductors are placed at forward and return path of crossed Z-source circuit breaker. The drawback of crossed Z-source circuit breaker is no common ground for this topology due to no common connection at the negative rail between the input and output terminal.

A parallel Z-source circuit breaker is a modification topology of the crossed Z-source circuit breaker[34]. The inductor and capacitor circuit are placed only in the forward path. The placement of the capacitor is in parallel to the inductor. [35] proposed an evolvement of the parallel Z-source circuit breaker to achieve the series Z-source circuit breaker. The series Z-source circuit breaker rearrange the source capacitor by connecting it across forward and return path. The parallel and series Z-source circuit breakers have an inductor that is placed on the source side. This inductor

placement could reflect a significant current remain at the source after fault clearance. The current across source inductor cannot vanish immediately. Hence, the reflected fault current appeared at the source after fault tripping taken place.

TABLE 2-VI: Summary of Z-source circuit breaker

Impedance source circuit breaker	Crossed Z-source[33]	Parallel Z-source[34]	Series Z-source[35]
Circuit diagram			
function	<ul style="list-style-type: none"> • Fault current source from the Z-source capacitor and revert the current, SCR cut off at zero current crossing point • No reflected source current 	<ul style="list-style-type: none"> • Fault current supplied from the Z-source capacitor and revert the source current, SCR cut off at zero current crossing point • a common ground connection 	<ul style="list-style-type: none"> • Fault Current source from the Z-source capacitor and revert the source current SCR cut off at zero current crossing point • A common ground connection • half the reflected source current compared to the parallel-connected topology
disadvantage	<ul style="list-style-type: none"> • no common ground 	<ul style="list-style-type: none"> • Reflected fault current at the source 	<ul style="list-style-type: none"> • Reflected fault current at the source

[36] introduced a transformer-based circuit breaker termed as the coupled-inductor circuit breaker. This topology preserves a common ground connection and zero-reflected current. However, the coupled-inductor circuit breaker has a notch filter ability but not a low pass filter. The chosen component parameter can cause a large surge fault current. [37] proposed another transformer-based circuit breaker termed as a T-source circuit breaker. The T-source circuit breaker can cope with common ground, zero reflected source current, and it has a resonator behavior. The T-source circuit breaker has a benefit of reducing an inductor core and utilize only a single capacitor. Of all the listed advantages of the T-source circuit breaker, the chosen component sizing of the T-source circuit breaker is oversized in the laboratory test. The proposed components in the simulation have a large fault surge current to the nominal current ratio.

TABLE 2-VII: Summary of the transformer-based impedance source circuit breaker

Transformer Impedance source circuit breaker	Coupled Inductor[36]	T-source [37]
Circuit diagram
function	<ul style="list-style-type: none"> • The Fault current source from the capacitor through the secondary winding, the current reflected primary winding push the SCR current and cut off at zero current crossing point • Common ground connection • No reflected source current 	<ul style="list-style-type: none"> • The Fault current flow from the capacitor through the secondary winding, the current reflected primary winding push the SCR current and cut off at zero current crossing point • Common ground connection • No reflected source current
disadvantage	<ul style="list-style-type: none"> • notch filter behavior 	

2.1.6 Summary of the circuit breaker

The adoption of circuit breaker has two major concerns which are the interruption time and the power loss in normal operation. From the literature review previously, the comparison of interruption time from fastest to slowest is 1) solid-state circuit breaker, 2) hybrid circuit breaker, 3) mechanical circuit breaker. The review in [73] also state the interruption time for a mechanical circuit breaker is up to 60ms, the solid state circuit breaker can achieve interruption time below 1ms, and the hybrid circuit breaker has the interruption time of 2-30ms. The review in [73] also mention the power loss of mechanical and hybrid circuit breaker is 0.01% and 0.1% respectively, and the solid state circuit breaker power loss can reach up to 30%. Among all the solid-state circuit breaker, the thyristor-based circuit breakers such as IGCT and GTO breaker can achieve a low power loss, and this is due to thyristor device has a low conduction loss compare to IGBT device. Hence, the introduction of impedance source based circuit breaker which utilizes the thyristor device as the tripping device is the tradeoff for the power loss of solid state circuit breaker.

For the impedance source based circuit breaker, there are two categories can be separated as transformer based and transformerless impedance source circuit breaker. The transformer-based impedance source circuit breaker has the advantage of less one capacitor and one inductor core which in turn less component count has better system reliability. The T-source circuit breaker is a resonator and has a low pass filter behavior at high-frequency whereas coupled inductor circuit breaker is a notch

filter. Hence, the T-source circuit breaker is chosen as the fault isolation device in the DC system.

The transformer inductance and the capacitance selection of the T-source circuit breaker prototype design in [37] are 232mH and 940uF respectively. These components values are oversized and relatively large for 15V input voltage. The simulation work shows the output fault surge current is 15000A and the nominal current is 1000A give the result of the metric ratio is 15. For the practical work, the output surge current is 3A, and the nominal current is 0.44A which the metric ratio is 6.8. The low output surge current to nominal current ratio is due to the high-value transformer magnetizing inductance 232mH. Hence, an optimal design of the T-source circuit breaker is based on the tripping operation in the fault event, and a low output surge fault current after tripping.

2.2 Fault identification

[74] presents a general review of fault location identification in the distribution network. The fault location identification methods are impedance method, the traveling wave method, signal injection method, the zero-sequence component-based method, and the compositive location method. The fault identification technique for the conventional transmission network is summarized as shown in Fig 2-8. However, only the traveling wave method and the injection-based method are the suitable fault location identification approaches that can be used in the DC system. The reason is due to the absence of the zero-sequence component and the impedance information for the fast interruption in the DC system. The DC system network requires an offline fault identification method to justify the fault location.

Fig 2-8. Fault identification technique in the conventional transmission line

2.2.1 Travelling wave method

The traveling wave is a propagation wave that generated from fault and travel along the transmission line. The traveling time and the known velocity of a respective medium can estimate the fault location. The traveling wave method utilizes the propagation wave along the transmission line and the surge arrival time to determine the fault location. Fig 2-9 shows the traveling wave concepts with the wave propagates to the detectors of two end during the fault occurrence. This method required a known traveling wave velocity and the length of transmission line between two detectors. With the known distance between two detectors, the difference traveling time to both end detectors, and the wave traveling speed, fault distance can be determined.

Fig 2-9. The traveling wave propagates to the two end detectors at the fault occurrence

[44] proposed a technique that can identify a fault location in a multiterminal DC system. This technique requires only a single detector with a common joint over the transmission line such as ring network. The surge arrival time for the two consecutive signals at the detector is used for computing the shortest path transmission line traveling time. Besides, the fault surge arrival time of two different pair detectors and the time takes to travel from a specific location to the paired detector can be used as the fault segment identification. A single end fault identification method using the natural frequency of traveling wave, velocity, and the reflection coefficient to identify the fault location[47]. The multiple signal classification transforms the signal into spectrum analysis, and it is used as the natural frequency extraction. Another single end traveling wave that using the continuous wavelet transform of traveling wave to obtain the signal energy over different frequency [43]. The frequency of the highest amplitude signal energy in the spectrogram is using as the traveling wave speed frequency. The continuous wavelet transform then also provides the energy decomposition of the signal in the integrated frequency-time domain. The frequency difference of two consecutive signals performs a frequency compensation. Finally, the fault location can be calculated based on the traveling wave speed frequency equation.

[49] utilizes the surge arrival time difference of the fault traveling wave between a pair surge detector located at two different location to identify the fault

location for a mixed transmission media. The time difference and the proposed fault segment identification flow can determine the fault segment and fault location simultaneously. The traveling wave propagation velocity for each segment can be calculated at the pre-fault condition using the time difference method. This method requires an accurate time synchronize measurement to obtain high accuracy fault location identification. [50] using the two-end traveling wave method associated with the continuous wavelet transform to extract the time indices of traveling wave. The signal with wavelet transform provides a precise time of wave arrival to the detector.

In summary, the single end and two end traveling wave methods in the literature have the benefit of less surge at the detector. However, the accuracy of fault distance measurement is dependent on the data acquisition rate and the traveling wave propagation velocity.

Traveling wave method	Single end technique[43, 44, 47]	Two end techniques [49-51]
Circuit diagram
function	<ul style="list-style-type: none"> using two consecutive reflected waves to determine the fault location identification 	<ul style="list-style-type: none"> captures the waves at both ends of the feeder
disadvantage	<ul style="list-style-type: none"> High dependencies of sampling time uncertainties of traveling wave propagation velocity determine the accuracy of fault location identification 	<ul style="list-style-type: none"> High dependencies of sampling time uncertainties of traveling wave propagation velocity determine the accuracy of fault location identification sampling synchronization

TABLE 2-VIII: Summary of traveling wave fault location identification

2.2.2 Signal Injection based method

The principle of the signal injection method is based on an external signal injection on the common bus and observe the current or voltage behavior to determine the fault branch and identify the corresponding fault location. The signal injection is usually using a compensation coil or a transformer connected to the common bus for signal injection. Fig 2-10 shows the signal injection method schematic as an illustration for fault branch and fault location identification.

Fig 2-10. The signal injection method schematic

[53] proposed a signal injection method with a sine current injection over a transformer connected to the common bus. The signal injection is triggered when there is a dropping in-phase voltage. Then a current signal injection and voltage measurement at each branch line. The fault branch line is identified with a result of larger current injection amplitude than the non-fault branch. Then, the determination of fault distance is based on the resistive characteristic of transition resistance whereby making the imaginary part of the resistive characteristic equation equal to zero.

[52] shows an injection method using multiple measurement points for the fault location identification. By using several sensors located cascaded from point to point, the locating signal sensor will be activated when the injected signal pass through. Then the fault point is locating in between the activated and non-activated locating signal sensor.

[54] proposed a method using the inter-harmonic frequency signal generator and the ancillary suppression coil for signal injection. The high frequency of the injected signal voltage and current are used as values the failure loop impedance. Then, equating the lumped wiring impedance parameters and the failure loop impedance to identify the fault distance. Similarly, a method that based on the wiring reactance parameter to calculate the fault distance [75]. The fault line impedance is obtained using the changing of voltage over the changing of current at the faulted phase.

In overall, the signal injection method has the disadvantages of only allow the radial network fault location identification, and the shunt capacitance current effect in the transmission can limit the acquisition of fault distance.

TABLE 2-IX: Summary of signal injection method fault location identification

Impedance-based circuit breaker	Transformer-based [52, 53]	Compensation coil [54]
Circuit diagram
function	<ul style="list-style-type: none"> • A sine current is injected over a transformer that connected to the common bus • The fault branch line is identified with a result of larger current injection amplitude than the non-fault branch • the determination of fault distance is based on the resistive characteristic of transition resistance 	<ul style="list-style-type: none"> • using the inter-harmonic frequency signal generator for the injection • equating the lumped wiring impedance parameters and the failure loop impedance to identify the fault distance
disadvantage	<ul style="list-style-type: none"> • only allow the radial network fault location identification 	<ul style="list-style-type: none"> • only allow the radial network fault location identification

2.2.3 Offline Injection method

The offline method has a great advantage of localized fault after source-fault isolation. The offline method can priory cut-off the source before taking the action of measurement for the fault location. This action can reduce the harmfulness of DC system with the continuous feeding of current toward the fault point just for the measurement on fault location.

The time-frequency Domain Reflectometry method is an offline method using the Euclidean distance measurement as the fault location[56]. The fault distance is measured by taking the time differences of time-frequency distribution of injected reference signal to the cable and the reflected signal. However, the propagation wave signal attenuated when traveling along cable can lower the reliability of the fault location measurement.

Another offline injection method using the probe power unit as the device for fault location identification [13]. The probe power unit consists of a pre-charged capacitor in series with an inductor. The activation of the switches forms an RLC circuit and the capacitor energy will discharge at the same time. The discharging of the injection current decaying with time and the decay factor contains the fault information which allows identifying fault location. The probe power unit has the benefits of high

accuracy with low data acquire needed for fault location identification. The identification of fault location is based on the injected current damping frequency, the transmission line parameter, and probe power unit component parameter. The natural frequency is assumed to equal the damping frequency.

In the extension, [58] shows the utilization of the probe power unit to find the fault location identification with the least square error technique can find out the damping coefficient and compensate the damping frequency to find out the natural frequency. The acquisition of the damping coefficient can help reduce the error of fault distance measurement. However, the least square error technique requires high numbers of data reading with using pseudo-inverse matrix solution. This technique has the disadvantages of slow computation time and low accuracy due to overdetermine reading.

TABLE 2-X: Summary of offline injection method fault location identification

Offline injection method	Time-frequency Domain Reflectory[56]	Probe Power Unit [13, 58]
Circuit diagram
function	<ul style="list-style-type: none"> The fault location is determined by taking the time differences of time-frequency distribution of injected reference signal to the cable and the reflected signal 	<ul style="list-style-type: none"> The damping frequency of the injected current, the transmission line parameter, and probe power unit component can determine the fault location
disadvantage	<ul style="list-style-type: none"> The injected signal can be distorted when traveling along the transmission, which can lower the reliability of the fault location 	<ul style="list-style-type: none"> Low accuracy at the close in fault and high impedance fault

2.2.4 Summary of fault identification technique

There are three major fault identifications in the literature review termed as traveling wave method, signal injection method, and offline injection method. Among all methods shown, the offline injection method is considered as the most fitted solution for the fault identification of DC system. The fast speed interruption to reduce the harmfulness of DC system fault continuously drawing high magnitude current. The offline injection method has the advantage of determining the fault location even the source current has been priory cut-off and can be triggered as many time as desired.

For the offline injection method, the probe power unit is chosen as the fault location identification technique over the time-frequency domain reflectory technique. The injected current from probe power unit has no distorted effect, and the information can be read from the current measurement instantly without waiting for the reflected signal in comparison with the time-frequency domain reflectory technique.

However, the probe power unit has a drawback of accurate reading at the close in fault and high fault resistance. The derivation of the damping coefficient using least square error technique can increase some accuracy of fault location identification but require high numbers of data reading. In addition, the chosen LC pair for probe power unit can only locate the fault with the maximum fault resistance up to 9.866ohm. The injected probe current will turn into overdamped current when the fault resistance is higher. The overdamped current does not contain the fault information due to the absence of second peak current.

2.3 Fault Recovery

For the AC system, the traditional method for voltage recovery is the injection of reactive power using the STATCOM device[76]. A closed loop extinction angle control function to the power converter is another method that can achieve voltage recovery of DC system when there is a fault in the AC system[77]. However, both methods can only compensate the voltage sag of the DC system but not take into account the permanent fault with totally turn off and reenergize the DC system.

[18] proposed a 'handshaking method' whereby the DC switch is opened when the current of cable ends flow into the cable. The recovery stage begins with voltage control mode for all the power converter, and the switch will reclose when the voltage of the cable is charging up to 90% of the rated voltage. Then, restart all the voltage source converter and change back to original controlled mode.

[57] using a delayed-auto reconfiguration scheme as the fault management scheme to recover the faulty system into a new form of DC system. All the power converter of the HVDC system are the modular multilevel converter. There are at least one of the power converter is chosen as the voltage control mode to balance the power of the DC system. The other power converters in the HVDC system are power control mode to export and import power from the DC system. The DARC scheme shows a

manner of resume the voltage control mode power converter followed by another power converter with power control mode can achieve an efficient system.

[78] shows the modular multilevel converter can drive the current down to zero and allow the mechanical connector and AC circuit breaker to isolate the fault cable segment. The reconnection of the facilities back to the DC system started with the voltage-controlled terminal then followed by the renewable generation terminal can achieve stable recovery system.

[20] presents three investigations system recovery for HVDC system using the modular multilevel converter as the only power converter. The three investigations are 1) the time start for the recovery control, 2) the sequence between deblocking the modular multilevel converter and the reclosing of AC circuit breaker, 3) the reconnection sequence of each HVDC terminal. The begin time for system recovery is when all the current in the DC system have completely decayed to zero. The reconfiguration step for the wind generated energy system deblock the power converter before the reclosing of the AC circuit breaker. For other power converter terminal, the AC circuit breaker is reclosed before the deblocking of the power converter. The sequence of reconnecting the terminal back to the DC system is shown in Fig 2-11.

Fig 2-11. Fault Reconnection Sequence for the modular multilevel converter in the multiterminal DC system

In the extension, the low voltage microgrid with various power converter is using for different facilities. The facilities include grid interfacing system, storage system, and distributed generation system. The DC circuit breaker reacts much faster than the AC circuit breaker. Hence, the speed consideration is the reason for choosing the DC circuit breaker as the fault current interruption device. The adoption of system reconfiguration proposed in [20, 57] using the AC circuit breaker can have different result compare to the DC circuit breaker due to the placing of DC circuit breaker is different. The DC circuit breaker that using the same reconfiguration step as AC circuit breaker can result with high transient DC voltage at the initialization stage. Hence, a knowledge of system reconfiguration is required for a DC distribution system with different facilities require to achieve a stable system recovery. The reconfiguration step

of reclose the DC circuit breaker and reactivate the power converter for different facilities does not show in the literature. Additionally, there is no comparison of simultaneous connection and sequential connection for all the facilities to the DC network. The sequence of reconnecting each facility back to the DC system is also an important factor to achieve a stable voltage for the DC network.

Chapter 3. A Low Output Surge Current and Optimal Design for T-source DC Circuit Breaker

3.1 T-source circuit breaker overview

The T-source circuit breaker circuit arrangement is shown as in Fig 3-1. This topology is termed as T-source circuit breaker is due to the arrangement of element and circuit is similar to a T-network circuit and it is based on the T-source inverter term introduced in [79-81]. The T-source circuit breaker starts operating when the output terminal has shorted. The ramp up discharging current from the capacitor passes across secondary winding transformer which in turn lower down the transformer primary winding current. The reason is due to the transformer primary winding has a polarity opposes to the secondary winding. The transformer primary winding current is similar to the SCR(Silicon Controlled Rectifier) current. Fig 3-1 shows the current flown operation of the T-source circuit breaker during a fault event. The rising of secondary winding current prompt a falling current at the primary current. When the SCR or primary current reaches zero, the SCR device will turn off. The input and output terminal is then isolated when the SCR device stop conducting.

Fig 3-1. T-source Circuit Breaker and the current flow at a fault state

In this section, the voltage transfer function of the T-source circuit breaker and the source reflected current is presented. The transfer function section illustrates the T-source circuit breaker behavior and Q-factor. The zero-reflected source current for the T-source circuit breaker is discussed and compared against other circuit breaker topologies.

3.1.1 Transfer Function

The overview of the T-source circuit breaker behavior begin with the components parameter is prior chosen as shown in TABLE 3-I. The transient event of the T-source circuit breaker circuit as shown in Fig 3-1 can be redrawn as Fig 3-2 using the transformer equivalent model with the mutual inductance of the transformer is taken into consideration. The voltage transfer function at the transient event is then

derived as shown in (3.1). (3.2) shows a second-order transfer function when replacing the Z_{RC} and Z_L with a capacitance and load resistor respectively. The L_1 and L_2 are the transformer self-inductance at the primary and secondary side. The ratio of the transformer primary to secondary self-inductance metric is shown in (3.3). M is the mutual inductance of the transformer as shown in (3.4) and k is the coefficient of coupling with 1 if it is assumed perfectly coupled.

TABLE 3-1: Component parameter for T-source circuit breaker

Element	Description	Value
C	Capacitor	100uF
L_1	Transformer Primary Leakage Inductance	50uH
L_2	Transformer Secondary Leakage Inductance	50uH
L_m	Transformer Magnetizing inductance	1mH
N_1	Transformer Primary Winding Turns	80
N_2	Transformer Secondary Winding Turns	80
V_0	Source Voltage	100
R_L	Load Resistance	50

Fig 3-2. The T-source circuit breaker at pre-tripping state equivalent circuit

$$\frac{V_o}{V_s} = \frac{-sM + Z_{RC}}{sL_1 + s(L_1 + L_2 + 2M) \frac{Z_{RC}}{Z_L} + Z_{RC}} \quad (3.1)$$

$$\frac{V_o}{V_s} = \frac{-s^2M + \frac{1}{C}}{s^2L_1 + s(L_1 + L_2 + 2M) \frac{1}{RC} + \frac{1}{C}} \quad (3.2)$$

$$L_2 = L_1 \left(\frac{N_2}{N_1} \right)^2 \quad (3.3)$$

$$M = k\sqrt{L_1 L_2} \quad (3.4)$$

A Bode plot of (3.2) is shown in Fig 3-3 using the parameters as given in Table 3-1. The plot shows a unity function at low frequency and resonance frequency at 3.2kHz. At high frequency, it attenuates the signal, and the output voltage is opposed to the input voltage. The bode plot concludes that the T-source circuit breaker has a resonator and attenuation behavior.

Fig 3-3. The Bode plot of T-source circuit breaker voltage transfer function

The T-source circuit breaker transfer function that shown in (3.2) and resonator behavior can represent the pre-tripping state operation which is the transient state before the SCR device tripped. The T-source circuit breaker being a second order resonator system, the T-source circuit breaker Q-factor can be obtained as (3.5).

$$Q = R \frac{\sqrt{L_1 C}}{(L_1 + L_2 + 2M)} \quad (3.5)$$

3.1.2 Fault Clearing Waveform Overview

A simulation is conducted for the comparison of the T-source circuit breaker to all other Z-source circuit breakers. For a fair comparison, the simulation components parameter for all topologies is based on TABLE 3-I, and the MATLAB Simulink is the software for the simulation. Fig 3-4 shows a full set of faults clearing simulation waveforms with SCR current, SCR voltage, capacitor current, and output currents with the occurrence of a fault at $t=1s$. The waveform for all circuit breaker topologies is identical at the steady state which is the state before the fault and after fault clearance. The identical waveforms can conclude the T-source circuit breaker has a similar operation effect compare to previous introduced Z-source circuit breaker topologies at the short circuit fault condition. In comparison, the T-source circuit breaker shows a less ringing voltage waveform than other topologies which has the benefit of less voltage stress on the SCR device at a transient state. The waveform shows a less current ripple at the output, and a less current fluctuation at the capacitor of T-source circuit breaker compare with the crossed, parallel, and series Z-source circuit breaker.

Fig 3-4. Fault clearance waveforms of a) SCR current, b) SCR voltage, c) Capacitor current, d) Output Current

3.1.3 Reflected Source Current

The reflected source current is defined as a ringing current which appears continuously on the source side after fault clearance. Fig. 3-5 shows the reflected source current for different topologies. The parallel and series Z-source circuit breakers have a ringing current at the source after the fault clearance. The series Z-source circuit breaker can reduce reflected source current by half as compared to the parallel Z-source circuit breaker. The crossed Z-source and the T-source circuit breakers present the source current fall to zero immediately after fault clearance. The immediate falling current result indicates the T-source circuit breaker has a zero-reflected source current behavior after tripping. The result of reflected current falls zero immediately is due to the fault current is fully supplied from the capacitor in the circuit breaker but not drawn from the source.

Fig 3-5. Reflected source current at fault state

3.2 Circuit Breaker Operation and analysis

To ensure the reliable tripping operation of T-source circuit breaker the circuit breaker capacitor value and the transformer inductance are important parameters to be considered. The following analysis assumes the existence of a load capacitor at the circuit breaker output terminal. This can be referred to as the DC system capacitance or downstream inverter input capacitor.

The T-source circuit breaker operation can be divided into normal state and fault transient state. The fault transient state operation comprises of pre-tripping state and post-tripping state. The pre-tripping state is the state where before the SCR current has fallen crossing zero. The post-tripping state is the state where the input and output terminal has completely isolated. The pre-tripping state affects the tripping operation while the post tripping affects the output surge current. Last, a design procedure for a T-source circuit breaker is shown.

3.2.1 Tripping Operation Analysis

A short circuit fault creates a large current drawn from the source when the positive DC rail is connected directly to the negative DC rail or over a small resistance. Consequently, a huge current will be drawn from the source. During the start of a short circuit fault, the T-source circuit breaker discharge the capacitor stored energy towards the fault terminal and the discharging current is ramped up through the transformer secondary winding, causing the current across the SCR to fall towards zero due to the opposite polarity between the primary and secondary windings of the transformer. Fig 3-1 illustrates the current flown of the T-source circuit breaker at the fault event. Fig 3-6 presents the equivalent T-source circuit breaker modeling for transient analysis of the pre-tripping state of short circuit. The model uses the transformer mutual inductance T equivalent circuit of with the consideration the load capacitance at the output terminal.

Fig 3-6. T-Source Circuit Breaker Modelling of Pre-Tripping State

The current across circuit breaker capacitance and load capacitance are expressed in (3.6) and (3.7) respectively. The voltage across each junction of transformer inductance are shown as (3.8), (3.9), and (3.10).

$$-C_B \frac{dv_{CB}}{dt} = i_{L2} - i_{L1} \quad (3.6)$$

$$-C_L \frac{dv_{CL}}{dt} = \frac{v_{CL}}{R_f} - i_{L2} \quad (3.7)$$

$$(L_1 + M) \frac{di_{L1}}{dt} = v_s - v_x \quad (3.8)$$

$$(L_2 + M) \frac{di_{L2}}{dt} = v_x - v_{CL} \quad (3.9)$$

$$-M \frac{di_M}{dt} = v_{CB} - v_x \quad (3.10)$$

Equations (3.6) to (3.10) can be rewritten as continuous time-invariant state space equation as shown in (3.11). Applying Laplace transform, (3.11) can be expressed as (3.12) with the space variables are circuit breaker capacitor voltage, load capacitor voltage, primary winding inductance current, secondary winding inductance current. The initial circuit breaker capacitor voltage and the load capacitor are defined as V_0 and the initial current across transformer primary and secondary winding are termed as I_0 . The primary winding inductance current is derived as (3.13). Using Matlab as a tool, the primary winding inductance current in the time domain can be easily obtained by using the inverse Laplace transform function.

$$\dot{x}(t) = Ax(t) + Bu(t) \quad (3.11)$$

$$X(s) = [sI - A]^{-1}[BU(s) + x(0)] \quad (3.12)$$

$$A = \begin{bmatrix} 0 & 0 & \frac{1}{C_B} & -\frac{1}{C_B} & 0 \\ 0 & -\frac{1}{C_L R_f} & 0 & \frac{1}{C_L} & 0 \\ \frac{L_2 + M}{M^2 - L_1 L_2} & -\frac{M}{M^2 - L_1 L_2} & 0 & 0 & 0 \\ -\frac{L_1 + M}{M^2 - L_1 L_2} & \frac{M(L_1 + M)}{(L_2 + M)(M^2 - L_1 L_2)} - \frac{1}{L_2 + M} & 0 & 0 & 0 \\ -\frac{(L_2 + M)(L_1 + M)}{M(M^2 - L_1 L_2)} - \frac{1}{M} & \frac{L_1 + M}{M^2 - L_1 L_2} & 0 & 0 & 0 \end{bmatrix};$$

$$B = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L_1 + M} - \frac{M(L_2 + M)}{(L_1 + M)(M^2 - L_1 L_2)} \\ \frac{M}{M^2 - L_1 L_2} \\ \frac{L_1 + M}{M^2 - L_1 L_2} \end{bmatrix}, x(t) = \begin{bmatrix} v_{CB} \\ v_{CL} \\ i_{L1} \\ i_{L2} \\ i_M \end{bmatrix}, x(0) = \begin{bmatrix} V_0 \\ V_0 \\ I_0 \\ I_0 \\ 0 \end{bmatrix}, u(t) = v_s = V_0$$

$$\begin{aligned}
& I_{L1}(s) \\
& \left(I_0 + \frac{V_0}{s} \left(\frac{1}{L_1 M} - \frac{M(L_2 + M)}{(M^2 - L_1 L_2)(L_1 + M)} \right) \right) \times \\
& \left((L_1 + M) + [C_L R_f (L_1 + M) + C_B L_1 R_f] s - C_B (M^2 - L_1 L_2) s^2 - C_L C_B R_f (M^2 - L_1 L_2) s^3 \right) \\
& + \left(I_0 + \frac{V_0}{s} \left(\frac{M}{(M^2 - L_1 L_2)} \right) \right) (L_2 + M + (C_L R_f (L_2 + M) + C_B M R_f) s) \\
& = \frac{- (C_B V_0 (R_f + (L_2 + M) s + C_L R_f (L_2 + M) s^2)) + (C_L R_f V_0 (C_B M s^2 + 1))}{R_f + (L_1 + L_2 + 2M) s + [C_L R_f (L_1 + L_2 + 2M) + C_B L_1 R_f] s^2 - C_B (M^2 - L_1 L_2) s^3 - C_L C_B R_f (M^2 - L_1 L_2) s^4}
\end{aligned} \quad (3.13)$$

The current across SCR is also represented by the primary winding inductance current. The tripping operation of the T-source circuit breaker takes place when the SCR current crosses the zero crossing. The SCR current angular frequency is expressed in (3.14). and the time of SCR minimum current is approximated as (3.15).

$$w_0 \approx \frac{1}{\sqrt{(L_2 - M)C_B}} \quad (3.14)$$

$$t_p \approx \frac{\pi}{w_0} \quad (3.15)$$

A design flowchart is shown in Fig. 3-7 to determine the minimum capacitor value designed for the T-source circuit breaker. The initial iteration for the load capacitance is 1mF, and circuit breaker capacitance is 10uF, respectively. Then, the parameters of angular frequency, peak time, and SCR current are determined. The ending criterion is such that the minimal SCR current must be less than zero to ensure the tripping operation of SCR device. The circuit breaker capacitance is increased with 10uF until the ending criterion is obtained.

Fig 3-7. The design flowchart of circuit breaker capacitance

The component parameters of the T-source circuit breaker is priory set to the values as shown in TABLE 3-I, Fig 3-8 shows the plot of different load capacitance value with the result of minimum circuit breaker capacitance. The result shows an exponential increase of the circuit breaker capacitance value with the increase of load capacitance. Using the same design flowchart and changing the transformer inductance to 0.1mH, the obtained result has a similar result to the transformer induction of 1mH. The fault resistance is changing to 5ohm using the same flowchart, and the transformer inductance is retained as 1mH. The result shows when the fault resistance is increased to 5ohm, it requires higher circuit breaker capacitance for the tripping operation at the fault state.

Fig 3-8. The flowchart result of the circuit breaker capacitance versus load capacitance

A simulation is conducted to verify the validity of process flow to compute circuit breaker capacitance. The selection of the T-source circuit breaker capacitance is carried out by assuming a 2mF load capacitance and 1ohm fault resistance at the output terminal. The MATLAB Simulink is the software for the simulation. In Fig 3-8, the minimum circuit breaker capacitance required is 90uF for the 2mF load capacitance. Fig 3-9 shows the simulation result of SCR current with a circuit breaker capacitance value of 80uF and 90uF for the 2mF load capacitance. It can be clearly shown that 90uF capacitance trips the circuit breaker but not 80uF. This means the minimum requirement for the circuit breaker capacitance is 90uF to ensure the tripping operation to occurred at 2mF load capacitance. This further shows that the design flowchart in Fig 3-7 is valid and able to determine the minimum circuit breaker capacitance for tripping operation to occur.

Fig 3-9. Simulation of the tripping operation for various circuit breaker capacitance over 2mF load capacitance

The next parameter to be examined is the transformer inductance. The circuit breaker capacitance is chosen as 90uF with assuming 2mF load capacitance and 1ohm fault resistance, the transformer inductance of value 0.1mH and 1mH are tested for the tripping operation. Fig 3-10 shows the corresponding simulation result of the SCR current with the two transformer inductance values. Fig 3-10 shows no changes to the tripping operation of the circuit breaker with the different values of the transformer inductance. The result verifies the process flow as shown in Fig 3-8 with the same effect for different transformer inductance and no changing of the circuit breaker capacitance has been made.

Fig 3-10. Simulation of the tripping operation for various transformer inductance over 2mF load capacitance and 1ohm fault resistance

A simulation is carried out to determine the tripping current of the circuit breaker for different fault resistance. A 2mF load capacitance and a 90uF circuit breaker capacitance is assumed for the test, and the MATLAB Simulink is the software for the simulation. Fig 3-11 shows the simulation result for various fault resistance with the SCR current. The result shows that a 1ohm and 0.5ohm fault resistance causes the circuit breaker to trip, but a 2ohm fault resistance does not. Fig 3-12 shows another simulation carried out for different fault resistance, from 4 to 6 ohms, and with the

circuit breaker capacitance to be 440 μ F and the load capacitance as 2mF. The result shows a 4ohm and a 5ohm fault resistance can trip the circuit breaker, but 6ohm fault resistance does not trip. The results further validate that the design flowchart in Fig 3-8 is valid. The result shows that for a 1ohm fault resistance or the current rating 100A, the circuit breaker requires 90 μ F capacitance. Correspondingly, a 5ohm fault resistance or 20A current rating circuit breaker requires 440 μ F circuit breaker capacitance.

Fig 3-11. Simulation of the tripping operation for various fault resistance over 2mF load capacitance and 90 μ F circuit breaker capacitance

Fig 3-12. Simulation of the tripping operation for various fault resistance over 2mF load capacitance and 450 μ F circuit breaker

The above simulation results have validated the proposed design flowchart can be used to select circuit breaker capacitance for successful tripping operation to take place at system side fault. The transformer inductance value plays a minimal impact on the tripping operation. For a smaller tripping current rating, the capacitance of the circuit breaker required is larger.

3.2.2 Output Surge Current

The output fault surge current is an oscillation of fault current at the output terminal that happens at the post-tripping state. A higher transformer inductance can reduce the output surge current. However, high transformer inductance can increase

the cost, weight, and bulkiness of the circuit breaker. In determining the inductance value of the transformer, the circuit breaker tripping current rating plays a crucial role.

The maximum amplitude of the output surge current must not higher than the current rating of the T-source circuit breaker which is determined in (3.16) where the fault tolerance resistance value is R_{ft} . This is to prevent damage to the downstream device. A 5ohm fault tolerance resistance and 100v source voltage will have a 20A current rating as the maximum amplitude for the output surge current.

$$I_r = \frac{V_s}{R_{ft}} \quad (3.16)$$

After the isolation of the source and the system, Fig. 3-13 shows the resulting model of the disconnected circuit breaker. Due to isolation, the transformer model is left with only consideration of the secondary winding. The current across the circuit breaker and load capacitor can be re-written as (3.17) and (3.18), respectively. The voltage across the transformer secondary winding inductance is described as (3.19). Similar as (3.11) and (3.12), a third order form transformer secondary winding inductance current is obtained and shown as (3.20) with the circuit breaker capacitor and load capacitor initial voltage are written as V_0 and the transformer inductance initial current is $2I_0$

Fig 3-13. Modeling of the T-source circuit breaker at post-tripping state

$$-C_B \frac{dv_{CB}}{dt} = i_{LB} \quad (3.17)$$

$$-C_L \frac{dv_{CL}}{dt} = \frac{v_{CL}}{R_f} - i_{LB} \quad (3.18)$$

$$L_B \frac{di_{LB}}{dt} = v_{CB} - v_{CL} \quad (3.19)$$

$$I_{LB}(s) = \frac{V_0 C_B + I_0 (L_B C_B C_L R_f s^2 + L_B C_B s)}{L_B C_B C_L R_f s^3 + L_B C_B s^2 + (C_B R_f + C_L R_f) s + 1} \quad (3.20)$$

The secondary winding current angular frequency and the peak time for the output surge current can be obtained as shown in (3.21) and (3.22), respectively. The

substitution of peak time to the inverse Laplace Transform of (3.20) can determine the peak of output surge current. This peak output surge current is a metric to determine the transformer inductance such that the peak value should not be higher than the current rating.

$$w_1 = \frac{1}{\sqrt{L_B C_B}} \quad (3.21)$$

$$t_{p1} \approx \frac{\pi}{w_1} \quad (3.22)$$

To compute the transformer inductance, we must first determine the current rating for the circuit breaker. For a T-source circuit breaker with 5ohm fault tolerance resistance, the current rating is 20A, and this is the desired maximum amplitude of the output surge current. Taking the example of 2mF load capacitance at the output terminal, it would require 440uF circuit breaker capacitance based on Fig 3.8. Based on the parameter described, Fig 3-14 shows the maximum output surge current over various transformer inductance and different fault resistance at the output terminal. For a 5ohm fault resistance triggered at the output terminal, the amplitude of the maximum of output surge current is kept at very small value, and it has a minimal change for different transformer inductance. However, the peak of the output surge fault current increases when a smaller fault resistance is at the output terminal. The computed result shows that the maximum output surge current with 20A falls on 11.4mH transformer inductance for 0.01ohm fault resistance. In another word, the selection of transformer inductance is 11.4mH would give a result of the maximum output surge current not exceeding 20A for a fault resistance with value 0.01ohm and above.

Fig 3-14. Maximum output surge current over transformer inductance for various fault resistance

A simulation is conducted to verify the selected transformer inductance over the maximum of output surge current. The parameter at the output terminal and the T-source circuit breaker component parameter is shown in TABLE 3-II. The current rating of the circuit breaker is 20A. A 0.01ohm to 1ohm fault resistance is later triggered at the output terminal. The simulation result of the output surge current is shown in Fig 3-15. The result shows the maximum output surge current does not exceed the current rating 20A. This simulation result also validates the modeling of the T-source circuit breaker at post-tripping state as shown in Fig 3-13 and the output surge fault current equation as shown in (3.20) that provide the selection of the minimum transformer inductance for the T-source circuit breaker design.

TABLE 3-II: The selected parameter for T-source circuit breaker

Element	Description	Value
CB	Circuit Breaker Capacitor	440uF
CL	Load Capacitance	2mF
L1	Transformer Primary Inductance	11.4mH
L2	Transformer Secondary Inductance	11.4mH
Vin	Source Voltage	100V
RL	Load Resistance	50 Ω
Rf	Fault Resistance	0.01-1 Ω

Fig 3-15. Simulation result of the output surge current with 11.4mH transformer inductance with various fault resistance

3.2.3 T-source Circuit Breaker Design Procedure

In section 3.2.1, the tripping operation is merely depending on the circuit breaker capacitor value to the respective load capacitance and current rating. The simulation result also shows the transformer inductance has no impact on the T-source circuit breaker tripping operation. In section 3.2.2, the transformer inductance is calculated to lower the magnitude of the output surge current to the current rating. In overall, the simulations have quantitatively shown a high accuracy matching to the

derived equation. In another word, we can say the proposed models at the pre-tripping and the post-tripping state can be used as modeling for the T-source circuit breaker operation. Hence, a proposed design step for the T-source circuit breaker is introduced as follows:

1. Determine the circuit breaker current rating, load capacitance at the output terminal, and source voltage.
2. Using the design flowchart as shown in Fig 3-7 to compute the minimum required circuit breaker capacitance to ensure tripping operation always takes place when the current drawn at the load more than the current rating.
3. Reduce the peak of the output fault surge current by increase the transformer inductance until the maximum of the output surge current is less than the current rating. The maximum current is obtained using the inverse Laplace transform of (3.20) at peak time (3.22)

3.3 Experiment Validation

This section shows an experiment that validates the T-source circuit breaker capacitor that has shown in section 3.2.1. A laboratory prototype setup with the output terminal has a 2mF load capacitance, and the desired current rating is set to 20A. Based on the computed flowchart result as shown in Fig 3-8, the chosen circuit breaker capacitor value is 440uF. The other parameters for the experiment are shown in TABLE 3-III.

TABLE 3-III: The Experiment Parameter for T-source Circuit Breaker

Element	Description	Value
CB	Circuit Breaker Capacitor	440uF
CL	Load Capacitance	2mF
L1	Transformer Primary Inductance	1mH
L2	Transformer Secondary Inductance	1mH
Vin	Source Voltage	100V
RL	Load Resistance	50 Ω
Rf	Fault Resistance	1/6.8 Ω

The experiment is tested with two different triggered resistance which is 1ohm and 6.8ohm. The DC power source is chroma, and the current limit of the DC power source is up to 8A. Fig 3-16 and Fig 3-17 show the experimental waveform of triggering 1ohm and 6.8ohm fault resistance respectively. The waveforms show the terminal voltage(yellow), the source current(red), and output current(green). For a 1ohm fault resistance triggered, the output voltage and the source current fall to zero and the output fault surge current rise to a peak 27A. The zero-fallen current indicates the tripping operation of the T-source circuit breaker. The peak result validates the

maximum output fault surge current over the transformer inductance as shown in Fig 3-14. For a 6.8ohm triggered fault resistance, the current is step up from 2A to 8A. The actual load stepping current for 6.8ohm is 14.7A, but the limit current of the DC power source is 8A. In overall, these two-experimental results validate the circuit breaker capacitance over the load capacitance as shown in Fig 3-8. In another word, the experimental result verified the proposed T-source circuit breaker pre-tripping model and post-tripping model, and all the derived mathematical equations.

Fig 3-16. Experimental result of triggering 1ohm fault resistance

Fig 3-17. Experimental result of triggering 6.8ohm fault resistance

3.4 Modified T-source Circuit breaker

Reference [36] proposed a modification circuit for the impedance-source circuit breaker with a resistor is placed in series to the circuit breaker capacitor, and a thyristor is placed in parallel to the capacitor for manual tripping. The modification circuit can protect the internal device and smoothen the charging of circuit breaker capacitor at the initial state. The chosen series resistor of the modified coupled inductor circuit breaker topology is large for smoothening the charging of circuit breaker capacitor at the initial state. However, this modification is completely not applicable for the T-source circuit breaker because the series resistor to the circuit breaker capacitor can bypass the tripping operation as the minimum SCR current does not cross zero and this assumption made is verified in the following.

Adding a resistor in series to the circuit breaker capacitor as shown in Fig 3-6, the voltage across the transformer mutual inductance and X-point voltage are rewritten as shown in (3.23) and (3.24) respectively. Again, all the equations in (3.6), (3.7), (3.8), (3.9), and (3.23) are written in (3.11) form and then transformed to s-domain as (3.12). Then, using the Inverse Laplace Transform to obtain the SCR current.

$$-M \frac{di_M}{dt} = v_{CB} + v_{RB} - v_x \quad (3.23)$$

$$v_x = \frac{M(L_2 + M)}{M^2 - L_1 L_2} v_s - \frac{(L_1 + M)(L_2 + M)}{M^2 - L_1 L_2} v_{CB} + \frac{M(L_1 + M)}{M^2 - L_1 L_2} v_{CL} + \frac{(L_1 + M)(L_2 + M)}{M^2 - L_1 L_2} R_B i_m \quad (3.24)$$

Taking 20A as the current rating circuit breaker and the T-source circuit breaker parameter as shown in TABLE 3-II as an example, Fig 3-18 shows the computed minimum SCR current over various series resistance value. The tripping operation of the circuit breaker can only take places if the SCR current is less than zero. The result shows 1ohm fault resistance at the output terminal would allow a maximum 2.2ohm series resistance to be placed in the circuit breaker. However, the 5ohm fault resistance has a result of the minimum SCR current would not fall to zero for any value of series resistor except zero value. This implies that the T-source circuit breaker might not trip at the fault state if a series resistance is in place with the circuit breaker capacitor.

Fig 3-18. Simulation result of minimum SCR current over different series resistor value and various fault resistance

On the other hand, the achievement of manual tripping function can still be made for modification of T-source circuit breaker. The modification of T-source circuit breaker is shown in Fig 3-19. An additional resistor and a thyristor are added at the output terminal of the T-source circuit breaker to form the modification circuit. The purpose of the manual tripping function is to prevent the current pass through the SCR device over the current rating. Furthermore, the manual tripping allows the T-source circuit breaker to react as a DC switch in a DC system.

Fig 3-19. Manual tripping modification for T-source circuit breaker

Fig. 3-19 shows the modified T-source circuit breaker has an SCR T2 added as the switch for manual tripping. The T1 SCR protection function can be realized by activating T2 SCR when the output current measurement exceeds the current rating threshold of the SCR device. The activation of T2 SCR turns the circuit breaker into the tripping state, and the operation of the modified T-source circuit breaker is as follows:

1. The activation of T2 prompts a resonant current flow through transformer secondary winding, thyristor, and the resistor from the circuit breaker capacitor.
2. The T1 will turn off once the current has fallen to zero.

Higher resistor value for the modified circuit can reduce the output surge current and the current feeding from load capacitance. However, there is a limit of

resistor value can be used for the modified T-source circuit because overrating the resistor leads to malfunction tripping operation. The resistor value in the modified circuit to thyristor resistor can be determined as the rated source voltage over the current rating as shown in (3.25). Using the current rating is 20A, and the rated source voltage is 100V as an example, the modified circuit resistor is 5ohm.

$$R_m = \frac{V_s}{I_r} \quad (3.25)$$

A simulation is carried out for the observation of different modified resistor value to the manual tripping function. Using the component as shown in TABLE 3-II, Fig 3-20 shows the simulation result of the SCR current with the modified resistor value of 1ohm, 5ohm, and 6ohm. Fig 3-20 shows the simulation result of the SCR current with the modified resistor value of 1ohm, 5ohm, and 6ohm. This implies that (25) can be used as the guide to determine the modified resistor value.

Fig 3-20. Simulation result of different modified resistance over the SCR current

3.5 T-source Circuit Breaker Location in the DC Distribution System

The T-source circuit breaker can interrupt the fault current from the source feeding the fault continuously, and isolate the source facilities from the fault DC system. The fast tripping speed T-source circuit breaker can further reduce the rising of fault current magnitude and protect the downstream equipment in the DC system. The proposed location for the T-source circuit breaker is at the connection point between the power converter of each source terminal and the load terminal to the DC microgrid network. Based on the meshed network DC microgrid system as shown in Fig 1-2, the T-source circuit breaker is located at the output terminal of each facility power converter and is connected to the DC system as plotted in Fig 3-21.

Fig 3-21. The proposed location for the T-source circuit breaker in DC microgrid system

Few simulation tests are conducted to demonstrate the T-source circuit breaker reaction to the DC system and the MATLAB Simulink is the software for the simulation. Test 1 demonstrates a load added to the load terminal. Test 2 presents a fault at the load terminal. Test 3 illustrates a fault occurred at the transmission line in between bus 1 and bus 3. The original load resistance at the load terminal is set to 10 which means the load is drawing 21A initially. All test actions are taken places at 3s with the load added or triggering a fault. The simulation will show the results of the current measurement of all facilities power converter output and the voltage of DC microgrid. The current measurement with positive magnitude indicates the current is supplying to the DC system and the negative magnitude indicates the current is drawn out from the DC system.

Fig 3-22 plots the simulation result of test 1 with a 50Ω load added to the load terminal. The simulation waveform results show the current drawing at the load terminal is changing to 28.5A. All T-source circuit breaker in the DC system would not trip with the adding load at the load terminal. The voltage of the DC system is kept regulated at 380Vdc with a very little transient in load changing period.

Fig 3-22. The buses current simulation result of 50Ω load added at the load terminal

The simulation result of test 2 is depicted in Fig 3-23 with a fault resistance 1Ω at the load terminal. The fault happens in the load terminal would trip not only the T-source circuit breaker at the load terminal but all the T-source circuit breaker in the DC microgrid system. This is due to similar current rating design for all the T-source circuit breaker in the DC microgrid system. This result is not the desired operation of the circuit breaker which the fault in load terminal should only trip the circuit breaker at the load terminal. Such operation can assure other facilities in the DC microgrid system continue to operate normally without breaking. Nevertheless, the same current rating for the circuit breaker with interruption simultaneously can still prevent the fault continuously propagates to the other healthy facilities attached to the DC microgrid system.

Fig 3-23. The buses current simulation result of 1Ω fault resistance triggered at the load terminal

Fig 3-24 shows the simulation result of test 3 with a fault resistance of 1Ω happen at the transmission line between bus 1 and bus 3. The voltage of DC system falls to zero immediately during the happening of the fault. Same as the fault happen at load terminal, the transmission line fault would trip all the T-source circuit breaker in the microgrid system.

Fig 3-24. The buses current simulation result of 1Ω fault resistance triggered at the transmission line between bus 1 and bus 3

3.6 Conclusion

In this research, the modeling of the T-source circuit breaker using the transformer equivalent model for pre-tripping state and a single inductor for the post-tripping state are discussed. The time-invariant state-space equation and inverse Laplace transform method are used to derive the SCR current and the output current. The minimum value of the SCR current must cross the zero-crossing to ensure the tripping operation of the circuit breaker takes place. Then, the minimum required circuit breaker capacitor with respect to the load capacitance at the output terminal can be obtained by using the proposed design flowchart. It is also discussed that the use of higher transformer inductance can lower the output surge current. In determining the transformer inductance, the current rating of the circuit breaker is used as the design metric. The simulation results verify the proposed modeling for the pre-tripping and post-tripping state and all the derived equations. Based on the proposed modeling method and simulation result, a design flowchart and current rating for the T-source circuit breaker is proposed to size the circuit breaker capacitor and the transformer inductor respectively. Comparing the design in [37], the proposed design flowchart shows a significant reduction in the size of the T-source circuit breaker with a much lower value of transformer inductance and capacitor. The proposed design method of the T-source circuit breaker can be used to determine its tripping operation

effectiveness for different DC power system architectures and provide a result with lower output fault surge current. In addition, a modified version of the T-source circuit breaker is presented with the ability to protect internal SCR device from overcurrent. The selection of the resistor value is based on the rated voltage and current rating of the circuit breaker. In addition, all the T-source circuit breakers will trip the fault at the transmission line and the load side and retain in the non-trip mode when a load is added to the DC system.

Chapter 4. A High Accuracy Fault Location Identification for Single and Multipath Transmission Line

A single-end injection method using a probe power unit as shown in Fig 4-1 to identify the fault location. A simpler fault location identification technique that using logarithm decrement technique to obtain the damping coefficient is proposed in this section. The logarithm decrement technique can replace the least square error technique as shown in [58] to obtain the current damping coefficient. The logarithm decrement technique is shown in the following section. It has the advantages of high accuracy, less data reading needed, and fast processing speed.

Fig 4-1. Probe Power Unit

A low damping ratio is used to determine the probe power unit inductor and capacitor pair value. The low damping ratio can achieve a better fault measurement accuracy. The determination of the low damping ratio value is based on the high Q-factor bandwidth.

In the extension of the fault location identification for a single transmission line, a modification probe power unit with adding current probe at each junction terminal associated with the proposed multipath fault identification flow can identify the fault segment and fault location of the complex meshed network.

4.1 DC Line for Distribution System

A short transmission line can be used as a representative for the transmission line in DC distribution system network. The short transmission line is considered as a line length up to 80km. Series resistance and inductive reactive are the components considered for a short transmission line but neglect the capacitive effect. Fig 4-2 shows the model of the short transmission line for the unipolar and bipolar transmission line. By using the model of the short transmission line for the DC distribution system, the

fault location can be identified by connecting the probe power unit to the input terminal with a fault resistance assumed at the fault terminal.

Fig 4-2. DC distribution transmission line modeling for (a) unipolar system (b) bipolar system

4.2 Logarithm Decrement Technique

To understand the behavior of the probe power unit operation, we need to derive the current across the probe power unit. First, connecting the probe power unit as shown in Fig 1 to the transmission line as shown in Fig 4-2. Then, open the S1 and close the S2 of the probe power unit at the same time and this action forms an RLC series circuit. Then, the capacitor voltage is derived as in (4.1) and the C_p and L_p are denoted as the probe power unit capacitor and inductor respectively. The L_d and R_d are the inductance and resistance of the transmission line from the probe power unit to the fault point. The fault resistance is denoted as R_f is assumed at the fault terminal as shown in Fig 4-2. The capacitor current is the differentiation of the capacitor voltage. The probe power unit current is the opposite direction flow of the capacitor current. Hence, the probe power unit current is shown as (2) with a negative polarity. Based on (4.1) and (4.2), a second-order equation to the capacitor voltage is derived as (4.3).

$$V_{Cp} = V_{Lp} + V_{Ld} + V_{Rd} + V_{Rf} \quad (4.1)$$

$$i_p = -C_p \frac{dV_{Cp}}{dt} \quad (4.2)$$

$$(L_p + L_d)C_p \frac{d^2V_{Cp}}{dt^2} + (R_f + R_d)C_p \frac{dV_{Cp}}{dt} + V_{Cp} = 0 \quad (4.3)$$

The solution of the capacitor voltage as in (4.3) is shown as (4.4). The α and w_d are the damping coefficient and damping frequency respectively. The natural frequency is shown as w_n .

$$V_{cp}(t) = e^{-\alpha t} \left(V_0 \cos w_d t + \frac{\alpha V_0}{w_d} \sin w_d t \right) \quad (4.4)$$

$$\alpha = \frac{(R_f + R_d)}{2(L_p + L_d)}, w_d = \sqrt{w_n^2 - \alpha^2}, w_n = \frac{1}{\sqrt{(L_p + L_d)C_p}}$$

Based on the capacitor voltage as shown in (4.4) and the probe power unit current is presented as (4.2), the probe power unit damping current to the time is derived as (4.5). The peak of the injected current is shown as (4.6) with $k=0,1,2,\dots,n$.

$$i_p(t) = C_p V_0 \left(\frac{w_0^2}{w_d} \right) e^{-\alpha t} \sin w_d t \quad (4.5)$$

$$i_{p(k+1),peak} \approx C_p V_0 \left(\frac{w_0^2}{w_d} \right) e^{-\alpha \frac{(4k+1)\pi}{2w_d}} \quad (4.6)$$

The first and second peak current can be approximately denoted at $t_1 = \pi/2w_d$ and $t_2 = 5\pi/2w_d$ respectively. The two peak currents reading are acquired from the current measurement as shown in Fig 4-3. The damping frequency, w_d can be obtained from the period of the resonant current with the equation shown as (4.7). Finally, dividing the first peak current to the second peak current, the damping coefficient is obtained as shown in (4.8).

Fig 4-3. The probe power unit damping current with the first peak at $t_0 = \pi/2w_d$ and $t_1 = 5\pi/2w_d$

$$w_d = \frac{2\pi}{t_d} \quad (4.7)$$

$$\alpha = \frac{w_d}{2\pi} \ln \left(\frac{i_{p,peak1}}{i_{p,peak2}} \right) \quad (4.8)$$

The fault distance is the sum of fault inductance divide a unit cable inductance as shown in (4.8). Using the natural frequency equation as shown in (4.4) and the sum of inductance as shown in (4.9), the fault distance is derived as (4.10). The error measurement of fault distance in percentage is presented as (4.11). This error measurement is the difference between the calculated fault distance to the actual fault

distance. The low error measurement indicates the result of high accuracy for the fault distance measurement.

$$L_d = dL_u \quad (4.9)$$

$$d = \left(\frac{1}{(w_d^2 + \alpha^2)C_p} - L_p \right) \frac{1}{L_u} \quad (4.10)$$

$$e = \left| \frac{d_{cal} - d_{act}}{d_{act}} \right| \times 100\% \quad (4.11)$$

A simulation is carried out to compare the accuracy of the logarithm decrement technique with the no damping coefficient technique and the least square error technique. The MATLAB Simulink is the software for the simulation. Based on [13], the selected probe power unit capacitor and inductor values are 27 μ F and 657 μ H respectively. The transmission line and other component parameters are shown as in TABLE 4-I. The data acquisition from the simulation is the damping frequency using (4.7) and the two consecutive peak currents.

TABLE 4-I: Simulation parameter for the probe power unit and transmission line

Element	Description	Value
R_u	Line Resistance per unit km	121m Ω /km
L_u	Line Inductance per unit km	0.97mH/km
l	Total Line length	0.5 – 3km
R_f	Fault Resistance	0 – 2 Ω
V_0	Initial Voltage	100 V
C_p	Probe Capacitance	27 μ F
L_p	Probe Inductance	657 μ H

For a fair comparison, the simulation obtained data is similar, and these data are used as a comparison for the no damping coefficient, the least square error, and the logarithm decrement techniques. The simulation data of the peak currents and the damping frequency from MATLAB Simulink are recorded and shown in Appendix A.1. TABLE 4-II show the fault distance error results for these three techniques. Fig 4-4 plots the result of the error measurement to different fault resistance and different fault distance. In Fig 4-4, the plot presents all techniques have high accuracy at long fault distance and low fault resistance. However, the measurement accuracy has a significant difference in short fault distance and high fault resistance. The least square error technique has only a slight reduction of error measurement compare to the no damping coefficient technique. In Fig 4-4, the simulation results show the logarithm decrement technique has a low error measurement result significantly as compared to the no damping coefficient technique and least square error technique. The calculation result shows the including of logarithm decrement technique to obtain the damping

coefficient can achieve a better measurement accuracy on the fault distance calculation compare to no damping coefficient technique and least square error technique.

TABLE 4-II: Error Measurement of the no damping, least square error, and logarithm decrement technique

$\frac{R_f}{d_f}$	0.5			1			1.5			2		
	E_{nd}	E_{ls}	E_{ld}	E_{nd}	E_{ls}	E_{ld}	E_{nd}	E_{ls}	E_{ld}	E_{nd}	E_{ls}	E_{ld}
0.5	0.4378	0.2745	0.000276	1.5754	1.2651	0.000315	3.4384	3.0308	0.000188	6.0607	5.5886	0.000354
1	0.2685	0.1622	0.000305	0.8790	0.6798	0.000015	1.8484	1.5826	0.000214	3.1901	2.8776	0.000109
1.5	0.2157	0.1279	0.000110	0.6502	0.4896	0.000302	1.3239	1.1085	0.000293	2.2418	1.9849	0.000114
2	0.1921	0.1129	0.000221	0.5387	0.3980	0.000168	1.0645	0.8757	0.000222	1.7718	1.5468	0.000233
2.5	0.1794	0.1050	0.000074	0.4739	0.3452	0.000128	0.9108	0.7386	0.000103	1.4931	1.2874	0.000057
3	0.1732	0.1014	0.000237	0.4321	0.3527	0.000356	0.8108	0.6500	0.000428	1.3087	1.1164	0.000337

Fig 4-4. Error measurement over the fault resistance and fault distance for the no damping coefficient technique, the least square error technique, and the logarithm decrement technique

With such high accuracy fault location identification, the fault condition such as fault resistance can be easily retrieved by using the damping coefficient equation as shown in (4.4). The calculated fault resistance based on the logarithm decrement technique is shown in TABLE 4-III. The calculated fault resistance shows a result of very close to the actual fault resistance.

TABLE 4-III: The Calculated Fault Resistance using Damping Coefficient

$\frac{R_{f,act}}{d_f}$	Calculated Fault Resistance			
	0.5	1	1.5	2
0.5	0.49999	1.00001	1.49999	2.00001
1	0.50000	1.00001	1.49999	1.99998
1.5	0.50000	0.99999	1.49997	2.00002
2	0.50000	1.00003	1.50003	1.99996
2.5	0.50000	1.00001	1.50002	1.99999
3	0.49996	1.00000	1.49996	1.99996

In overall, the logarithm decrement method is a technique to find the damping coefficient. This method has a result of increasing the accuracy of fault location identification using probe power unit current injection. Furthermore, the logarithm

decrement method has a benefit of fewer data captured and faster processing to obtain the damping coefficient than least square error method. The data needed for the logarithm decrement method is only two consecutive peak current and the damping angular frequency.

4.3 High Fault Resistance Probe Power Unit Design

Previous probe power unit design shows a low accuracy fault distance measurement at high fault resistance. High fault resistance can cause the injected resonance current damping very fast. The overdamped current does not contain the fault information due to the absence of second peak current. The analysis of the probe power unit design with respect to the quality factor will be shown in the following.

Since the probe power unit injected current is a resonator of a second-order system, the quality factor is derived as (4.12). The Q-factor is the energy loss of a circuit. High Q-factor has a low rate of energy loss. Using (4.12) and the probe power unit parameter from TABLE I, a plot of quality factor over fault resistance for various fault distance is shown in Fig 4-5. In overall, Fig 4-5 shows fault distance closer to probe power unit has a result of a lower quality factor especially when the fault resistance is going higher. This means 0km has the lowest quality factor in overall compared to others fault distance.

$$Q = \frac{1}{R_d + R_f} \sqrt{\frac{L_d + L_p}{C_p}} \quad (4.12)$$

Fig 4-5 Error measurement with constant C_p and varying L_p

In addition, Fig 4-5 shows the fault distance 0km has a result of quality factor less than half when the fault resistance is more than 9.866ohm. The value of quality factor less than half indicates the injected current is overdamped. The overdamped current will cause the logarithm decrement technique and other method related to

probe power unit no applicable to find the fault location. The incapability of applying logarithm decrement technique is due to no two-consecutive peak will appear after the probe power unit current injection. Hence, the probe power unit inductance and capacitance value introduced in [13] as shown in TABLE 4-I cannot be used as the fault location identification for a wider range of fault resistance.

The only way to have a wider range of fault resistance for the fault location identification is to increase the quality factor. High Q factor can ensure the current is in underdamped mode. Based on equation (4.12), high Q factor can cause the inductance to the capacitance ratio of the probe power unit become large. The large inductance to capacitance ratio has a result of large inductance value and small capacitance value. This is impractical for an oversize and overweigh probe power unit to be used for fault location identification. Alternatively, we can analyze the quality factor by taking the derivative of the probe current from (4.5) with the result as shown in (4.13). The peak time for the injected current is derived as (4.14), and the damping frequency over the damping coefficient ratio is derived as (4.15). In order to fulfill equation (4.6) with the peak of sine function at $\pi/2$, the peak time has to be $t_p = \pi/2\omega_d$. This will result with the damping frequency over the damping coefficient ratio must reach infinity for the inverse tangent function as shown in (4.14). In another word, the quality factor as shown in (4.15) must be infinitely large to fulfill (4.6) with the peak at $\sin \frac{\pi}{2}$.

$$\frac{di_p}{dt} = C_p V_0 \left(\frac{\omega_n^2}{\omega_d} \right) e^{-\alpha t} [-\alpha \sin \omega_d t + \omega_d \cos \omega_d t] \quad (4.13)$$

$$t_p = \frac{1}{\omega_d} \tan^{-1} \left(\frac{\omega_d}{\alpha} \right) \quad (4.14)$$

$$\frac{\omega_d}{\alpha} = \sqrt{4Q^2 - 1} \quad (4.15)$$

Since quality factor with infinitely large is unachievable, the peak will not achieve $\pi/2$ according to (4.14). Hence, a determination of small peak deviation tolerance percentage is required to avoid a bad accuracy for the logarithm decrement technique fault location identification. Due to the fact of large fault resistance can lower the quality factor as shown in (12), the determination of maximum detectable fault resistance is required to obtain the best inductance and capacitance value for the probe power unit. Once the peak tolerance percentage and maximum detectable fault

resistance parameter are determined, the ratio of probe power unit inductance to capacitance can be obtained using the proposed flowchart as shown in Fig 4-6.

Fig 4-6. The proposed flowchart for the ratio of L_p to C_p

Assuming 3% peak deviation tolerance and 100ohm maximum detectable fault resistance is the parameter for the calculation of probe power unit inductance to capacitance ratio. The inverse of sine to 0.97 is 1.3265. Using (4.14), the tangent of 1.3265 is 4.0108 and has a result of quality factor is 2.0668. This means the quality factor of 2.0668 will fall on 100ohm fault resistance, and this is the minimum quality factor value over the range of 100ohm fault resistance as shown in Fig 4-7. Finally, the probe power unit inductance to capacitance ratio is obtained as 42715.91, and the plot of various capacitance to inductance value with the ratio 42715.9 is shown in Fig 4-8.

Fig 4-7. The fault resistance over the quality factor

Fig 4-8. The inductance L_p value with varying capacitance C_p value with Q is 2.0668

A simulation is carried out to test the quality factor with a minimum value is 2.0668. Based on Fig 4-8, the chosen value of the probe inductance and capacitance are 4.3mH and 0.1uF respectively. The simulation test various fault length up to 10km with the maximum fault resistance is 100ohm. TABLE 4-IV shows the simulation parameter for the probe power unit and the transmission line. The simulation is tested using MATLAB Simulink with the data is captured and recorded in APPENDIX A.2. The captured data is the two-consecutive peak currents and the damping angular frequency. Then, using the logarithm decrement technique to generate the fault distance result. The error is the difference of actual fault distance to the calculated fault distance as shown in (4.11) and the error result is shown in TABLE4-V. Fig 4-9 shows the error versus various fault distance with different fault resistance. As seen from the result, the error is affected by the fault distance but not much variation for the different value of fault resistance. The percentage of error is high at the short fault distance, which can up to 3% of error measurement at 0.01km fault distance. The high value of error at short fault distance is acceptable in the maintenance point of view due to the variation of measurement is not much for the short fault distance. For instance, 3% error of 0.01km has a result of 30cm error measurement. With the Q factor chosen as 2.0668 for 100ohm as the maximum fault resistance, the error is remains kept at a low level in overall. This result shows the effectiveness of the proposed flowchart for the probe power unit design at high fault resistance.

TABLE 4-IV: Simulation parameter for the probe power unit and the transmission line for $Q=2.0668$

Element	Description	Value
R_u	Line Resistance per unit km	121m Ω /km
L_u	Line Inductance per unit km	0.97mH/km
l	Total Line length	0 – 10km
R_f	Fault Resistance	0 – 100 Ω
V_0	Initial Voltage	100 V
C_p	Probe Capacitance	0.1 μ F
L_p	Probe Inductance	4.3mH

TABLE 4-V: The error value of Q is 2.0668 for various fault resistance and fault distance

R_f d_f	error			
	0.1	1	10	100
0.01	1.991720	1.969923	1.934451	3.090711
0.1	0.215224	0.213830	0.220940	0.099343
1	0.023485	0.023333	0.023680	0.011576
10	0.003417	0.003379	0.003740	0.001142

Fig 4-9. The error value over fault distance and fault resistance for Q is 2.0668

In overall, we can conclude a high Q factor can widen the range of the fault resistance measurement. High Q factor can prevent the oscillation falls into overdamped system especially at high fault resistance. As such, the proposed flowchart can be used as the reference for design a probe power unit for wide range fault resistance.

4.4 Parallel path fault branch identification

The parallel path transmission line is multiple paths that have two common joints, and it is commonly seen in the power system. The parallel path is a connection of several cables in parallel for the transmission line. A DC system meshed network as shown in Fig 4-10a can be seen as the parallel connection transmission line. When a fault occurs, the current flown from the faulted cable and the parallel cable path toward the fault point. Hence, it is also necessary to identify the fault segment for the complex network before the recovery process.

A modification of the probe power unit is needed to identify the fault of multiple parallel paths. The modification of the probe power unit is to add a current probe to each junction. The total number of current measurement probe for the parallel probe power unit is the sum of the current measurement at each terminal junction and the source. For n numbers of the terminal junction, there would be an $n+1$ number of current probes are needed in total for a parallel probe power unit. The parallel probe power unit is shown in Fig 4-10b. The operation of the modified probe power unit is similar to the previous probe power unit. The capacitor is pre-charging for a long time with the S1 switch is closed, and the S2 switch is opened. Then, triggering the S1 switch to open and S2 switch to close at the same time for the current injection. The information of first peak current and the time of one cycle are recorded. These reading are used as the information to determine the fault path and fault location of the multiple parallel transmission paths.

Fig 4-10 (a) DC meshed network as the representation of parallel connection transmission line (b) Parallel probe power unit

For a network with multiple transmission paths with no connection of transmission line at both ends such as radial network, the fault path can be easily identified as the only current oscillation at among the current probes. However, the fault path cannot be directly identified by observing the current probe for the parallel connection network. Consider a network with multiple parallel transmission paths is connected with two common buses at both end terminal as shown in Fig 4-11a. L_n and d are denoted as the cable length and the fault distance respectively. Z indicates the impedance of a unit kilometer. The fault happens at one of the multiple parallel paths transmission lines. The parallel probe power unit is then triggered and injects the

currents with different magnitude at each junction and flow toward the fault point. An equivalent circuit of a fault in the parallel path is depicted as shown in Fig 4-11b. The impedance of the non-fault parallel paths is shown as (4.16), and n is denoted as n number of junction parallel path. Then, the equivalent impedance seen from the injection source is obtained as (4.17). The subscript fp is denoted as the fault path among multiple paths.

$$Z_{pa} = \frac{1}{\left(\sum_{k=1}^n \frac{1}{L_{en_k} Z_k}\right) - \frac{1}{L_{en_{fp}} Z_{fp}}} \quad (16)$$

$$Z_{eq} = \frac{[Z_{pa} + (L_{en_{fp}} - d)Z_{fp}]dZ_{fp}}{Z_{pa} + L_{en_{fp}} Z_{fp}} \quad (17)$$

Fig 4-11. a) Fault at one of the multiple parallel transmission line path b) Equivalent circuit of a fault at one of the multipath transmission line paths

Based on the equivalent circuit as shown in Fig 4-11b and the current divider rule, the fault path current is derived as shown in (4.18), and the fault distance is derived as (4.19).

$$i_{fp} = i_t \left(\frac{Z_{eq}}{dZ_{fp}} \right) \quad (4.18)$$

$$d = \frac{(Z_{pa} + L_{en_{fp}} Z_{fp})(i_t - i_{fp})}{Z_{fp} i_{fp}} \quad (4.19)$$

4.4.1 Fault Identification of Multiple Parallel Path with Different Type and Different Length

By using the fault distance identification as derived in (4.19), an assumption can be made for the calculated fault distance accuracy is affected with varying the fault resistance. A simulation test with two cables test is conducted to verify the assumption made. TABLE 4-VI shows the cable parameter of different unit resistance, different unit inductance, and different cable length. The MATLAB Simulink is the software for the simulation.

TABLE 4-VI: Different Cable Parameter

Cable	Length km	Unit Resistance Ω/km	Unit Inductance mH/km
A	2	0.121	0.97
B	3	0.121	0.97
C	2	0.2	2

A simulation test is conducted with two similar cables are used as the transmission cable, and one of the cables has a fault. Two cable A from Table 4-III are employed as the simulation test. The capacitor and inductor value of probe power unit are of $0.273\mu\text{F}$ and $400\mu\text{H}$ respectively as shown in the previous section. Fig 4-12 plots the simulation result of the error of calculated fault distance with varying the fault distance and fault resistance. The result shows a high accuracy fault distance identification with less than 0.03% of error measurement. This result can conclude the error measurement is almost the same for varying the fault resistance at the same fault distance. Hence, the following simulation test case only takes into consideration the result of fault distance identification with varying fault distance only, but the fault resistance stays constant at 2Ω . The test cases to verify the (4.19) are:

Case 1: Two parallel cables of same cable length and same cable type

Case 2: Two parallel cables of different cable length and same cable type

Case 3: Two parallel cables of same cable length and different cable type

Case 4: Two parallel cables of different cable length and different cable type

Fig 4-12 Error measurement of varying fault resistance test

For multiple parallel paths with same cable length and same cable type, the fault path identification is always at the largest positive magnitude current among all junction. Case 1 simulates a test of two parallel arrangement cables with the same cable length and impedance. Two cables A are chosen for case 1 and denoted as A1 and A2. A fault is presumed at cable A1 for the simulation. The simulation result of case 1 test is shown in Fig 4-13 with the fault segment is identified as cable A1 only and provide a calculated fault distance is very close to the actual fault distance. The calculated fault distance of cable A2 is zero value due to the fault segment is not identified as cable A2. Based on the assumption of fault at the positive largest magnitude current, the simulation shows the identification of the fault segment is correct.

Fig 4-13 The simulation of result case 1 with same cable type and length

However, the appearance of the fault path is not always at the largest magnitude current especially for a multiple paths transmission line with different cable length and different cable type. The following simulation test cases take into consideration multiple transmission paths with a different combination of cable impedance and cable length. The following simulation tests are conducted to test the effectiveness of identifying the fault segment of multiple paths using only the positive largest magnitude method. The simulation test using a modified probe power unit with the component parameter of C_p is $0.1\mu\text{F}$ and L_p is 4.3mH .

Case 2 simulates a test with same cable impedance but different cable length. The simulation conducts with two cables are connected in parallel. The simulation test using a cable A and a cable B from TABLE 4-III as the cable parameter. Case 2a is a simulation test with the actual fault happens at cable A, and case 2b simulates the occurrence of the fault path at cable B. Fig 4-14 shows the simulation of the fault distance versus the calculated fault distance. Fig 4-14a and Fig 4-14b depict the simulation result of the case 2a and case 2b respectively. Based on Fig 4-14b result where the actual fault path is at cable B, the positive largest current magnitude method identifies a fault at cable A when the fault distance at cable B is more than 2.5km. Using

(4.25) for the fault distance calculation, the obtained fault distance of cable A from the calculation shows the calculated fault distance is longer than the cable A length.

Fig 4-14. The simulation result of case 2: same cable type but different cable length: a) fault happens at cable A, b) fault occurs at cable B

Similarly, case 3 tests multiple transmission paths with same cable length but different cable impedance. Two parallel connected cables with a cable A and a cable C from TABLE 4-III are chosen as the simulation test cable parameter. The fault path is at the cable A for case 3a, and the fault path is at cable C for case 3b respectively. Fig 4-15a plots the simulation result of the case 3a and Fig 4-19b shows the simulation result of case 3b. As seen in Fig 4-15b, the fault path is identified as cable A which has a calculated fault distance with longer value than the cable length with more than 2km.

Fig 4-15 The simulation result of case 3: same cable length but different cable type: a) fault happens at cable A, b) fault occurs at cable C

Case 4 shows different cable impedance and length is simulated. This case chooses a Cable B and a Cable C as the test cable of simulation. The actual fault path is assumed to happen at cable B and cable C for case 4a and case 4b respectively. Fig 4-16a depicts the simulation result of Case 4a, and Fig 4-16b presents the simulation of case 4b. Similar to case 2 and case 3, the chosen wrong fault path as cable B has a longer calculated fault distance than the 3km cable length.

Fig 4-16 The simulation result of case 4: different cable type and different cable length: a) fault path at cable B, b) fault happens at cable C

In the simulation test with various cases, it is found that the calculated fault distance can be longer than the particular cable length if a wrong identification of fault

path. The false fault path identification is usually happening when the fault distance is closed to the cable length. With such a simulation test assumption, a fault identification flow is needed to develop to identify the fault path and fault distance correctly.

4.4.2 Parallel Path Fault Identification Flow

Using the derived equation from (4.16) to (4.19) and the parallel probe power unit, a propose fault identification flow for the parallel transmission line is shown Fig 4-17. The subscript M is denoted as the sequences of positive largest amplitude among the cable path current measurement. M=1 indicates the first largest amplitude, M=2 is the second highest amplitude, and the following. Initially, M is 1, and the positive largest current amplitude among the several paths is chosen as the fault path. Once the fault distance of the largest current magnitude path is computed, the fault distance will be taken as a comparison with the corresponding cable length. In the condition of the calculated fault distance is longer than the fault cable length, the fault identification flow will increase M by 1 and choose the next largest current magnitude path as the fault path and compute for the fault distance. The fault distance and fault path is determined and ended with the condition of the calculated fault distance have a smaller value than the total fault path length.

Fig 4-17 Flowchart of parallel path fault identification

To verify the proposed flowchart for the multiple parallel path fault identification, a DC meshed network as shown in Fig 4-10a is used as the parallel path network for the simulation. The DC meshed network is assumed with a unipolar system, and all the transmission line segments are presumed with a length of 2km. The cables parameter for each segment is the same and is shown in TABLE 4-VII. The parallel probe

power unit is placed at bus 1 as shown in Fig 4-10a and the component parameter is shown in TABLE 4-VII. The simulation result for the fault of F1, F2, and F3 are shown as TABLE 4-VIII which the peak current at each junction, the total current, and the damping frequency are captured. Using the proposed flowchart to compute the fault distance and fault path, the result in TABLE 4-VIII shows an accurate result whereby F1 fault is at segment 13 with the fault distance is 1.1993km, F2 fault is at segment 14&43 with the fault distance is 3.4996km, and F3 fault falls at segment 12&23 with the fault distance is 0.7001km. Since the length of segment 14 is 2km, the fault would fall on segment 43 with the fault distance is 1.4996km from bus 4. The calculated fault distance and the fault segment result verify the proposed parallel path fault identification flowchart is feasible to be used as identifying the fault distance and fault path for multiple parallel path networks.

TABLE 4-VII: Simulation parameter for the probe power unit and transmission line

Element	Description	Value
R_u	Line Resistance per unit km	121m Ω /km
L_u	Line Inductance per unit km	0.97mH/km
l	Total Line length for each segment	2km
R_f	Fault Resistance	10 Ω
V_0	Initial Voltage	100 V
C_p	Probe Capacitance	0.1 μ F
L_p	Probe Inductance	4.3mH

TABLE 4-VIII: Simulation parameter for the probe power unit and transmission line

	F1	F2	F3
$i_{12}\&i_{23}$	0.064	0.0904	0.3792
i_{13}	0.2989	0.1808	0.0382
$i_{14}\&i_{43}$	0.064	0.1421	0.0191
i_t	0.4269	0.4133	0.4365
f	7023.02	6793.15	7182.2
M	1	2	1
d_{cal}	1.1993	3.4996	0.7001
Fault segment	13	14&43	12&23

4.5 Conclusion

For a single transmission line fault, the logarithm decrement technique can achieve better accuracy for fault location identification with a less reading is needed. The measurement reduces the error significantly compared to the least square error technique and the no damping technique. Alternatively, the determination of the LC pair parameter for the probe power unit is based on the peak deviation tolerance and the maximum detectable fault resistance. The proposed LC pair value can achieve a wider range of fault resistance and provide a high accuracy measurement of fault distance. The introduced parallel probe power unit associated with parallel fault identification flow was proven can accurately identify the fault path and fault distance

of multiple parallel transmission paths. The parallel probe power unit and the parallel fault identification flow can be used identifying the fault for a complex network such as a ring network or a meshed network. However, this research does not cover the fault identification for medium length transmission which includes the parasitic capacitance in the cable and the fault identification for a single transmission line with the different material at a different section. These two topics are crucial for the fault identification aspect which will be covered in the future research. In overall, the achievement of high accuracy fault location identification is shown for a different type of network configuration using a single-ended probe power unit device and the proposed algorithm.

Chapter 5. A Stable Restoration Sequence in Fault Recovery State

This chapter presents the fault recovery action to restore back the power of the DC network. The benefit of system recovery is the reboot of entirely or partially system back to normal operation without an outage of the whole system. The fault recovery process aim is to achieve a stable DC voltage.

A meshed network DC distribution system with the DC switches and circuit breaker as presented in Fig 4-20 is used in this chapter. The DC distribution system consists of a grid interfacing system, a storage system, and a distributed generation system. Once the fault segment is identified and isolated, the recovery action will be made immediately to restore power back to normal operation.

The adoption of the DC circuit breaker for the DC system is due to faster interruption speed and has a result of reducing the fault current magnitude. The adoption of system reconfiguration proposed in [20, 57] using the AC circuit breaker can have different result compare to the DC circuit breaker due to the placing of DC circuit breaker is different. The DC circuit breaker that using the same reconfiguration step as AC circuit breaker can result with high transient DC voltage at the initialization stage. Hence, a knowledge of system reconfiguration is required for a DC distribution system with different facilities require to achieve a stable system recovery.

The reconfiguration step is the priority of deblocking the power converter or reclose the DC circuit breaker for restoring the facility back to the DC microgrid. For a smooth post-fault operation, the implementation of the reconfiguration step for a different facility is different. A comparison of the reconfiguration step for different facilities shown in this chapter. Additionally, the simultaneous and sequential connection of all facilities back to the DC system is shown in this paper. Finally, the comparison of different sequences of reconnecting different facilities to the DC network is presented in this chapter.

5.1 DC Microgrid system configuration

A meshed network DC distribution system is shown in Fig 5-1. The meshed network has higher reliability than radial network due to the capability of entirely recover the facilities operation with any fault at the transmission line and partially recover facilities operation with the fault at one of the buses. For each transmission line in the meshed network, there are two DC switches placing at each end terminal

and connected to the bus. The DC switch provides the necessary selectivity to the DC network and allows the implementation of fault recovery to isolate the fault segment transmission line. The DC circuit breaker is used as the fault tripping device instead of a long breaking time AC circuit breaker. The fast tripping speed DC circuit breaker can lower the risk of high magnitude fault current feeding toward the fault. The DC circuit breaker is placed at the connection of facility power converter to the DC network.

Fig 5-1. DC Meshed Network

The commonly seen facilities in the DC distribution system are grid interfacing system, storage system, distributed generation system, and load. The typical power converter for each facility is shown in Fig 5-2. Each facility power converter performs differently toward the DC network.

Fig 5-2. Power converter for a) grid interfacing system, b) storage system, c) photovoltaic system

In the DC distribution system, the grid interfacing system is served a slack bus terminal to regulate a constant DC voltage of the DC network and balance the power in the DC microgrid system. Hence, three phase[82] or single phase PWM boost type rectifier[83-86] is chosen as the power converter of the grid interfacing system. The control mode of the grid interfacing system power converter is the voltage control mode that can regulate the voltage level to 380Vdc. The rectifier converts the AC energy to a DC energy. In a small-scale DC microgrid system with below 5kW, the single-phase PWM boost rectifier is sufficient as the grid interfacing system power converter. TABLE 5-I shows the components parameter for single phase PWM rectifier with the derivation of the parameter is shown in APPENDIX-B.1.

TABLE 5-I: Single Phase PWM Rectifier Components Parameter

Component	Description	Value
V_{in}	Input Voltage	230Vrms
V_o	Output Voltage	380Vdc
P	Power Rating	5kW
f_s	Switching Frequency	20kHz
Δi_L	Input Current Variation	5%
ΔV_o	Output Voltage Variation	1%
L	Input Inductor	3.09mH
C	Output Capacitor	19.15mF

The storage system function as import and export the power of the DC network. The storage system deposits the excess generated power from the DC distribution system and supplies power to the insufficient power DC distribution system. Hence, an active power control mode is exploited for the storage system to control the power feeding or storing in the DC distribution system. In a circumstance where insufficient power in the DC distribution system, the voltage level of the DC distribution system will sag. The battery system will convert into a voltage control mode and regulate the DC distribution system voltage.

There are various power converters for the storage system with a different number of switches [87]. Among all the power converters, the synchronous boost DC-DC converter[88, 89] and the dual active bridge converter[90-93] are the most popular power converter for the storage system. For a power level below 5kW storage system, the synchronous boost converter is typically selected as the storage system converter because of a low number switching device. The synchronous boost converter allows bi-directional power flow. It has the function of stepping down the voltage level on the battery side and stepping up the voltage level at the DC network terminal. The synchronous boost converter components parameter is derived in APPENDIX-B.2 and is presented in TABLE 5-II.

TABLE 5-II: Synchronous Boost Converter Components Parameter

Component	Description	Value
V_{in}	Input Voltage	200Vdc
V_o	Output Voltage	380Vdc
P	Power Rating	5kW
f_s	Switching Frequency	10kHz
Δi_L	Input Current Variation	5%
ΔV_o	Output Voltage Variation	0.1%
L	Input Inductor	10.7mF
C	Output Capacitor	820 μ F

The distribution generation system in a DC distribution system is usually renewable energy such as photovoltaic and wind energy. For a country in the tropical zone such as Singapore has rich sunlight and the photovoltaic is the most common distributed generation source in the DC distribution system. The photovoltaic system has a time-varying output power that depends on solar irradiance level and ambient temperature. The wide range of photovoltaic system voltage with the variations of power level is due to the fluctuation of energy source which greatly depends on solar irradiance, temperature, partial shading, complex roof structure and orientation conditions. Typically, the energy harvested from the photovoltaic system decreases when the temperature increases and the harvested power increases when the solar irradiation increases. There is a unique operating point whereby the photovoltaic generator produces maximum output power. The harvested power is depending on the voltage level of the photovoltaic cell, and it is sourced to the DC distribution system.

A commonly seen power converter for the photovoltaic system is an isolated boost converter [94] and boost converter[95-99]. For a small-scale power harvesting, the boost converter is selected as the photovoltaic system converter. The boost converter can step up the harvest energy voltage from the photovoltaic system to the DC distribution system voltage level, and the input voltage can be controlled to achieve maximum power harvesting. The boost converter components parameter derived in APPENDIX-B.3 is shown in TABLE 5-III.

TABLE 5-III: Boost Converter Components Parameter

Component	Description	Value
V_{in}	Input Voltage	210Vdc
V_o	Output Voltage	380Vdc
P	Power Rating	5kW
f_s	Switching Frequency	10kHz
Δi_L	Input Current Variation	5%
ΔV_o	Output Voltage Variation	0.1%
L	Input Inductor	10.7mF
C	Output Capacitor	774 μ F

5.2 Reconfiguration Step of power converter and DC circuit breaker

The reconfiguration step in this paper is termed as the sequence of reclosing the DC circuit breaker and deblock power converter. For system recovery, the reconfiguration step of facilities has a significant impact on the transient of DC voltage. An effective reconfiguration step can reduce the transient level and result in better voltage stability. In the following section, the reconfiguration step of three main

facilities in the DC network such as grid interfacing system, distributed generation, and storage system is presented.

5.2.1 Grid Interfacing System

The power converter for grid interfacing system as shown in Fig 5-2a is a type of voltage source converter. The input to the power converter is tied to the grid with a distribution AC voltage level at 230Vac. The voltage is regulated with 380Vdc at the output of the power converter. The power converter output will result in the maximum voltage level is two times to the RMS voltage but not boost up to the desired 380Vdc voltage level. The reconnection of load to the DC network is before deblock the grid interfacing system converter can cause an insufficient voltage at the end terminal, and this result can degrade the load efficacy. The non-regulated voltage at the power converter DC terminal is because the current will continuously flow to the power converter DC terminal through the antiparallel diode of the switches when the switches are not given any control signal at the blocking state. Additionally, the DC circuit breaker is reclosed after deblock the grid interfacing system can suppress the inrush current of the switches at the initial state. The high inrush current can damage the power converter switches. A simulation test is conducted to validate the assumption made of the load connected before and after deblock the grid interfacing system. The simulation is conducted in the way of the power converter is deblocked at 1s, and the DC circuit breaker is reclosed at 0.5s and 1.5s respectively. The MATLAB Simulink is used as the software for the simulation.

Fig 5-3 plots the simulation result of the DC terminal voltage and current, and the high side switches current of the grid interfacing system power converter. The simulation results show the output terminal DC voltage is regulated up to 380v and the current is stepped up smoothly for both cases. However, there is an inrush current at the switches for prior and after reclose circuit breaker cases. The simulation result shows the reclosing of the circuit breaker after deblocking the power converter has a lower inrush current compared to the case of reclosing the circuit breaker before the deblocking of the power converter.

Fig 5-3 Simulation test result of grid interfacing system with the reactivation of power converter at 1s and dc circuit breaker at 0.5s and 1.5s: a) load voltage, b) load current c) power converter switch current

5.2.2 Battery System

The synchronous boost converter as shown in Fig 5-2b is chosen as the power converter of the battery system. This power converter has the capability of flowing current in both directions. In the event of regulated voltage at the DC system, the active power control mode would be taken as the control of power converter to store the excess power generated from DC network or supply the insufficient power to the DC network. Deblock the power converter prior to the reclosing dc circuit breaker can cause an increase of voltage at the smoothing capacitor of the power converter. This will cause the output voltage and output current have a large overshoot at the DC network terminal in the event of reclosing the dc circuit breaker to connect the power converter to the DC network. A simulation test is conducted to examine the result of deblocking synchronous boost converter priory and after the reclosing of dc circuit breaker. The power converter is activated at 1s, and the dc circuit breaker is reclosed at 0.5s and 1.5s respectively. The MATLAB Simulink is used as the software for the simulation.

The simulation result of the storage system with the DC network voltage, DC network current, and the switches of the power converter is shown in Fig 5-4. For the power converter is deblocked before reclosing the dc circuit breaker, the voltage of the smoothing capacitor in the power converter is kept charging. When the dc circuit breaker is reclosed, a large overshoot voltage and current at the DC network is obtained. As a comparison, the DC circuit breaker is reclosed before deblocking the power converter can eliminate the overshoot voltage and current at the DC network. The result of switch current in the power converter shows no difference for reconfiguration step of the DC circuit breaker and the power converter.

Fig 5-4. Simulation result of the active power control mode battery system with the reactivation of power converter at 1s and dc circuit breaker at 0.5s and 1.5s: a) Load voltage, b) load current c) zoom in load current in between 0.75s to 1.8s d) power converter switch current

Based on the simulation result, the conclusion of the reconfiguration step of the storage system is the dc circuit breaker should have reclosed before deblock the power converter. This reconfiguration step for battery system can eliminate the overshoot of output voltage and current at the DC network that can damage the downstream load and facilities attached to the DC network.

5.2.3 Distributed Generation System

For a photovoltaic system represented as the distributed generation system, a boost converter as shown in Fig 5-2c is chosen as the power converter. The power converter tracks the maximum power point of the solar panel and transfers the harvested power toward the DC network. The deblock of boost converter before reclosing the dc circuit breaker(which is without a constant DC voltage at the converter output) will increase the smoothing capacitor voltage. The increase of smoothing capacitor voltage is due to charging of smoothing capacitor in the power converter without permitted to flow out. Reclose the DC circuit breaker to the DC network with energy stored in smoothing capacitor can cause a large discharging overshoot voltage and current occur at the DC network. A simulation test is run to examine the assumption made of deblocking the boost converter with reclosing of the dc circuit breaker at before and after. The power converter is activated at 1s, and the DC circuit breaker is reclosed at 0.5s and 1.5s respectively.

The simulation result of the photovoltaic system with the boost DC-DC converter is shown in Fig 5-5. The reclosing of the DC circuit breaker after deblocking the power converter create a large rising of the output voltage at the power converter. The reclose of DC circuit breaker then generates a large overshoot current at the output terminal. Based on the photovoltaic system simulation result, it is necessary to connect to a stable DC voltage before deblocking the power converter. A stable DC voltage at the power converter output can eliminate the overshoot current and prevent damage the load and facilities attached to the DC system. Hence, the DC circuit breaker must reclose before the activation of the power converter. Additionally, there are no different for the power converter switch current for both cases.

Fig 5-5. Simulation result of the photovoltaic system with the reactivation of power converter at 1s and dc circuit breaker at 0.5s and 1.5s: a) power converter output voltage, b) load current, c) power converter switch current

5.2.4 Summary of Reconfiguration Step

For grid interfacing system, reclose DC circuit breaker after deblocking the power converter has the benefit of reducing the inrush current of the power converter at start-up state and prevent the degradation of load performance due to the insufficient load current and load voltage. The reclose of DC circuit breaker before deblocking the power converter for the battery system, and the photovoltaic system can eliminate the overshoot voltage at the output terminal. The reconfiguration step of reclosing DC circuit breaker prior to deblock the power converter sequence for each individual facility back to the DC network can achieve a more stable voltage.

5.3 The Reconnection Sequence of facilities to the DC Microgrid System

5.3.1 Simultaneous versus Sequential connection

After removing the fault from the DC system, all facilities will reconnect back to the DC network for the system recovery. There is an impact on the performance for a different reenergizing sequence of each facility in MTDC. The ineffective reenergizing sequence can cause a large transient voltage, unstable voltage, and non-equilibrium

power in the DC system. The system recovery can be differentiating into simultaneous connection or sequential connection. A simulation is conducted to observe the transient of simultaneous connection and sequential connection of facilities to the DC network. For the simultaneous connection, the DC circuit breaker of all facilities is reclosed at 1s, and all the power converter facilities are deblocked at 1.5s. Fig 5-6 shows the simulation result of all the facilities connected to the DC network simultaneously. The positive magnitude current mean current flow into the DC network and negative is the current is flown out from the DC system. The simulation of DC buses voltage and DC buses current at each power converter output terminal are shown. For the sequential connection, the timing of connection is shown in TABLE IV with the sequence is 1) grid interfacing system, 2) battery system, 3) photovoltaic system. The load draws 4kW power from the DC network, and the maximum power capacity of storing and sourcing the battery system is set to 2kW. Fig 5-7 shows the simulation result of the sequences connection of each facility to the DC network.

Fig 5-6. The Simulation result of the Simultaneous connection of facilities to the DC network: a) The DC bus voltage b) The DC bus current

TABLE 5-IV: The action timing of each facility in the DC system

Time(s)	Recovery Action
1	Activate the grid interfacing system converter
1.5	Reclose the grid interfacing system dc cb
2	Reclose the battery system dc cb
2.5	Activate the battery system converter
3	Reclose the photovoltaic system dc cb
3.5	Activate the photovoltaic system converter

Fig 5-7. The Simulation result of the sequential connection of facilities to the DC network: a) The DC bus voltage b) The DC bus current (case A connection sequence of grid interfacing system, battery system, photovoltaic system)

Taking the simulation result of simultaneous and sequential connection as shown in Fig 5-6 and Fig 5-7 respectively as a comparison, there are not many changes for DC voltage transient on each bus. However, the connection of the facilities in the sequence has a smaller current transient of each bus when the DC circuit breaker is reclosed. Based on these simulation result, the conclusion can be made with the sequential connection of the facilities to the DC network is more stable due to the transient current is smaller than simultaneous connection.

5.3.2 Facilities Reconnecting Sequence

The priority of connecting each individual facility back to the DC network has a great impact on the DC network voltage and the transient current. The distributed generation system necessitates a stable voltage prior to function effectively. Hence, the grid interfacing system that acts as the slack bus should be the first facility connected

back to the facility. The storage system monitors the DC network voltage and decides the control mode. The battery system will turn into active power control mode if the DC network has a full rated voltage. From the assumption made, the proposed reconnection sequence of the facilities back to the DC system is: 1) grid interfacing system, 2) battery system, 3) photovoltaic system. A simulation test is conducted to examine the priority of reconnection to the DC network for system recovery. The reconnection action of each facility is included of deblocking power converter and reclose DC circuit breaker. The reconnection timing is 1s, 1.5s, 2s, 2.5s, 3s, and 3.5s. There are six possibilities of sequences for the reconnection of facilities to the DC network, the simulation cases are:

- A. grid interfacing system, battery system, photovoltaic system
- B. grid interfacing system, photovoltaic system, battery system
- C. battery system, grid interfacing system, photovoltaic system
- D. battery system, photovoltaic system, grid interfacing system
- E. photovoltaic system, grid interfacing system, battery system
- F. photovoltaic system, battery system, grid interfacing system

Case A and B test on the connection of the grid interfacing system prior to other facilities. The simulation results of case A and case B are shown in Fig 5-7 and 5-8 respectively. Fig 5-7 and 5-8 plot the DC buses voltage and current. The DC buses voltage shows not much different for the transient of DC voltage. The transient current magnitude is the same for case A and case B. From the simulation result, case A and case B can be chosen as the facilities connection sequence to the DC network.

Fig 5-8. The simulation result of case B with the sequence connection is grid interfacing system, photovoltaic system, battery system: a) DC bus voltage and b) DC bus current

Case C and Case D examine the connection of battery system prior to other facilities. The simulation result of case C and case D connection sequences are shown in Fig 5-9 and Fig 5-10 respectively. The battery system will turn into voltage control mode at the initial stage to regulate DC network voltage and balance the power of the DC network. Fig 5-9 and Fig 5-10 show the simulation result of the DC network voltage and current. Case C and case D show a high overshoot voltage on all buses when the battery system is connected to the DC network. There is a voltage sag for the DC bus voltage and large transient current when the battery system changing the control mode from voltage control mode to power control mode at the moment grid interfacing system is connected back to the DC network. The connection of grid interfacing system has a huge fluctuation of current flow to the DC network.

Fig 5-9. The simulation result of case C with the sequence connection is battery system, grid interfacing system, photovoltaic system: a) DC bus voltage and b) DC bus current

Fig 5-10. The simulation result of case D with the sequence connection is battery system, photovoltaic system, grid interfacing system: a) DC bus voltage and b) DC bus current

Case E and case F test the connection of the photovoltaic system to the DC network prior to other facilities. The simulation result of case E and case F is shown in Fig 5-11 and Fig 5-12 respectively. The photovoltaic system that connected to DC network with the voltage does not regulate to the rated voltage 380Vdc can cause the photovoltaic system does not perform maximum power harvested from the renewable energy source.

Fig 5-11. The simulation result of case E with the sequence connection is photovoltaic system, grid interfacing system, battery system: a) DC bus voltage and b) DC bus current

Fig 5-12. The simulation result of case F with the sequence connection is photovoltaic system, battery system, grid interfacing system: a) DC bus voltage and b) DC bus current

In a comparison of all the system recovery cases, case A and case B are the suggested reconnection sequence of facilities due to low transient DC voltage and current in the DC network than other sequences. Case A and case B system recovery sequence can realize a stable DC voltage. Hence, the assumption made with the proposed reconnection sequence of the facilities back the DC system is valid and can use as a reference for fault recovery.

5.4 Conclusion

A novel of fault recovery of the DC system facilities is presented. The fault recovery covers the reconfiguration step of reclose DC circuit breaker and deblock power converter, the comparison of simultaneous connection and sequential connection of the facilities to the DC network, and the priority of reconnecting individual facility to the DC network. The DC system facilities include grid interfacing system, storage system, and photovoltaic system. Each facility assigns an appropriate power converter to serve the DC system. The chosen of the power converter is based on the common seen in the literature review. The reconfiguration step of reclosing DC circuit breaker after deblocking the power converter for the grid interfacing system can

reduce the inrush current within the power converter upon initialization stage. The reconfiguration step of recloses the DC circuit breaker prior to deblocking the battery and photovoltaic system can achieve a more stable DC voltage that has a result of preventing the high overshoot voltage and current to the DC network. The preference of the sequential connection of the facilities back to the DC system than the simultaneous connection is due to less transient voltage and current in the DC network. For the facilities recovery sequence, the grid interfacing system is the first connecting facilities can achieve the least transient voltage and current. In overall, the fault recovery can achieve a more stable voltage and current for the DC system.

Chapter 6. Conclusion and Future Work

6.1 Conclusion

This thesis demonstrates the entire fault tolerance process methodology. The fault tolerance process covers the fault detection, fault isolation, fault identification, and fault recovery.

The T-source circuit breaker accomplishes the fault detection and fault isolation. The T-source circuit breaker pre-tripping and post-tripping modelings are introduced. The pre-tripping model is used as a tool to determine the circuit breaker capacitor with respect to various load capacitor condition. The post-tripping model and the circuit breaker current rating is used as a reference to determine the transformer inductance. The redesign of the T-source circuit breaker component parameter can achieve a smaller size, ensure the tripping operation at the fault state, and has a lower output surge fault current as compared to the previous design T-source circuit breaker in the literature. Consequently, the introduced T-source circuit breaker design has a rapid fault current interruption that can reduce high magnitude fault current propagates from source to the DC system. In addition, the modification circuit introduced for the T-source circuit breaker has a benefit of internal SCR device protection.

The fault identification is a bridge step in between the source interruption and system recovery. This step identifies the fault segment and location, then isolate the fault segment for the non-fault section to continue operation. An accurate fault identification has a benefit of facilitating the maintenance task, reduce the repair cost, and speed up the restoration process. A probe power unit carries out as the fault location identification due to the advantages of good accuracy and applicable in offline mode where the source has completely interrupted in the system. An improvement with more precise fault distance and less computation are achieved by using the proposed logarithm decrement technique to obtain the decay constant. For a wider fault resistance range of fault distance measurement, the changing of the LC pair in the probe power unit is based on the peak deviation tolerance and the maximum detectable fault resistance. The peak deviation tolerance determines the Q-factor. The parallel probe power unit by adding a current probing at each terminal and the parallel fault identification flow was introduced. The parallel probe power unit and the parallel

fault identification flow can be used identifying the fault for a complex network such as a ring network or a meshed network.

The system recovery reboots entirely or partially system back to normal operation without an outage of the whole system. A least transient DC voltage and DC current are the goals of fault recovery in term of stability. The commonly seen facilities in the DC distribution system are grid interfacing system, storage system, and photovoltaic system. Each facility has two components as the bridge to the DC system. The bridge components are the power converter and the DC circuit breaker. Various power converters are used due to each facility function differently. With such a different power converter for each facility and the DC circuit breaker placement at the DC network, the reconfiguration step of the bridge component to the system for various facilities are different. For the grid interfacing system, the power converter is recommended to deblock before reclosing the DC circuit breaker. For the photovoltaic system and the battery system, the power converter must enable after the reclose of DC circuit breaker to avoid overcharging the smoothing capacitor and prevent the large overshoot current happen. The sequential connection of facilities shows a less current transient than simultaneous connection. For the system recovery with a stable voltage, the sequences of reconnection facilities back to the DC system are 1) grid interfacing system, 2) storage system, 3) photovoltaic system.

In overall, a robust and resilience DC system will be achieved with the fault tolerance and protective scheme introduced for each stage. The scheme provides a 'self-healing' action with the continuous operation when facing a fault condition in the DC system.

6.2 Future work

6.2.1 Circuit Breaker Tripping Characteristic at Different Location

Fig 3-21 shows the T-source circuit breaker can achieve an automated breaking for any fault event in the DC system. All the circuit breakers trip at the same time regardless of the fault location. The same time tripping is due to the same type of design for the T-source circuit breaker are used in the DC system.

However, the load terminal fault must not affect the DC system, and the downstream circuit breaker(load terminal) should have tripped priory to the upstream circuit breaker(source terminal) as illustrated in Fig 6-1. This action can assure continuous operation of the DC system. As such, the source and load terminal circuit

breaker require a different current rating circuit breaker design. The current rating of the source terminal circuit breaker should be larger than the load terminal circuit breaker. The determination of the circuit breaker current rating was presented in [100] and can be used as the reference the for the circuit breaker design in the future. For such current rating design of circuit breaker in the DC system, the load fault would not need to interrupt the power source service such as grid interfacing system, storage system, and the distributed generation system to the DC system.

Fig 6-1. The tripping characteristic of DC circuit breaker at a different location

6.2.2 Power converter Internal Fault

There is a high number of power converters in the DC microgrid system. Redundant converter for each facility is the option to increase system reliability. However, this option increase system complexity and is not economical. A second option to improve the reliability is to develop fault protection within power converters in DC distribution systems. Internal faults have much more concern due to many different components in the power converter. The cause of internal defects is either due to the power switch or component degradation or due to overcurrent experienced from the power system. The fault protection ability should also be integrated into the power converter to mitigate these faults. A fault identification technique was proposed in [101] using the wavelet decomposition analysis. Alternatively, a polar plot associated with fuzzy logic can recognize the fault type and the fault location of power converter[102]. The introduction of fault protection scheme into the power converters can increase overall system reliability and availability with the elimination of redundant converter.

APPENDIX

A.1 Simulation data of the peak currents and damping frequency using TABLE 4-I

R_f d_f	0.5		1		1.5		2	
	Ip1	T1	Ip1	T1	Ip1	T1	Ip1	T1
0.5	14.3956	0.000269	13.6126	0.000262	12.9039	0.000257	12.2598	0.000251
1	12.1164	0.000321	11.5578	0.000315	11.0443	0.000309	10.571	0.000303
1.5	10.658	0.000366	10.2237	0.00036	9.8206	0.000354	9.4456	0.000348
2	9.6215	0.000406	9.2664	0.0004	8.9344	0.000394	8.6234	0.000388
2.5	8.8357	0.000443	8.5354	0.000436	8.2531	0.00043	7.9874	0.000424
3	8.2132	0.000476	7.9532	0.00047	7.7077	0.000464	7.4757	0.000458

R_f d_f	0.5		1		1.5		2	
	Ip2	T2	Ip2	T2	Ip2	T2	Ip2	T2
0.5	10.9783	0.001373	8.1417	0.001369	6.039	0.001368	4.47386	0.001368
1	9.4219	0.001639	7.3338	0.001635	5.7104	0.001633	4.4443	0.001633
1.5	8.365	0.001868	6.7133	0.001864	5.3897	0.001861	4.3262	0.00186
2	7.5848	0.002071	6.2198	0.002067	5.1022	0.002064	4.1853	0.002063
2.5	6.9773	0.002256	5.8154	0.002252	4.8485	0.002249	4.0425	0.002248
3	6.4864	0.002427	5.476	0.002423	4.6244	0.00242	3.9054	0.002418

R_f d_f	0.5		1		1.5		2	
	Ip3	T3	Ip3	T3	Ip3	T3	Ip3	T3
0.5	8.3722	0.002477	4.8686	0.002476	2.8262	0.002479	1.6326	0.002486
1	7.3266	0.002957	4.6536	0.002956	2.9525	0.002957	1.8685	0.002963
1.5	6.5653	0.003369	4.4082	0.003367	2.9579	0.003368	1.9815	0.003372
2	5.9792	0.003736	4.1749	0.003734	2.9138	0.003734	2.0313	0.003738
2.5	5.5098	0.00407	3.9622	0.004068	2.8484	0.004068	2.0459	0.004071
3	5.1226	0.004379	3.7704	0.004377	2.7744	0.004377	2.0402	0.004379

R_f d_f	0.5		1		1.5		2	
	Ip4	T4	Ip4	T4	Ip4	T4	Ip4	T4
0.5	6.3847	0.003581	2.9125	0.003583	1.3226	0.003591	0.5958	0.003603
1	5.6973	0.004275	2.9529	0.004276	1.5266	0.004281	0.7855	0.004291
1.5	5.1528	0.004871	2.8946	0.004871	1.6233	0.004876	0.9075	0.004884
2	4.7135	0.005401	2.8023	0.005401	1.664	0.005405	0.9858	0.005412
2.5	4.3509	0.005884	2.6996	0.005884	1.6734	0.005887	1.0355	0.005894
3	4.0455	0.00633	5.596	0.00633	1.6646	0.006333	1.0658	0.006339

R_f d_f	0.5		1		1.5		2	
	Ip5	T5	Ip5	T5	Ip5	T5	Ip5	T5
0.5	4.8691	0.004686	1.742	0.00469	0.619	0.004702	0.2174	0.004721
1	4.4303	0.005593	1.8737	0.005596	0.7893	0.005606	0.3303	0.005621
1.5	4.0442	0.006372	1.9007	0.006375	0.8909	0.006383	0.4157	0.006369
2	3.7158	0.007066	1.881	0.007068	0.9503	0.007076	0.4785	0.007087
2.5	3.4358	0.007698	1.8393	0.0077	0.9831	0.007706	0.5241	0.007717
3	3.1949	0.008281	1.7874	0.008283	0.9987	0.008289	0.5568	0.008299

R_f d_f	wd							
	0.5		1		1.5		2	
0.5	5689.6		5675.93		5653.756		5622.98	
1	4767.35		4758.71		4745.09		4726.43	
1.5	4184.55		4178.31		4168.69		4155.69	
2	3773.73		3768.86		3761.51		3751.69	
2.5	3464.14		3460.14		3454.23		3446.4	
3	3220.03		3216.64		3211.7		3205.24	

A.2 Simulation data of the peak currents and damping frequency using

TABLE 4-IV

$\frac{R_f}{d_f}$	Ip1			
	0.1	1	10	100
0.01	0.4814	0.4798	0.4641	0.3464
0.1	0.4767	0.4751	0.4595	0.344
1	0.4353	0.4339	0.4209	0.3221
10	0.2665	0.266	0.2611	0.2197
100	0.0984	0.0983	0.0977	0.0913

$\frac{R_f}{d_f}$	Ip2			
	0.1	1	10	100
0.01	0.4807	0.4726	0.399	0.0729
0.1	0.4758	0.4678	0.3955	0.0735
1	0.4339	0.4273	0.3665	0.0791
10	0.2636	0.2611	0.2376	0.0932
100	0.0947	0.0944	0.0912	0.0643

$\frac{R_f}{d_f}$	wd			
	0.1	1	10	100
0.01	48171.06	48170.91	48157.1	46751.56
0.1	47690.52	47690.37	47676.97	46313.21
1	43561.62	43561.49	43551.07	42512.5
10	26726.4	26726.32	26723.46	26480.75
100	9935.46	9935.44	9935.05	9920.23

B.1 Grid Interfacing Converter Component Parameter Derivation

The AC voltage from the grid is 230Vrms with frequency is 50Hz. The power rating of the single-phase PWM rectifier is 5KW and output voltage regulated at 380Vdc. The variation of the output voltage and inductor current is 1% and 5% respectively. The switching frequency is assumed 20kHz.

Using the second harmonic ripple power as shown in [103], the output smoothing capacitance with 1% of ripple output voltage variation is obtained as:

$$C = \frac{P_o}{2\omega V_o \Delta V_o} = 5.51\text{mF} \quad (\text{B.1})$$

However, the grid interfacing system is defined as the slack bus of the DC microgrid. It is required to be able to hold-up a short-term voltage sag at the grid. Typically, 10 AC cycle of hold up time to prevent outage of the DC system. For a minimum withstand voltage 200Vdc. The output capacitance is obtained as:

$$C = \frac{2P_o t_{\text{hold}}}{V_{o,\text{max}}^2 - V_{o,\text{min}}^2} = 19.15\text{mF} \quad (\text{B.2})$$

The input inductance with 5% variation is obtained as:

$$L = \frac{V_o}{4\Delta i_L f_{\text{sw}}} = 3.09\text{mH} \quad (\text{B.3})$$

B.2 Battery Interfacing Converter Component Parameter Derivation

The battery nominal voltage is 200Vdc with the full charged voltage is 230Vdc. The nominal discharging current is 18Vdc, and the maximum discharging power can reach 4140W. The synchronous boost converter is chosen as the battery interfacing converter, and the power rating is set to 5kW. The output terminal of the synchronous boost converter is connected to the DC system with 380Vdc. The switching frequency is set to 10kHz. The output voltage and input current variation are set to 0.1% and 5% respectively.

Based on the boost converter capacitance energy equation, the output smoothing capacitor with 1% variation output voltage is obtained as:

$$C = \frac{P_{o,max}D}{2V_o\Delta V_o f_s} = 820\mu F \quad (B.4)$$

Based on the boost converter input inductor turn-on state equation, the inductance with 5% variation input current is obtained as:

$$L = \frac{V_{in,nom}D}{2\Delta i_L f_s} = 3.79mH \quad (B.5)$$

However, for the boost converter to operate in a continuous current mode at light load condition with 100W, the minimum input inductance is shown as:

$$L_{min} = \frac{2}{27} \frac{V_o^2}{P_{o,max}f_s} = 10.7mF \quad (B.6)$$

B.3 Photovoltaic Interfacing Converter Component Parameter Derivation

An example of photovoltaic cell current-voltage and power-voltage characteristics are shown in Fig B-1. The maximum power generation based on this characteristic curve is 5kW of power generation at 210Vdc. This voltage is the photovoltaic cell voltage. It is regulated and feeds into the DC-DC boost converter input terminal. The output terminal is connected to the DC microgrid system with a constant voltage 380Vdc. The switching frequency is assumed 10kHz. The maximum variation of the inductor current and capacitor voltage is 5% and 1% respectively.

Fig B-1. The Photovoltaic Cell voltage-current and voltage-power Characteristic

Based on the boost converter capacitance energy equation, the output smoothing capacitor with 0.1% variation output voltage is obtained as:

$$C = \frac{P_{o,max} D}{2V_o \Delta V_o f_s} = 774 \mu F \quad (B.7)$$

Based on the boost converter input inductor turn-on state equation, the inductance with 5% variation input current is obtained as:

$$L = \frac{V_{in} D}{2\Delta i_L f_s} = 3.95 mH \quad (B.8)$$

However, for the boost converter operates in a continuous current mode at light load condition with 500W, the minimum input inductance is shown as:

$$L_{min} = \frac{2}{27} \frac{V_o^2}{P_{o,light} f_s} = 10.7 mF \quad (B.9)$$

Reference

- [1] G. S. Seo, J. Baek, K. Choi, H. Bae, and B. Cho, "Modeling and analysis of DC distribution systems," in 8th International Conference on Power Electronics - ECCE Asia, 2011, pp. 223-227.
- [2] D. J. Hammerstrom, "AC Versus DC Distribution Systems Did We Get it Right?," in 2007 IEEE Power Engineering Society General Meeting, 2007, pp. 1-5.
- [3] D. J. Becker and B. J. Sonnenberg, "DC microgrids in buildings and data centers," in 2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC), 2011, pp. 1-7.
- [4] J. Inamori, T. T. Hidekazu Hoshi, T. Babasaki, and K. Hirose, "380-VDC power distribution system for 4-MW-scale cloud facility," 2014 IEEE 36th International Telecommunications Energy Conference (INTELEC), 2014.
- [5] D. E. Geary, D. P. Mohr, D. Owen, M. Salato, and B. J. Sonnenberg, "380V DC eco-system development present status and future challenges," Intelec 2013; 35th International Telecommunications Energy Conference, SMART POWER AND EFFICIENCY, 13-17 Oct. 2013 2013.
- [6] D. Van Hertem and M. Ghandhari, "Multi-terminal VSC HVDC for the European supergrid: Obstacles," Renewable and Sustainable Energy Reviews, vol. 14, pp. 3156-3163, 2010/12/01/ 2010.
- [7] W. Leterme, N. Ahmed, J. Beerten, L. Angquist, D. V. Hertem, and S. Norrga, "A new HVDC grid test system for HVDC grid dynamics and protection studies in EMT-type software," in 11th IET International Conference on AC and DC Power Transmission, 2015, pp. 1-7.
- [8] W. Leterme, J. Beerten, and D. V. Hertem, "Nonunit Protection of HVDC Grids With Inductive DC Cable Termination," IEEE Transactions on Power Delivery, vol. 31, pp. 820-828, 2016.
- [9] D. Salomonsson, L. Soder, and A. Sannino, "Protection of Low-Voltage DC Microgrids," IEEE Transactions on Power Delivery, vol. 24, pp. 1045-1053, 2009.
- [10] J. C. Das and R. H. Osman, "Grounding of AC and DC low-voltage and medium-voltage drive systems," IEEE Transactions on Industry Applications, vol. 34, pp. 205-216, 1998.
- [11] M. G. Jahromi, G. Mirzaeva, S. D. Mitchell, and D. Gay, "Advanced fault tolerance strategy for DC microgrids in mining excavators," in 2015 IEEE 24th International Symposium on Industrial Electronics (ISIE), 2015, pp. 1502-1507.
- [12] K. J. Tseng and G. Luo, "Power electronic-based protection for direct-current power distribution in micro-grids," in 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), 2014, pp. 2145-2151.
- [13] J. D. Park, J. Candelaria, L. Ma, and K. Dunn, "DC Ring-Bus Microgrid Fault Protection and Identification of Fault Location," IEEE Transactions on Power Delivery, vol. 28, pp. 2574-2584, 2013.

- [14] L. Fang, C. Jian, L. Xinchun, K. Yong, and D. Shanxu, "A novel solid state fault current limiter for DC power distribution network," in 2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, 2008, pp. 1284-1289.
- [15] S. Chen, P. Li, R. Ball, J. F. d. Palma, and B. Lehman, "Analysis of a Switched Impedance Transformer-Type Nonsuperconducting Fault Current Limiter," IEEE Transactions on Power Electronics, vol. 30, pp. 1925-1936, 2015.
- [16] U. Ghisla, I. Kondratiev, and R. A. Dougal, "Branch circuit protection for DC systems," in 2011 IEEE Electric Ship Technologies Symposium, 2011, pp. 234-239.
- [17] W. Sanusi, M. A. Hosani, and M. S. E. Moursi, "A Novel DC Fault Ride-Through Scheme for MTDC Networks Connecting Large-Scale Wind Parks," IEEE Transactions on Sustainable Energy, vol. 8, pp. 1086-1095, 2017.
- [18] L. Tang and B. T. Ooi, "Locating and Isolating DC Faults in Multi-Terminal DC Systems," IEEE Transactions on Power Delivery, vol. 22, pp. 1877-1884, 2007.
- [19] R. Dantas, J. Liang, C. E. Ugalde-Loo, A. Adamczyk, C. Barker, and R. Whitehouse, "Progressive Fault Isolation and Grid Restoration Strategy for MTDC Networks," IEEE Transactions on Power Delivery, vol. PP, pp. 1-1, 2017.
- [20] P. Wang, X.-P. Zhang, P. F. Coventry, R. Zhang, and Z. Li, "Control and protection sequence for recovery and reconfiguration of an offshore integrated MMC multi-terminal HVDC system under DC faults," International Journal of Electrical Power & Energy Systems, vol. 86, pp. 81-92, 2017/03/01/ 2017.
- [21] J. Zyborski, T. Lipski, J. Czucha, and S. Hasan, "Hybrid arcless low-voltage AC/DC current limiting interrupting device," IEEE Transactions on Power Delivery, vol. 15, pp. 1182-1187, 2000.
- [22] L. Novello, E. Gaio, and R. Piovan, "Feasibility Study of a Hybrid Mechanical-Static DC Circuit Breaker for Superconducting Magnet Protection," IEEE Transactions on Applied Superconductivity, vol. 19, pp. 76-83, 2009.
- [23] S. Roy, D. Kanabar, C. Dodiya, and S. Pradhan, "Development of a Prototype Hybrid DC Circuit Breaker for Superconducting Magnets Quench Protection," IEEE Transactions on Applied Superconductivity, vol. 24, pp. 1-6, 2014.
- [24] A. Maistrello, E. Gaio, A. Ferro, M. Perna, C. Panizza, F. Soso, et al., "Experimental Qualification of the Hybrid Circuit Breaker Developed for JT-60SA Quench Protection Circuit," IEEE Transactions on Applied Superconductivity, vol. 24, pp. 1-5, 2014.
- [25] L. Liu, J. Zhuang, C. Wang, Z. Jiang, J. Wu, and B. Chen, "A Hybrid DC Vacuum Circuit Breaker for Medium Voltage: Principle and First Measurements," IEEE Transactions on Power Delivery, vol. 30, pp. 2096-2101, 2015.
- [26] P. Meckler, F. Gerdinand, R. Weiss, U. Boeke, and A. Mauder, "Hybrid switches in protective devices for low-voltage DC grids at commercial used buildings," in ICEC 2014; The 27th International Conference on Electrical Contacts, 2014, pp. 1-6.
- [27] W. Lin, D. Jovcic, S. Nguéfeu, and H. Saad, "Modelling of high-power hybrid DC circuit breaker for grid-level studies," IET Power Electronics, vol. 9, pp. 237-246, 2016.

- [28] F. Lei, G. Ruifeng, Z. Fang, Y. Xiaoping, and Z. Fan, "Development of a 10kV solid-state DC circuit breaker based on press-pack IGBT for VSC-HVDC system," in 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016, pp. 2371-2377.
- [29] K. Sano and M. Takasaki, "A Surgeless Solid-State DC Circuit Breaker for Voltage-Source-Converter-Based HVDC Systems," IEEE Transactions on Industry Applications, vol. 50, pp. 2690-2699, 2014.
- [30] A. Mokhberdoran, A. Carvalho, N. Silva, H. Leite, and A. Carrapatoso, "A new topology of fast solid-state HVDC circuit breaker for offshore wind integration applications," in 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), 2015, pp. 1-10.
- [31] M. Kempkes, I. Roth, and M. Gaudreau, "Solid-state circuit breakers for Medium Voltage DC power," in 2011 IEEE Electric Ship Technologies Symposium, 2011, pp. 254-257.
- [32] E. L. Wellner and A. R. Bendre, "IGCTs vs. IGBTs for circuit breakers in advanced ship electrical systems," in 2009 IEEE Electric Ship Technologies Symposium, 2009, pp. 400-405.
- [33] K. A. Corzine and R. W. Ashton, "A New Z-Source DC Circuit Breaker," IEEE Transactions on Power Electronics, vol. 27, pp. 2796-2804, 2012.
- [34] P. Prempraneerach, M. G. Angle, J. L. Kirtley, G. E. Karniadakis, and C. Chrysostomidis, "Optimization of a z-source DC circuit breaker," in 2013 IEEE Electric Ship Technologies Symposium (ESTS), 2013, pp. 480-486.
- [35] A. H. Chang, B. R. Sennett, A. T. Avestruz, S. B. Leeb, and J. L. Kirtley, "Analysis and Design of DC System Protection Using Z-Source Circuit Breaker," IEEE Transactions on Power Electronics, vol. 31, pp. 1036-1049, 2016.
- [36] K. A. Corzine, "A New-Coupled-Inductor Circuit Breaker for DC Applications," IEEE Transactions on Power Electronics, vol. 32, pp. 1411-1418, 2017.
- [37] L. Changle, N. Ziling, L. Huayu, and Z. Yinfeng, "A novel solid-state protection scheme for DC system," in 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016, pp. 2039-2042.
- [38] L. Ying-Hong, L. Chih-Wen, and Y. Chi-Shan, "A new fault locator for three-terminal transmission lines using two-terminal synchronized voltage and current phasors," IEEE Transactions on Power Delivery, vol. 17, pp. 452-459, 2002.
- [39] M. Venugopal and C. Tiwari, "A novel algorithm to determine fault location in a transmission line using PMU measurements," in 2013 IEEE International Conference on Smart Instrumentation, Measurement and Applications (ICSIMA), 2013, pp. 1-4.
- [40] L. Kai-Ping, L. Chih-Wen, J. A. Jiang, C. Ching-Shan, and Y. Chi-Shan, "A novel fault location algorithm for multi-terminal lines using phasor measurement units," in Proceedings of the 37th Annual North American Power Symposium, 2005., 2005, pp. 576-581.

- [41] J. Joe-Air, Y. Jun-Zhe, L. Ying-Hong, L. Chih-Wen, and M. Jih-Chen, "An adaptive PMU based fault detection/location technique for transmission lines. I. Theory and algorithms," *IEEE Transactions on Power Delivery*, vol. 15, pp. 486-493, 2000.
- [42] S. M. Brahma, "Fault location scheme for a multi-terminal transmission line using synchronized Voltage measurements," *IEEE Transactions on Power Delivery*, vol. 20, pp. 1325-1331, 2005.
- [43] A. Borghetti, M. Bosetti, C. A. Nucci, M. Paolone, and A. Abur, "Integrated Use of Time-Frequency Wavelet Decompositions for Fault Location in Distribution Networks: Theory and Experimental Validation," *IEEE Transactions on Power Delivery*, vol. 25, pp. 3139-3146, 2010.
- [44] S. Azizi, M. Sanaye-Pasand, M. Abedini, and A. Hasani, "A Traveling-Wave-Based Methodology for Wide-Area Fault Location in Multiterminal DC Systems," *IEEE Transactions on Power Delivery*, vol. 29, pp. 2552-2560, 2014.
- [45] P. Jafarian and M. Sanaye-Pasand, "A Traveling-Wave-Based Protection Technique Using Wavelet/PCA Analysis," *IEEE Transactions on Power Delivery*, vol. 25, pp. 588-599, 2010.
- [46] D. Spoor and Z. Jian Guo, "Improved single-ended traveling-wave fault-location algorithm based on experience with conventional substation transducers," *IEEE Transactions on Power Delivery*, vol. 21, pp. 1714-1720, 2006.
- [47] Z. Y. He, K. Liao, X. P. Li, S. Lin, J. W. Yang, and R. K. Mai, "Natural Frequency-Based Line Fault Location in HVDC Lines," *IEEE Transactions on Power Delivery*, vol. 29, pp. 851-859, 2014.
- [48] H. Livani and C. Y. Evrenosoglu, "A Machine Learning and Wavelet-Based Fault Location Method for Hybrid Transmission Lines," *IEEE Transactions on Smart Grid*, vol. 5, pp. 51-59, 2014.
- [49] O. M. K. K. Nanayakkara, A. D. Rajapakse, and R. Wachal, "Location of DC Line Faults in Conventional HVDC Systems With Segments of Cables and Overhead Lines Using Terminal Measurements," *IEEE Transactions on Power Delivery*, vol. 27, pp. 279-288, 2012.
- [50] D. Tzelepis, G. Fusiek, A. Dyśko, P. Niewczas, C. Booth, and X. Dong, "Novel Fault Location in MTDC Grids with Non-Homogeneous Transmission Lines Utilizing Distributed Current Sensing Technology," *IEEE Transactions on Smart Grid*, pp. 1-1, 2017.
- [51] D. Tzelepis, A. Dyśko, G. Fusiek, P. Niewczas, S. Mirsaedi, C. Booth, et al., "Advanced fault location in MTDC networks utilising optically-multiplexed current measurements and machine learning approach," *International Journal of Electrical Power & Energy Systems*, vol. 97, pp. 319-333, 2018/04/01/ 2018.
- [52] Z. He, J. Zhang, W. h. Li, and X. Lin, "Improved Fault-Location System for Railway Distribution System Using Superimposed Signal," *IEEE Transactions on Power Delivery*, vol. 25, pp. 1899-1911, 2010.

- [53] B. Yong, C. Wei, L. Jiansheng, D. Lei, L. Qingdong, and Y. Ning, "Single phase to earth fault location method in distribution network based on signal injection principle," in 2011 4th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), 2011, pp. 204-208.
- [54] P. Toman, J. Orsigova, and D. Topolaneck, "Location of the Earth Faults in MV Compensated Networks," in 2008 IET 9th International Conference on Developments in Power System Protection (DPSP 2008), 2008, pp. 327-331.
- [55] A. Dán and D. Raisz, "Comparison of different methods for earth fault location in compensated networks," in Proceedings of the 2010 Electric Power Quality and Supply Reliability Conference, 2010, pp. 237-242.
- [56] G. Y. Kwon, C. K. Lee, G. S. Lee, Y. H. Lee, S. J. Chang, C. K. Jung, et al., "Offline Fault Localization Technique on HVDC Submarine Cable via Time–Frequency Domain Reflectometry," IEEE Transactions on Power Delivery, vol. 32, pp. 1626-1635, 2017.
- [57] P. Wang, Z. Li, X. P. Zhang, R. Zhang, and P. F. Coventry, "DC fault management for VSC MTDC system using delayed-auto-re-configuration scheme," in 11th IET International Conference on AC and DC Power Transmission, 2015, pp. 1-7.
- [58] R. Mohanty, U. S. M. Balaji, and A. K. Pradhan, "An Accurate Noniterative Fault-Location Technique for Low-Voltage DC Microgrid," IEEE Transactions on Power Delivery, vol. 31, pp. 475-481, 2016.
- [59] W. Wen, Y. Wang, B. Li, Y. Huang, R. Li, and Q. Wang, "Transient Current Interruption Characteristics of a Novel Mechanical DC Circuit Breaker," IEEE Transactions on Power Electronics, pp. 1-1, 2018.
- [60] W. Lin, D. Jovcic, S. Nguéfeu, and H. Saad, "Modelling of high power mechanical DC circuit breaker," in 2015 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), 2015, pp. 1-5.
- [61] D. E. Geary, D. P. Mohr, D. Owen, M. Salato, and B. J. Sonnenberg, "380V DC eco-system development: present status and future challenges," in Intelc 2013; 35th International Telecommunications Energy Conference, SMART POWER AND EFFICIENCY, 2013, pp. 1-6.
- [62] T. Liangyi, W. Bin, V. Yaramasu, C. Weirong, and H. S. Athab, "Fast acting DC circuit breaker for HVDC transmission line based on DC/DC chopper," in 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), 2014, pp. 3695-3701.
- [63] M. E. Baran and N. R. Mahajan, "Overcurrent Protection on Voltage-Source-Converter-Based Multiterminal DC Distribution Systems," IEEE Transactions on Power Delivery, vol. 22, pp. 406-412, 2007.
- [64] J. Yang, J. Zheng, G. Tang, and Z. He, "Characteristics and Recovery Performance of VSC-HVDC DC Transmission Line Fault," in 2010 Asia-Pacific Power and Energy Engineering Conference, 2010, pp. 1-4.

- [65] X. Zhenxue, Z. Bin, S. Sirisukprasert, Z. Xigen, and A. Q. Huang, "The emitter turn-off thyristor-based DC circuit breaker," in 2002 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No.02CH37309), 2002, pp. 288-293 vol.1.
- [66] A. Shukla and G. D. Demetriades, "A Survey on Hybrid Circuit-Breaker Topologies," IEEE Transactions on Power Delivery, vol. 30, pp. 627-641, 2015.
- [67] Y. Sato, Y. Tanaka, A. Fukui, M. Yamasaki, and H. Ohashi, "SiC-SIT Circuit Breakers With Controllable Interruption Voltage for 400-V DC Distribution Systems," IEEE Transactions on Power Electronics, vol. 29, pp. 2597-2605, 2014.
- [68] Z. J. Shen, G. Sabui, Z. Miao, and Z. Shuai, "Wide-Bandgap Solid-State Circuit Breakers for DC Power Systems: Device and Circuit Considerations," IEEE Transactions on Electron Devices, vol. 62, pp. 294-300, 2015.
- [69] Z. Miao, G. Sabui, A. M. Roshandeh, and Z. J. Shen, "Design and Analysis of DC Solid-State Circuit Breakers Using SiC JFETs," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, pp. 863-873, 2016.
- [70] H. Iwamoto, K. Satoh, M. Yamamoto, and A. Kawakami, "High-power semiconductor device: a symmetric gate commutated turn-off thyristor," IEE Proceedings - Electric Power Applications, vol. 148, pp. 363-368, 2001.
- [71] P. Steimer, O. Apeldoorn, E. Carroll, and A. Nagel, "IGCT technology baseline and future opportunities," in 2001 IEEE/PES Transmission and Distribution Conference and Exposition. Developing New Perspectives (Cat. No.01CH37294), 2001, pp. 1182-1187 vol.2.
- [72] U. Vemulapati, M. Arnold, M. Rahimo, A. Antoniazzi, and D. Pessina, "Reverse blocking IGCT optimised for 1 kV DC bi-directional solid state circuit breaker," IET Power Electronics, vol. 8, pp. 2308-2314, 2015.
- [73] A. Mokhberdoran, A. Carvalho, H. Leite, and N. Silva, "A review on HVDC circuit breakers," in 3rd Renewable Power Generation Conference (RPG 2014), 2014, pp. 1-6.
- [74] Y. Li, H. Gao, Q. Du, X. Qi, Q. Pang, and G. Zhu, "A review of single-phase-to-ground fault location methods in distribution networks," in 2011 4th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), 2011, pp. 938-943.
- [75] D. Raisz and J. Gönczi, "Fault location methods at compensated MV networks," in 2014 49th International Universities Power Engineering Conference (UPEC), 2014, pp. 1-5.
- [76] T. Bharat and D. Reddy, "Recovery of HVDC system after fault with reactive power injection.," J Electrical Electron Eng Res. , 2013.
- [77] N. Sato, N. Honjo, K. Yamaji, T. Yoshino, and J. Arai, "HVDC converter control for fast power recovery after AC system fault," IEEE Transactions on Power Delivery, vol. 12, pp. 1319-1326, 1997.

- [78] E. Kontos, R. T. Pinto, and P. Bauer, "Providing dc fault ride-through capability to H-bridge MMC-based HVDC networks," in 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015, pp. 1542-1551.
- [79] P. C. Loh and F. Blaabjerg, "Magnetically Coupled Impedance-Source Inverters," IEEE Transactions on Industry Applications, vol. 49, pp. 2177-2187, 2013.
- [80] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-Source Networks for Electric Power Conversion Part I: A Topological Review," IEEE Transactions on Power Electronics, vol. 30, pp. 699-716, 2015.
- [81] W. Qian, F. Z. Peng, and H. Cha, "Trans-Z-Source Inverters," IEEE Transactions on Power Electronics, vol. 26, pp. 3453-3463, 2011.
- [82] R. K. Behera and S. K. Parida, "DC Microgrid Management Using Power Electronics Converter.pdf," 2014 Eighteenth National Power Systems Conference (NPSC), Guwahati, pp. pp. 1-6, 2014.
- [83] M.-H. Ryu, H.-S. Kim, J.-W. Baek, H.-G. Kim, and J.-H. Jung, "Effective Test Bed of 380-V DC Distribution System Using Isolated Power Converters," IEEE Transactions on Industrial Electronics, vol. 62, pp. 4525-4536, 2015.
- [84] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active Power Decoupling for High-Power Single-Phase PWM Rectifiers," IEEE Transactions on Power Electronics, vol. 28, pp. 1308-1319, 2013.
- [85] H. Wu, S. C. Wong, C. K. Tse, and Q. Chen, "Control and Modulation of Bidirectional Single-Phase AC–DC Three-Phase-Leg SPWM Converters With Active Power Decoupling and Minimal Storage Capacitance," IEEE Transactions on Power Electronics, vol. 31, pp. 4226-4240, 2016.
- [86] S. Somkun and V. Chunkag, "Simple and fast synchronous reference frame current control for single-phase grid-connected voltage source converters," in IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, 2015, pp. 002276-002281.
- [87] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," IEEE Transactions on Power Electronics, vol. 29, pp. 4091-4106, 2014.
- [88] L. N. Rao and S. Gairola, "A comparative study of Bidirectional DC-DC converter & its interfacing with two battery storage system," 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, pp. pp. 1-6, 2016.
- [89] V. V. S. K. Bhajana and P. Drabek, "A novel ZCS non-isolated bidirectional buck-boost DC-DC converter for energy storage applications," 2015 IEEE 24th International Symposium on Industrial Electronics (ISIE), Buzios, 2015, pp. pp. 1224-1229, 2015.
- [90] R. Singh, S. F. Taghizadeh, and N. M. L. Tan, "Battery energy storage system for PV output leveling based on bidirectional isolated DC-DC converter," pp. 84-89, 2013.
- [91] S. Talbi, A. M. Mabwe, and A. E. Hajjaji, "Control of a bidirectional dual active bridge converter for charge and discharge of a Li-Ion Battery," IECON 2015 - 41st Annual

Conference of the IEEE Industrial Electronics Society, Yokohama, pp. 000849-000856, 2015.

[92] R. T. Naayagi, A. J. Forsyth, and R. Shuttleworth, "High-Power Bidirectional DC-DC Converter for Aerospace Applications," IEEE Transactions on Power Electronics, vol. 27, pp. 4366-4379, 2012.

[93] Y. C. Jeung and D. C. Lee, "Sliding mode control of bidirectional dual active bridge DC-DC converters for battery energy storage systems," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, 3385-3390 2017.

[94] R. K. Behera and S. K. Parida, "DC microgrid management using power electronics converters," in 2014 Eighteenth National Power Systems Conference (NPSC), 2014, pp. 1-6.

[95] U. Sharma, B. Singh, and S. Kumar, "Intelligent grid interfaced solar water pumping system," IET Renewable Power Generation, vol. 11, pp. 614-624, 2017.

[96] P. Kumar, R. K. Pachauri, and Y. K. Chuahan, "Duty ratio control schemes of DC-DC boost converter integrated with solar PV system," in 2015 International Conference on Energy Economics and Environment (ICEEE), 2015, pp. 1-6.

[97] T. V. Thang, A. Ahmed, C. i. Kim, and J. H. Park, "Flexible System Architecture of Stand-Alone PV Power Generation With Energy Storage Device," IEEE Transactions on Energy Conversion, vol. 30, pp. 1386-1396, 2015.

[98] C. W. Chen, K. H. Chen, and Y. M. Chen, "Modeling and Controller Design of an Autonomous PV Module for DMPPT PV Systems," IEEE Transactions on Power Electronics, vol. 29, pp. 4723-4732, 2014.

[99] L. Song, L. Qin, H. Mao, H. Xuxu, and S. Xie, "Stable operating area of photovoltaic cells feeding the interface converter in output current regulation mode," in 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016, pp. 185-192.

[100] L. L. Qi, A. Antoniazzi, L. Raciti, and D. Leoni, "Design of Solid-State Circuit Breaker-Based Protection for DC Shipboard Power Systems," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, pp. 260-268, 2017.

[101] H. G. Yap and K. J. Tseng, "Wavelet based fault tolerance in grid interface system for DC power distribution network," in 2015 IEEE International Telecommunications Energy Conference (INTELEC), 2015, pp. 1-6.

[102] H. G. Yap and K. J. Tseng, "Towards a Fault-Tolerant grid interface system for DC power distribution networks in Green Buildings," in 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015, pp. 1796-1802.

[103] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, et al., "A High Power Density Single-Phase PWM Rectifier With Active Ripple Energy Storage," IEEE Transactions on Power Electronics, vol. 26, pp. 1430-1443, 2011.