Low-power high-performance SAR ADC with redundancy and digital error-correction

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**Low-Power High-Performance SAR ADC with
Redundancy and Digital Error-Correction**

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Summary

The demands for data converters have soared in the last decade with the boom in consumer electronics, smart devices, autonomous vehicles, and automotive segments. The current trend among Nyquist-rate data converters, for example successive approximation register (SAR) analog-to-digital converters (ADC), tends towards high speeds and medium-to-high resolution. Applications such as vehicle-to-everything (V2X) communication, wireless internet of things, test systems, etc., benefit from high-speed and high resolution ADCs. An in-depth analysis of data converter trends, and current state-of-the-art SAR ADCs are discussed. The topics discussed include data converters using binary and non-binary redundancy techniques, digital error correction schemes, DAC switching schemes, and associated hardware overheads.

This thesis focuses on six important contributions to high speed and medium resolution SAR ADC research. The first one is the introduction of binary-scaled redundancy embedded in the conventional capacitive DAC (CDAC), and the second is optimizing the use of redundancy by introducing a new CDAC switching scheme. The third contribution introduces a simple “bit overlap and add” digital error correction-technique for a 10-bit SAR ADC. Multiple erroneous decisions can be corrected over nine conversion cycles, independent of where the erroneous conversion cycle occurred. The implementation of the technique requires no additional conversion cycles to obtain a 10-bit resolution. Fourth, this thesis introduces a new area-efficient switching scheme for a multi-bit per cycle SAR ADC. The proposed constant common-mode fractional reference voltage (CCM-

FRV) switching scheme offers a 50% area reduction of each CDAC used when compared to a conventional switching scheme [1] modified to implement a similar redundancy and error correction concept. The implementation of the CCM-FRV switching scheme requires no special arithmetic units or additional hardware overheads to compute the DAC switching pattern, thus eliminating any speed bottlenecks due to logic delay. The fifth contribution introduces a low-energy and chip-area-efficient switching scheme for a 1.5-bit/cycle SAR ADC with digital error-correction. The proposed switching scheme reduces CDAC switching energy by 88.55%, along with a 75% CDAC area reduction when compared to a conventional switching scheme [1] implementing a similar 1.5-bit/cycle conversion. Finally, a “more than Moore” design and fabrication methodology is explored to compare III-V compound semiconductors (CS) and CMOS sampling switch performance.

The first four contributions are implemented using a 65 nm 1P9M mixed-signal RF CMOS technology. The test chip occupies a 0.038 mm² chip area and consumes 4.06 mW from a 1.2 V power supply. The prototype achieves Nyquist SNDR of 57.81 dB and an ENOB of 9.31 at 150 MS/s. The Walden figure of merit (FoM) is 42.6 fJ/conversion-step. The sixth contribution implements an on-chip fully integrated SAR ADC with III-V CS (i.e., InGaAs) sampling switch and remaining circuits in CMOS technology. The 6-bit 125 MSps SAR ADC occupies a 0.0225 mm² chip area, achieves a post-layout simulated peak SNDR of 35.56 dB/35.98 dB and an SFDR of 48.7 dB/53.17 dB for ADCs using a CMOS/InGaAs sampling switch. The ADC using an InGaAs sampling switch has a better SFDR

performance by 4.47 dB when compared to an ADC using a CMOS sampling switch for the given technology nodes.

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List of Abbreviations

ADC: Analog-to-digital converter

ADEC: Addition only digital error correction

CDAC: Capacitive digital-to-analog converter

CS: Compound semiconductor

CMOS: Complementary metal oxide semiconductor

CCM-FRV: Constant common mode fractional reference voltage

CP: Cyclic prefix

DAC: Digital-to-analog converter

DUT: Device under test

DNL: Differential non-linearity

DSRC: Dedicated short-range communications

EOC: End of conversion

ENOB: Effective number of bits

FA: Full Adder

FOM: Figure of merit

FFT: Fast fourier transform

HA: Half Adder

HEMT: High electron mobility transistor

INL: Integral non-linearity

INV: Inverter

IoT: Internet of things

ISSCC: International solid state circuits conference

LDO: Low dropout regulator

LSB: Least significant bit

LEES: Low energy electronics system

MU-MIMO: multiple-input, multiple-output

MSB: Most significant bit

MUX: Multiplexer

OFDMA: orthogonal frequency division multiple access

PVT: Process, voltage, and temperature

PLL: Phase locked loop

PSRR: Power supply rejection ratio

PEX: Parasitic extraction

PCB: Printed circuit board

PDK: Process development kit

QAM: Quadrature amplitude modulation

RF: Radio frequency

ROM: Read only memory

SoC: System-on-chip

SNR: Signal to noise ratio

SAR: Successive approximation register

SNDR: Signal to noise and distortion ratio

SFDR: Spurious free dynamic range

TSMC: Taiwan Semiconductor Manufacturing Corporation

TDC: Time to digital converter

UV: Ultraviolet

V2x: Vehicle-to-everything

VLSI: Very large scale integration

Chapter 1

Introduction

1.1 Motivation

The data converter is an essential building block of any electronic system and acts as an interface between the analog and digital worlds. Increasingly more research is being carried out on low-power, energy-efficient data converters for sensor, mobile-communication, and automotive applications. Advancements in transistor manufacturing nodes have benefited digital circuits both in terms of speed, area, and power consumption.

A recent boom in low-cost portable wireless communication systems has resulted in increased systems-on-chip (SoC) integration of digital, analog and radio-frequency circuits. This limits the power dissipation, chip area, and performance of sub-systems such as data converters with an 8–12-bit resolution operating at speeds greater than 100 MSps in a noisy SoC environment. Technology scaling offered by Moore’s law is not always beneficial, however, especially for analog circuits. Lower supply voltage, limited transistor headroom restricting signal swing, and lower transistor intrinsic gain and gate-oxide thickness make analog circuit design challenging. Thus necessitating new techniques to achieve the goal of low-power design.

SAR data converters are preferred over other Nyquist-rate data converters such as pipeline, flash, and folding converters, due to the former’s high digital dependence and their power consumption which scales down with Moore’s law. However,

scaling down technology nodes (65 nm and below) poses several challenges to designing analog circuits, including increase in leakage currents. For example, pipeline ADC requires inter-stage residue amplifiers, which operate at lower supply voltages in deep sub-micron CMOS technology. This low-supply-voltage operation requires special op-amp design techniques or architectures in order to achieve the desired signal gain. Multiple op-amp stages might have to be cascaded, as cascoding transistors is not feasible. This increases chip area and power consumption. However, the inherent error-correction capabilities of a pipeline ADC make it advantageous to use for high-speed and high-resolution applications, but a conventional SAR ADC [1] lacks this inherent capability. A SAR ADC taking advantage of Moore's law and with error-correction capabilities akin to a 1.5-bit/stage pipeline ADC is highly desirable for high-speed single-channel operations in a noisy SoC environment.

One of the several challenges for high-speed SAR ADCs is mitigating the speed bottleneck caused by incomplete voltage settling on the CDAC, resulting in an erroneous decision. A 10-bit CDAC requires a total of 7.63 time constants for the voltage to settle within a precision of 0.5 least significant bits (LSB). For example, a 10-bit 160 MSps SAR ADC using a 1-bit/cycle operation has 189 ps available for the DAC voltage to settle. In this example, it is assumed that the sampling time is equivalent to one conversion cycle period, which is equally divided into comparator regeneration time, SAR logic delay, and DAC settling time. The 189 ps available for DAC voltage settling is extremely challenging to meet across process, voltage, and temperature (PVT) corners when using a conventional SAR

architecture. Additional challenges include noise coupling from supply rails and DAC reference voltages that can result in erroneous conversion and degrade dynamic performance. Introducing redundancy and multiple error-correction capabilities to a SAR ADC can be beneficial for preserving its dynamic performance, especially with the data converters operating within a SoC's noisy environment.

Introducing binary or non-binary redundancy methods [2-16] requires additional conversion cycles in order to obtain the required data-converters resolution. Adding conversion cycles is worthwhile because it relaxes the DAC voltage settling time and, in some cases, facilitates error correction. The time constants saved by relaxing the DAC voltage settling time can be traded off for either increased conversion frequency or relaxed voltage reference buffer requirements. Relaxing the voltage reference buffer for a high-speed ADC can result in immense power savings. These tradeoffs have to be decided by the system designer. Implementing redundancy techniques for SAR ADCs requires complex CDAC architectures such as additional compensative capacitors [2] or split CDACs [3], which are asymmetrically metal-routed in their layout, prolonging the capacitor charge transfer time and resulting in longer CDAC voltage-settling times. Furthermore, the increasing interconnect line impedance for advanced nano-technology nodes increases the capacitor charge transfer time, which prolongs CDAC voltage-settling time and may result in a speed bottleneck. Using additional compensative capacitors suffer from increased input capacitance, which reduces bandwidth than when using unmodified binary-scaled CDACs [3]. A SAR ADC

with in-built DAC redundancy using an unmodified binary-scaled DAC architecture would simplify the implementation of redundancy and move towards the goal of achieving high-speed single-channel operation for high-resolution SAR ADCs.

Another problem is that some redundancy techniques require large control logic overhead, decoders, arithmetic units [4], ROM, additional offset DACs [16], and large digital error correction logic [2, 4] to convert the additional redundancy-induced conversion cycles output to the required resolution.

A low-power SAR ADC requires innovations regarding the CDAC switching scheme because the scheme is an important contributor to the overall energy consumption. Switching schemes such as V_{CM} -based switching [18], set- and down-based switching [2, 7, 17], conventional switching [1], and monotonic switching [19] have been widely used for 1-bit/cycle SAR ADCs with or without redundancy. These switching schemes offer an 81% [2, 17, 19] and an 87% [18] reduction in CDAC switching energy when compared with a conventional switching scheme [1]. However, reducing switching energy and maintaining DAC metal-routing symmetry and a constant common mode operation for a multi-bit per cycle conversion with redundancy has its own challenges. Extra energy is required to create the required redundancy margins through switching additional capacitors in the CDAC array.

The final problem for high-speed, single-channel SAR ADC design is the sampling switch linearity limitation. Moore's law has helped reduce the on-resistance of the

sampling switch and the SAR logic delay. The digital logic in deep submicron technology nodes can often run at much higher speeds, but the overall ADC speed is restricted due to CMOS sampling switch dynamic performance limitations.

To summarize, there is an acute need for a SAR ADC that has inherent error-correction capabilities and embedded DAC redundancy, that does not require any significant hardware overhead, and that minimizes the data converters' need for additional conversion cycles. An appropriate switching scheme to mitigate the challenges associated with multi-bit/cycle conversion with redundancy that does not require any significant hardware overhead or arithmetic units is required to achieve the goal of creating low-power, high-speed, single-channel SAR ADCs. Furthermore, a “more than Moore” approach for exploring new circuit techniques and fabrication technologies utilizing III-V compound semiconductors and CMOS integration is desirable. Advantages of both worlds, for example digital-logic implementation in CMOS and sampling-switch implementation in III-V CS technologies can be explored to address the sampling switch linearity problem for high-speed, single-channel data converters.

1.2 Objectives

The thesis goals can be summarized as an attempt to implement a low-power, high-speed, single-channel SAR ADC with inbuilt CDAC redundancy capable of correcting multiple errors without any dependence on where the erroneous conversion cycle occurred. Furthermore, the ADC should have a simplified digital error correction logic and it should maintain constant common mode and low switching energy CDAC operation without reducing the overall ADC speed. The

prototype will be fabricated using deep submicron technology. The next goal is to investigate the sampling switch limitations of CMOS technology when compared to III-V compound semiconductor technology.

1.3 Major Contributions of this Thesis

This work focuses on six important contributions to the development of high-performance SAR ADCs. The first contribution introduces binary-scaled redundancy embedded in a conventional CDAC. This requires no additional capacitors or offset CDACs and therefore simplifies the DAC layout and redundancy implementation.

Second, this thesis discusses optimizing the use of redundancy by introducing a new CDAC switching scheme. This switching scheme utilizes bottom-plate sampling and fractional reference voltage switching so that any noise on the V_{CM} reference voltage is cancelled due to the differential arrangement of the CDAC. Additionally, the first conversion cycle provides sufficient time for the CDAC voltage to settle in order to prevent errors made on the most significant bit (MSB) decision. Thus, this technique alleviates the need for redundancy in the first conversion cycle, therefore reducing the need for additional conversion cycles to obtain the required output bits.

The third contribution involves introducing a simple bit-overlap-and-add error-correction technique for a 10-bit SAR ADC. Inspiration for the technique is drawn from the inherent error correction of a 1.5-bit/stage pipeline ADC. An initial 1-bit conversion cycle followed by eight 1.5-bit cycles is adopted. This implementation

requires no additional conversion cycles to obtain a 10-bit resolution. Multiple erroneous decisions can be corrected over nine conversion cycles, irrespective of where the erroneous conversion cycle occurs. The bit-overlap-and-add error-correction logic provides an opportunity for the error to propagate to the next conversion cycle, where it can be corrected. With a high-speed, single-channel SAR ADC, multiple errors can occur during the first four conversion cycles due to insufficient DAC settling time. More errors can occur in the remaining conversion cycles because of comparator metastability, and noise coupling from the supply rails or the reference voltages, which may also be due to operation in a noisy SoC environment.

Fourth, this thesis introduces a new area-efficient switching scheme for a multi-bit per cycle SAR ADC. The proposed constant common-mode fractional reference voltage (CCM-FRV) switching scheme offers a 50% CDAC area reduction when compared to a conventional switching scheme [1] implementing a similar redundancy and error-correction concept. Implementation of the CCM-FRV switching scheme requires no special arithmetic units or additional hardware overheads to compute the DAC switching pattern, thus eliminating any speed bottleneck due to logic delay. Furthermore, the redundancy is built into the CDAC. Using CCM-FRV switching scheme results in reducing the chip area and power consumption, and increasing the speed of the data converter. All of the above four contributions are implemented using a 65 nm 1P9M mixed-signal RF CMOS technology.

The fifth contribution in this thesis introduces an alternative technique to the CCM-FRV switching scheme. Behavior modeling of a SAR ADC using the alternative technique demonstrates its effectiveness to reduce the DAC switching energy and chip-area. When compared to a conventional switching scheme [1] implementing a similar redundancy and error-correction concept, the proposed switching scheme reduces CDAC switching energy by 88.55%, along with a 50% CDAC area reduction. Except for the last two conversion cycles, the proposed switching scheme maintains constant common-mode voltage to the comparators input. The 1.5-bit/cycle technique provides an error tolerance range and relaxes the CDAC voltage settling time, which enables faster conversion cycles.

The sixth contribution explores a “more than Moore” design and fabrication methodology in order to compare the sampling switch performance of a SAR ADC using III-V CS HEMT device and CMOS device. An on-chip, fully integrated SAR ADC with a III-V CS (i.e., InGaAs) sampling switch and remaining circuits in CMOS technology is implemented. A hybrid PDK that allows direct integration of III-V devices to back-end-of-the-line CMOS metal fabrication is used. Additionally, on-chip integration of a III-V CS sampling switch reduces parasitic elements when compared to off-chip implementation. The reduction of parasitic elements is beneficial for enhancing the CDAC voltage settling time and results in superior dynamic performance.

1.4 Thesis Organization

This work is divided into seven chapters in addition to the current introductory chapter. Chapter 2 provides background information on SAR ADCs as well as a

literature review. An analysis of the trends among Nyquist-rate data converters is presented, followed by a discussion of trends regarding SAR ADCs. The need for redundancy, redundancy techniques, redundancy-facilitated error-correction techniques, and CDAC switching schemes is discussed. This is followed by an analysis of the hardware overhead related to different types of redundancy, error correction, and CDAC switching schemes.

Chapter 3 discusses the noise budget specification and some design choices made (e.g., regarding the unit capacitor size) in order to achieve the target specification of the designed 10-bit SAR ADC

Chapter 4 discusses the design considerations related to developing a multi-bit per cycle SAR ADC with redundancy. The proposed redundancy concept, digital error correction technique, and constant common-mode fractional reference voltage (CCM-FRV) switching scheme are discussed. Furthermore, the proposed techniques are elaborated on using several examples. The area reduction of the proposed switching scheme is compared to a conventional switching scheme. The hardware overhead, including metrics such as control logic complexity, error-correction complexity, the number of CDAC switches, and the need for additional conversion cycles, is analyzed and compared with other error-correction SAR ADCs. Thesis contributions one-to-four are explained in this chapter.

Chapter 5 introduces the design and implementation of a 160 MSps 10-bit SAR ADC with binary-scaled redundancy-facilitated error correction. Architecture level details along with key building blocks – asynchronous timing generator,

comparator, CDAC, control logic and error-correction logic – are discussed. Layout techniques used to achieve a good mixed-signal performance are discussed. Thesis contributions one-to-four are implemented on a circuit level in this chapter.

Chapter 6 discusses the printed circuit board design and the testing considerations regarding maintaining the performance of the designed data converter. The test setup and the measurement results of the proposed 10-bit SAR ADC with redundancy-facilitated error correction are discussed. Thesis contributions one-to-four are tested using a printed circuit board in this chapter.

Chapter 7 discusses the proposed low-energy and chip-area-efficient switching scheme for a 1.5-bit/cycle SAR ADC with digital error-correction. The implementation of the proposed switching scheme for a 10-bit SAR ADC is elaborated on. A switching-scheme analysis and a comparison with different switching schemes are done. Thesis contribution five is explained in this chapter.

Chapter 8 consists of the conclusion and plans for future work. Future avenues include a “more than Moore” design and a fabrication methodology to implement a fully integrated III-V/CMOS SAR ADC in order to achieve superior dynamic performance. Thesis contribution six is explained in this chapter.

Chapter 2

Background to the research topic and Literature review

This chapter discusses the potential applications for the designed SAR ADC. Next, an analysis of the trends among Nyquist-rate data converters is presented, followed by a discussion of trends regarding SAR ADCs. The need for redundancy, redundancy techniques, redundancy-facilitated error-correction techniques, and CDAC switching schemes is discussed. This is followed by an analysis of the hardware overhead related to different types of redundancy, error correction, and CDAC switching schemes.

2.1 Applications

The popularity of connected devices forming the internet of things (IoT) is soaring. In 2016, 431 million wireless sensor devices were sold, and sales are estimated to reach 2.2 billion in 2021 [20]. IoT extends the role of the internet by connecting sensors, compute power, and devices to enable communications. These communications often occur machine to machine, and this has given rise to several new applications and has affected existing fields. Systems enabled by IoT, also called smart systems, are positively impacting sectors such as home automation, agricultural technologies, the automotive industry, waste management, retail, climate monitoring, and the medical field. Connected cities can also run more efficiently and optimize their daily operations such as transport, parking, traffic,

on-demand services, and much more. Table 2.1 summarizes wireless sensor devices by their application.

Table 2.1: Global market volume for wireless sensor devices, through 2021
(Millions of Units) [20].

Wireless sensors	2015	2016	2021	CAGR % 2016–2021
Home automation & indoor app.	141	190	931	37.4
Energy infrastructure	77	100	443	34.7
Medicine	30	42	235	41.1
Industrial installations	20	29	209	48.4
Logistics & transport	19	27	138	38.6
Ecology & agriculture	14	20	126	44.5
Defense & surveillance	14	23	127	40.7
Total	315	431	2,209	38.7

These IoT-connected devices generate round-the-clock big-data streams, which need to be sent wirelessly to a main computing unit. This transfer is often implemented using a cloud-based server where the data can be analyzed for deciding subsequent actions. Making IoT systems low power is essential for long-term success. This low-energy requirement for highly integrated SoCs trickles down to the sub-systems such as high-speed data converters and wireless transceivers.

Wireless IoT sensors can use numerous wireless standards, summarized in Table 2.2. Technologies based on 802.15.4 are used for low-data-rate applications requiring up to 250 Kbps within a transmission distance of 10 meters. ZigBEE and Bluetooth are some of the prominent standards used for medium-data-rate applications that require less than 3 Mbps over-the-air data rate within a distance of 100 meters. Wi-Fi or the IEEE 802.11 standard can be used for high-data-rate applications, with the 802.11ac protocol providing a data rate of 1.3 Gbps. The upcoming IEEE 802.11ax Wi-Fi standard, to be introduced in 2019, will further increase the data rate and bandwidth to accommodate user congestion, which is a growing concern given the vast number of connected devices. Implementing the new standard requires high-speed ($f_s > 100$ MSps) and high-resolution (10–12 bits) ADCs [21].

Table 2.2: Global market volume for wireless sensor devices, by wireless standard, through 2021 (Millions of Units) [22].

Wireless standards or technology	2015	2016	2021	CAGR % 2016–2021
ZigBEE and RF4CE	141	193	1,028	39.7
Bluetooth and Bluetooth Smart	33	47	242	38.8
RFID (e.g., NFC)	18	25	84	27.4
Wi-Fi and 6LoWPAN	16	23	107	36.0
Other 802.15.4-based technologies (e.g., EnOcean, Z-Wave, WirelessHART, ISA100.11a)	107	143	748	39.2
Total	315	431	2,209	38.7

2.1.1 802.11ac Wave 2 and 802.11ax

Wi-Fi forms an integral part of most electronic devices from laptops to IoT sensor devices. The 802.11n standard revolutionized Wi-Fi with the introduction of channel bonding [23]. The newest 802.11ax technology (in development when this thesis was written) is backward-compatible with previous Wi-Fi standards while quadrupling average throughput in high-density scenarios such as airports, train stations, and stadiums. It uses multi-user, multiple-input, multiple-output (MU-MIMO) and orthogonal frequency division multiple access (OFDMA) technology. Additionally, it improves traffic flow and channel access and has better power management for longer battery life [24]. Table 2.3 summarizes the key differences between the 802.11ac and 802.11ax standards. The maximum channel bandwidth, depending on the wireless spectrum available in each respective country, can be 160 MHz. The 10-bit 160MSps SAR ADC developed as part of this thesis can cater for the 80 MHz channel bandwidth specifications while optimizing power and area. Figure 2.1 shows the location of the data converter in a typical wireless receiver.

Table 2. 3: Comparison of 802.11ac and 802.11ax [24].

	802.11ac	802.11ax
Bands	5 GHz	2.4 GHz and 5 GHz
Channel B.W	20 MHz, 40 MHz, 80 MHz, 80+80 MHz & 160 MHz	20 MHz, 40 MHz, 80 MHz, 80+80 MHz & 160 MHz
FFT sizes	64, 128, 256, 512	256, 512, 1024, 2048
Subcarrier spacing	312.5 kHz	78.125 kHz
OFDM symbol duration	3.2 μ s + 0.8/0.4 μ s cyclic prefix (CP)	12.8 μ s + 0.8/1.6/3.2 μ s CP
Highest modulation	256-QAM	1024-QAM
Data rates	433 Mbps (80 MHz, 1SS) 6933 Mbps (160 MHz, 8SS)	600.4 Mbps (80 MHz, 1SS) 9607.8 Mbps (160 MHz, 8SS)

Fig. 2.1: Simplified block diagram of an archetypal superheterodyne WLAN radio [25]

2.1.2 802.11p

The 802.11p standard serves vehicle-to-everything (V2x) communication, which involves vehicles exchanging data with other vehicles and the infrastructure (e.g., buildings, traffic lights). Devices implementing this IEEE standard are called dedicated short-range communications (DSRC) devices and work on the 5.8 GHz spectrum with a 75 MHz bandwidth. An orthogonal frequency division multiplexing (OFDM) modulation scheme provides robustness against time-dispersive channels [26]. IEEE802.11p standard requires extremely low latency, for example 50 ms for a pre-crash warning message. Figure 2.2 shows a typical application scenario for an 802.11p standard. The SAR ADC developed as part of this thesis meets these specifications while optimizing power and area.

Fig. 2. 2: 802.11p connectivity with other vehicles and infrastructure [27].

2.1.3 Non-Networking Applications

Apart from the IoT application described, ADCs discussed in this thesis are general purpose and can serve applications that are not limited to the above-mentioned communication standards. Here are some of the additional applications:

- Medical Imaging
- Automotive applications
- Radar applications
- Industrial applications

Increasing demands for portable and low cost medical imaging systems such as positron emission tomography, X-rays, ultrasound and wireless capsule endoscopy can benefit from the designed SAR ADC in this thesis. Figure 2.3 shows the

location of the ADC in a typical positron emission tomography system. The specifications of the ADC developed as part of this thesis is selected such that the speed is high enough to demonstrate the proposed redundancy concept and its advantages.

Fig. 2. 3: Block diagram for positron emission tomography system.

2.2 ADC Overview

Data converters can be broadly divided into two categories, namely oversampling ADCs and Nyquist-rate ADCs. Oversampling data converters are used for noise shaping: sigma-delta converters, for example, have the ADC running at much higher sampling speeds than the input signal frequency in order to shape noise out of the input frequency band. Nyquist-rate converters include flash, pipeline, folding, interpolating, and time-to-digital converters as well as the SAR ADC.

Data converters can be used based on the resolution of the application: sigma-delta converters for high resolution (>16 bits), pipeline ADCs for medium resolution (up

to 16 bits), and flash ADCs for low resolution (<7 bits). In general, SAR architecture overlaps with the low- and medium-resolution space. However, by introducing noise shaping to SAR ADCs, they can be used for high-resolution applications. Because of the topic of this thesis, SAR architecture is emphasized in the discussion below. Pipeline architecture is briefly discussed because of its error-correction capability.

2.2.1 Pipeline ADCs

Fig. 2. 4: Pipeline ADC architecture [28].

Figure 2.4 shows a typical pipeline ADC architecture, where the input signal is sampled by the sample-and-hold circuit of the first stage, followed by an N-bit ADC whose digital output is converted to an N-bit DAC analog output subtracted from the sampled input signal. This subtracted signal, or the residue, is then amplified by a factor of K_j . The output of the amplifier $V_{res,j}$ then passes to the next

stage of the pipeline ADC. Equation 2.1 represents the new residue voltage of a typical pipeline ADC stage.

$$V_{\text{res}}(j) = \{V_{\text{res}}(j-1) - V_{\text{DAC}}(b_j)\} K_j. \quad (2.1)$$

In order to avoid out-of-range conditions, which may cause erroneous conversion, using multi-threshold ADCs such as 1.5-bit/stage and 2.5-bit/stage is a common practice. A 1.5-bit/stage design has two thresholds, namely $V_{\text{TH,Lower}}$ and $V_{\text{TH,Upper}}$. This results in three decision regions with three potential binary-coded outputs: “00”, “01”, and “10”. The digital error correction utilizes a bit-overlap-and-addition technique to obtain the required ADC resolution.

Latency is one of the drawbacks of a pipeline ADC, restricting its usage in closed-loop systems. The amount of latency depends on the number of stages used and translates into a corresponding cycle delay for the first ADC data output. Pipeline architecture is widely used for high-speed (>100 MSps) and medium-resolution applications.

2.2.2 SAR ADCs

A conventional SAR data converter, illustrated in Figure 2.5, typically comprises of four fundamental blocks: the comparator, control logic, memory and the DAC. One complete analog conversion requires $N+1$ conversion cycles, where N is the resolution of the data converter. One additional conversion cycle is used to sample the analog input value (V_i). A typical DAC without any redundancy has to settle within a precision of $\frac{1}{2}$ LSB in order for the converted result to be error-free. After

all the conversion cycles have been completed, the multi-bit output D_0 is available in the shift register.

Fig. 2. 5: A typical SAR data-converter architecture [29].

Considering a conventional 1-bit/cycle SAR ADC with the help of Figure 2.6, we can see that in the first conversion cycle, half of the DAC is switched to a positive reference voltage, i.e., V_{REFp} . This creates a DAC reference voltage of $\frac{1}{2}V_{FS}$. After this, the comparator compares V_i to $\frac{1}{2}V_{FS}$. If the input voltage is greater than the DAC-generated voltage, a logic “1” is available at the comparator’s output. The next conversion cycle compares the input voltage with another quantity of DAC-generated voltage, i.e., $\frac{3}{4}V_{FS}$, and this repeats until the DAC-generated voltage converges to the input voltage within an error of $\frac{1}{2}$ LSB. If the DAC-generated voltage does not settle within the $\frac{1}{2}$ LSB margin, a decision error is made in the conversion cycle in question. Without error correction, this erroneous conversion-cycle decision cannot be corrected in the subsequent cycle and will result in degraded dynamic performance.

Fig. 2. 6: Binary search algorithm steps [29].

Figure 2.7 details the charge-redistribution principle based DAC operation and its ability to sample the input voltage using the same capacitor bank. During phase ϕ_1 , the 4-bit capacitive DAC samples the input voltage V_i with a precision of $\frac{1}{2}$ LSB, after which the MSB of the DAC switches to a positive reference voltage (V_R). The resulting node voltage, V_X , $V_X = V_R/2 - V_i$, is then compared using a comparator. Similarly, depending on the output of first cycle, the MSB-1 capacitor switches to either V_{REFp} or a negative reference voltage (V_{REFn}). Eventually, the DAC voltage converges to the analog input value with a precision of $\frac{1}{2}$ LSB where $1\text{LSB} = V_R/2^N$.

Fig. 2. 7: A single-ended 4-bit SAR ADC implementing the charge-redistribution principle [29].

2.3 Literature Review

This section of the thesis provides details on the nyquist rate data converter landscape from 1997 onwards, covering the recent trends. Existing redundancy techniques, digital error correction, DAC switching schemes, and the associated hardware overhead are discussed.

2.3.1 ADC Trends

This sub-section contains my own analysis of and corresponding figures visually representing the data-converter trends. The analysis shows that the adoption of data-converter architecture and trends greatly depends on advancements in transistor-manufacturing-technology nodes. Figure 2.8 shows the rapid development of advanced technology nodes. This is followed by a slowdown after 2011, due to increased research and development costs and more time required to achieve high manufacturing yields, to effectively model short channel transistor

effects, to develop compatible lithography tools such as extreme-UV technology, and to develop further supporting technology. Moving to technology nodes smaller than 130 nm has enabled ADCs to achieve low power and a smaller chip area. Rapid adoption of digital-intensive architecture such as the SAR ADC meant that they prevailed over analog-dependent counterparts such as pipeline ADCs. Figure 2.9 shows the growing number of publications indexed in the IEEE with the search keyword “SAR ADC”. Significant research and innovation have occurred regarding SAR architecture, and this has resulted in high-speed and energy-efficient data converters.

Fig. 2. 8: Time series plot of Intel’s transistor-manufacturing technology, from the company’s website www.intel.com [22].

Fig. 2. 9: Number of IEEE-indexed publications with the keyword “SAR ADC” since 1997.

An ADC’s performance can be evaluated using either the Walden figure of merit (FOM) or the Schreier FOM. Both FOMs work well across a limited range of the SNDR. Equation 2.2 is used to calculate the Walden FOM. As can be seen, metrics such as technology-node and chip area are not considered. Here, ENOB refers to the effective number of bits of an ADC.

$$\text{Figure of merit (FOM) (fJ /conv. – step)} = \frac{\text{Power (mW)}}{(2^{\text{ENOB}} \cdot f_{\text{sampling}})} \quad (2.2)$$

Fig. 2. 10: A cross-plot of the sampling frequency and the Walden figure of merit for single-channel Nyquist-rate ADCs published in the ISSCC and VLSI conferences from 1997 to 2016. (Data adapted from [30].)

A plot showing the relationship between sampling frequency and the FOM, illustrated in Figure 2.10, is a well-known way to visualize the performance of a data converter. This figure covers the performance of several single-channel Nyquist-rate architectures: pipeline, flash, folding, and other Nyquist-rate architectures – two-step, algorithmic, incremental and binary search. The graphic shows that pipeline ADC architecture has been extensively used for high-speed designs greater than 40 MSps and with resolutions between 8–16 bits. Advancements in technology nodes and SAR architecture, such as control logic, comparators, and DAC voltage settling relaxation, seem to have placed SAR

architecture in direct competition with pipeline architecture, covering the same application space and specifications. SAR architecture is without a doubt the winner within the low-frequency (<1 MSps) sampling and medium resolution application space. Folding ADCs can operate at a higher sampling frequency but show a poor FOM. Only 17 folding ADCs were published between 1997–2016 in the ISSCC and VLSI conferences.

Figure 2.11 shows a cross-plot with the occupied chip area and resolution of various single-channel Nyquist-rate ADCs. It shows that SAR architecture overlaps with the other ADCs within the medium- and high-resolution data-converter space. SAR architecture, due to its digital nature, offers an area advantage when compared to other architectures with up to 14-bit resolution.

Fig. 2. 11: A cross-plot of area and resolution for single-channel Nyquist-rate ADCs published in the ISSCC and VLSI conferences from 1997 to 2016. (Data adapted from [30].)

Fig. 2. 12: A cross-plot of area and the Walden figure of merit for single-channel Nyquist-rate ADCs published in the ISSCC and VLSI conferences from 1997 to 2016. (Data adapted from [30].)

Figure 2.12 shows the advantages of SAR architecture in terms of occupying less chip area and a superior Walden FOM over several single-channel Nyquist-rate architectures: pipeline, flash, folding and other Nyquist-rate architectures – two-step, algorithmic, incremental, and binary search. The Walden FOM (lower numbers are better because less energy is consumed from the power supply) incorporates ADC metrics: sampling frequency, ENOB, and power consumption. Lower Walden FOM along with less chip area, make SAR ADC a good candidate for integration within SoC.

Trends among single-channel SAR ADCs are classified into two broad categories: SAR without redundancy and SAR with redundancy. The impact of adding redundancy on performance is illustrated by Figures 2.13, 2.14, and 2.15. The

sample size of the published SAR ADCs with and without redundancy is not statistically significant to draw conclusion. Reference work [30] shows the predicted trend of FOM.

Figure 2.15 shows that technology-node scaling does not improve the achievable SNDR and that SAR ADCs with and without redundancy can be used for high-resolution applications. It should be noted that one additional bit of resolution when approaching the kT/C noise limit leads to quadrupled capacitances and equivalent increases in power consumption. Maintaining a very low FOM while increasing the ENOB is therefore quite challenging and certainly not straightforward.

Fig. 2. 13: A cross-plot of the Walden FOM and the sampling frequency for single-channel SAR ADCs published in the ISSCC and VLSI conferences from 1997 to 2016. (Data adapted from [30].)

Fig. 2. 14: A cross-plot of area and the sampling frequency for single-channel SAR ADCs published in the ISSCC and VLSI conferences from 1997 to 2016. (Data adapted from [30].)

Fig. 2. 15: A cross-plot of the technology node and the SNDR for single-channel SAR ADCs published in the ISSCC and VLSI conferences from 1997 to 2016.

(Data adapted from [30].)

2.3.2 Redundancy

2.3.2.1 Need for redundancy and error correction and its applications

For a typical high-performance data converter operating within an automotive, the SoC (with analog, digital, and radio sub-systems – a typical IoT product) and industrial applications are usually plagued by the noisy environment. A noisy environment can affect the operation of a data converter and may cause incorrect digitized results or degrade the signal-to-noise ratio.

Figure 2.16 shows the three circuit blocks of a SAR ADC – control logic, the DAC, and the comparator – that contribute to the minimum time required for each conversion cycle and which set the upper limit of the obtainable sampling speed. Control-logic delay and dynamic comparator regeneration time have shortened due to technology scaling. However, for high-speed operation, the CDAC poses a speed bottleneck, affecting settling behavior which might result in erroneous conversion.

Fig. 2. 16: The typical timing split for the SAR ADC sub-blocks during one conversion cycle.

For the first conversion cycle, a 10-bit CDAC requires 7.63τ time constants for the voltage to settle within a precision of $\frac{1}{2}$ LSB. Figure 2.17 shows the settling waveform of a CDAC, where V_{ref} is the desired voltage value of a CDAC at the time of comparison, V_{set} is the settled voltage of a DAC and k is the conversion cycle number. For example, a 160 MSps 10-bit SAR ADC only has 189 ps available for the DAC settling time, assuming that the sampling time is equivalent to one conversion cycle period equally divided into comparator regeneration time, control-logic delay, and DAC settling time.

Fig. 2. 17: The voltage settling waveform of a Capacitive DAC [11].

Adding redundancy to an ADC has several benefits, such as relaxing settling time requirements for the DAC, increasing the internal conversion cycle speed of the ADC (resulting in faster ADC sampling), compensating for process and environmental effects [15], and reducing circuit (system level) power.

$$T = \tau \times \ln \left(\frac{1}{2} \times \frac{1}{2^N} \right) \quad (2.3)$$

Equation 2.3 can be used to calculate the DAC voltage settling time for an N-bit data converter. For a 10-bit SAR ADC with 12.5% redundancy, the DAC voltage settling can be relaxed by a factor of 3.67 for the first conversion cycle. The time constants saved can be used to either increase the sampling frequency of the data converter or reduce the power consumption of an analog voltage reference buffer. The power consumption can be reduced by relaxing the closed loop bandwidth of an analog voltage reference buffer such as a flipped-voltage source follower (if the

sampling frequency of ADC is not increased after adding redundancy, the buffer has more time to replenish the charges on the output decoupling capacitor).

Redundancy is also required to correct any erroneous conversion cycle. This is possible because redundancy provides a small overlap with the full-scale of previous and current conversion cycle. This overlap offers another opportunity for the SAR ADC to provide a decision in order for the output to converge within $\frac{1}{2}$ LSB to the approximated analog input. Redundancy can be implemented by using either a binary or non-binary approach. Error-correction techniques vary depending on the type of redundancy used. These techniques are discussed in section 2.3.3.

2.3.2.2 Non-binary Redundancy

The concept of non-binary, weighted redundancy was first demonstrated by Boyacigiller *et al.* [8] in 1981. A radix of 1.85 was used instead of radix-2 so that the digital-to-analog converter codes cover the entire analog output range without any missing codes. In 2002, Franz [4] reintroduced the concept of non-binary redundancy for a single-channel SAR ADC. Here, a non-binary DAC of sub-2 radix, i.e., 1.87, is utilized. The amount of redundancy is implemented in terms of percentage full scale and is used in all conversion cycles. A binary SAR conversion, in other words a radix-2 implementation, requires no extra conversion cycles to obtain the required resolution. However, a sub-2 radix implementation requires additional conversion cycles to obtain the required data-converter resolution. The number of additional conversion cycles required increases as the sub-2 radix number decreases. An example of sub-2 radix (1.78) or non-binary redundancy implementation for a 4-bit SAR ADC is shown in Figure 2.18. The

figure shows that the 4-bit implementation requires one additional conversion cycle in order to converge to the required 4-bit resolution. The output, Dout, requires large error-correction logic, discussed in the section 2.3.3.

Fig. 2. 18: Example of a 4-bit SAR ADC using a non-binary redundancy technique.

Franz's [4] implementation uses a thermometer-coded DAC and decoder in order to implement redundancy. For 12.7% redundancy, three extra cycles are utilized to obtain a 10-bit resolution. ROM and an adder are used to compute the following conversion cycles full scale, adding to the complexity of control logic and to the speed bottleneck apart from the DAC settling time. A thermometer-coded DAC yields good linearity and uses less power from the reference generation circuit [4].

The non-binary redundancy technique [31–40] has been widely used for relaxing DAC voltage settling. Scandurra *et al.* [41] describe the methodology for selecting a non-binary radix implementation. Redundancy can also be utilized for other purposes. For example, Ogawa *et al.* [15] utilize non-binary redundancy to increase

the yield of ADC chips in different process corners. In their work, the yield is referred to as the sampling-rate specifications for a data converter. The amount of redundancy is traded off for the additional cycles required to achieve a 10-bit resolution in the given chip specification. Figure 2.19 tabulates this tradeoff. However, this technique is applicable only if DAC settling is the speed bottleneck.

TABLE I	TABLE II	TABLE III																																																																														
FAST CHIP (ESTIMATED DAC TIME CONSTANT τ = 3.5ns), 10-BIT 11-STEP (LOW POWER)	MIDDLE SPEED CHIP ($\tau=4.0\text{ns}$), 10-BIT 12-STEP (MIDDLE POWER)	SLOW CHIP ($\tau=4.5\text{ns}$), 10-BIT 13-STEP (LARGE POWER)																																																																														
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Fig. 2. 19: Process variation based reconfigurable non-binary SAR ADCs [15].

The quest for further reducing the power consumption of SAR ADCs resulted in using a dual comparator approach, where the first half of the conversion cycles use a low-power, high-noise comparator, and the remaining conversion cycles use a high-power, low-noise comparator. However, using a dual comparator requires the calibration of the offset for both comparators so that the mismatch in the offset between the comparators does not result in erroneous decisions. A charge-sharing,

non-binary redundancy technique [12] can be used to eliminate the need for analog calibration of a dual comparator. Figure 2.20 tabulates the use of a dual-comparator approach where the seventh conversion cycle requires switching to a low-noise, high-power comparator due to the small comparator input differential signal.

	step k	weight p_k		step k	weight p_k
Low power high noise comparator	1	512	Low power high noise comparator	1	512
	2	256		2	256
	3	128		3	128
	4	64		4	64
	5	32		5	32
	6	16		6	16
	7	8	High power low noise comparator	7	8
	8	4		8	8
	9	2		9	4
High power low noise comparator	10	1		10	2
	11	1		11	1

Fig. 2. 20: A 10-bit SAR ADC algorithm with two comparators: left, conventional, right, proposed in [12].

Implementing non-binary redundancy requires a non-binary-scaled DAC and is done using a thermometer-coded DAC requiring a decoder and a large number of switches. This increases area and power consumption. Work by Ogawa *et al.* [11, 12, 14, 15] on non-binary redundancy includes a generalized non-binary algorithm, which replaces the conventional non-binary algorithm. The generalized algorithm utilizes a binary weighted DAC instead of a non-binary weighted DAC, which simplifies the DAC control logic.

2.3.2.2 Binary Redundancy

A radix-2 DAC implementing redundancy is called binary redundancy. Some binary-redundancy techniques have been introduced to relax DAC settling time [2, 3, 42, 43] and to facilitate error correction [2, 3, 42]. These techniques use CDAC architectures requiring additional compensation capacitors [2] and split capacitor DACs [2, 3, 42] which are asymmetrically metal-routed into the CDAC layout. The binary-with-compensation technique [2] for redundancy uses additional compensative capacitors, resulting in an increase in the sampling capacitance, which in turn results in a reduced bandwidth. The linearity of the ADC in [2] is degraded due to the mismatch between the compensative capacitors and the corresponding digital value.

The capacitor charge transfer time increases because of the increasing interconnect line impedance for advanced nano-technology nodes. This increase in the charge transfer time prolongs the CDAC voltage settling time [2] and can result in a speed bottleneck. Using additional compensative capacitors suffers from increased input capacitance and gain error when compared to an unmodified binary-scaled CDAC [3]. Another problem associated with adding redundancy [6–19] is that it can require additional conversion cycles. Furthermore, some redundancy techniques require a substantial control-logic overhead – decoders, arithmetic units [4], ROM, additional offset DACs [16], and large digital error-correction logic [2, 4] – to convert the additional redundancy-induced conversion cycles’ output to the required resolution.

Figure 2.21 shows an example of a 4-bit SAR ADC without redundancy (left) and another one using the binary-with-compensation technique (right). In both cases, the full scale is divided by two in every subsequent conversion cycle. The binary-with-compensation technique uses a level-shifting method of increasing the comparison threshold so that an error in the previous conversion cycle can be corrected. This 4-bit implementation requires one additional cycle to obtain the required 4-bit resolution. The digital logic to obtain the final output Dout is quite complex: for a 10-bit implementation, the binary-with-compensation technique requires five inverters, nine full adders, one half-adder, and ten multiplexers.

Fig. 2. 21: Example of a 4-bit SAR ADC using the binary and binary-with-compensation techniques.

Figure 2.22 shows the capacitor array weighted ratio, including the split capacitor ratio, for implementing a 10-bit SAR ADC with a binary-scaled recombination technique for implementing redundancy [42]. This implementation does not require additional compensative capacitors but still requires capacitor splitting and a complex logic to obtain the 10-bit output, Dout, from the 11 conversion cycles.

Fig. 2. 22: The capacitor array ratio for the binary-scaled recombination technique [42].

2.3.3 Error-correction techniques

The analysis described in section 2.3 shows that the quest for low power consumption leads to using multiple techniques such as split capacitor DACs, dual comparators (low power, a noisy comparator; high power, a less noisy comparator), energy-efficient DAC switching schemes, redundancy and configurable redundancy [44]. Introducing redundancy to an SAR ADC requires digital logic to calculate the final data output or the error-corrected output. The complexity of the error-correction logic can vary depending on the type of redundancy and the CDAC architecture, including the switching scheme used. A detailed discussion of this is presented below in section 2.3.5.

It is beneficial for SAR ADCs to possess multiple erroneous decision correction capabilities. For a high-speed SAR ADC, the first four conversion cycles are critical because this is when the ADC is most likely to make multiple erroneous decisions. Additional errors can occur in the remaining conversion cycles due to noise coupling from supply rails, or reference voltages and the metastability of the comparator. For example, four erroneous cycles can occur: two during the first four

conversion cycles, and another two during the remaining conversion cycles. Several error correction techniques [2, 3, 4] have been proposed. In Ref. [2] the precise error-tolerance range depends on where the erroneous conversion cycle occurs. Depending on the type of redundancy used, the amount of additional conversion cycles and corresponding error-correction logic varies. The number of additional conversion cycles required also depends on the amount of redundancy used.

Fig. 2. 23: An error-correction scheme for a 10-bit SAR ADC using the binary-with-compensation redundancy technique using compensative capacitors [2].

Figure 2.23 shows the error-correction logic of a 10-bit SAR ADC using the binary-with-compensation technique for redundancy, which uses 5 inverters, 9 full adders, 1 half-adder, and 10 multiplexers to convert the 13-conversion cycle output to a 10-bit output. The non-binary redundancy technique [4], for its part, requires

11 10-bit ROMs and arithmetic units to obtain a 10-bit result, leading to a cumbersome error-correction logic. Another error-correction scheme using the binary-with-compensation redundancy technique without additional compensative capacitors is shown in Figure 2.24. Its implementation requires two MUXs and 10 full adders to convert the 2 additional conversion cycle results to the desired 10-bit output.

Fig. 2. 24: An error-correction scheme for a 10-bit SAR ADC using the binary-with-compensation redundancy technique without additional compensative capacitors [42].

As long as the normalized analog input voltage is within the redundancy margin or error-tolerance range, the erroneous conversion result can be corrected. However, there should be no error in the last conversion cycle because there is no additional

cycle to correct the erroneous one. An error in the last conversion cycle will result in SNDR degradation.

Fig. 2. 25: Analysis of a 10-bit SAR ADC using the non-binary redundancy technique with a 12.7% redundancy margin.

Figure 2.25 illustrates the analysis done on the non-binary redundancy technique [4] that uses two additional cycles to obtain a 10-bit result. This example corrects two erroneous decisions. The example shown in Figure 2.25 features errors in conversion cycles two and six. The non-binary redundancy algorithm converges to the approximated analog input value with the help of eleven 10-bit ROMs and arithmetic units, which determine the DAC switching pattern and also form the error-correction logic. In order to achieve higher sampling speeds, error-correction data converters without additional cycles ($N+X$ cycles, where X is the number of additional cycles) for an N -bit resolution are desirable.

Other error-correction techniques, such as addition-only error correction (ADEC) [3], utilizing an offset DAC to generate M.5-bit/stage and then M-bit/stage redundancy [16], and a redundancy-facilitated background-error detection and

correction scheme [5], have been published. There is room for improvement in terms of reducing chip area, power consumption, the number of additional conversion cycles, DAC size, error-correction logic, and control-logic overhead. These are some of the parameters taken into consideration in the work described in this thesis.

2.3.4 DAC Switching Techniques

The DAC switching scheme plays an important role in determining SAR ADCs' overall energy consumption, DAC area, SAR control-logic complexity, reference voltage design, and linearity.

Integral non-linearity (INL) and differential non-linearity (DNL) are two key linearity parameters for a data converter. To achieve better linearity with no missing codes, large unit capacitors are often used to minimize mismatch, which results in increasing the chip area. DAC calibration techniques [45, 46] can also be used to achieve up to 12-bit linearity. Switching schemes such as correlated reverse switching [31] can reduce the maximum $\sigma_{\text{INL, best-fit}}$ and σ_{DNL} by a factor of $\sqrt{2}$ or more. Furthermore, non-binary techniques can be combined with DAC calibration to achieve superior static linearity performance when a generalized non-binary algorithm is used [45–49].

Table 2.4 summarizes and compares 10 switching schemes based on their switching energies, CDAC area requirement, control-logic complexity, and accuracy requirement regarding V_{cm} reference voltage. The common-mode voltage, the V_{cm} of the differential DAC arrangement voltage waveforms shown in Figure

2.26, should ideally remain constant throughout the conversion cycles in order to provide robust ADC operation. Changing the common-mode voltage to the input of the comparator affects the comparator dynamic offset and the input referred noise of the comparator, which negatively affects the robustness of SAR ADC operation. In general, the number of CDAC switches increases with the resolution of the CDAC and the number of reference voltages implemented. SAR logic complexity varies between different switching schemes and can be implemented with low to moderate digital complexity. The switching scheme also plays a part in determining the overall hardware overhead for an error-correcting SAR ADC. This is further explained in the following section 2.3.5.

Fig. 2. 26: The waveform of V_{cm} -based switching scheme [50] for a 6-bit SAR ADC.

Reducing switching energy and maintaining DAC metal-routing symmetricity and a constant common-mode operation for a multi-bit per cycle conversion with redundancy has its own challenges. Extra energy is required to create the required redundancy margins by switching additional capacitors in the CDAC array. An

appropriate switching scheme to mitigate these challenges without any significant hardware overhead or arithmetic units is required to achieve the goal of a low-power, high-speed, single-channel SAR ADC. This thesis proposes two new DAC switching schemes for a multi-bit/cycle SAR ADC with redundancy that will address the need for an appropriate switching scheme to mitigate these challenges.

Table 2. 4: A parameter comparison of various single-bit per cycle CDAC switching schemes.

Switching scheme	CDAC area reduction	Average switching Energy (CV_{ref}^2)	Energy saving	Accuracy requirement on V_{cm}	Logic complexity
Conventional [51]	Reference	1363.4	Reference	Not used	Low
Cap splitting [51]	-	852.3	37.49%	Not used	Low
V_{cm} based [18]	50%	170.2	87.52%	From MSB	Low
Set and down [19]	50%	255.5	81.26%	Not used	Low
Higher-side-reset-and-set [56]	50%	106.2	92.21%	From MSB	Medium
Tri-level [52]	75%	42.4	96.98%	From MSB	Medium
V_{cm} based monotonic [53]	75%	31.9	97.66%	From MSB	Medium
Sanyal and Sun [54]	75%	21.3	98.43%	From 3 rd bit	Low
Xingyuan and Zhang [55]	75%	15.8	98.84%	From 3 rd bit	Medium
Rahimi and Yavari [50]	75%	84.9	93.77%	From MSB but low dependence (only LSB)	Low

2.3.5 Hardware Overhead: Redundancy, Error Correction, and the DAC Switching Scheme

Table 2. 5: Comparison of various parameters, including hardware overhead, for error-correcting SAR ADCs.

	Non-binary <i>ISSCC'02 [4]</i>	Binary with compensation <i>ISSCC'10 [2]</i>	ADEC <i>JSSC'11 [3]</i>
Switching scheme	Conventional	Set and down	Straightforward
Control logic	ROM, decoder, arithmetic Unit, MUX	Transistor logic based on counter, comparator, async. timing logic	Transistor logic based on counter, comparator, timing logic, MUX
In-built DAC redundancy	No, digital part does the compute	No, uses compensation level shift instead	Yes
Error-correction logic	11- 10b ROM, Arithmetic Unit	5 INV, 9 F.A, 1 H.A, 10 MUX	1 F.A, 6 H.A
# Additional cycles	2	3	2
# CDAC switches (single ended ver.)	774	25	61
# Reference voltages	2	2	3
Redundancy	12.7%	12.5%	3.125%
Speed (MHz) / resolution (bits)	30 / 10	100 / 10	40 / 10
ENOB	>8.01	>9.01	8.11

Table 2.5 shows that the relation between the type of redundancy used and other parameters such as control logic complexity, error-correction logic complexity, number of additional conversion cycles, and overall sampling speed. The additional conversion cycles for binary-with-compensation [2] and ADEC [3] techniques are used to level-shift the comparison threshold so that an erroneous decision (within the redundancy margin) in any previous conversion cycle can be corrected. For the non-binary redundancy [4] technique, the number of additional conversion cycles depends on the amount of redundancy used. For a 12.7% non-binary redundancy, a total of 12 conversion cycles would be required to converge to the approximated analog input voltage value with a 10-bit precision.

The number of CDAC switches depends on the switching scheme, the number of reference voltages utilized, and the DAC architecture. The DAC architecture for a non-binary implementation uses a thermometer-coded CDAC for better linearity, and the number of switches used is therefore high: 774. The ADEC [3] technique uses a split capacitor CDAC and bottom-plate sampling, which increases the number of switches when compared to the binary-with-compensation technique, which uses top-plate sampling and two reference voltages. Although the binary-with-compensation technique uses fewer CDAC switches, its CDAC switching scheme results in large common-mode variation to the comparator's input.

Chapter 3

Specifications

This chapter discusses the noise-budget specification and some design choices made in order to achieve the target specifications of the 10-bit SAR ADC designed as part of this thesis.

3.1 Noise Budget

Fig. 3. 1: A simplified ADC model with noise sources.

The noise sources for a successive-approximation register ADC are shown in Figure 3.1. The figure ignores phase-locked loop (PLL) noise contribution. HD_3 represents the third harmonic of the input sinusoidal signal. The differential arrangement of the proposed architecture will ideally cancel the even-order harmonics, resulting in the third harmonic dominating the ADC noise floor. Random jitter is added to the ideal clock, resulting in an aperture error of the sampled signal. Thermal noise is added due to the charge-redistribution based capacitive DAC, and a sample-and-hold switch that is used to sample the filtered

input signal. Non-linearity such as integral non-linearity (INL), differential non-linearity (DNL), and offset errors also contribute to the overall noise in an ADC.

The DNL noise is assumed to be $\frac{1}{2}$ LSB uniformly distributed and is equal to the quantization noise shown in equation 3.1. P_q represents the quantization noise voltage. A 1.2V positive reference voltage and a 10-bit quantizer is used for calculating the quantization noise. This results in a 0.338mVrms contribution of both quantization and DNL noise towards the total noise budget.

$$\sqrt{P_q} = \sqrt{\frac{1}{12}} \cdot \frac{1.2V}{2^{10}} = 0.338mVrms \quad (3.1)$$

$$\sqrt{P_q} = \sqrt{P_{DNL}} = 0.338mVrms \quad (3.2)$$

3.1.1 Timing Noise: Aperture Error

There are several types of jitter from a PLL that contribute to timing noise such as period, accumulated, and long-term jitter. However, aperture uncertainty or aperture error is one of the parameters that set the limit of achievable SNR. Hence, additional importance is given to the sampling instance where the positive edge of the sampling clock arrives. A tradeoff between input frequency (f_{in}), jitter (σ_t), the size of the buffer inverter, and supply noise is done to achieve the desired performance for a 10-bit 160 Msps SAR ADC.

$$SNR_{Aperture} [dB] = 20 \cdot \log \left[\frac{1}{2\pi f_{in} \sigma_t} \right] \quad (3.3)$$

$$\Delta v_{in} = \frac{\partial v_{in}}{\partial t} \cdot \Delta t \quad (3.4)$$

Equation 3.3 shows the tradeoff between SNR, input frequency, and timing jitter. The technology-dependent rise time of the inverter also sets the jitter specification. In one example, a supply noise of 20 mv for a supply of 1V and an inverter rise time of 10 psec yields a jitter of 0.2 psec. In order to reduce the rise time, a large sized inverter should not be used because the inverter has a poor power-supply-rejection ratio (PSRR) and the supply noise contribution to jitter could dominate the overall jitter. Alternate solutions to sizing up the inverter can be using a lower (better) transistor fabrication node where the inverter rise time is less, or reducing the supply noise. Equation 3.4 shows the relation between aperture uncertainty and its translation into a change in input voltage. Δt represents the aperture uncertainty, and Δv_{in} represents the change in input voltage during Δt . We ensure that the sampling clock edge jitter does not set the SNDR ceiling. The wideband noise on the clock or aperture uncertainty manifest as wideband periodic noise around the sampling rate. Figure 3.2 shows the theoretical limit of the SNDR, imposed by jitter values of 1 psrms and 0.1 psrms in published papers from 1997 onwards [30].

Using equation 3.3 for an 80 MHz sinusoidal signal with a 1 psrms jitter on the sampling clock results in an achievable SNDR of -65.97 dB. This is sufficient for our 10-bit ADC and does not result in aperture error setting the limits on the SNDR.

Fig. 3. 2: The theoretical limit of the SNDR, imposed by jitter in published papers from 1997 onwards [30].

3.1.2 Thermal Noise

Thermal noise is due to the sample-and-hold switch, which samples the analog input voltage on a capacitor. Equation 3.5 shows the relation between thermal noise ($\overline{v_n}$) and the sampling capacitor (C). Here, k represents the Boltzmann constant and T represents temperature. Since a charge redistribution principle based CDAC is used and the input voltage is sampled using the same CDAC, the total CDAC size is important as it sets the thermal noise for the required 10-bit resolution. The analysis in section 3.2 was used to determine the size of the unit capacitor. The charge redistribution CDAC uses 512 unit capacitors, resulting in a CDAC size of 378.88fF. At a temperature of 300 Kelvin, the thermal noise value is 104.56 μ Vrms.

$$\overline{v_n} = \sqrt{\frac{kT}{C}} \quad (3.5)$$

3.2 Capacitor sizing

The unit capacitor (C_u) value is calculated from the derivation shown below. Yield and acceptable thermal noise for a 10-bit SAR ADC are considered [70]. Equation 3.6 represents the standard deviation of maximum differential non-linearity (DNL). σ_u is the standard deviation of unit capacitor, and N is the resolution or the number of bits. Equation 3.7 represents the standard deviation of maximum integral non-linearity (INL).

$$\sigma_{DNL,max} = \frac{\sigma_u}{C_u} \cdot \sqrt{2^N - 1} \quad (3.6)$$

$$\sigma_{INL,max} = \frac{\sigma_u}{C_u} \cdot \sqrt{2^{N-1}} \quad (3.7)$$

Standard deviation of capacitor mismatch is given by equation 3.8.

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K_\sigma}{\sqrt{A}} \quad (3.8)$$

We use the foundry data provided for the MIM capacitor.

$$C_u = K_C \cdot A \quad (3.9)$$

$$\frac{\sigma\left(\frac{\Delta C}{C}\right)}{\sqrt{2}} = \frac{\sigma_u}{C_u} \quad (3.10)$$

In equations 3.8, 3.9, and 3.10, the variable K_σ represents the matching coefficient for the capacitor, K_C is the capacitor density parameter, A is the area of the capacitor, and $\sigma\left(\frac{\Delta C}{C}\right)$ is the standard deviation of a capacitor mismatch. We assume that DNL limits capacitor matching. In order to maximize the silicon yield, equation 3.11 is used [70].

$$\sigma_{DNL,max} < \frac{1}{3} LSB \quad (3.11)$$

Equations 3.8, 3.10, and 3.11 are used to calculate the lower boundary for a mismatch limited unit capacitor, shown in equation 3.12.

$$C_u = 18 \cdot (2^{N-1}) \cdot K_\sigma^2 \cdot K_C \quad (3.12)$$

Fig. 3. 3: The foundry measurement and simulation results of 1,000 random Monte

Carlo tests for a MIM capacitor of $2 \frac{fF}{\mu m^2}$.

We substitute the technology parameters for the TSMC 65 nm 1P9M mixed-signal RF CMOS technology in equation 3.12 to calculate the unit capacitor value. K_σ is 0.86% μm , and K_c is 2 fF/ μm^2 . K_σ is calculated from the slope of the line shown in Figure 3.3. The unit capacitor value for a single-ended implementation is 1.363 fF. Since our architecture uses a differential DAC, the new unit capacitor value is half of that required for a single-ended implementation. Therefore, the minimum unit capacitor value for a differential CDAC arrangement is 0.68 fF.

3.3 Asynchronous Timing

For a low-power, high-speed data converter design, it is beneficial to adopt an asynchronous timing architecture. With a synchronous timing scheme, each conversion cycle duration has to cater to the worst-case comparator regeneration time, which in turn depends on the comparator's metastability condition. This leads to reduction in the ADC sampling rate, as comparator metastability does not occur in all conversion cycles. In addition, the high-frequency clock required makes the PLL design stringent and requires very low jitter. Jitter on the clock edge causes aperture uncertainty and sets the limit of achievable SNDR.

Equation 3.13 shows the total time (T) required to convert an analog input to a digital one. Here, f_s denotes the sampling frequency of the ADC.

$$T = \frac{1}{f_s} = \frac{1}{160\text{MHz}} = 6.25\text{ns} \quad (3.13)$$

We allocate 1.2 ns for sampling the analog input signal. This leaves 5.05 ns for completing all the nine conversion cycles required for our proposed architecture.

Each conversion cycle comprising of the DAC settling time, SAR logic delay, and the comparator regeneration time has only 561 ps to complete. The redundancy margin implementation helps to relax the DAC settling requirement. We allocate 200 ps for the DAC settling time, 161 ps for the comparator regeneration time, and 200 ps for the SAR control logic.

Selecting a multi-bit per cycle architecture requires a region detection logic, and this consumes part of the time available for SAR logic delay. Hence, we have to simplify the method of adding a redundancy margin to the DAC-generated comparator thresholds so that the operation can be completed in the remaining time available for SAR control logic. With our 160 MSps SAR ADC, it is not possible to use an adder and a subtractor to compute the DAC switching pattern and meet the SAR logic-delay requirements. This necessitates a new switching scheme that does not require an arithmetic unit. A constant common-mode fractional reference voltage switching scheme that meets this requirement is described in section 4.3 of this thesis.

In our design, the 10-bit error-corrected SAR output is valid after the falling edge of the sampling clock. This gives approximately 1.2 nsec for the error-correction circuit block to compute the final output.

Chapter 4

Redundancy, Error Correction & the DAC Switching Scheme

The following aspects were taken into consideration while designing a multi-bit per cycle SAR ADC with redundancy:

- Optimizing the use of redundancy.
- Selecting an appropriate redundancy margin or % redundancy so that no extra conversion cycles are required.
- The possibility of trading off redundancy margins for circuit non-linearity.
- Embedding redundancy within the DAC for reducing hardware overhead. For example, avoiding the use of arithmetic unit to compute the CDAC switching pattern.
- Using binary-scaled capacitive DAC without any modifications or extra capacitors.
- The inherent error-correction capability of the SAR ADC.
- Simplified error-correction logic and the ability to correct multiple erroneous decisions.
- Constant common-mode CDAC operation.
- Reducing the switching energy for multi-bit per cycle conversion.
- Reducing the CDAC size without affecting the performance of the converter.

4.1 Proposed Redundancy Concept

Figure 4.1 shows the top-level architecture of the proposed 10-bit SAR ADC, which uses an initial 1-bit conversion cycle followed by eight conversion cycles with 1.5-bit operation. The last conversion cycle does not require a 2-bit operation to achieve a 10-bit resolution, therefore removing the need for an additional comparator if threshold interpolation technique is implemented.

Fig. 4. 1: Top-level architecture of a 10-bit SAR using the proposed 1.5-bit/cycle technique.

The number of additional conversion cycles required depends on the extent of the redundancy margin selected. Converting the additional conversion cycle output to the desired resolution, in certain cases could make the error-correction logic cumbersome. In the proposed SAR ADC, the 1.5-bit/cycle operation enables a 12.5% redundancy margin. The 12.5% redundancy margin or the error tolerance range provides the ability to correct multiple erroneous decisions. Here, the error

tolerance range remains fixed, independent of where the conversion cycle errors occurs.

Fig. 4. 2: Example of 5-bit SAR ADC using proposed 1.5-bit/cycle technique.

Figure 4.2 shows an example of 5-bit SAR ADC using the proposed redundancy concept. A 1.5-bit/cycle setup requires two comparator thresholds and results in

three asymmetric binary coded decision regions, i.e., “00”, “01”, and “10”. The initial 1-bit conversion cycle results in two binary coded decision regions, i.e., “0” and “1”. The black triangles from conversion cycle 3 (P3) shows the extra input range occupied by the decision regions ‘00’ and ‘10’. The 12.5% redundancy margin in the second conversion cycle (P2) results in a 2LSBs CDAC voltage settling relaxation. The full scale (input range) of the second conversion cycle is divided into four decision regions by three decision thresholds. These three decision thresholds are then offset by $1/8V_{ref}$ in order to obtain the two comparator thresholds for the 1.5-bit/cycle operation. This decision offset scales by two, cycle-by-cycle, from P2 onwards. The 12.5% redundancy margin in conversion cycle 3 provides an overlap with the full scale of conversion cycle 2. This overlap provides the ADC an opportunity to correct any errors and to converge to the approximated analog input value within a $\frac{1}{2}$ LSB precision. There are two cases elaborated in the Figure 4.2, with and without DAC settling errors. It can be noticed that the final digital output $D_1D_2D_3D_4D_5$ remains the same irrespective of the erroneous conversion cycle. The CDAC decision thresholds for the 5-bit operation are shown in the figure 4.2.

Table 4.1 summarizes the cycle-specific redundancy margins implemented using an unmodified binary-scaled CDAC for a 10-bit SAR ADC. A 12.5% redundancy margin for the second conversion cycle results in a CDAC voltage settling relaxation of ± 32 LSBs, which translates to saving 4.16 time constants (Equation 4.1). A 35.38% overall ADC speed advantage is gained when compared to a non-redundancy 1-bit/cycle SAR ADC (sampling time is excluded).

Equation 4.1 provides the relation between the time required for an N-bit DAC to settle within ½LSB precision. Where, T is the total DAC settling time, τ is the time constants, and 2^N is the conversion range in LSBs

$$T = \tau \cdot \ln\left(\delta \cdot \frac{1}{2^N}\right) \quad (4.1)$$

Table 4. 1: Redundancy (in LSB) by conversion cycle.

Conversion cycle	1	2	3	4	5	6	7	8	9
Redundancy (LSB)	-	64	32	16	8	4	2	1	0.5

Fig. 4. 3: Decision regions and the redundancy margin for a 10-bit SAR ADC.

Figure 4.3 shows the redundancy margin for the CDAC generated comparator thresholds. A capacitor mismatch within a CDAC will result in a small variation in the CDAC-generated comparator threshold. An assumption is made that one-fourth of the redundancy margin is utilized due to the capacitor mismatch after the fabrication of the chip.

In order to reduce the hardware overhead related to implementing redundancy, the proposed constant common-mode fractional reference voltage (CCM-FRV) switching scheme uses an unmodified binary-scaled CDAC to generate the 12.5% redundancy margin. Hence, the CCM-FRV switching scheme maintains a symmetric CDAC metal routing and does not affect static or dynamic performance. Irrespective of erroneous decisions, at the end of the ninth conversion cycle the CCM-FRV switching scheme enables the CDAC-generated comparator thresholds to converge to the normalized analog input voltage value. The simplicity of the CCM-FRV switching scheme allows for the generation of the DAC switching pattern without requiring arithmetic units, decoders, ROMs, or complex control-logic overhead.

4.2 Proposed Error Correction

The 1.5-bit/stage specification is a prominent feature of pipeline ADCs. In the proposed SAR ADC architecture, the 1.5-bit/cycle operation does not require inter-stage residue amplifiers. The concept of error correction is borrowed from a 1.5-bit/stage pipeline ADC. Any errors within the redundancy margin (i.e., 12.5% error tolerance range) can be corrected. However, any error in the last conversion cycle will lead to degradation in the SNDR because there is no subsequent cycle to correct it.

As mentioned in section 2.3.3, for a high-speed SAR ADC, the first four conversion cycles are critical because this is when the ADC is most likely to make multiple erroneous decisions. Additional errors can occur in the remaining conversion cycles due to noise coupling from supply rails, or reference voltages

and the metastability of the comparator. Figure 4.4 shows an example where two errors occur during the first four conversion cycles and another two during the remaining conversion cycles. The occurrence of comparator metastability can result in an erroneous decision. As long as the metastability event occurs when the normalized analog input voltage is within the redundancy margin, the erroneous decision can be corrected.

Different CDAC switching procedures enable the representation of a single analog input value using different digital codes. This technique provides an opportunity for an error to propagate to the subsequent conversion cycle where it can be corrected. A bit-overlap-and-add digital error correction technique is used to achieve the above-mentioned error-correction capability. Therefore, the proposed architecture possesses an inherent error-correction capability and does not require additional conversion cycles.

Fig. 4. 4: The error-correction logic and its implementation.

Figure 4.4 shows the ripple-carry adder circuit for implementing the 1.5-bit/cycle digital error correction. Seven full adders (F.A) and two half-adders (H.A) are used. The bit-overlap-and-add operation begins from the third conversion cycle. A

logic “1” is added to the bit B_9 . The MSB of the error-corrected output is the 1-bit output of the first conversion cycle.

Ideally, there should be no overflow from the H.A, which adds the bit A_2 and carry generated from the previous F.A. This overflow pin was monitored during testing, and no overflow was detected.

Fig. 4. 5: An example of the proposed error-correction technique.

Figure 4.5 illustrates an example of a conversion with four erroneous decisions made during conversion cycles 2, 4, 6, and 8. These four erroneous decisions are corrected within the nine conversion cycles. For conversion cycle 2, the correct decision region should be “01”, but due to a voltage settling error, a “00” was detected. Due to the 12.5% redundancy, an incorrect decision of up to $704+32$ LSBs can be corrected in the next conversion cycle, i.e., cycle 3. Similarly, an incorrect decision is made in cycle 4, and since the normalized analog input of 725.5 LSBs is within the error-correction limits ($720+8$ LSBs), cycle 5 corrects the incorrect decision. The third incorrect decision is made in conversion cycle 6 and is corrected during cycle 7. Finally, the erroneous decision in conversion cycle 8 is

Another error-correction example is shown in Figure 4.6, where the normalized analog input value of 204 LSBs is converted into a corresponding digital code, correcting one erroneous decision.

The 1.5-bit/cycle transfer function for the proposed SAR ADC is shown in Figure 4.7. Since there is no residue amplification stage used, the transfer function varies with the past comparator decisions. The transfer function of the second conversion cycle (Figure 4.7) depends on the comparator output of the first cycle, A_1 . When $A_1=1$, the two decision thresholds, $3/8V_{ref}$ and $5/8V_{ref}$ for 1.5-bit conversion are found by offsetting the three decision thresholds ($1/4V_{ref}$, $1/2V_{ref}$, and $3/4V_{ref}$) of a 2-bit conversion and neglecting the third threshold. Since there is no decision threshold at $1/8V_{ref}$ and $7/8V_{ref}$, larger input voltage range is covered by digital outputs '00' and '10' when compared to digital output '01'. The larger input voltage range (i.e., black triangles) is shown in figure 4.2.

4.3 Proposed Constant Common-mode Fractional Reference

Voltage Switching Scheme

In this section, a new switching scheme is proposed to generate redundancy margins without changing the differential DAC's common-mode voltage and without using a split capacitor or an additional capacitor bank. A fixed common-mode voltage is beneficial as it preserves the comparator offset voltage correction, which is usually done before the start of a new conversion cycle. Additionally, the root mean square thermal noise due to the input pair of the preamplifier has a fixed value at a given common-mode voltage. Hence, a constant common-mode operation does not influence the conversion cycle's output and provides a robust SAR ADC operation.

The 1.5-bit/cycle operation enables a 12.5% redundancy margin, which is implemented by a charge-redistribution-based CCM-FRV switching scheme. The two CDACs are independently switched to generate the two comparator thresholds required for 1.5-bit/cycle operation.

Fig. 4. 8: Proposed CCM-FRV switching procedure for a 4-bit SAR ADC using 1.5-bit/cycle technique.

Figure 4.8 shows the 1.5-bit/cycle operation for a 4-bit SAR ADC. First, the differential input signal is bottom plate sampled (sampling phase) while the top plate is connected to Vcm common-mode voltage. In the next step, the bottom

plate is connected to V_{cm} and after providing sufficient voltage settling time, the first decision bit A_1 is obtained. The capacitors responsible to create the redundancy margin are “pre-set” to either reference voltages $1/4V_{ref}$ (i.e, V_{OFFn}) or $3/4V_{ref}$ (V_{OFFp}). The pre-set occurs immediately after the comparator regeneration with the help of cycle specific token signals. This technique helps to create the redundancy margin in advance such that when the capacitors are “set” to either V_{CM} , V_{REFp} or gnd (V_{REFn}) reference voltages, these voltages can settle within the created redundancy margin. Depending on the output of second conversion cycle (A_2B_2), the figure 4.8 illustrates the CDAC switching procedure where one of the three reference voltages V_{CM} , V_{REFp} or gnd (V_{REFn}) are used to create the next conversion cycle’s decision thresholds.

The following paragraphs describe the CCM-FRV switching scheme for the proposed 10-bit SAR ADC using 1.5-bit/cycle operation. Figure 4.9 illustrates the single-ended version of the CCM-FRV switching scheme. The analog input voltage is bottom-plate sampled onto the capacitive DAC, while the V_{TOPCM} (common-mode voltage) is applied to the top plate. This sampling operation is illustrated in Figure 4.9(a). The positive DAC samples the analog input negative voltage (V_{in}), while the negative DAC samples the analog input positive voltage (V_{ip}).

The first conversion cycle is shown in Figure 4.9(b). The CDAC’s bottom plate is connected to V_{cm} ($1/2 V_{REFp}$) reference voltage results in dividing the 1024 LSBs full scale into two regions. After providing sufficient voltage settling time, the first comparator is turned on to implement a 1-bit conversion cycle.

Figure 4.9(c) shows the second conversion cycle. Depending on the output of the first conversion cycle, the MSB capacitor is connected to either V_{REFp} or V_{REFn} (i.e., GND) reference voltages. The MSB-1 capacitor is used to generate the required 12.5% redundancy margin. The MSB-1 capacitor in the CDAC1 and the CDAC2 is switched to V_{OFFn} ($\frac{1}{4} V_{REFp}$) and V_{OFFp} ($\frac{3}{4} V_{REFp}$), respectively. This step creates the two thresholds required for 1.5-bit/cycle operation. The redundancy margins are fixed throughout the nine conversion cycles.

Figure 4.9(d) illustrates the switching procedure for the third conversion cycle. The MSB-2 capacitor in the CDAC1 and the CDAC2 is switched to V_{OFFn} ($\frac{1}{4} V_{REFp}$) and V_{OFFp} ($\frac{3}{4} V_{REFp}$), respectively, to create the required 12.5% redundancy margin. This step divides the amount of redundancy of the previous conversion cycle by two. Since the second conversion cycle's output is "00", the MSB-1 capacitor is connected to V_{REFp} .

Figure 4.9(e) illustrates the switching procedure for the fourth conversion cycle. The MSB-3 capacitor in the CDAC1 and the CDAC2 is switched to V_{OFFn} ($\frac{1}{4} V_{REFp}$) and V_{OFFp} ($\frac{3}{4} V_{REFp}$), respectively, to create the required 12.5% redundancy margin. This step divides the amount of redundancy of the previous conversion cycle by two. Since the third conversion cycle's output is "10", the MSB-2 capacitor is connected to V_{REFn} .

Similarly, the 12.5% redundancy margins for the fifth conversion cycle are created by connecting the MSB-4 capacitor in the CDAC1 and the CDAC2 to V_{OFFn} ($\frac{1}{4}$

V_{REFP}) and V_{OFFP} ($\frac{3}{4} V_{REFP}$). Since the output of the fourth conversion cycle is “01”, the MSB-3 capacitor is connected to the V_{cm} reference voltage.

The differential CDAC1 and CDAC2 top-plate waveform for the proposed switching scheme is illustrated in Figure 4.9. A binary output of “00”, “01”, and “10” represents the CDAC1 and CDAC2 top-plate voltages going “down”, “remain”, and “up”.

(a)

(b)

(c)

(d)

(e)

Fig. 4. 9: A single-ended version of the CCM-FRV switching scheme (a) sampling phase (b) conversion cycle 1 (c) conversion cycle 2 (d) conversion cycle 3 and (e) conversion cycle 4.

Fig. 4. 10: The CCM-FRV switching scheme waveform.

Tables 4.2 and 4.3 summarize the DAC switching to implement the CCM-FRV switching scheme. The capacitors in the binary-scaled array are switched depending on the conversion-cycles comparators output. For example, if the comparators output for conversion cycle 2 is “00”, then the $128C_U$ and $64C_U$ capacitors in the CDAC1 are connected to the reference voltage V_{REFp} (2) and V_{OFFn} (5), respectively. V_{OFFn} and V_{OFFp} serve as the fractional reference voltages. Here, $V_{CM} = \frac{1}{2} V_{REFp}$; $V_{OFFn} = \frac{1}{4} V_{REFp}$; $V_{OFFp} = \frac{3}{4} V_{REFp}$; $V_{REFn} = GND$ (0 V); and $V_{REFp} = 1.2$ V.

Table 4. 2: A CCM-FRV switching scheme table for the CDAC1.

CDAC 1 (Positive)	2^{N-2} $128C_U$ $+128 C_U$	2^{N-3} $128C_U$	2^{N-4} $64C_U$	2^{N-5} $32C_U$	2^{N-6} $16C_U$	2^{N-7} $8C_U$	2^{N-8} $4C_U$	2^{N-9} $2C_U$	2^{N-10} C_U	2^0 C_U
Sampling	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}
Cycle 1	1	1	1	1	1	1	1	1	1	1
Cycle 2	2; 3	5	1	1	1	1	1	1	1	1
Cycle 3	2; 3	2; 1; 3	5	1	1	1	1	1	1	1
Cycle 4	2; 3	2; 1; 3	2; 1; 3	5	1	1	1	1	1	1
Cycle 5	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	5	1	1	1	1	1
Cycle 6	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	5	1	1	1	1
Cycle 7	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	5	1	1	1
Cycle 8	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	5	1	1
Cycle 9	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	5	1
Comparator output	0; 1	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	

Where 1= V_{CM} ; 2= V_{REFp} ; 3= V_{REFn} ; 4= V_{OFFp} ; 5= V_{OFFn} .

Table 4. 3: A CCM-FRV switching scheme table for the CDAC2.

CDAC 2 (Positive)	2^{N-2} $128C_U$ $+128 C_U$	2^{N-3} $128C_U$	2^{N-4} $64C_U$	2^{N-5} $32C_U$	2^{N-6} $16C_U$	2^{N-7} $8C_U$	2^{N-8} $4C_U$	2^{N-9} $2C_U$	2^{N-10} C_U	2^0 C_U
Sampling	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}
Cycle 1	1	1	1	1	1	1	1	1	1	1
Cycle 2	2; 3	4	1	1	1	1	1	1	1	1
Cycle 3	2; 3	2; 1; 3	4	1	1	1	1	1	1	1
Cycle 4	2; 3	2; 1; 3	2; 1; 3	4	1	1	1	1	1	1
Cycle 5	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	4	1	1	1	1	1
Cycle 6	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	4	1	1	1	1
Cycle 7	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	4	1	1	1
Cycle 8	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	4	1	1
Cycle 9	2; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	2; 1; 3	4	1
Comparator output	0; 1	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	00; 01; 10	

Where 1= V_{CM} ; 2= V_{REFp} ; 3= V_{REFn} ; 4= V_{OFFp} ; 5= V_{OFFn} .

4.4 Redundancy Optimization

All nine conversion cycles can use the 1.5-bit/cycle technique, but in order to optimize the use of redundancy, the initial conversion cycle uses a 1-bit conversion. There are four reasons for choosing 1-bit conversion as part of the design. First, the differential CDAC architecture cancels any noise from the V_{CM} reference voltage used in the CCM-FRV switching scheme. Second, the first conversion cycle only compares the differential analog input voltages (i.e., if $V_{ip} > V_{in}$) and does not depend on the accuracy of the V_{CM} reference voltage. Third, the small CDAC size of 379 fF and the adequate CDAC voltage settling time ensure that no erroneous decisions are made due to incomplete voltage settling. Fourth, the input-referred noise of the comparator is kept at less than $\frac{1}{2}$ LSB. These four reasons remove the probability of an erroneous first conversion cycle.

The benefits of using an initial 1-bit cycle include saving switching energy, additional transistor-switches to implement a redundancy margin for the first conversion cycle, and comparator power for one comparison.

4.5 CDAC Size Reduction & Associated Hardware Overhead

Table 4.4 compares the hardware overhead associated with various redundancy and error-correction techniques. The hardware overhead also determines the attainable data-converter sampling speed, energy consumption, and overall chip area. The switching scheme, along with the number of reference voltages, determines the complexity of the control logic, the number of switches, the DAC size, and the switching energy. A difference in the above-mentioned parameters can be noticed

between the implementation of the proposed 1.5-bit/cycle technique using a conventional switching scheme and our proposed CCM-FRV switching scheme.

The conventional switching scheme [51] when modified to implement a 1.5-bit/cycle technique uses two reference voltages (V_{REFp} and V_{REFn}), an arithmetic unit, and ROM in order to generate the CDAC switching pattern required to generate the two comparator thresholds. Implementing an arithmetic unit requires additional power from the control-logic circuit block. Furthermore, in a high-speed ADC, the arithmetic unit can become a speed bottleneck.

The CCM-FRV switching scheme saves 50% of the CDAC area when compared to a conventional switching scheme [51] implementing an identical redundancy technique. Reducing or adding reference voltages is of limited value. The CCM-FRV switching scheme uses two additional reference voltages, V_{OFFp} and V_{OFFn} , which are only used to generate redundancy margins. It is possible to use only three reference voltages (V_{REFp} , V_{REFn} , and V_{CM}) to implement a 1.5-bit/cycle technique, but this reduction in reference voltages results in either increasing the CDAC size by 1-bit (i.e., 100% increase) or a slight change in the CDAC common-mode voltage. A reduction in reference voltages only reduces the number of switches from 89 to 81 (without splitting the MSB capacitor).

Our technique can correct multiple errors while also reducing the CDAC size, not requiring additional conversion cycles and further simplifying the digital error correction logic. The downside of using a 1.5-bit/cycle approach is that it requires two CDACs, twice the number of CDAC switches, and two comparators. Our

design, however, addresses the first issue and suggests layout technique for the second issue. The proposed switching scheme reduces the CDAC size, hence mitigating the chip area penalty due to a second CDAC. Similar to Franz's work [4], the additional CDAC switches can be laid out under the CDAC with metal shielding. The second comparator is a necessity for 1.5-bit/cycle operation and cannot be avoided.

The ADEC digital error correction technique requires additional MUX delay in the control-logic path and therefore reduces the overall attainable sampling speed when compared to the binary-with-compensation [2] or our proposed technique.

Table 4. 4: A comparison of various parameters, including hardware overhead,
among error-correcting SAR ADCs.

	Non-binary <i>ISSCC'02 [4]</i>	Binary with compensation <i>ISSCC'10 [2]</i>	ADEC <i>JSSC'11 [3]</i>	1.5-bit conversion (optional config.)	Proposed 1.5- bit conversion
Switching scheme	Conventional	Set and Down	Straightforward	Conventional (modified)	CCM-FRV
Control logic	ROM, decoder, arithmetic unit, MUX	Transistor logic based on counter, comparator, async. timing logic	Transistor logic based on counter, comparator, timing logic, MUX	ROM, Arithmetic Unit, Region Detection, Counter, Timing logic, MUX	Transistor logic based on sequencer (3-bit counter), region detection, async. timing logic
In-built DAC redundancy	No, digital part does the compute	No, uses compensation level shift instead	Yes	No, digital part does the compute	Yes
Error- correction logic	11- 10b ROM, arithmetic unit	5 INV, 9 F.A, 1 H.A, 10 MUX	1 F.A, 6 H.A	7 F.A, 2 H.A	7 F.A, 2 H.A
# Additional cycles	2	3	2	0	0
# CDAC switches (single ended ver.)	774	25	61	59	97/89 (with/without MSB splitting)
# Reference voltages	2	2	3	2	3+2
Redundancy	12.7%	12.5%	3.125%	12.5%	12.5%
Speed (MHz) / resolution (bits)	30 / 10	100 / 10	40 / 10	-	150 / 10

Design & Implementation of a SAR ADC with Redundancy & Error Correction

5.1 ADC Architecture

Fig. 5. 1: The architecture of an asynchronous SAR ADC with digital error correction.

The proposed SAR ADC implements an initial 1-bit conversion cycle followed by eight cycles of 1.5-bit conversion to achieve a 10-bit resolution. The initial cycle has zero redundancy, hence the 1-bit conversion. The ADC is based on simple building blocks, shown in Figure 5.1. The system comprises of the following sub-blocks: a CDAC switch matrix, a bootstrap sampling switches, CDACs, an asynchronous timing generator, a sequencer, comparators, control logic, region detection, thermometer-to-binary converter, memory, and error-correction logic.

Bootstrap switches are used for bottom-plate sampling on the positive edge of the sampling clock signal, *Clk S*. An event-based asynchronous timing generator is used to generate the high-frequency (9*150 MHz) comparator clock signals, *Clk Reset 1* and *Clk Reset 2*. This enables using a low-frequency clock signal, *Master Clk*, to initiate the ADC operation. The master clock frequency is equal to the sampling speed of the data converter. An event occurs when the comparator regenerates and provides an output, i.e., either the logic level “0” or “1”. The two comparators’ ready signals, *Ready’1* and *Ready’2*, are generated for the 1.5-bit conversion cycle. These comparator’ ready signals are then used to generate the comparator clocks for subsequent conversion cycles.

A sequencer implemented using a 3-bit counter keeps track of the conversion cycles. A typical SAR ADC keeps track of the conversion cycle because of a number of functions, such as storing the comparator output in the corresponding memory cell, and switching the CDAC based on the comparator output. The sequencer generates conversion-cycle-specific token signals, *Token 1* to *Token 9*. These token signals are used for two reasons: First, they activate parts of the control logic that are specific to a given conversion cycle. Second, they act as direct control signals for the CDAC MOSFET switch used to implement redundancy. By doing these two things, token signals not only reduce static current consumption but also simplify the control-logic hardware overhead for implementing a 1.5-bit per conversion cycle architecture. The signal *Counter Clk* is used to generate the token signals, while the comparator clock signal *Clk Reset 1* is used to create *Counter Clk*.

In our design, the 1-bit conversion yields two decision regions, i.e., “0” and “1”, and the 1.5-bit conversion cycle yields three decision regions: “00”, “01”, and “10”. A region-detection logic is used to find these binary-coded decision regions after the comparator’s output. These decision regions were previously shown in Figure 4.1. The proposed CCM-FRV switching scheme switches the appropriate capacitor within the CDAC to either a V_{CM} (0.6 V), V_{REFp} (1.2 V), or V_{REFn} (0 V) reference voltage. This switching depends on the decision region, and the logic is implemented by the switch controller. The CCM-FRV switching scheme maintains a constant common-mode operation throughout the SAR conversion cycles.

The comparator output is converted from thermometer code to binary code before being stored in the memory for an error-correction operation. No delay is added to the control-logic path, as this conversion logic is not a part of the SAR control logic. The sequencer generates the end-of-conversion signal *EOC*, and this signal clears any residue pulse remaining in the asynchronous timing generator. The memory contains the valid 10-bit error-corrected output after the falling edge of the signal, *Initial Pulse*.

5.2 Key Building Blocks and their Implementation

5.2.1 Asynchronous Timing Generator

Figure 5.2 shows the circuit schematic of the event-driven asynchronous timing generator based on the comparators’ ready signals, *Ready’1* and *Ready’2*, used to generate high-frequency internal conversion cycle clocks. In this design, each conversion cycle duration does not have to account for the worst-case comparator

regeneration time scenario. The comparator ready signal is generated from a digital OR gate connected to the inverted differential output of the comparator's second stage, the sense-amplifier-based latch shown in Figure 5.5. The falling edge of the comparator clock signals *Clk Reset 1* and *Clk Reset 2* is triggered by the comparators' ready signal. Two dynamic logic transistor branches are used on the left and right sides in Figure 5.2 to feed the comparators' ready signals. Before generating the comparator clock signal for the next conversion cycle, the transistor logic branches wait for the arrival of both of the comparators' ready signals. Any residue pulse in the asynchronous loop is terminated by the signal *Stop*.

Fig. 5. 2: The implementation of an asynchronous timing generator circuit.

Figure 5.3 shows the glitch-generation circuit used to generate the signal *Token 1 Clk*. The signal *Initial Pulse* is split into two replica signals, *Initial Pulse U* and *Initial Pulse L*. This is done due to layout placement constraints of the control logic of the two differential CDACs and the inverter drive capability of a single signal trace travelling to the control logics of both CDACs. As shown in Figure 5.3, a similar glitch-generation circuit is used to generate the signal *Counter Clk*. The ninth counter clock pulse triggers the end of the conversion signal, after which the error-correction circuit performs the bit-overlap-and-add operation.

Fig. 5. 3: The logic to generate the signal *Token 1 Clk*.

Figure 5.4 shows the timing diagram for the asynchronous timing generator circuit shown in Figure 5.2. The arrows in Figure 5.4 show the corresponding signal triggers based on falling or rising edge signals. The layout of the asynchronous timing generator uses a global double guard ring to collect minority carriers. A deep N-well boundary is used to isolate the high-frequency operating circuit layout from the rest of the data converter. The asynchronous timing generator circuit, including the clock buffers, occupy a chip area of $47 \times 14 \text{ } \mu\text{m}^2$.

Fig. 5. 4: A diagram of event-based asynchronous timing.

5.2.2 Comparator

A 3-stage comparator, shown in Figure 5.5 and comprising of a static preamplifier, a sense-amplifier-based latch, and an SR latch, is used. The static preamplifier uses a common-source amplifier topology with resistor as a load and an N-type input pair transistor to achieve the desired gain of 6 dB and 3 dB bandwidth (f_{3dB}) of 3.8 GHz. The preamplifier reduces the kickback noise generated by the second comparator stage, i.e., a high-gain dynamic sense-amplifier-based latch. The preamplifier also reduces the second comparator stage's voltage offset by its gain. The tail transistor in this common source amplifier circuit mirrors 10 times the current of the current mirror circuit. A gm/Id design methodology is used to optimize the gain, bandwidth, and power consumption.

Fig. 5. 5: A three-stage comparator.

The sense-amplifier-based latch utilizes an N-type transistor input pair for a faster regeneration time. A short regeneration time requires large transistors to form the cross-coupled inverters as well as the comparator input pair. This adds to additional parasitic capacitors at the drain of the input transistor pair, hence increasing the reset time and power consumption of the comparator. A tradeoff is made between area, power, reset time, and regeneration time. Post-layout simulations using a 0.1 mV input differential voltage resulted in comparator reset and regeneration times of 120 ps and 70 ps respectively. The offset in a dynamic comparator can be systematic, random, and due to the unequal capacitance at the drain of the input transistor pair. A systematic offset can be corrected by layout techniques, and an unequal drain capacitance at the input pair can be minimized using symmetric layout techniques, but an offset still remains due to random mismatches in the system. An additional input pair is used for off-chip calibration purposes. This additional calibration input pair can also be used to address a voltage offset mismatch between the two comparators. The differential output during the second stage uses inverters for load balancing. This reduces any mismatch caused at the

drain of the second-stage input pair transistor that can result in an offset. The third stage of the comparator is an SR latch to hold the current conversion cycle's comparator output until the next cycle's output is available. This provides sufficient time for the memory element to store the output.

The layout extensively uses local and global guard rings to achieve a good transient comparator performance in a mixed-signal environment. A common-centroid arrangement, with dummy and guard rings for input pair transistors, an off-chip calibration transistor pair, cross-coupled inverters, and a p+ poly resistor without salicide is used. The preamplifier's resistor load value is derived by connecting four resistors in parallel. The current-sink transistors of both preamplifiers are laid out together in a common-centroid arrangement with a dummy transistor at both end. The entire layout has symmetric metal routing. A deep N-well boundary is used to isolate the preamplifier and the dynamic sense-amplifier-based latch from the rest of the ADC sub-systems.

5.2.3 Capacitive DAC

A charge-redistribution principle based DAC is used in this SAR ADC. The 1.5-bit per cycle architecture requires two differential CDACs. In order to achieve small chip area and to maintain competitiveness with state-of-the-art error-correction SAR ADCs, special focus is given to the switching scheme. The proposed constant common-mode fractional reference voltage (CCM-FRV) switching scheme helps to achieve the objective of reducing the CDAC size at the cost of introducing additional voltage references. Another CDAC switching technique in chapter 7 of this thesis provides an alternative switching technique to CCM-FRV and also

reduces the amount of reference voltages used.

Custom-sandwiched metal-over-metal (MOM) unit capacitors are used to construct the binary-weighted capacitor array. The Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm CMOS technology offers nine metal layer stacks. Metal layer 5 is sandwiched between layers 4 and 6 to obtain a 740 aF unit capacitor. A total of 512 unit capacitors are laid out using the common-centroid technique.

The MSB capacitor is divided into two equal-sized capacitors of $128C_U$ in order to reduce the RC time constants and to aid in faster CDAC voltage settling. This division of MSB capacitor is important because the first conversion cycle does not have redundancy. Additionally, it is ensured that sufficient time is allocated for the CDAC voltage settling time in the first conversion cycle. Table 5.1 shows the CDAC capacitor ratio using the parasitic extraction (PEX) tool from Mentor Graphics. The unit capacitor value is derived in section 3.2.

Table 5. 1: The CDAC capacitor ratio using the Calibre PEX tool.

	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
Bit 1A/1B	128.031	63.969	32.075	16.007	7.994	3.999	2.000	1.000
Bit 2	128.026	63.967	32.074	16.006	7.994	3.999	2.000	
Bit 3	64.011	31.982	16.036	8.002	3.997	1.999		
Bit 4	32.014	15.995	8.020	4.002	1.999			
Bit 5	16.014	8.001	4.011	4.011				
Bit 6	7.998	3.996	2.003					
Bit 7	3.991	1.994						
Bit 8	2.001							

The common-centroid arrangement (excluding dummy capacitors on all sides) of a

single CDAC is shown in Figure 5.6. Same color represents unit capacitors forming the capacitor weight in the CDAC. The unit capacitor occupies an area of $1.38 \times 1.74 \text{ } \mu\text{m}^2$. It is challenging to meet the metal-density requirements for achieving a small DAC layout. The spacing between the capacitor columns is determined by the width of the dummy metal layers required to meet the chip-density requirements. A manual fill for the metal, polysilicon, and diffusion layers is done for the CDAC layout. Exclude-metal layers are used to avoid an automatic metal fill, which can impact the DAC performance. The metal layers 1 and 9 are used for shielding the DAC: layer 1 shields the DAC's top plate, which connects to the preamplifier, and layer 9 forms a metal sheet on top of the DAC. Layer 9 metal sheet is cheesed to reduce metal stress during back-end-of-line metal fabrication. Furthermore, the DAC is placed within a deep N-well to reduce any substrate noise coupling to the sensitive top plate of the CDAC, affecting the comparator's output. The shielding adds to the parasitic capacitance at the top plate, and as a result charge sharing occurs and the top-plate signal is attenuated. The fixed parasitic capacitance results in a fixed gain error of the ADC. The DAC bit lines, connected to the CMOS switches for each binary weighted capacitor in the array, are kept symmetric. This arrangement helps to maintain a similar parasitic resistor and capacitor for all the DAC bit lines. Dummy unit capacitors are placed on all sides of the array to maintain a similar environment during back-end-of-line fabrication. Routing of bottom plate connections for bits B8, B9, and B10 becomes challenging as the capacitance is quite small and the routing parasitics can easily influence the performance of the data converter. Special emphasis and multiple layout routing

attempts were made to minimize these layout parasitics. Figure 5.7 shows the schematic of the CDAC, along with the comparators for a 10-bit SAR ADC using the 1.5-bit/cycle technique.

Fig. 5. 6: A common-centroid arrangement of the DAC layout.

Our proposed design reduces the dependency of the mismatch between two CDACs and also the accuracy of the reference voltage settling, which is a common problem with a typical 2-bit/cycle SAR ADC design that requires two CDACs and three comparators. In the 2-bit/cycle architecture, the middle comparator threshold is generated by interpolating the two CDAC-generated comparator thresholds. This interpolation technique increases the dependency of the mismatch between the two CDACs and is critical to the ADC performance. Additionally, the 2-bit/cycle architecture has a high dependence on the accuracy of the reference voltages and the reference voltage settling on the CDACs.

In contrast, the two comparator thresholds required for the 1.5-bit/cycle architecture are generated independently using their own respective CDACs. This greatly reduces the dependency on the mismatch between the two CDACs. Layout techniques, such as the symmetric layout of the CDAC, the reference voltage metal line, differential input signal metal lines, and the common-centroid DAC

arrangement with dummy capacitors, help to reduce the mismatch between the two CDACs. The 12.5% redundancy margin in the 1.5-bit/cycle architecture helps to relax the reference voltage requirements, including CDAC reference voltage settling.

Fig. 5. 7: A 10-bit charge-redistribution-based CDAC schematic, including comparators to implement a 1.5-bit/cycle technique.

5.2.4 Control Logic and Memory

Control logic forms an essential part of the SAR data converter and is required during every conversion cycle. Figure 5.8 shows the control logic for the initial 1-bit conversion cycle, while Figure 5.9 shows the logic for the 1.5-bit conversion cycle. Replica circuits of the schematic shown in Figure 5.9, with different inverter drive strengths, are used to control the scaled-down CDAC transistor switches. The control signals $R0$, $R0(\overline{BAR})$, $R1$, $R2$, and $R2(\overline{Bar})$ are used to control the differential CDAC switches connected to one of the three reference voltages – V_{CM} , V_{REFp} , and V_{REFn} . *Output 0* and *Output 1* are the region-detection logic output signals for the 1-bit conversion cycle, while *Output 00*, *Output 01*, and *Output 11* are the corresponding signals for the 1.5-bit/cycle conversion. The signal *Clk S* denotes the sampling clock signal.

Dynamic logic implementation is used to reduce control-logic delay and static current consumption. The output is pre-charged before the first cycle starts, and the evaluation phase begins once the pertinent signal, *Token N*, arrives. (N denotes the current conversion cycle, and its value ranges from 1 to 9.) Cross-coupled inverters are used at the output node to counter for leakage and charge sharing at parasitic nodes during the evaluation phase.

Figures 5.10 and 5.11 show the region-detection logic for the first conversion cycle (1-bit) and the remaining eight conversion cycles (1.5-bit), respectively. The intermediate comparator output signals after the second stage are *Vintp1*, *Vintn1*, *Vintp2*, and *Vintn2*. These signals are used to minimize the overall control-logic delay.

Fig. 5. 8: The control logic for a differential CDAC switch implementation for a 1-bit conversion cycle.

Fig. 5. 9: The control logic for a differential CDAC switch implementation for a 1.5-bit conversion cycle.

Fig. 5. 10: The region-detection logic for the first conversion cycle.

Fig. 5. 11: The region-detection logic for the 1.5-bit/cycle.

The sequencer shown in Figure 5.12 is implemented by a 3-bit counter and is used to keep track of conversion cycles and to generate conversion-cycle-specific token signals, *Token 1* to *Token 9* based on the signal, *Clk Reset*. These tokens are used to activate the conversion-cycle-specific parts of the control logic. Additionally, these token signals also act as direct control signals for the CDAC transistor switches to implement redundancy. The reutilization of token signals simplifies the control logic.

Fig. 5. 12: A schematic of the sequencer.

The comparator's output is stored in the memory, implemented using a differential topology modified from Tripathi's work [57]. At the end-of-conversion signal, *EOC*, the content in the memory is temporarily stored in D-flip-flops for error correction. After this operation, the memory is reset for the next cycle.

After the final conversion cycle, a bootstrapped NMOS switch is used to reset the top plate of the CDAC to the common-mode voltage. This removes any memory effect on the conversion of the next analog input voltage based on the previous conversion. An extra effort was made to carefully size this switch using circuit simulation so that the charge injection is minimized and does not affect the ADC's performance. The NMOS switch is laid out using a dummy transistor at both sides and a guard ring around the transistors. The control-logic and switch array connected to the CDAC is surrounded by a C-shaped global double guard ring shown in Figure 5.13. This helps to collect minority charge carriers, which can affect the transistor switch's threshold. Figure 5.13 only shows one-half of the entire SAR ADC (the complete CDAC layout is not shown).

Fig. 5. 13: The layout showing a C-shaped guard ring for switches.

5.2.5 Error Correction

Digital error correction is implemented by a ripple-carry adder circuit consisting of seven full adders and two half-adders. Section 4.2 describes the error correction in detail. Figures 5.14 and 5.15 show the digital error correction logic schematic and layout. The layout includes the memory elements for storing the final 10-bit error-corrected output.

Fig. 5. 14: The error-correction logic and its implementation.

Fig. 5. 15: The layout of the error-correction logic and memory.

5.3 Chip Layout

Figure 5.16 shows the layout of the proposed 10-bit SAR ADC. The wire-bonded silicon die fabricated using 65 nm CMOS technology is shown in Figure 5.17. The layout of a multi-bit ADC is critical to its performance. Wherever possible, the layout is symmetric along both axes. The circuit sub-blocks – the counter, error-correction logic, registers, asynchronous timing generation, the preamplifier, and the dynamic comparator – were laid out at the center of the core for routing simplicity to the circuit blocks. Additional care was taken to create multiple voltage islands for the comparator, the clock, and the digital and analog domains. A deep N-well was used in addition to guard rings to isolate the voltage islands. The entire digital-logic domain was surrounded by P-sub contacts to reduce substrate noise and to isolate the CDACs.

Fig. 5. 16: The layout of the test chip to implement an asynchronous 10-bit SAR

ADC with redundancy-facilitated error correction.

Fig. 5. 17: A wire-bonded silicon die implementing an asynchronous 10-bit SAR

ADC with redundancy-facilitated error correction.

PCB Design, Test Setup & Measurement Results

6.1 PCB and Wire Bonding

Printed-circuit-board (PCB) design plays an important role in the performance of the high-speed 10-bit data converter under test. The concept of noisy ground and quiet ground is implemented on the PCB. A four-layer FR4 printed circuit board with a domain-specific ground layer is shown in Figure 6.1. The digital, I/O, comparator, clock, and analog-voltage domains have their own ground layers. In Figure 6.1, layer 2 of the PCB, highlighted in brown, is the domain-specific ground layer. Layer 3 of the PCB, highlighted in light blue, is the common ground layer. The top (red) and bottom (dark blue) layers of the PCB are used for signal and power-supply routing. A 1Ω surface mount resistor connects the domain grounds to the common ground layer on the PCB. A hard gold surface finish was selected to support the chip-on-board wire bonding using gold wire. Another version of the PCB uses a QFN-40 package and does not require a hard gold surface finish. The fabricated and assembled board is shown in Figure 6.2.

Additionally, Figure 6.1 illustrates that the 10-bit output signal traces are length-matched on the PCB so that the time-of-arrival of the signals are synchronized to the logic-analyzer equipment. The via-shielding technique for PCBs is used for the differential analog input signal traces and the master clock signal trace.

The silicon die is placed close to the differential analog input PCB pads to reduce bond-wire inductance, which contributes to a ringing effect for the high-speed analog input signal and can deteriorate the signal quality. Extra care was taken during the chip assembly to maintain symmetric analog differential input bond wire lengths. This technique helps to suppress even-order distortion introduced due to the PCB and wire bonding. An external 5Ω series surface mount resistance was placed very close to the differential input signal trace, the master clock trace, and the I/O PCB pads. This was done to reduce resonance created by the bond wire, and the PCB metal trace parasitic capacitance and inductance.

Fig. 6. 1: A four-layer PCB layout.

Fig. 6. 2: A four-layer PCB, fabricated and assembled.

6.2 Test Setup

Design for testability is an important criterion during IC design, and extensive post-layout simulations of the entire system with external parasitic elements and test equipment probe models were done prior to chip fabrication. Figure 6.3 shows the setup used for the simulations. The test chip was designed to maintain the ease

of testing and allow debugging chip issues post-fabrication. The test setup used to measure the performance of the 10-bit SAR ADC, the device under test (DUT), is shown in Figure 6.4. The power supply unit, HMP2030, powers the low-dropout (LDO) regulator boards from Texas Instruments. The LDO board supplies 1.2 V to the different voltage domains and 2.5 V to the I/O domain. An internal level shifter converts the 10-bit parallel output signal from 1.2 V to 2.5 V logic. A multi-channel, 12-bit buffered DAC from Analog Devices is used to supply the DAC reference voltages and the common-mode voltage to the center-tap balun used before the clock and analog input pads. The peak-to-peak noise on the reference voltages is 0.39 mV_{PP}. The test setup also uses an alternate test bench where a voltage buffer using op-amps is used to supply the fractional reference voltages. The power consumption of these op-amps with and without capacitive load i.e., CDAC is estimated to calculate the power consumption of the reference voltages.

An arbitrary waveform generator, 81180A, generates the signals required to characterize the dynamic and static performance of the designed ADC. A multi-band pass filter is used to reduce the equipment-generated signal harmonics. A center-tap balun converts the single-ended filtered analog input signal into a differential signal. The balun causes a phase imbalance from 0.01 degree to 1.18 degree and an amplitude imbalance from 0 dB to 0.05 dB. This phase and amplitude imbalance results in even-order harmonics that can be observed in the FFT plot (Figure 6.8). Additionally, the mismatch between the on-chip input signal metal traces also contributes to the phase imbalance between the input differential signals, which contributes to the amplitude of the even-order harmonics. The

N5183A analog-signal generator is used as the master clock signal source. On-chip clock buffers correct the clock-signal amplitude. The logic-analyzer equipment, 16852A, captures the final, error-corrected 10-bit SAR output.

Fig. 6. 3: A schematic of the parasitic elements and the test equipment probe models.

The comparator offset mismatch is solved by using an off-chip 12-bit DAC to provide the gate biasing voltage to the additional input pairs available in the comparators. The tuning step size of the DAC or its LSB is $1/4\text{LSB}$ of the ADC under test. This ensures that the individual comparator offset is less than $1/4\text{LSB}$ and the offset mismatch between the comparators is much less than $1/2\text{LSB}$. There are four comparator offset mismatch cases: ++, +-, -+, and --. Where ‘+’ denotes the positive comparator offset and ‘-’ denotes the negative comparator offset. The comparator outputs (buffered) are routed to the I/O pads. The access to the comparator outputs provide more flexibility in offset calibration process. A degradation in the calibrated comparator offset such that the offset mismatch increases beyond $1/2\text{LSB}$ will result in SNDR degradation and can serve as an indicator that the comparators require offset re-calibration.

Fig. 6. 4: The test setup for measuring the performance of the 10-bit SAR ADC.

6.2.1 Reference Voltage Requirement

The effective redundancy margin is determined by the accuracy of the reference voltages V_{OFFp} and V_{OFFn} and these reference voltages DAC settling time. A sufficient DAC settling time and 10-bit accuracy of the V_{OFFp} and V_{OFFn} reference voltages result in a 12.5% redundancy margin. The CCM-FRV switching scheme charges all of the capacitors up to a V_{CM} reference voltage as the capacitors initial state. Transferring the appropriate charge to a capacitor already charged up to V_{CM} results in reducing the time required for the DAC voltage to settle within a 10-bit accuracy. Furthermore, the redundancy margin is created using a capacitor that is

half the value of the next capacitor in the binary-scaled DAC array that is switched to either V_{REFn} , V_{REFp} , or V_{CM} in the same cycle. Furthermore, the capacitors responsible for creating the redundancy margin are “pre-set” by the cycle specific Token signals irrespective of the value of the comparator’s output. This technique therefore results in creating a redundancy margin in advance in order to relax the reference voltage (V_{REFn} , V_{REFp} , or V_{CM}) settling within the created redundancy margin for the next larger capacitor in the DAC array.

6.3 Results

The die micrograph shown in Figure 6.5 was fabricated using 65 nm 1P9M CMOS technology with an active area of 0.038 mm^2 , including clock buffers, a pre-driver buffer, and power-supply decoupling capacitors. The digital error correction circuit occupies a $38 \times 7 \text{ }\mu\text{m}^2$ chip area.

Fig. 6. 5: A wire-bonded die micrograph.

Figure 6.6 shows the measured SNDR and SFDR plotted against the sampling frequency for an input frequency of 10 MHz, while Figure 6.7 shows the measured

SNDR and SFDR cross-plotted against the input frequency at 150 MSps. Increasing the sampling frequency from 60 MHz to 150 MHz has a minimal effect on dynamic performance. A degradation of performance is noticed at 160 MSps. This degradation might be because in some cases the last conversion cycle might not be completed. A 50 mV increase in supply voltage of the clock domain solves the problem of SNDR degradation at 160 MSps. The event-based asynchronous timing generator's sequence of events does not vary proportionally with the changes in the sampling frequency. This is because the comparator still requires the same regeneration time and its ready signal arrives at the specified frequency to the asynchronous timing generator loop in order to generate the next conversion cycle clock. A degradation of the measured SFDR is observed with respect to the post-layout simulation, where the simulated SFDR is 72 dB. Figure 6.7 shows robust operation of the SAR ADC at various input frequencies from close to dc up to Nyquist.

Figure 6.8 shows the output FFT spectrum for an input frequency of 10 MHz at 150 MSps. An SNDR of 59 dB and an SFDR of 67.45 dB were measured. Figure 6.9 shows the output spectrum for input close to the Nyquist frequency, 73.03 MHz: the SNDR is 57.81 dB and the SFDR is 64.78 dB. Wherever possible, a coherent sampling technique is used for the input signal frequencies. The center-tap balun located at the analog input causes a phase and amplitude imbalance of the input differential signals. This imbalance results in even-order harmonics and can be seen in the FFT plot. Additionally, the mismatch between the on-chip input signal metal traces also contributes to the phase imbalance between the input

differential signals, which contributes to the amplitude of the even-order harmonics.

Fig. 6. 6: The measured dynamic performance plotted against the sampling frequency.

Fig. 6. 7: The measured dynamic performance plotted against the input frequency.

Fig. 6. 8: The measured FFT results with a 10 MHz input at 150 MSps.

Fig. 6. 9: The measured FFT results with a 73.03 MHz input at 150 MSps.

Figure 6.10 shows the measured static performance with a peak integral nonlinearity (INL) of +0.96/-0.86 LSB. Figure 6.11 shows the measured static performance with a peak differential nonlinearity (DNL) of +0.97/-0.83 LSB. The

ADC uses a 1.2 V supply and consumes 4.06 mW at 150 Msps, which leads to a Walden figure of merit (equation 6.1) of 42.6 fJ/conv-step at the Nyquist frequency.

$$\text{Figure of merit(fJ/conv step)} = \frac{\text{Power (mW)}}{(2^{\text{ENOB}} * f_{\text{sampling}})} \quad (6.1)$$

Fig. 6. 10: The measured INL.

Fig. 6. 11: The measured DNL.

Figure 6.12 shows the breakdown of the power consumption. The 4.06 mW of power was divided between different block as follows: comparators including analog pre-amplifiers used up 1.23 mW; the DAC reference voltage, 0.29 mW; the digital domain, 2.24 mW; and the asynchronous clock generator (excluding the clock buffer to correct signal amplitude), 0.3 mW. The digital domain consumed the most power, followed by the comparator domain; together, these domains add

up to 85.46% of the total power consumption. Using low- V_{TH} CMOS devices in the control logic to gain extra speed resulted in larger leakage currents, which can be avoided in future design. Porting the proposed SAR ADC design to more advanced technology nodes can result in a major reduction in the digital- and comparator-domain power consumption, resulting in a better FOM.

Table 6.1: Performance summary and comparison.

Parameters	This Work	[65]	[66]	[67]	[58]
Architecture	1.5-bit/cycle SAR	2-bit/cycle SAR	1-bit/cycle SAR	1-bit/cycle SAR	Pipeline-SAR
CMOS (nm)	65	40	180	65	40
Supply (V)	1.2	1.2	1.8	1.2	1.1
Resolution / # Cycles	10 bit / 9	10 bit / 8	10 bit / 10	10 bit / 11	12 bit / 12
Redundancy	Bin. 12.5%	1-bit Bin.	No	Non-Bin. 1-bit	Non-Bin.
Digital Error-Correction	7 F. A, 2 H. A	Yes	No	8 F. A	N/A
Sampling (MS/s)	150	300	80	150	160
ENOB (bit)	9.31	7.51	9.13	8.2	10.85
Power (mW)	4.06	2.1	2.61	1.4	4.96
FOM (fJ/conv-step)	42.6	38.4	74.4	31.8	20.6
Area (mm ²)	0.038	0.008	1.61	0.079	0.042
$V_{in,pp,diff}$ (V)	2.4	N/A	1.6	2.1	2

Fig. 6. 12: The post-layout power breakdown of the proposed SAR ADC.

Fig. 6. 13: A cross-plot of the figure of merit and the sampling frequency for single-channel ADCs with redundancy and error correction. (Data adapted from

[30].)

Figure 6.13 illustrates the relationship between the figure of merit and the sampling frequency for single-channel SAR ADCs with redundancy and error correction [30]. Table 6.1 summarizes and compares the performance of our ADC with published SAR ADCs [58, 65, 66, 67]. Advantages of our proposed SAR ADC include- no modification to binary-scaled DAC, using no additional conversion cycles, simple error correction logic, and the ability to correct multiple erroneous decisions. The pipeline ADC [58] relaxes the linearity and noise requirements of the residue amplifier by implementing a high-resolution first stage. Furthermore, the first SAR stage uses a sub-binary DAC, which helps to achieve a high conversion speed and to decrease power consumption at the same time. The 2-bit/cycle SAR ADC [65] achieves high sampling speed, but suffers from degraded effective number of bits. The SAR ADC [67] uses non-binary redundancy in the first five decision bits and achieves same sampling frequency as this work.

6.4 Conclusion

A 160 MSps 10-bit SAR ADC prototype implementing binary-scaled, redundancy-facilitated error correction was successfully tested. Adopting the layout techniques for high-speed mixed-signal circuit design described in this thesis helped to achieve good ADC performance. A peak INL of $+0.96/-0.86$ LSB and a peak DNL of $+0.97/-0.83$ LSB was measured. A peak SNDR of 59 dB and an SFDR of 67.45 dB result in an effective number of bits (ENOB) of 9.5. The data converter consumes 4.06 mW of power from a 1.2 V supply.

Proposed Switching Scheme for a 1.5-bit/cycle SAR ADC with Digital Error-Correction

7.1 Introduction

Fig. 7. 1: Example of a 4-bit SAR ADC using the proposed 1.5-bit/cycle architecture.

A CDAC for an SAR ADC consumes a considerable amount of energy and chip area. To reduce the overall power used by an SAR ADC, the CDAC switching scheme needs to be improved. Compared to a conventional switching scheme [51], advanced schemes can greatly reduce the switching energy and the CDAC area for

a single-bit per cycle: a set-and-down scheme [19] reduces switching energy by 81.2% and the CDAC area by 50%; a tri-level one [52] needs 96.89% less energy and 75% less area; the higher-side-reset-and-set scheme [56] reduces energy by 92.92% and area by 50%; and a V_{cm} -based scheme [50] cuts the switching energy by 93.7% and CDAC area by 75%. These switching schemes [19, 52, 56], however, cause large shifts in the common-mode voltage to the input of the comparator, which negatively affects the comparator offset, thermal noise, and the regeneration time for a high-speed ADC. Hence, in order to maintain robust operation, it is beneficial to minimize shifts in the common-mode voltage for a multi-bit per cycle SAR ADC architecture.

The proposed low-energy and area-efficient switching scheme using a V_{cm} -based switching technique with the addition of a $V_{cm}/2$ reference voltage for the last conversion cycle is discussed in this chapter. Figure 7.1 shows the architecture of a 4-bit SAR ADC using the 1.5-bit/cycle technique. Two CDACs are switched to one of the available reference voltages in order to create the three decision regions necessary for the 1.5-bit/cycle operation. Comparator outputs A_iB_i are then available as the input to the error correction logic, where bit-overlap- and-add operation occurs. The final digital output is available in the SAR memory. Figure 7.2 illustrates the 1.5-bit/cycle operation for the architecture shown in Figure 7.1, including the CDAC switching pattern for both the cases – with/without erroneous conversion. It can be noticed that the digital output ($D_1D_2D_3D_4$) converges to the same value irrespective of the erroneous conversion result caused by the incomplete CDAC voltage settling.

Fig. 7. 2: Proposed CDAC switching technique for a 4-bit SAR ADC using 1.5-bit/cycle operation.

A $\frac{1}{4} V_{ref}$ decision offset is added to the decision thresholds of a 2-bit conversion in order to obtain the two thresholds for 1.5-bit/cycle conversion. In this example, a 4

LSBs settling tolerance is available for the first conversion cycle. This error tolerance margin relaxes the voltage settling requirement and enables faster conversion cycles. Irrespective of the erroneous cycle, the CDAC switching pattern (Figure 7.2) adjusts such that the CDAC voltages, V_{DAC1} and V_{DAC2} converges to the analog input value of $9/32 V_{ref}$.

7.2 Proposed Switching Scheme for a 10-bit SAR ADC

Fig. 7. 3: The proposed CDAC switching scheme (first and second conversion cycles) for a 10-bit SAR ADC using 1.5-bit/cycle operation.

Figure 7.3 shows the first two conversion cycles of the proposed switching scheme. The operation begins with top-plate sampling of the differential analog input signal (V_{ip} , V_{in}), while the bottom plate is connected to the V_{cm} (i.e., $\frac{1}{2} V_{ref}$) reference voltage. A multi-bit per cycle SAR ADC requires multiple comparator thresholds; for example, a 1.5-bit/cycle operation requires two thresholds. The two comparator thresholds are generated by using two CDACs. The thresholds create three asymmetric binary-coded decision regions, i.e., “00”, “01”, and “10”. Figure 7.4 illustrates these decision regions for the first and second conversion cycles. 0.5-bit redundancy results in a 12.5% error-tolerance margin around the comparator threshold, and this 12.5% margin in turn results in a cumulative redundancy margin of 128 LSBs or ± 64 LSBs around the comparator threshold for the first conversion cycle. The DAC voltage settling time in the first conversion cycle is relaxed by 2.75x. The effective redundancy margin remains constant and therefore scales in a binary fashion as the conversion cycles progress.

Fig. 7. 4: The binary-coded decision regions for a 10-bit SAR ADC using 1.5-bit/cycle operation.

After the input voltage is sampled, the sampling switch is disconnected and the 0.5-bit redundancy margin is created for the first conversion cycle by switching the MSB-1 capacitor to either V_{ref} or GND (i.e., 0 V). The energy spent on creating the redundancy margin is also illustrated in Figure 7.3. The comparator output A_0B_0 is then obtained. Depending on the output of the conversion cycle, the MSB capacitor is connected to one of the three reference voltages: V_{cm} , V_{ref} , or gnd. The first cycle's redundancy margin is removed by connecting the MSB-1 capacitor back to the V_{cm} reference voltage. To account for the reduction in the full scale, a redundancy margin for the second conversion cycle is created by connecting the MSB-3 capacitor to either V_{ref} or gnd. Additionally, the MSB-2 capacitor is connected back to V_{cm} in order to remove the previous conversion cycle's redundancy margin.

Figure 7.5 shows all the possible switching procedures depending on the output of the second conversion cycle, i.e., A_1B_1 . To reduce the size of the CDAC, a different method (i.e., using $V_{cm}/2$ reference voltage) to create the redundancy margin is used and illustrated in Figure 7.6. The eighth and ninth (final) conversion cycle results in a small (i.e., $V_{ref}/1024$ and $V_{ref}/2048$) shift in the common-mode voltage to the comparator input. A total of nine conversion cycles are required to obtain the 10-bit output. Figure 7.7 shows the differential CDAC switching waveform. Depending on the binary output of the comparators ("00", "01", or "10"), results in the CDAC-generated voltages go "down", "remain constant", or go "up". The CDAC voltage relaxation and the simple control logic of the

proposed switching scheme are beneficial for high-speed, single-channel SAR ADCs.

(a)

(b)

(c)

Fig. 7. 5: The proposed DAC switching scheme for the third conversion cycle of a 10-bit SAR ADC using 1.5-bit/cycle operation when (a) $A_0B_0=11$ (b) $A_0B_0=01$ (c) $A_0B_0=00$.

Fig. 7. 6: The proposed DAC switching scheme for the last (i.e., the ninth) conversion cycle of a 10-bit SAR ADC using 1.5-bit/cycle operation.

Fig. 7. 7: The waveform of the proposed DAC switching scheme for a 10-bit SAR ADC using 1.5-bit/cycle operation.

7.3 Error-Correction Logic

The 1.5-bit/cycle technique is responsible for the simple bit-overlap-and-add error-correction logic. Before the error-correction operation, the 1.5-bit/cycle output is converted from a thermometer code format into a binary-code one. The encoding scheme is shown in Figure 7.8 and comprises eight full adders and two half-adders. The bit-overlap-and-add operation begins with the second conversion cycle.

Fig. 7. 8: The digital error correction logic for a 10-bit SAR ADC using 1.5-bit/cycle operation.

7.4 Switching Energy Calculations

The switching energy required for the sampling phase, the first and second conversion cycles are calculated with the help of equations (7.1) – (7.52). Due to top-plate sampling, the sampling phase does not require any switching energy. The following variables are used: $V_{XP}[\text{Sample}]$ denotes the positive top-plate voltage during the sampling phase; $V_{XN}[\text{Sample}]$ denotes the negative top-plate voltage during the sampling phase; $V_{XP,CDAC1}[1]$ denotes the positive top-plate voltage of the CDAC1 during the first conversion cycle; $V_{XP,CDAC2}[1]$ denotes the positive

top-plate voltage of the CDAC2 during the first conversion cycle; $V_{XN,CDAC1}[1]$ denotes the negative top-plate voltage of the CDAC1 during the first conversion cycle; $V_{XN,CDAC2}[1]$ denotes the negative top-plate voltage of the CDAC2 during the first conversion cycle; V_{CM} denotes the common-mode voltage; and V_{REF} denotes the positive reference voltage.

$$V_{XP}[Sample] = V_{IP} - V_{CM} \quad (7.1)$$

$$V_{XN}[Sample] = V_{IN} - V_{CM} \quad (7.2)$$

The charge redistribution principle is applied to derive the following equations.

First Conversion Cycle:

$$V_{XP,CDAC1}[1] = V_{IP} - V_{CM} - \frac{V_{CM}}{4} \quad (7.3)$$

$$V_{XP,CDAC2}[1] = V_{IP} - V_{CM} + \frac{V_{CM}}{4} \quad (7.4)$$

$$V_{XN,CDAC1}[1] = V_{IN} - V_{CM} + \frac{V_{CM}}{4} \quad (7.5)$$

$$V_{XN,CDAC2}[1] = V_{IN} - V_{CM} - \frac{V_{CM}}{4} \quad (7.6)$$

$$Energy_{sampling \rightarrow 1 | positiveCDAC1} = 0 \quad (7.7)$$

Since the 64C capacitor is switched in the negative CDAC1, the switching energy can be expressed as equation (7.8).

$$Energy_{sampling \rightarrow 1 | negativeCDAC1} = -V_{REF} \cdot 64C \cdot \{(V_{XN,CDAC1}[1] - V_{CM}) - (V_{XN}[Sample])\} \quad (7.8)$$

Substituting equations (7.5) and (7.2) in (7.8):

$$Energy_{sampling \rightarrow 1 | negativeCDAC1} = 24CV_{REF}^2 \quad (7.9)$$

$$Energy_{sampling \rightarrow 1 | negativeCDAC2} = 0 \quad (7.10)$$

Since the 64C capacitor is switched in the positive CDAC2, the switching energy can be expressed as equation (7.11).

$$Energy_{sampling \rightarrow 1 | positiveCDAC2} = -V_{REF} \cdot 64C \cdot \{(V_{XP,CDAC2}[1] - V_{CM}) - (V_{XP}[Sample])\} \quad (7.11)$$

Substituting equations (7.4) and (7.1) in (7.11):

$$Energy_{sampling \rightarrow 1 | negativeCDAC1} = 24CV_{REF}^2 \quad (7.12)$$

Using equations (7.7), (7.9), (7.10), and (7.12):

$$Total\ Energy_{sampling \rightarrow 1} = 48CV_{REF}^2 \quad (7.13)$$

Second Conversion Cycle:

If A_0B_0 is "11"

The variables used are as follows: $V_{XP}[2]$ denotes the positive top-plate voltage of the CDAC during the second conversion cycle; $V_{XN}[2]$ denotes the negative top-plate voltage of the CDAC during the second conversion cycle.

Switching Energy for CDAC1:

$$V_{XP}[2] = V_{IP} - V_{CM} - \frac{5 \cdot V_{CM}}{8} \quad (7.14)$$

$$V_{XN}[2] = V_{IN} - V_{CM} + \frac{5.V_{CM}}{8} \quad (7.15)$$

Since the 128C capacitor is switched in the positive CDAC1, the switching energy can be expressed as equation (7.16).

$$Energy_{1 \rightarrow 2 | positiveCDAC1} = -V_{REF} \cdot 128C \cdot \{(V_{XP}[2] - V_{CM}) - (V_{XP}[1])\} \quad (7.16)$$

Substituting equations (7.14) and (7.3) in (7.16):

$$Energy_{1 \rightarrow 2 | positiveCDAC1} = 44CV_{REF}^2 \quad (7.17)$$

Since the 128C and 32C capacitors are switched in the negative CDAC1, the switching energy can be expressed as equation (7.18).

$$Energy_{1 \rightarrow 2 | negativeCDAC1} = -V_{REF} \cdot (128C + 32C) \cdot \{(V_{XN}[2] - V_{CM}) - (V_{XN}[1])\} \quad (7.18)$$

Substituting equations (7.15) and (7.5) in (7.18):

$$Energy_{1 \rightarrow 2 | negativeCDAC1} = 50CV_{REF}^2 \quad (7.19)$$

Switching Energy for CDAC2:

$$V_{XP}[2] = V_{IP} - V_{CM} - \frac{3.V_{CM}}{8} \quad (7.20)$$

$$V_{XN}[2] = V_{IN} - V_{CM} + \frac{3.V_{CM}}{8} \quad (7.21)$$

Since the 32C capacitor is switched in the positive CDAC2, the switching energy can be expressed as equation (7.22).

$$Energy_{1 \rightarrow 2 | positiveCDAC2} = -V_{REF} \cdot 32C \cdot \{(V_{XP}[2] - V_{CM}) - (V_{XP}[1])\} \quad (7.22)$$

Substituting equations (7.20) and (7.4) in (7.22):

$$Energy_{1 \rightarrow 2 | positiveCDAC2} = 26CV_{REF}^2 \quad (7.23)$$

Since the 128C and 64C capacitors are switched in the negative CDAC2, the switching energy can be expressed as equation (7.24).

$$Energy_{1 \rightarrow 2 | negativeCDAC2} = -V_{REF} \cdot (128 + 64)C \cdot \{(V_{XN}[2] - V_{CM}) - (V_{XN}[1])\} \quad (7.24)$$

Substituting equations (7.21) and (7.6) in (7.24):

$$Energy_{1 \rightarrow 2 | negativeCDAC2} = 36CV_{REF}^2 \quad (7.25)$$

$$\mathbf{Total\ Energy_{1 \rightarrow 2} = 156CV_{REF}^2} \quad (7.26)$$

If A_0B_0 is “01”

Switching Energy for CDAC1:

$$V_{XP}[2] = V_{IP} - V_{CM} - \frac{V_{CM}}{8} \quad (7.27)$$

$$V_{XN}[2] = V_{IN} - V_{CM} + \frac{V_{CM}}{8} \quad (7.28)$$

Since the 64C capacitor is switched in the positive CDAC1, the switching energy can be expressed as equation (7.29).

$$Energy_{1 \rightarrow 2 | positiveCDAC1} = -V_{REF} \cdot 64C \cdot \{(V_{XP}[2] - V_{CM}) - (V_{XP}[1])\} \quad (7.29)$$

Substituting equations (7.27) and (7.3) in (7.29):

$$Energy_{1 \rightarrow 2 | positiveCDAC1} = 28CV_{REF}^2 \quad (7.30)$$

Since the 32C capacitor is switched in the negative CDAC1, the switching energy can be expressed as equation (7.31).

$$Energy_{1 \rightarrow 2 | negativeCDAC1} = -V_{REF} \cdot 32C \cdot \{(V_{XN}[2] - V_{CM}) - (V_{XN}[1])\} \quad (7.31)$$

Substituting equations (7.28) and (7.5) in (7.31):

$$Energy_{1 \rightarrow 2 | negativeCDAC1} = 18CV_{REF}^2 \quad (7.32)$$

Switching Energy for CDAC2:

$$V_{XP}[2] = V_{IP} - V_{CM} + \frac{V_{CM}}{8} \quad (7.33)$$

$$V_{XN}[2] = V_{IN} - V_{CM} - \frac{V_{CM}}{8} \quad (7.34)$$

Since the 32C capacitor is switched in the positive CDAC2, the switching energy can be expressed as equation (7.35).

$$Energy_{1 \rightarrow 2 | positiveCDAC2} = -V_{REF} \cdot 32C \cdot \{(V_{XP}[2] - V_{CM}) - (V_{XP}[1])\} \quad (7.35)$$

Substituting equations (7.33) and (7.4) in (7.35):

$$Energy_{1 \rightarrow 2 | positiveCDAC2} = 18CV_{REF}^2 \quad (7.36)$$

Since the 64C capacitor is switched in the negative CDAC2, the switching energy can be expressed as equation (7.37).

$$Energy_{1 \rightarrow 2 | negativeCDAC2} = -V_{REF} \cdot 64C \cdot \{(V_{XN}[2] - V_{CM}) - (V_{XN}[1])\} \quad (7.37)$$

Substituting equations (7.34) and (7.6) in (7.37):

$$Energy_{1 \rightarrow 2 | negativeCDAC2} = 28CV_{REF}^2 \quad (7.38)$$

$$\mathbf{Total\ Energy_{1 \rightarrow 2} = 92CV_{REF}^2} \quad (7.39)$$

If A_0B_0 is “00”

Switching Energy for CDAC1:

$$V_{XP}[2] = V_{IP} - V_{CM} + \frac{3 \cdot V_{CM}}{8} \quad (7.40)$$

$$V_{XN}[2] = V_{IN} - V_{CM} - \frac{3 \cdot V_{CM}}{8} \quad (7.41)$$

Since the 128C and 64C capacitors are switched in the positive CDAC1, the switching energy can be expressed as equation (7.42).

$$Energy_{1 \rightarrow 2 | positiveCDAC1} = -V_{REF} \cdot (128 + 64)C \cdot \{(V_{XP}[2] - V_{CM}) - (V_{XP}[1])\} \quad (7.42)$$

Substituting equations (7.40) and (7.3) in (7.42):

$$Energy_{1 \rightarrow 2 | positiveCDAC1} = 36CV_{REF}^2 \quad (7.43)$$

Since the 32C capacitor is switched in the negative CDAC1, the switching energy can be expressed as equation (7.44).

$$Energy_{1 \rightarrow 2 | negativeCDAC1} = -V_{REF} \cdot 32C \cdot \{(V_{XN}[2] - V_{CM}) - (V_{XN}[1])\} \quad (7.44)$$

Substituting equations (7.41) and (7.5) in (7.44):

$$Energy_{1 \rightarrow 2 | negativeCDAC1} = 26CV_{REF}^2 \quad (7.45)$$

Switching Energy for CDAC2:

$$V_{XP}[2] = V_{IP} - V_{CM} + \frac{5 \cdot V_{CM}}{8} \quad (7.46)$$

$$V_{XN}[2] = V_{IN} - V_{CM} - \frac{5 \cdot V_{CM}}{8} \quad (7.47)$$

Since the 128C and 32C capacitors are switched in the positive CDAC2, the switching energy can be expressed as equation (7.48).

$$Energy_{1 \rightarrow 2 | positiveCDAC2} = -V_{REF} \cdot (128 + 32)C \cdot \{(V_{XP}[2] - V_{CM}) - (V_{XP}[1])\} \quad (7.48)$$

Substituting equations (7.46) and (7.4) in (7.48):

$$Energy_{1 \rightarrow 2 | positiveCDAC2} = 50CV_{REF}^2 \quad (7.49)$$

Since the 64C capacitor is switched in the negative CDAC2, the switching energy can be expressed as equation (7.50).

$$Energy_{1 \rightarrow 2 | negativeCDAC2} = -V_{REF} \cdot 64C \cdot \{(V_{XN}[2] - V_{CM}) - (V_{XN}[1])\} \quad (7.50)$$

Substituting equations (7.47) and (7.6) in (7.50):

$$Energy_{1 \rightarrow 2 | negativeCDAC2} = 44CV_{REF}^2 \quad (7.51)$$

$$\mathbf{Total\ Energy}_{1 \rightarrow 2} = \mathbf{156CV_{REF}^2} \quad (7.52)$$

7.5 Analysis and Comparison of Different Switching Schemes

Behavior simulations for a fully differential 10-bit SAR ADC using 1.5-bit/cycle operation were performed in the MATLAB environment. The simulation results are shown in Figure 7.9. Compared to a 1-bit/cycle architecture, the 1.5-bit/cycle architecture requires two CDACs and switching additional capacitors within the two CDACs in order to generate the two comparator thresholds. The extra CDAC and additional capacitor switching results in an increase in the switching energy and an uneven waveform for the 1.5-bit/cycle architecture. The digital conversion of the analog input voltage consumes less switching energy if it falls inside the middle decision region (i.e., “01”) than if it falls within the upper (i.e., “10”) or lower (i.e., “00”) decision region. This difference in switching energy can make the decision regions and the corresponding comparator thresholds observable, as shown in Figure 7.9.

Fig. 7. 9: A cross-plot of switching energy and output code for switching schemes modified to implement a 10-bit SAR ADC using 1.5-bit/cycle operation.

A comparison of two broad categories of switching schemes, using symmetric differential switching and asymmetric differential switching, are highlighted in Table 7.1. A constant common-mode operation results from the symmetric differential switching. The conventional switching scheme modified to implement 1.5-bit/cycle operation requires an arithmetic unit and read-only-memory containing information about redundancy in order to calculate the CDACs switching pattern. The set-and-down and reverse- V_{cm} switching schemes do not require an additional arithmetic unit and the redundancy is built into the CDAC.

The absence of an arithmetic unit makes the logic complexity of set-and-down, Rahimi and proposed switching technique simpler than that of a conventional switching scheme. The energy savings of both the set-and-down and the Rahimi's switching scheme are approximately equal. However, a large common-mode variation results from the asymmetric differential CDAC switching of the set-and-down scheme. This variation negatively affects the comparator's performance in a high-speed SAR ADC.

Table 7. 1: A comparison of switching schemes modified to implement a 10-bit SAR ADC using 1.5-bit/cycle operation.

Switching scheme	Average switching energy (CV^2_{REF})	Energy savings	Area reduction	Logic complexity	Common-mode variation
Conventional [51]	2883.45	Ref.	Ref.	Medium	-
Set-and-down [19]	638.83	77.84%	50%	Low	$V_{ref}/4$
Rahimi [50]	662.74	77.01%	50%	Low	$V_{cm}/512$ (only LSB)
Proposed	330.2	88.55%	75%	Low	$V_{cm}/512$ (LSB-1)

7.6 Conclusion

The proposed CDAC switching scheme results in 88.55% energy savings and a 75% reduction in the CDAC size when compared to a conventional switching scheme modified to implement an identical 1.5-bit/cycle operation. Except for the last two conversion cycle, the proposed switching scheme offers constant common-mode voltage to the comparator input. The 1.5-bit/cycle technique requires simple control logic, provides a 12.5% error-tolerance margin, and relaxes the CDAC voltage settling time. All of these features are beneficial for low-power, smaller-chip-area, high-speed, single-channel SAR ADCs.

Conclusion & Suggestions for Future Work

8.1 Conclusion

The thesis primarily focuses on our seven important contributions to SAR ADC research. Additionally, the topics discussed include state-of-the-art SAR ADCs using binary and non-binary redundancy techniques, digital error-correction schemes, DAC switching schemes, hardware overheads, data-converter trends, and potential applications that benefit from this research.

A new technique using binary-scaled redundancy for a multi-bit per cycle conversion was proposed. A 10-bit SAR ADC using a conversion technique with an initial 1-bit followed by a 1.5-bit/cycle was developed using a 65 nm CMOS technology. The measured results show the strength of the design. The use of redundancy is optimized by not implementing redundancy in the first conversion cycle. 12.5% redundancy margins for subsequent conversion cycles enable a simple bit-overlap-and-add digital error-correction scheme, similar to a 1.5-bit/stage pipeline ADC. A new constant common-mode fractional reference voltage switching scheme was developed to implement an in-built binary-scaled CDAC redundancy. The new CCM-FRV switching scheme reduces the CDAC area by 50% when compared to a conventional switching scheme modified to implement an identical redundancy technique. The CCM-FRV switching scheme maintains constant common-mode to the input of the comparator, which results in robust

SAR ADC operation. The in-built DAC redundancy and the CCM-FRV switching scheme reduces the hardware overhead. A custom MOM unit capacitor of 740 af was used to construct the CDAC. One-fourth of the total redundancy margin is traded off for the capacitor mismatch within the CDAC. Multiple erroneous decisions can be corrected, independent of where the erroneous conversion cycles occur and without requiring additional conversion cycles. This further advances the state-of-the-art error-correction capabilities of SAR ADCs. The gains from the 12.5% redundancy margins can be used to relax the CDAC voltage settling requirements, which increases the speed of the conversion cycles and results in a high-speed design.

A new energy-efficient switching scheme for a 1.5-bit/cycle SAR ADC with digital error-correction was also proposed. Nine conversion cycles of 1.5-bit/cycle are required to achieve 10-bit output. The proposed switching scheme reduces energy consumption by 88.55% and the CDAC area by 75% when compared to a conventional switching scheme modified to implement similar 1.5-bit/cycle technique. Top-plate sampling is used to reduce the switching energy spent during the first conversion cycle. The proposed switching scheme offers constant common-mode operation for all except the final two conversion cycles. Behavior simulations to model a 10-bit SAR ADC using the proposed switching scheme demonstrate its effectiveness for a high-speed, single-channel ADC. Additionally, the simple control logic required for its implementation and the CDAC voltage settling time relaxation is beneficial for achieving low-power, smaller-chip-area, and high-speed operation.

The current work on SAR ADCs with redundancy and error correction has generated support from the industry, who are interested in continuing this research for automotive applications.

8.2 Future Works

This thesis work can be further extended by exploring the following topics: First, suitable wide-bandwidth voltage reference buffer architectures for high-speed and high-performance SAR ADCs; second, circuit techniques to share a voltage reference buffer for a multi-bit per cycle SAR ADC; third, circuit techniques or fabrication technologies to address the sampling switch linearity limitation for high-sampling-speed ADCs.

Preliminary progress on addressing the sampling switch linearity has been made and “more-than-Moore” fabrication technology to address the sampling switch limitation has been explored. A brief discussion on our published work is presented in the following sections.

8.2.1 More-than-Moore Design – A Fully Integrated III-V/ CMOS SAR ADC

As Moore’s law nears its inevitable end, design methodologies such as using an on-chip integrated III-V HEMT and CMOS platform will be ushered in. One such integrated process [68] has been fabricated through a partnership between universities (the low-energy electronics systems group of the Singapore-MIT alliance for research and technology) and industry (Global Foundries). A designer can choose between III-V HEMT and CMOS devices.

Moore's law has enabled faster digital logic requiring less power. This enables faster SAR control logic, which is beneficial for high-speed SAR ADCs. However, for a high-speed, single-channel SAR ADC, the sampling switch poses a performance bottleneck for the available input bandwidth. The sampling switch also contributes to the overall data converters' non-linearity that can be observed in the SFDR plot shown in Figure 8.3.

Our experimental work uses an InGaAs sampling switch (i.e., a III-V HEMT device) and CMOS circuits such as a CDAC, a comparator, control logic, timing logic, and memory, in order to construct a 6-bit SAR ADC. A hybrid process design kit (PDK), compatible with a cadence design environment, is used to design the schematic and to conduct post-layout simulations. A foundry-proven CMOS metallization process is used to establish physical connectivity between the InGaAs and CMOS devices.

The InGaAs transistor offers ultra-low threshold voltage, low on-resistance, superior noise performance, and high breakdown voltage. This leads to higher bandwidth and better linearity when compared to a CMOS transistor in an identical manufacturing node. Since there is no bulk connection for an InGaAs transistor, the sampling switch is resilient to substrate noise coupling, which can affect its threshold. An InGaAs transistor using LEES technology has a threshold of 150 mV, which results in lower on-resistance. Due to the integrated metallization stack connecting the III-V HEMT and CMOS devices, there is no additional off-chip overhead.

The bootstrapped InGaAs sampling switch schematic is shown in Figure 8.1. Here, the signal Clk_S , denotes the sampling clock, and V_{INp} denotes the analog input

voltage. A 2D electron gas in the rectangular quantum well [69] forms the InGaAs transistor channel. Due to the low on-resistance of the InGaAs transistor, the top-plate sampling time is reduced by 1.94x when compared to a CMOS sampling switch used with similar technology. On-chip integration results in a reduction of parasitic elements such as inductance and capacitance, which provides a speed advantage when compared to off-chip integration. The HEMT transistor offers high electron mobility when compared to the CMOS, and this results in faster switching speeds. In our design, the sampling duration is 1 ns.

Fig. 8. 1: A bootstrap circuit including an InGaAs sampling switch.

8.2.2 Experimental Results

The ADC layout shown in Figure 8.2 occupies a $150 \times 150 \text{ } \mu\text{m}^2$ chip area. The InGaAs switch layout is marked with “1”. The post-layout results at 125 MSps for an input sinusoid at a frequency of 61.52 MHz show an SNDR of 33.7 dB and an SFDR of 52.07 dB. At a supply voltage of 1.8 V, the ADC consumes 1.99 mW (including clock buffers), resulting in a FOM of 0.4 pJ/conv-step at the Nyquist

frequency (equation 8.1). The timing circuit block dominates the power consumption at 1.16 mW, followed by the dynamic comparator circuit.

$$\text{FOM} = \text{Power (mW)} / (2^{\text{ENOB}} * f_{\text{sampling}}) \quad (8.1)$$

Figure 8.3 compares the SNDR and the SFDR with the frequency at 125 MSps for a 6-bit SAR ADC using an InGaAs and a CMOS sampling switch, respectively. A peak SNDR of 35.98 dB/35.56 dB and an SFDR of 53.17 dB/48.7 dB for the InGaAs / CMOS ADC are observed. The ADC with an InGaAs sampling switch has an SFDR 4.47 dB better than a CMOS-only ADC (Fig. 8.3). The performance summary is shown in Table 8.1.

Fig. 8. 2: The layout of the presented ADC with an InGaAs HEMT formed within the indicated active (yellow box) region on the ADC's III-V/CMOS layout.

Table 8. 1: Performance summary.

Architecture	SAR
Technology	180 nm CMOS / 350 nm HEMT
Resolution	6
Supply voltage	1.8 V
SNDR near Nyquist	33.7 dB
Sampling speed	125 MS/s
Power	1.99 mW
Area	0.0225 mm ²

Fig. 8. 3: A cross-plot of input signal frequency against the SNDR and the SFDR for InGaAs and CMOS sampling switch implementations.

8.2.3 Conclusion: A Fully Integrated III-V/ CMOS SAR ADC

An on-chip integrated III-V HEMT sampling switch and a CMOS 6-bit 125 MSps SAR ADC using a hybrid PDK with a foundry-proven metallization process was discussed. On-chip integration offers advantages drawing from both the III-V HEMT and CMOS technologies. An InGaAs transistor offers faster switching speed, faster settling, and low on-resistance, which results in improved dynamic performance. CMOS technology offers low-power and area-efficient digital logic intensive sub-systems.

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3. T. Krishna, S. B. Chia, A. Balachandran, **S. Sharma**, B. Wang, Z. Li, J. Michel, K. E. K. Lee, and L. S. Peh, “Automatic synthesis, place and route of III-V LED devices within a commercial silicon CMOS CAD tool”, US provisional 62/323028.
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