Pulsed laser scan methodology for single event effect (SEE) qualification

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**PULSED LASER SCAN METHODOLOGY FOR SINGLE
EVENT EFFECT (SEE) QUALIFICATION**

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SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

2018

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EVENT EFFECT (SEE) QUALIFICATION**

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SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

A thesis submitted to the Nanyang Technological University in
partial fulfilment of the requirement for the degree of Doctor of
Philosophy

2018

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

24 Aug 2018

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Date

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Chua Chung Tah

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

24 Aug 2018

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Date

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Prof Gan Chee Lip

Authorship Attribution Statement

This thesis contains material from papers published in the following peer-reviewed journals where I was the first and/or corresponding author.

Chapter 4 is accepted and to be published as C.T. Chua, S. Chef, K. Sanchez, G. Bascoul, P. Perdu, S.H. Tan and C.L. Gan, “Integrating pulsed laser for a galvo mirror based SEE scanning microscope with optical failure analysis capabilities,” in Proceedings of International Conference on Radiation Effects of Electronic Devices and RADECS Workshop, 2018.

The contributions of the co-authors are as follow:

- Prof Chee Lip Gan and Dr Philippe Perdu provided the initial direction for this study and edited the manuscript drafts.
- I co-designed the study with Dr Samuel Chef and performed the laboratory work at the School of Materials Science and Engineering, NTU and CNES, France.
- I prepared the manuscript drafts which were later revised by all the co-authors.
- I collected and analyzed the data which were presented in this publication.
- I prepared the devices under test, knife edge and automated data collection procedures required for this study.
- Dr Kevin Sanchez and Dr Guillaume Bascoul assisted in the set-up of pulse picker and monitoring photodiodes at CNES, France.
- Dr Samuel Chef provided guidance in the interpretation of the laser spot size and laser energy measurement data.
- Mr Soon Huat Tan provided guidance on the optical and scanning properties of the microscope system.

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- Prof Chee Lip Gan and Dr Philippe Perdu provided the initial direction for this study and edited the manuscript drafts.
- I co-designed the study with Dr Hock Guan Ong and performed the laboratory work at the School of Materials Science and Engineering, NTU and CNES, France.
- I prepared the manuscript drafts which were later revised by all the co-authors.
- I collected and analyzed the data which were presented in this publication.
- I prepared the microelectronic devices under test, electrical test boards and electrical characterization procedures required for this study.
- Dr Kevin Sanchez and Dr Philippe Perdu assisted in the set-up of electrical test equipment at CNES, France.
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- Prof Chee Lip Gan and Dr Philippe Perdu provided the initial direction for this study and edited the manuscript drafts.
- Dr Samuel Chef collected and analyzed the data which were presented in this publication. He also prepared the manuscript drafts.
- I assisted in the design of this study with Dr Samuel Chef and performed the preparatory laboratory work at the School of Materials Science and Engineering, NTU.
- I revised the manuscript drafts and provided advice on the interpretation of single event latch up phenomenon presented in this study.
- I calibrated and measured the laser energy data which were presented in this publication.
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- I prepared the manuscript drafts which were later revised by all the co-authors.
- I collected and analyzed the data which were presented in this publication.
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- Dr Qing Liu assisted in the conduct of focused ion beam cross-sectioning, scanning electron microscopy, transmission electron microscopy and energy dispersive x-ray analysis.
- Dr Kevin Sanchez and Dr Philippe Perdu assisted in the set-up of electrical test equipment, photon emission microscopy, laser frequency mapping and laser frequency probing at CNES, France.
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Abstract

This thesis addresses the need for alternative methods of single event effect (SEE) radiation testing in a period when microelectronic technology nodes are scaling to ever smaller dimensions. This results in increasingly complex devices and compels radiation test engineers to demand radiation test techniques which are capable of providing more information (both spatially and temporally) as compared to conventional broad beam heavy ion radiation test. Moreover, reliability and lifetime of advanced microelectronic devices are getting lower and thus, this thesis aims to study the influence of device ageing on its SEE radiation response. These issues are further complicated by demands for efficient radiation test methods to cope with the industry-wide shift towards the use of large amount of commercially-off-the-shelf (COTS) components which are not manufactured with radiation hardness and high reliability as primary priorities.

This thesis initiates with an introduction of the space radiation environment and its associated radiation damage on semiconductor materials, with particular focus on a type of spontaneous radiation damage called SEE. Through the discussion on the overview of Singapore's small satellite landscape and limited land area, this thesis first aims to establish an efficient radiation test methodology, based on the proposed pulsed laser scanning technique, in a laboratory setting. Details of the considerations made for the choice of scanning microscope system, laser source and optical delivery fiber are elaborated. Characterization of the laser spot size and measurement of pulsed laser energy stability are reported. Pulsed laser SEE tests were conducted on two separate devices fabricated with bipolar and CMOS process technologies, in order to benchmark this proposed scan system to other existing facilities.

The second objective of this thesis is to study the effects of ageing on SEE sensitivity in old and advanced microelectronic devices. LM124 operational amplifier, which was fabricated with old bipolar process technology, was investigated via use of various load resistors in order to vary the device's output current. Changes in electrical parameters were monitored but little change in the SEE sensitivity of this device was observed after 1002 hours of electrical and thermal stress. In contrast for advanced microelectronic

devices, significant change (at least doubling) in the SEE sensitivity of 65 nm CMOS chain of flip flops was observed after 130 hours of voltage stress.

The third and final objective of this thesis is to demonstrate the applications of the proposed pulsed laser SEE scan methodology and explore its advantages and possible areas of concern. This methodology was shown to be capable of assessing the various SEE sensitivities of LM124 in different bias conditions. In addition, the advantage of pulsed laser SEE scan methodology in localizing SEE-sensitive regions and applying mitigation schemes were demonstrated on PIC16 microcontroller. Results revealed SEE-sensitive structures and subsequent laser probing technique identified the source of sensitivity. Mitigation was carried out and SEE sensitivity was eventually resolved. For all of its benefits, the technique is not without vulnerabilities. A heavy ion test campaign was conducted on test structures containing chains of inverters. Pulsed laser test was conducted in an attempt to further understand the heavy ion results but no meaningful results were obtained. Further analysis via laser probing technique and frequency tests revealed issues with test structure design. Subsequent test board re-design improved bandwidth of the test setup but still fell short of observing meaningful results. In such a case, the laser scan methodology can be used as a screening test before heavy ion test campaign in order to identify possible bottlenecks in chip or test board design. Lastly, the proposed pulsed laser SEE scan methodology was demonstrated to induce damage in advanced microelectronic devices. A series of optical failure analysis and fault localization techniques were utilized to pinpoint the location of the laser-induced damage. Thereafter, focused ion beam cross-sectioning, transmission electron microscopy and energy dispersive x-ray spectroscopy found that the damage was related to nickel (in silicide layer) diffusion towards the gate terminal of the transistor.

In overall, this proposed methodology has shown the potential to support radiation testing, especially in Singapore where limited land area renders particle accelerators as an impractical method of test. This methodology builds on existing laser system by employing the scan methodology to improve efficiency and repeatability. On the other hand, this thesis also highlights the potential areas of concern in applying this methodology on advanced microelectronic devices as possible laser-induced damage and importance of test board design has to be carefully considered.

Lay Summary

The harsh space radiation environment induces a particular type of radiation damage which can potentially cause permanent device failure in a single strike. This type of radiation damage is known as Single Event Effect (SEE) and is a major concern for satellite engineers who need to preserve the functionality of the satellite throughout its mission lifetime. Conventionally, the qualification of SEE hardness is evaluated via the heavy ion test method. However, this ‘gold’ standard for SEE testing requires particle accelerator which occupies a large area of land. Moreover, this test method suffers from several limitations such as long waiting time, restricted access and high cost.

As microelectronic devices move towards smaller structural sizes and higher operational speed, the complexity of SEE test procedure and data analysis increases. These factors compel radiation test engineers to demand other radiation test techniques which can provide more information on the location and time of occurrence of SEE in the device. In addition, there is an industry-wide shift towards the use of commercially-off-the-shelf (COTS) components which are not manufactured with radiation hardness and high reliability as top priorities. This results in the demand for other efficient radiation test methods to cope with the large amount of COTS components to be evaluated for SEE hardness.

The first objective of this thesis is therefore to propose an alternative and efficient method of SEE radiation testing based on the use of pulsed laser SEE scan methodology. Details of the choice of scanning microscope system and optical components are elaborated. Laser spot size and energy are characterized and pulsed laser SEE tests were conducted on two separate devices for benchmarking purposes.

The second objective of this thesis is to study the effects of ageing on SEE sensitivity in old and advanced microelectronic devices. This investigation arises from the need to understand the interactions between reliability and SEE radiation hardness. LM124 operational amplifier, which was fabricated with old bipolar process technology, was stressed under high current and temperature. Changes in electrical parameters were monitored but little change in its SEE sensitivity was observed. In contrast, significant

change (at least doubling) in SEE sensitivity was observed after 130 hours of voltage stress for the chain of flip flops fabricated with advanced 65 nm CMOS technology.

The third and final objective of this thesis is to demonstrate the applications of this pulsed laser scan methodology and explore its advantages and possible areas of concern. This methodology was shown to be capable of assessing the various SEE sensitivities of LM124 in different bias conditions. In addition, the advantage of pulsed laser SEE scan methodology in localizing SEE-sensitive regions and applying corrective schemes were demonstrated on PIC16 microcontroller. For all of its benefits, the technique is not without limitations. Differences in test board design was found to affect the test results from heavy ion and pulsed laser tests. In such a case, the laser scan methodology can be used as a screening test before heavy ion test campaign in order to identify possible bottlenecks in chip or test board design. Lastly, the proposed pulsed laser SEE scan methodology was demonstrated to induce damage in advanced microelectronic devices. Optical failure analysis, fault localization and material analysis techniques were utilized to localize and characterize the laser-induced damage.

In summary, this proposed methodology has shown the potential to support radiation testing, especially in Singapore where limited land area renders particle accelerators as an impractical method of test. This scan methodology improves efficiency and repeatability. On the other hand, this thesis also highlights the potential areas of concern in applying this methodology on advanced microelectronic devices as possible laser-induced damage and importance of test board design has to be carefully considered.

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Abbreviations

APC	Angled Physical Contact
BTI	Bias Temperature Instability
CCD	Charge-Coupled Device
CMOS	Complementary Metal-Oxide-Semiconductor
CNES	Centre National d'Etudes Spatiales
COM	Comparator
COTS	Commercially-Off-The-Shelf
DD	Displacement Damage
DUT	Device Under Test
EDS	Energy Dispersive X-ray Spectroscopy
EEPROM	Electrically Erasable Programmable Read-Only Memory
EM	Electromigration
EOD	Electro-Optic Deflector
EOFM	Electro-Optical Frequency Mapping
EOP	Electro-Optical Probing
FC	Ferrule Connector
FDSOI	Fully Depleted Silicon On Insulator
FIB	Focused Ion Beam
FPGA	Field Programmable Gate Array
FWHM	Full-Width-Half-Maximum
GEO	Geostationary Earth Orbit
HCI	Hot Carrier Injection
I/O	Input/Output
IR	Infra-Red
LEO	Low Earth Orbit
LET	Linear Energy Transfer
LIVA	Light Induced Voltage Alteration
LTP	Laser Timing Probe
MEO	Medium Earth Orbit
NBTI	Negative Bias Temperature Instability
NRL	Naval Research Laboratory

NTU	Nanyang Technological University
OBIC	Optical Beam Induced Current
OBIRCH	Optical Beam Induced Resistance Change
PC	Physical Contact
PCB	Printed Circuit Board
PEM	Photon Emission Microscopy
PETS	Pre-irradiation Elevated Temperature biased Stress
RSIL	Refractive Solid Immersion Lens
SAA	South Atlantic Anomaly
SEE	Single Event Effect
SEL	Single Event Latchup
SEM	Scanning Electron Microscopy
SET	Single Event Transient
SEU	Single Event Upset
SMU	Source-Measure Unit
SPA	Single Photon Absorption
SRAM	Static Random Access Memory
TAMU	Texas A&M University
TDDB	Time dependent dielectric breakdown
TEM	Transmission Electron Microscopy
TID	Total Ionizing Dose
TIVA	Thermal Induced Voltage Alteration
TPA	Two Photon Absorption
USA	United States of America
VDD	Power Supply Voltage
VF	Voltage Follower
VTC	Voltage Transfer Curve

Chapter 1

Introduction

In 2011, the first Singapore-built satellite, X-SAT [1], was launched into space orbit. Since then, more than 10 other Singapore-built small satellites [2] were designed and launched into orbit. Averaging more than one satellite launch per year, this highlights the short development cycle of small satellite programmes and its need for efficient radiation test methods. In addition to the increasing use of high-performance advanced commercially-off-the-shelf components in small satellites, Singapore is also interested in building up capabilities for radiation hardening of devices. In this chapter, the motivation behind this thesis and an overview on the engineering need for alternative radiation test methodology will be explained. In addition, the scientific interests to evaluate the hypothesis that in advanced microelectronic devices, ageing can significantly affect its radiation sensitivity will be detailed. In realizing these engineering needs and scientific interests, specific objectives of this thesis will be defined and key findings will be highlighted in this chapter.

1.1 Motivation

Traditionally, the space and satellite industry has been dominated by large government agencies which hold considerably huge budget, long development and planning cycles with plenty of safety overheads in order to ensure long term viability of mission critical satellites [3-5]. In order to meet these high margins of safety overheads, satellite engineers typically rely on a small market of specially designed radiation hardened microelectronic devices which inherently suffer from long lead time and high cost [6].

In recent years, microelectronic technology nodes have been scaling [7] to unprecedented smaller dimensions rapidly. This has brought about commercial devices which are incredibly high in performance but offered at an affordable price. This greatly increases the gap between the price and performance of electronic components used in space, as compared to those used on Earth. This advancement in microelectronic technology is already currently imposing three main disruptions to the space and satellite industry, namely: (1) Recent industry-wide shift towards the adoption of small satellites [8-11] (with short development cycle) which are commonly initiated by new players such as universities or private companies, (2) Increasing use of state-of-the-art advanced microelectronic devices [12], and (3) Increasingly complex commercial devices [13] which can greatly increase the performance of satellite capabilities. Together, all these factors lead to an increasing amount of commercially-off-the-shelf (COTS) components to be used in satellite missions. However, since these COTS components are not originally intended for space flights, their radiation sensitivity has to be first qualified [14] before actual application.

Traditional radiation test methods include particle (heavy ion [15], proton [16], electron [17] or neutron [18]) accelerators or Co60 gamma ray source [19] which suffers from long waiting time, limited accessibility and high cost [20]. Due to the limited accessibility of these facilities, test campaigns are usually: (1) Very intense (i.e., each hour of test time is expensive and it is common for test teams to work in shifts to fully utilize the allocated timeslot), (2) Few samples [21] of each device type are tested in conservation of precious test time and (3) Tests are usually conducted on fresh samples as devices fabricated with old process technology are widely known to have very stable electrical behavior throughout the satellite's mission lifetime. In view of these

limitations, this thesis looks into developing an alternative radiation test methodology to cope with the above-mentioned disruptions through: (1) Setting up a quick test method to assess the radiation response of large number of COTS components in the short development timeframe of small satellites, (2) Assessing the possible impact of ageing [22] on radiation response of advanced microelectronic devices and (3) Providing more information (both spatially and temporally) on radiation response of complex microelectronic devices.

In Singapore, the above-mentioned trends and disruptions are especially relevant. The ecosystem for small satellite is growing [23] but radiation qualification of microelectronic devices is still in its infancy. This is partly due to a lack of radiation test sites on or nearby the island and thus, more often than not, radiation test campaigns have to be conducted at the limited number of facilities available worldwide [24]. This is further complicated by the logistics difficulty in transporting bulky test equipment and teams of test engineers to overseas test sites. This not only incurs additional costs but more importantly, increases the time wasted during the satellite design feedback loop.

1.2 Hypothesis/Problem Statement

Engineering need:

In light of the above discussion, there is a real engineering need to set up an efficient radiation test method in order to provide a quick assessment of the radiation response of microelectronic devices. Moreover, this alternative test method will need to provide additional information (both spatially and temporally), as compared to conventional radiation test method, on the radiation response of the microelectronic device in order to help satellite engineers analyze complex advanced microelectronic designs.

Scientific hypothesis:

With the set-up of the radiation test methodology mentioned above, we will apply this methodology to investigate our scientific hypothesis. In view of the lower reliability margins (due to reduced device lifetime) in advanced microelectronic devices, there is scientific interest in evaluating the hypothesis that the effect of device ageing on radiation response will be more prominent in advanced microelectronic devices. This

will potentially raise concerns to the space radiation community in order to take into account of device ageing during radiation qualification process and thereby improve the overall reliability of the satellite system.

1.3 Objectives and Scope

With the aim of resolving the problem statement and scientific hypothesis as mentioned in section 1.2, this thesis aims to achieve the following objectives:

1. To develop and set up an approach to efficiently evaluate SEE sensitivity.
2. To evaluate the effects of ageing on radiation sensitivity in old and advanced microelectronic devices.
3. To assess applications (advantages or limitations) of the proposed approach.

These objectives will be achieved in the scope of:

1. Refining the broad topic of radiation and its diverse types of radiation damage to be limited to a particularly spontaneous type called Single Event Effect (SEE).
2. The microelectronic devices covered in this thesis will be only limited to silicon based devices.

1.4 Dissertation Overview

This thesis addresses the engineering need to set up an efficient SEE radiation test approach and using this employed approach, to evaluate the scientific hypothesis that ageing will have a significant impact on the radiation response of advanced microelectronic devices. Details of the proposed pulsed laser scan methodology will be covered and using this methodology, the effects of ageing on devices fabricated with old and advanced process technologies will be evaluated. Last but not least, applications (advantages and concerns) of this proposed methodology will be evaluated and discussed.

Chapter 1 Introduction

This chapter presents the overall motivation for this thesis with a strategic discussion that is conducted in close reference to the Singapore context. The engineering problem statement and scientific hypothesis are elaborated. Research objectives, scope and key findings are also summarized.

Chapter 2 Literature Review

This chapter reviews the literature in four different sections. The first section presents the space radiation environment, its associated radiation damages, radiation test methods and also the concept of total reliability (electrical, thermal and radiation) for space satellite systems. The next two sections address the limitations (lack of spatial and temporal information and lack of consideration for ageing effects) of the state-of-the-art radiation test methods while the last section defines the contributions of this thesis in the context of current literatures.

Chapter 3 Experimental Methodology

This chapter describes the underlying principles of the various techniques employed during the duration of the thesis. SEE test techniques (like broad beam heavy ion and pulsed laser) will be discussed. Importantly, methodologies to characterize the laser parameters of the proposed pulsed laser scan methodology will be presented. Next, sample preparation of devices for backside optical analysis and electrical characterization of samples will be presented. Various optical fault localization techniques (like laser frequency probing, photon emission microscopy, etc.) to pinpoint failure locations in semiconductor material will be discussed. Furthermore, material analysis techniques (like Focused Ion Beam, Transmission Electron Microscopy) will be presented. Last but not least, a brief description on simulation methods used in this thesis will be included.

Chapter 4 Set up, characterization and benchmarking of pulsed laser SEE scan system

This chapter presents the setting up of the proposed pulsed laser scanning microscope system as an alternative to evaluate SEE radiation in not only an efficient but also informative manner. Choice of the type of microscope configuration, laser source, fibers and connectors are detailed. Characterization results of laser parameters (like pulsed laser energy and laser spot size) are reported. Benchmarking results of pulsed

laser SEE tests conducted on two different devices of dissimilar technology processes/architectures will be included.

Chapter 5 Effects of ageing on radiation sensitivity in old and advanced microelectronics

This chapter details the study to evaluate the scientific hypothesis that ageing will have a significant effect on advanced microelectronic devices. This study also demonstrates the efficient feedback loop that the proposed pulsed laser scan methodology offers to evaluate the effects of ageing on SEE response of microelectronic devices. Ageing tests were conducted on two different device types with dissimilar technology processes and changes in electrical parameters are reported. Little change in SEE sensitivity was observed for the device fabricated with old bipolar process technology while significant changes in SEE sensitivity were observed for devices fabricated with advanced Complementary Metal-Oxide-Semiconductor (CMOS) process technology. Further simulation results on changes in threshold voltage and SEE sensitivity are also reported to provide insights into the vulnerability of advanced microelectronics to ageing effects.

Chapter 6 Applications of pulsed laser SEE scan methodology

This chapter details the applications of the proposed pulsed laser SEE scan methodology and demonstrates its additional advantages and concerns. Two advantages (ability to assess the effects of device configuration on SEE sensitivity, localization of SEE-sensitive regions and subsequent application of mitigation schemes) and two concerns (complications of test board and laser-induced damage in advanced microelectronic devices) are reported.

Chapter 7 Discussion and Future Work

This chapter presents the summary of the thesis by discussing on the implications of various research results. A small section on the temporal advantage of the pulsed laser SEE scan methodology is also reported. Refined approaches from the results of this thesis and strategies for future work will be elaborated.

1.5 Findings and Outcomes/Originality

This research started just one year after Singapore had just launched its first small satellite into space and understandably, space radiation qualification, at that time, was still a relatively foreign domain for the local community. Nevertheless, through helpful interactions with many researchers across the globe, this research realized several scientific contributions to the space radiation community by:

1. Establishing a pulsed laser SEE scan methodology with the aim to provide an efficient, relatively low cost, low footprint, easily accessible alternative to conventional SEE radiation testing. The use of a confocal scanning microscope, stable pulsed laser source, optical fiber delivery together with an entire suite of various optical failure analysis techniques are some of the special features of this setup. This has been shown to be exceptionally useful in navigating through the increasingly complex devices (aggressively considered for small satellites) of recent years. Attempts to accurately determine the pulsed laser energy delivered to the device and measurements on a photodiode to obtain the laser spot size are also valuable to the community. “Laser beam spill” phenomenon, which highlight the effect of optical misalignment between laser fiber and pulse picker on laser energy, was reported. Benchmarking results provide further evidence to the validity of this technique across various SEE test methods (heavy ion, short and long wavelength pulsed laser).
2. Pulsed laser SEE scan methodology was employed to study the effects of ageing on SEE response while demonstrating that SEE evaluation can be efficiently conducted at multiple time points of stress duration. Ageing was found to have little impact on the SEE sensitivity of device fabricated with old process technology but found to significantly change the SEE sensitivity of device fabricated with advanced process technology. This provides further evidence in a domain where few literatures are available in evaluating such interactions. This also serves as a caution to the space radiation community that in the near future, radiation qualification of microelectronic devices has to take the impact of ageing into consideration for accurate evaluation of the total reliability of satellite systems. Through the use of the pulsed laser scan methodology, satellite engineers could also locate the structures which had become more sensitive to

SEE after ageing so that additional mitigation schemes can be applied to improve its hardness.

3. Further advantage of the employed pulsed laser SEE scan methodology was shown to localize SEE-sensitive regions in a commercial microcontroller. Through a combination of various optical failure analysis techniques, the origin of SEE sensitivity was identified. Mitigation actions were taken and although the device was eventually operated at a lower clock frequency, its SEE hardness was improved. These were all conducted in a single microscope platform without the need to shift the device and thus, avoiding issues of alignment or repeatability. This is particularly beneficial for investigations on microelectronic devices with small feature sizes which are fabricated with advanced process technology.
4. Complications of the device and test board configurations were reaffirmed and serves as a caution while conducting radiation qualification tests. Laser probing technique was employed to verify the functionality of the device and rule out issues with propagation of signals along the core test structure.
5. Complications of laser-induced damage in advanced microelectronic devices were also reported. Photon emission microscopy and laser frequency mapping were utilized to locate the site of damage. Further laser frequency probing verified the termination of signal propagation after the site of damage. After the localization of the site of damage, physical cross-sectioning was performed via focused ion beam to reveal the damaged structures. Subsequent transmission electron microscopy and energy dispersive x-ray spectroscopy found that nickel (in silicide layer) diffusion was the root cause of the failure.

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Chapter 2

Literature Review

It has been well known that the space radiation environment poses unique challenges to the microelectronic devices on board satellites and that stringent reliability standards have to be upheld in order to ensure mission success over its intended operational lifetime. In this chapter, space radiation environment and its associated types of radiation damage will be introduced. Special focus will be paid to SEE which occurs spontaneously and can cause destructive damage to microelectronic devices. The current 'gold' standard for SEE qualification test via heavy ion test method will be reviewed and the concept of aggregated reliability (interaction of traditional microelectronic reliability issues with radiation response) will be introduced. Section 2.2 will review and highlight the limitations of heavy ion particle accelerators in investigating the impact of cross-interactions (e.g., ageing) on SEE response. Key existing literatures on this topic will be highlighted. Section 2.3 will review and highlight the limitations of heavy ion SEE test method in efficiently evaluating SEE sensitivity of advanced microelectronic devices. Key alternative (or complementary) methods to induce SEE will be highlighted. With these limitations in mind, section 2.4 will present the contributions of this thesis in the context of existing literatures.

2.1 Microelectronic Devices' Reliability in Space

In the current state of satellite research and rocket launch capabilities, repairs of satellites (if any) are still mainly carried out by humans and replacement of faulty parts require expensive rocket launch services. In such a scenario, the cost of repair is immensely huge and satellite operators would avoid such situation through the design of satellites with high reliability requirements. In addition to the structural parts of the satellite, microelectronic devices on board the satellite have to be highly reliable in order to provide functional capabilities to the satellite during its operational lifetime. Factors such as thermal, electrical and radiation affect the reliability of microelectronic devices on board satellites.

The electrical environment is mostly similar to that on Earth while the thermal and radiation environment are unique to space. Though similar, the electrical environment should not be overlooked as the service lifetime and reliability of modern advanced devices are much lower than that of legacy devices. New architectures and materials are frequently introduced into the fabrication process and the reliability of these components are yet to be fully understood. This results in a variety of failure mechanisms which are dependent and can be accelerated based on different operating conditions of the device. For the second factor (thermal), when the satellite orbits around the earth, it will face stresses from thermal cycling according to its period of orbit. For example, typical temperatures faced by a satellite's solar panel can reach as high as 125°C and as low as -100°C [1], depending on the position of the satellite in its orbit (i.e., direct sunlight exposure or in eclipse), orbit altitude and extent of exposure to external environment. This cycle induces periodic thermal stress on microelectronic devices and could cause failure due to thermal fatigue. Another factor, radiation, is also unique to the space environment. Harsh radiation would cause undesired charges to be generated in microelectronic devices and could potentially cause soft or hard errors. Hard errors would cause permanent failure of the devices and pose serious threats to the operational goals of the satellite mission.

In this section, these factors which affect the reliability of microelectronic devices in space will be discussed. The space radiation environment will first be introduced and the possible radiation-induced damages will be discussed in detail. Special focus will

be dedicated to the discussion on SEE as unlike the other two types of radiation damage, SEE is spontaneously induced by a single particle strike and can potentially cause permanent damage to the device. Next, the current ‘gold’ standard for qualification of microelectronic devices’ SEE response will be discussed. The discussion will review the current state of qualification tests commonly done on fresh samples and highlight the lack of consideration for synergistic effects between ageing and radiation response. The section will end with a review of traditional microelectronic reliability issues and introduction of the concept of aggregated reliability which considers the radiation response of the microelectronic device together with its ageing degradation.

2.1.1 Space Radiation Environment and Damage

In this sub-section, an overview of the space radiation environment and diversity of satellite orbits will first be presented. The satellite’s orbit will determine the types of particles (and energies) it will encounter during its operation lifetime and thereby defining the dominant type of radiation damage it will be impacted by. Next, these different types of radiation damage will be introduced with a particular focus on SEE (which is the main scope of this thesis). Characteristics and mechanisms for the critical types of SEEs will be detailed.

Space radiation environment

Satellites orbit around the Earth at different altitudes and inclinations with the most commonly known orbits being Low Earth Orbit (LEO) for International Space Station, Medium Earth Orbit (MEO) for Global Positioning System satellites and Geostationary Earth Orbit (GEO) for communications satellite. Figure 2.1 shows some of these common orbits and also the peak radiation bands for Van Allen belt, which is an important source of space radiation to be cautious of.

Figure 2.1 Different types of satellite orbits and relative altitude of Van Allen belt [2]

For each orbit, the space radiation environment differs according to the intensity of particles or electromagnetic waves propagating through it. In general, the space radiation environment is mainly characterized by protons, electrons and heavy ions (charged particle with atomic number greater or equal to two), with other smaller components such as x-rays, alpha particles and neutrons. The sources of these particles stem from galactic cosmic rays, solar flares and Van Allen belts. Typically, the Van Allen belt is categorized into two different zones of inner and outer belt. The inner belt, which exists at an altitude of 500-5500 km, consists mainly of energetic protons while the outer belt (altitude of 12000-22000 km) consists of electrons, protons and small amount of heavy ions (due to cosmic rays) [3]. Of particular interest and concern for low earth-orbiting satellites is the harsh environment posed by the Van Allen belt and South Atlantic Anomaly (SAA). The SAA is a region of intense radiation arising from the tilt of the Earth's magnetic poles and this region can dip to orbital altitudes as low as 300 km. Figure 2.2 shows the geometry of the Van Allen belt and also the dipping of the SAA into low altitudes.

Figure 2.2 Van Allen Belt, which contains highly energetic protons and electrons, with the dipping of the SAA to low altitudes and posing immense threat to satellites in low orbits [4]

The presence of these high radiation zones around Earth and high energy particles (from solar and cosmic origin) meant that electronic components in orbiting satellites will be exposed to high levels of radiation damage. Table 2.1 illustrates the range of high energy particles which produce radiation damage in the space environment.

Table 2.1 Energy range of particles in space radiation environment [5]

PARTICLE	ENERGY RANGE (MeV)	SOURCE
PROTONS	0.1 TO 500	EARTH'S RADIATION BELTS AND SOLAR FLARES
ELECTRONS	UP TO 7	EARTH'S TRAPPED RADIATION BELTS
GALACTIC COSMIC RAYS	UP TO 20,000 [†]	STEADY BACKGROUND IN DEEP SPACE (SLIGHTLY MODULATED BY SOLAR FLARE ACTIVITY)
NEUTRONS	0.001 TO 1000	TERRESTRIAL (FROM COSMIC RAY INTERACTIONS IN THE EARTH'S UPPER ATMOSPHERE)
ALPHA PARTICLES	UP TO 9	DECAY OF RADIOACTIVE IMPURITIES IN MATERIALS USED IN DEVICES

[†]A very small number of galactic cosmic rays have much higher energies.

As discussed above, the operating altitude and orbit of the satellite will greatly alter the radiation environment and particle energies. This will ultimately determine the type of radiation damage and required qualification tests prior to launch and space flight.

Space radiation damage

Space radiation damage in semiconductor material can be broadly categorized into total ionizing dose (TID), displacement damage (DD) and single event effects (SEE) [6]. The mechanisms responsible for these radiation damages are due to ionization effects for the case of TID and SEE, and atomic lattice displacement for DD. Figure 2.3 illustrates the ionization effects generated either by heavy ions or protons which could ultimately lead to either TID or SEE radiation damage or both. TID differs from SEE in that TID occurs in the dielectric layers under the gate while SEE occurs in both the dielectric and silicon substrate layers of a semiconductor device. TID can be broadly understood as a long-term accumulation of charges in the dielectric layers of the semiconductor device while SEE results from transient charges. Figure 2.4 illustrates the lattice displacement effects which could ultimately lead to DD radiation damage.

Figure 2.3 Ionization effects generated by heavy ions and protons, leading to either TID or SEE radiation damage or both [7]. TID occurs in the dielectric layer under the gate while SEE occurs in both the dielectric and silicon substrate layers.

Figure 2.4 Lattice displacement leading to DD radiation damage through (a) Atomic displacement, (b) Radiation induced vacancy and interstitial defects [8]

Furthermore, SEE can be categorized into soft error (non-destructive) and hard error (destructive) [9], with the various types of SEE being illustrated in Figure 2.5. Unlike TID and DD which are both dependent on cumulative doses over time, SEE is induced in microelectronics devices when the particle deposits large amount of energy into the device in a single strike. SEE can result in catastrophic failure and disrupt the device functionality way ahead of its intended useful lifetime. Common mitigation techniques like shielding, which work for TID and DD, are ineffective in protecting devices from SEE. These sudden and unpredictable occurrences of SEE in microelectronics devices have garnered much attention among the international community in finding new ways to characterize and predict SEE error rates. The unexpected nature of SEE is also the main motivation behind this thesis and forms the focus of our investigations. In this thesis, single event latchup (SEL), single event transient (SET) and single event upset (SEU) are investigated in detail and will be frequently mentioned. SET and SEU are not destructive effects while in severe cases, SEL can potentially be destructive to the device.

Figure 2.5 Different types of Single Event Effects (SEE). SEL, SET and SEU will be frequently mentioned in the rest of this thesis [9]. In severe cases, SEL can be destructive and lead to hard errors.

SEL

SEL is defined as an unexpected single event induced surge in current which can cause destructive damage to the device. In CMOS devices, there are many complex paths where low or high current SELs can occur. These paths form in the presence of parasitic p - n - p - n structures. For example, in the case of a CMOS inverter as shown in Figure 2.6, this can be formed by the PMOS's p -source, n -well, p -substrate and NMOS's n -source. The two intrinsic bipolar transistors are cross-coupled and when an ion hits, the generated track of charges can forward bias the base emitter junction. The positive feedback between the cross-coupled transistors increases and sustains the current flowing through it. This latched-up state can only be cleared by power resetting of the device and if left unattended, could lead to destructive damage to the device.

Figure 2.6 Parasitic p - n - p - n structures in a CMOS inverter composed of PMOS's p -source, n -well, p -substrate and NMOS's n -source [10]. Transient current generated from radiation strike can cause an increased current state or SEL.

With the scaling down of microelectronic devices' technology node, the operating voltage decreases and contributes (in general) to the decrease in sensitivity of devices to SEL. In this case, since the power supply voltage controls the base-collector voltage across both intrinsic bipolar transistors, the collector current is limited by the smaller operating voltages of more advanced technologies. Thus, it becomes harder to bias the transistors in forward bias mode. For example, Boselli and co-workers [11] reported on a decrease in SEL sensitivity as technology node scales down from 180 nm to 65 nm. This was mainly attributed to the decrease in power supply voltage as technology scales and thus, leading to a larger differential between the power supply voltage and the required holding voltage for latch up. This was further supported through more recent studies by Dodds and co-workers [12] who reported that the tested SRAMs in 45 nm technology node were immune (up to linear energy transfer, LET, of 118 MeVcm²/mg) to SEL at room temperature. On the consideration that the decreased operating voltage would decrease the likelihood of exceeding the holding voltage required for maintaining the latched state and ultimately leading to a decreased SEL sensitivity in more advanced technologies, Johnston [13] even postulated that advanced devices (operating at voltages below 2 V) could be immune to SEL. This was however not as straight-forward as several studies had reported SEL sensitivity in devices operating at low voltages [14-16].

SET

SET is defined as the single event induced temporary spike in the device voltage to a certain amplitude and duration. SET occurs in analog devices where there are no digital elements and this allows the induced transient voltage to propagate to the output of the device. When a particle traverses through the device, a track of electron-hole pairs will be generated. These charges will be swept by the electric field of the device and result in a transient current. This transient current will propagate to the output of the device where it will be observed as a transient voltage of a certain amplitude and duration. The amplitude and duration of a SET varies widely with input bias conditions, output loading and the amount of energy of the incident particle or photon. To complicate matters further, if the analog device is followed by a digital element, the generated SET can cause a change in the state of the digital element, thereby resulting in a SEU or corruption of stored information.

With the scaling down of microelectronic devices' technology node, the operating voltage decreases while the operating frequency increases. With an increase in operating frequency, the probability of a SET causing a change in state of a follow-on digital element at a valid clock edge increases too. For example, Benedetto and co-workers [17] reported on the increase in SET pulse width as technology node decreases from 0.25 μm to 0.13 μm . The paper also showed the strong effect of power supply voltage on SET pulse width. As the operating voltage of the device falls below its nominal value for a particular technology node, the SET pulse width increases. This trend was observed for the three technology nodes (0.25 μm , 0.18 μm and 0.13 μm) investigated in the paper. With SETs of longer pulse width, further verification was conducted with a DICE cell operated at different voltages. In line with expectation of higher capture probability with SETs of longer pulse width, the results showed that with lower operating voltage, the error rate of the DICE cell increases (i.e., increased SEE sensitivity).

SEU

SEU is defined as the single event induced change in information (due to charging or discharging) of a memory storage element. These changes are 'soft error' which can be cleared with a reset instruction or writing of new data into the memory storage element. In the illustration as shown in Figure 2.7, a typical Static Random Access Memory (SRAM) is commonly made up of a 6-transistor memory cell design. Two inverters are cross-coupled and when a particle traverses through the device, a track of electron-hole pairs will be generated. These charges will be swept by the electric field of the device and result in a transient current. This transient current could temporarily turn on an originally-off transistor and cause a transient voltage at the drain of the affected inverter. This drain terminal, which happens to be the gate of the other inverter, will be biased with the transient voltage and if the transient sustains for a sufficiently long duration, feedback in the cross-coupled inverter will change the states of the SRAM memory cell, resulting in a SEU.

Figure 2.7 SRAM bit cell composed of 6-transistor design with cross coupled inverters [18]. Each inverter consists of two transistors. BL represents bit-line while WL represents word-line. Transient current generated from radiation strike can cause a change in states of the memory cell, resulting in a SEU.

With the scaling down of microelectronic devices' technology node, the operating voltage and critical charge of the devices decrease and this could lead to higher sensitivity to SEU. However, it should be noted that the SEU-sensitive area also shrinks with technology advancement (i.e., probability of particle strike at sensitive region is lower) and thus, the trend is more complicated than anticipated. For example, across technology nodes of 0.25 μm , 0.18 μm , 0.13 μm and 90 nm, Hazucha and co-workers [19] reported an 8% per generation increase in the error rates per bit of the tested SRAM samples. In contrast, Gadlage and co-workers [20] reported relatively similar error rates per bit of the tested D-flip flop across technology nodes of 0.25 μm , 0.18 μm , 0.13 μm , 90 nm and 65 nm. Using the experimental data of threshold LET and saturation cross-section, Gadlage went on to project the scaling trend for technology nodes below 65 nm. It was projected that the error rates per bit will decrease for technology nodes smaller than 90 nm. In another report from Gaspard and co-workers [21], as technology node scales from 180 nm to 28 nm, the SEU cross section decreased for the tested D flip-flop samples. It should however be noted that in that paper, there were no attempt to compare the threshold LET and thus, it remains unclear whether a lower LET could trigger SEU in the tested designs. To complicate the matter even further, Dixit and Wood [22] reported a decrease in error rates per bit as technology node decreased from 180 nm to 65 nm but an increase for 40 nm in the tested SRAM samples. However, in the tested flop samples, the error rates per bit decreased continuously from technology node of 130 nm to 28 nm.

These conflicting results highlight the complexities of predicting SEE response for advanced microelectronic devices and explains the increased demand for ground-based SEE testing. However, the test methods for qualification of microelectronic devices for SEE response are limited and this imposes demand stress on the already crowded beam time at heavy ion particle accelerator test facilities. This ‘gold’ standard for SEE testing will be further elaborated in the following sub-section.

2.1.2 Current ‘Gold’ Standard for SEE Testing: Heavy Ion Test Method

In conventional heavy ion radiation testing, an energetic particle traverses through a semiconductor material and leaves behind an ion charge track. The electron-hole pair creation is due to coulomb interaction between the incident heavy ion and electrons in the host lattice. The incident heavy ion loses energy through coulomb scattering and the rate of energy transfer is commonly known as LET. Since this energy loss is directly proportional to the density of material, the heavy ion LET is commonly represented as shown in equation (1):

$$LET = \frac{1}{\rho} \frac{dE}{dx}, MeVcm^2 / mg \quad (1)$$

where ρ is the material density, x is the penetration depth and E is the incident energy of the heavy ion. Depending on the incident energy, atomic number of the ion and properties of the semiconductor material, the heavy ion will have varying penetration depth, also known as the range of the heavy ion.

As a result of the energy deposition discussed above, the passage of heavy ion through the semiconductor material will cause charge generation and collection at the transistors, which will ultimately cause SEE phenomenon in the device. The number of induced SEE, N_{see} , varies with different LET. The division of induced SEE failures by the number of ions per cm^2 will give an important parameter known as the SEE cross-section, as shown in Equation (2):

$$\sigma_{see} = \frac{N_{SEE}}{\Phi(E_p) \cdot \cos \theta} \quad (2)$$

where $\Phi(E_p)$ is the fluence in ions per cm^2 , at a particular energy, E_p and θ is the angle of incidence of the particle with respect to the normal of the device's surface. More often than not, heavy ion radiation testing will be carried out using an ion cocktail where a mixture of ion species with different energies will be accelerated and irradiated towards the semiconductor material. At various ion energies, the number of SEE events and ultimately SEE-sensitive cross-section will be recorded and plotted as a saturation curve. Another critical parameter from the curve is the SEE threshold, which is the minimum energy deposition in order to generate SEE. Any energy greater than this SEE threshold will result in an increase in SEE cross-section and ultimately, a saturation level will be attained.

The charge generation rate of heavy ion is defined by its incident energy and initial LET. In the case of heavy ion SEE testing, the variation in ion energy is commonly assumed to be negligible and therefore leads to a popular model, the Gaussian cylindrical model. This model is an approximation to the charge distribution which is inexpressible in the closed form and thus represented in equation (3) [23]:

$$g_{ion}(r, z, t) = \frac{1}{\pi^{\frac{3}{2}} r_0^2 \tau_{rad}} \frac{L_i}{E_p} e^{-\frac{r^2}{r_0^2}} e^{-\frac{t^2}{\tau_{rad}^2}} \quad (3)$$

where L_i is the initial LET, r_0 is the radius of the cylindrical generation rate (commonly assumed to be $0.1 \mu\text{m}$) and E_p is the average energy (3.6 eV in silicon) to generate an electron-hole pair. τ_{rad} is the time (order of 1 ps) of flight across the semiconductor material. Extending from equation (3), Figure 2.8 shows the plot of carrier density generated when a heavy ion traverses through a semiconductor material.

Figure 2.8 Carrier density generated in silicon using a ^{275}Fe ion with LET of $24\text{ MeVcm}^2/\text{mg}$ [23]

In practice, heavy ion SEE tests are conducted according to test standards such as the JESD57 [24], ESA/ESCC 25100 [25] or ASTM F1192-11 [26]. In the event that the heavy ion SEE LET threshold of the samples is found to fall below $40\text{ MeVcm}^2/\text{mg}$, several additional guidelines [27, 28] are also available in the community which advises on additional proton SEE tests to be conducted. Briefly, the test flow for such radiation test campaign starts with definition of the space radiation environment which the microelectronic device will be operating in. According to the space radiation environment and mission duration, various radiation tests (heavy ion or proton SEE, x-ray TID, proton or neutron DD, etc) have to be planned. In the case of heavy ion tests, a test plan has to be submitted to the radiation test facility while arrangements for an available time slot for the required beam time will be made. Due to the high demand for beam time at the limited number of particle accelerators around the world, the waiting time for a suitable time slot can be very long. This problem had recently been highlighted [29] and waiting time of six months for an eight-hour time slot was already very common. This amount of beam time is usually barely sufficient, after taking into account of the time needed to set up the test equipment, verification of the SEE detection schemes, troubleshooting of possible issues, recording of SEE events, change of heavy ion species and change of samples at the test facility.

In view of the unique situation of precious beam time and limited availability of heavy ion SEE tests, it can be understood that test standards usually recommend tests to be modestly conducted on two to three samples [25] for result verification. The community

recognizes that although more tests should be conducted, it is no longer practical and experience accumulated over the years had proven that the test standards' recommendations are sufficient for most cases. Also, in the interests of limited beam time, tests are conventionally conducted on fresh samples and influence of ageing on the devices were considered separately [30]. This was perhaps acceptable for legacy devices but more reports on the synergistic effects affecting SEE sensitivity [31, 32] triggered the consideration if ageing degradation is already imposing effects on the SEE sensitivity of the devices over time. This concept of aggregated microelectronic reliability, with consideration of ageing degradation and SEE response, will be discussed further in the following sub-section.

2.1.3 Aggregated Microelectronics Reliability

In this sub-section, the concept of aggregated microelectronic reliability, which takes into account both the effect of traditional reliability issues and radiation response of the microelectronic devices, will be introduced. Firstly, the decrease in devices' operational lifetime and reliability with scaling down of technology nodes will be reviewed. Next, traditional reliability issues such as electromigration (EM), bias temperature instability (BTI), time dependent dielectric breakdown (TDDB) and hot carrier injection (HCI) will be covered. Focus will be placed on EM (as it is one of the top issues for devices fabricated with bipolar process technology) and also on negative-BTI or NBTI in short (as it can induce significant threshold voltage shifts in CMOS transistors). Last but not least, the impact of these traditional reliability issues on radiation response of microelectronic devices will be discussed.

Decrease in devices' operational lifetime and reliability with technology node scaling

Microelectronic devices' reliability has been well studied with the aim of increasing the lifetime of devices and avoiding premature failures (which invites intense complaints and criticisms from customers, especially for cases where devices are dead-on-arrival). In the 1970s, the main factors affecting microelectronic devices' reliability are related to package-level issues from bonding, corrosion and ionic contamination [33]. On the interconnection-level, the main failure mechanism was EM in the metal interconnection lines [34]. It was only until the late 1970s and early 1980s when the scaling down of oxide thickness resulted in transistor degradation due to HCI [35, 36] and TDDB [37].

Figure 2.9 shows the decrease in devices' useful lifetime as technology node scales to smaller dimensions. This adversely affects the reliability of microelectronic devices and is particularly a big concern for satellite electronics which do not enjoy the luxury of repair or replacement in space. Thus, recent trends in technology node scaling and its effects on microelectronic reliability should be analyzed.

Figure 2.9 Decrease in useful lifetime of devices with technology scaling from 180 nm to 65 nm [38]

As indicated in the report from International Roadmap for Devices and Systems [39], the critical reliability issues for microelectronic devices in the near term (up to year 2024) are related to failures at the transistor-level. These issues include TDDB, BTI and HCI. In the long term (up to year 2033), reliability issues are focused around the use of new materials and design architecture in microelectronic devices. With technology node scaling, several impacts to reliability can be considered. For instance, with a thinner dielectric layer, the time to the first oxide breakdown is dramatically reduced. The shift in transistor threshold voltage is another concern due to scaling down of operating voltages and new introduction of silicon oxy-nitride (or other high-k dielectric materials based on hafnium, zirconium, etc.) to replace traditional silicon dioxide as the dielectric layer. The introduction of metal gates to replace traditional

polysilicon gates can also result in uncertainty over thermo-mechanical response in the device structure. Introduction of copper interconnects and low k dielectrics on the front-end fabrication process can result in higher operating temperatures on the die due to poorer thermal conductivity of low k dielectrics as compared to traditional solutions using aluminum and silicon dioxide. These factors contribute to the decrease in lifetime of microelectronic devices but fortunately, studies have been conducted and a device's failure mechanisms can be analyzed using a physics-based approach.

Traditional reliability issues

As discussed above, there are several failure mechanisms (EM, BTI, TDDB, HCI, etc.) leading to the decreased reliability of advanced microelectronic devices. EM and BTI will be the main focus in this thesis while TDDB and HCI will be briefly described. Due to the differences in structure between bipolar and CMOS process technologies, the failure mechanisms and accelerating factors for these two architectures are slightly different. For older devices fabricated with bipolar process technology, EM is one of the top reliability concerns.

EM is the failure of the metal interconnect due to mass transport of atoms in the direction of electron flow. This migration leaves void at its origin while building hillocks at the migration destination. With the migration of atoms away from the origin, the effective width of the interconnect ultimately decreases, causing an increase in current density and further accelerates the phenomenon. Figure 2.10 presents a simple schematic of the void and hillock formation due to EM.

Figure 2.10 Schematic of failure in metal interconnect due to EM. Voids form at the origin while hillocks form at the migration destination [40]

The mass transport of atoms is due to the momentum transfer from the energetic electrons to the metal atom. As the mass of the electron is much smaller than the metal atom, diffusion of the metal atom must be aided by vacancies in the interconnect. These vacancies are commonly found in the interconnects' grain boundaries and thus, diffusion of metal atoms will occur along these paths. EM is commonly described by the Black's model [41] and represented by equation (4) as follow:

$$t_{50} = A\left(\frac{1}{J}\right)^n \exp \frac{E_a}{kT} \quad (4)$$

where t_{50} is the median time to failure, A is material constant, J is the current density, n is the current density exponent, E_a is the activation energy, k is the Boltzmann's constant, T is temperature in Kelvins.

From equation (4), it is clearly evident that current density and temperature are the main acceleration factors for EM. In consideration of the current density, not only the main interconnect wire but also the contact holes and vias should be considered. Indeed, due to the small dimension of the vias, studies had found that voids frequently occur at the interconnect-metal vias interface [42]. Issues due to EM can be alleviated by designing multiple vias (to distribute the current evenly along the interconnect) and also to avoid 90-degree bends in wires (which will significantly increase the current density).

In older technology nodes, aluminum interconnects have been conventionally used due to its good conductivity and compatibility with silicon. Recent developments for faster devices have adopted copper as the interconnect material due to its higher melting point which could slow down atomic diffusion. Unlike the case of aluminum, copper atomic diffusion occurs dominantly along the interfaces instead of grain boundaries. This is due to the poor bonding between copper and the dielectric, thus forming a high mobility diffusion interface for copper ions. The quality of the interface is thus very critical and EM in copper interconnect remains a subject of investigation for devices fabricated with advanced process technology.

BTI, on the other hand, was found to occur mainly in the interface between silicon substrate and the dielectric layer. This phenomenon causes a shift in the threshold

voltage of the transistor and affects its ability to turn on and off. NBTI occurs in the PMOS when a negative bias is applied to the transistor while positive-BTI (or PBTI in short) occurs in the NMOS (which was observed to be more pronounced in newer technologies utilizing high k gate dielectrics) [43]. In devices utilizing silicon dioxide as the dielectric layer, NBTI was found to be more severe [44] as the holes in the PMOS inversion channel were found to interact with the oxide states. Figure 2.11 shows the schematic which illustrates the drift of H^+ ions into the silicon dioxide during negative gate bias to the PMOS transistor. Although negative bias alone can induce NBTI effects, further acceleration can be achieved at elevated temperatures [45].

Figure 2.11 Schematic diagram illustrating the case of NBTI in PMOS where the H^+ ions (released from broken Si-H bonds) drifts in the direction of the electric field into the silicon dioxide layer [46]. Black filled circles represent silicon atom, red filled circles represent hydrogen atom and unfilled circles represent oxygen atom.

With a negative gate voltage on the PMOS, the electric field points in the direction from the silicon to the silicon dioxide. During device operation, if the Si-H bond breaks, the H^+ ion will drift in the direction of this electric field into the silicon dioxide and cause degradation in the dielectric layer. Initial models suggested that interface traps are generated when the high electric field causes the dissociation of the Si-H bond and thus leaving de-passivated dangling bonds at the interface. In addition, pre-existing bulk defects in the dielectric layer can trap holes and cause a shift in the threshold voltage of the transistor. Several other models have been proposed to describe NBTI caused primarily by interface trap generation through hydrogen reaction-diffusion [47], by hole trapping in preexisting defects [48], by strong coupling between interface trap and hole traps through two-stage model [49], by uncoupled interface trap and hole traps [50, 51]

and by uncoupled interface trap, hole trap and oxide fixed charges [52, 53]. Although research debates are still on-going, it is generally accepted that the drift of H⁺ ions due to NBTI induces both interface traps [54] and fixed oxide charges [55].

A unique phenomenon for NBTI is the presence of defect recovery when the stress is removed [56]. Results have shown that this recovery is not entirely complete and there remains some permanent degradation in the device. In view of the permanent and recoverable components of NBTI, the following general equation has been proposed [33, 55, 57]:

$$\Delta V_{TH} \propto \left[\underbrace{\exp(\alpha_1 V_{GS}) t^{n_P}}_{\text{Permanent Part}} + \underbrace{V_{GS}^{\alpha_2} (C_R + n_R \log_{10}(t))}_{\text{Recoverable Part}} \right] \exp\left(-\frac{E_a}{kT}\right) \quad (5)$$

where ΔV_{TH} represents threshold voltage shift, α_1 and α_2 represents voltage scaling factor which are dependent on technology, V_{GS} represents gate-source voltage, t^{n_P} , C_R , n_R represents time exponents, E_a represents activation energy, k represents Boltzmann's constant and T represents temperature in Kelvins.

From equation (5), it is clearly evident that although negative bias alone can induce NBTI, temperature is also a main acceleration factor. Also, due to the recoverable part, NBTI is relatively complex to measure or model. Several measurement techniques involving fast measure-stress-measure [58-60], fast on-the-fly [61] and ultrafast on-the-fly [62] have been proposed. On-the-fly techniques are now the most commonly accepted due to its avoidance of recovery artifacts. However, such techniques require specific measurement instruments and process which requires careful consideration.

With the scaling down in gate oxide thickness, NBTI was found to worsen and thus, is a leading reliability concern in advanced microelectronic devices. Figure 2.12 shows the decrease in device lifetime as a function of technology node scaling. Although process improvements have been carried out over the years, new architectures such as FinFETs have been found to degrade BTI lifetimes [63] and NBTI remains a dominant reliability concern for advanced technology nodes.

Figure 2.12 Decrease in device lifetime due to NBTI as a function of technology node scaling [64]. FDSOI represents fully depleted silicon-on-insulator devices.

TDDDB, as its name suggests, is the degradation of the dielectric layer, resulting in a breakdown of the layer to act as an insulator and thus, leading to large leakage currents between the anode and cathode. With a breakdown in the dielectric layer, it will no longer be possible to control the current flow between the source and drain via the voltage applied at the gate and thus, resulting in the failure of the transistor. Experimental results have shown that TDDDB is highly affected by the electric field across the dielectric and could lead to soft (or hard) breakdowns in mild (or aggressive) cases. Although debates are still on-going, it is generally accepted that for moderately thick oxide layers with high defect densities, the originally empirical-based $1/E$ model [65] and the physical-based E model [66] are sufficient to explain this phenomenon at low and high electric fields, respectively. For very thin oxide layers (typically less than 5 nm), a voltage-driven model [67] is necessary. As the oxide layers become thinner, charges tunnel through the dielectric layers and form a conducting leakage path. This results in less occurrences of hard breakdowns and instead, soft breakdowns are usually observed in thin oxide layers. With the scaling down in operating voltages and increasing use of high- k dielectrics with technology node advancement, this issue will be partially moderated and thus, reducing the concern of TDDDB as compared to BTI in advanced technologies.

HCI is the injection of high energy carriers into the insulating gate oxide and thus, forming trap centers which can shift the threshold voltage and subthreshold leakage current. The modes of hot carrier injection had previously been proposed and discussed extensively by Takeda [68, 69]. A unique feature of HCI is that unlike most of the other degradation mechanisms, it is enhanced at low temperatures [70]. This is primarily due to the enhancement in electron free mean path and rate of impact ionization at low temperatures. With the reduction in power consumption and use of high k metal gate in advanced technology node, this issue is less of a problem [71]. However, it should also be noted that channel lengths are scaling much faster than operating voltages and this worsens the HCI issue. Last but not least, the increased operating frequencies of advanced microelectronic devices accelerates the negative impact of HCI on reliability (as the substrate current is the highest during state transitions) and thus, HCI remains a concern in advanced microelectronic devices.

Impacts of traditional reliability issues on radiation response

In view of the transistor parameter shifts induced by the above-mentioned traditional reliability issues, it can be understood that these changes in transistor parameters will affect its operating performance and consequently, its response to radiation effects. This problem is further aggravated by scaling down of technology nodes which causes a general decrease in reliability lifetime or margins in microelectronic devices. This trend increases the probability of these parameter shifts occurring during the operational lifetime of the satellite electronics and thus, potentially exerting significant influence on the radiation response of advanced microelectronic devices.

2.2 Limitations in Current SEE Test Standard (Effects of Ageing)

With the limitations of heavy ion beam time and tests conventionally conducted on fresh devices being covered in section 2.1, this section aims to review existing literatures and highlight the limitations of heavy ion particle accelerators to investigate the impact of cross-interactions (e.g., ageing) on SEE response. This section will first give a broad overview of studies on cross-interactions involving TID. As compared to SEE tests, TID tests (which were carried out via gamma-ray irradiation from cobalt-60 sources) are relatively easier to gain access to. Next, studies on cross-interactions involving SEE and the use of heavy ion particle accelerators will be covered. The

limited availability of heavy ion beam time poses the steepest barrier to studies of such nature. Last but not least, this leads to the use of alternative (or complementary) SEE test methods to further understand the impact of cross-interactions involving SEE. A focused review of state-of-the-art studies on interactions of ageing effects on SEE response of microelectronic devices will be finally discussed.

Since 1994, interactions of pre-irradiation elevated temperature biased stress (PETS) on the TID response of microelectronic devices had been reported in several papers [72-74]. It was found that PETS treatment significantly increased the device's sensitivity to subsequent TID tests. TID tests revealed larger shifts in threshold voltage and two orders of magnitude increase in power supply current [72] for devices which had been subjected to PETS. In another paper [75], a reduction in the dose level for TID failure (i.e., increase in TID sensitivity) was reportedly observed for two out of the three SRAM technologies investigated in the study. These studies serve as serious caution to the community that thermally-activated mechanisms during pre-irradiation tests can affect the radiation response of microelectronic devices. Further studies were conducted to investigate the interactions between HCI and TID [76], NBTI and TID [77] and TDDB and TID [78].

The above paragraph reviewed studies which involved TID tests (via gamma-ray irradiation generated from cobalt-60 sources) which are comparatively easier to gain access, as compared to heavy ion particle accelerators. Even so, studies had been carried out by relatively limited number of research groups and progress had been relatively slow. Indeed, for the case of cross-interaction studies involving SEE, there is even a smaller database of available literatures. In one study, Buchner and co-workers [79] reported on the effects of TID on the SET shapes in linear bipolar circuits. In the study, heavy ion irradiation was conducted on both fresh and TID-irradiated samples. It was found that TID can broaden SET at some transistors while narrowing SET at others. Further information was revealed by pulsed laser SEE tests which enabled localization of the origin of these SETs to various nodes in the circuit. Other studies investigating the cross-interactions involving SEE were commonly conducted using sources of radiation other than heavy ion particle accelerators. For instance, interactions were studied between TID and SEE [32] using pulsed laser test method and found that the amplitude of SETs can be amplified or reduced after TID irradiation.

Zooming further into the interactions between traditional reliability issues and SEE, one important study came from Bagatin and co-workers [80], who reported on the cross-interactions between NBTI and SEU response of SRAM cells fabricated with 130 nm process technology. In the study, heavy ion irradiation was conducted on both fresh and NBTI-aged samples. Alpha irradiations were conducted at several time points of NBTI stress to monitor the evolution of SEU sensitivity. However, even in this study, heavy ion irradiation was limited to two time points (fresh device and final aged device) due to limitations in heavy ion beam time. In both types of irradiation, it was found that NBTI stress did not significantly affect the SEU sensitivity of the tested samples. Comparing against a more advanced technology node, Cannon and co-workers [81] reported their research results on the effects of ageing on the soft error rates of 65 nm silicon-on-insulator SRAM. In the study, shifts in electrical parameter induced by TDDB and NBTI have been modelled and results showed that ageing can either cause an increase or decrease in the device's critical charge (Q_{crit}), depending on the site of breakdown. Upon consideration of experimental uncertainty, the authors ultimately concluded that ageing did not impose a significant impact on the soft error rates of the investigated SRAM.

In another study with the same technology node but on bulk CMOS technology, Moukhtari and colleagues [82] found a decrease in SET sensitivity after NBTI stress was imposed on a 65 nm bulk CMOS test vehicle. In the study, investigations were conducted on various chains of inverters, NOR gates and flip flops, with results showing a consistent decrease in SET sensitivity. Investigating on a more advanced technology node, Kauppila and co-workers [83] observed an increase in sensitivity cross-section of SEU after merely 12 hours of NBTI stress on 40 nm bulk CMOS flip flop. These conflicting results form the basis of focus in the scientific hypothesis of this thesis and thus, aiming to provide more experimental evidence in this area. In some of the reported cases, differences in technology and design of the tested structures could be the root cause of the conflicting results. In illustration, it is well known that silicon-on-insulator devices possess a minimal thickness of oxide layer with excellent isolation between the source and the drain. Therefore, electrical parameter shifts arising from ageing should be mild and this could eventually lead to subdued impacts on its radiation response. Moreover, different stress conditions (with the use of both voltage and

temperature) may confound the degree of ageing stress on the sample and increase the difficulty in making comparisons between various studies.

2.3 Limitations in Current SEE Test Standard (Test Efficiency on Advanced Devices)

With the limitations of heavy ion beam time and potential aggravation from the industry's increasing adoption of more COTS components being covered in section 2.1, this section aims to review existing literatures and highlight the limitations of heavy ion SEE test method in efficiently evaluating SEE sensitivity of advanced microelectronic devices. This section will first give a broad overview on the various alternative or complementary techniques to heavy ion SEE test method. Limitations of heavy ion SEE test method and advantages of these complementary techniques will be discussed. Last but not least, a focused review of state-of-the-art studies on pulsed laser SEE test method (choice of test method in this thesis) will be carried out. Limitations in existing pulsed laser SEE test method will be discussed and thereby forming the basis for engineering improvements investigated in this thesis.

In consideration of the industry's move to adopt more COTS components in space satellite missions, limited heavy ion beam time poses the steepest barrier to conducting SEE evaluation tests. COTS components offer better capabilities than most of the radiation-hardened space components but these devices are not qualified for space radiation environment. The large amount of COTS components to be space-qualified poses tremendous stress on the already congested beam time at heavy ion particle accelerators. Although not accepted as part of the 'gold' standard for SEE qualification, SEE can also be induced by other sources such as proton, Californium-252, neutrons, ion microbeam or focused pulsed laser. These methods will be reviewed in the following paragraphs.

Proton SEE tests induce SEEs through the by-products from the initial nuclear reaction between the incident proton and the device under test. The by-products cause ionization effects in the device which leads to the generation of electron-hole pairs and ultimately results in SEE. The illustration of this process had already been detailed in Figure 2.3. This test method is usually conducted in cases where the heavy ion LET_{th} was found to

be less than 37 MeVcm²/mg [28] and thus to verify the devices' sensitivity to low energy protons. In the case of proton testing, particle accelerators are needed and generally require a vast area of land. Proton testing is recommended for devices which have exceptionally low critical charge (currently shown on CMOS technologies less than 90 nm node) and thus, are sensitive to low energy (<10 MeV) proton SEE [28]. Other than the slight ease in arrangement for beam time, proton tests do not offer significant advantages over conventional heavy ion test. Also, the use of vast area of land is exceptionally impractical for Singapore.

Californium-252 radioactive source undergoes fission to produce a mixture of alpha particles, fission fragments and neutrons. The fission fragments are directed to the device under test to induce SEE. The advantage of this source is that it is relatively small (i.e., lab bench equipment) and cheap. However, a license to handle, store and operate a radioactive source is still mandatory. In addition, the fission fragments contain heavy and light components which can behave differently. Although typical LET levels can reach approximately 45 MeVcm²/mg [84], the range of the fission fragments (typically in tens of micrometers) are much shorter than that obtained at heavy ion particle accelerators (hundreds of micrometers). Thus, preparation of sample has to be carefully considered. This is particularly limiting for advanced microelectronic devices which have deep junctions or thick passivation layers.

Neutron-induced SEE is a specific problem to avionics operating in the terrestrial environment and would be briefly discussed here. Although not particularly critical in space, neutron-induced SEE is increasingly becoming a concern for avionics and also for ground-based electronics. In the terrestrial environment, neutrons are generated from the interactions of cosmic rays with atmospheric oxygen and nitrogen atoms. On the ground, neutron test facilities are electrostatic accelerators which produces 14 MeV neutrons from a deuteron-triton reaction [85]. Other methods of producing neutrons at the ground level are also available [86] and these sites produce much higher energy neutrons. In these cases, the setup requires particle accelerators which again requires vast area of land. The main drawback is the limited energy of this source as compared to the real environment. On the other hand, in recent technology nodes where the critical charge of the devices is sufficiently small, it had been demonstrated that this form of radiation test provides a good estimate of the SEU rate in SRAM devices [87].

Ion microbeam are generated through precise confinement of the broad heavy ion beam. This can be achieved through placement of a pin-hole aperture and collimation of the heavy ion beam to few micrometers. The final achievable spot size is usually on the order of 2 μm [88]. Another method involves the magnetic focusing [89] of the broad heavy ion beam and subsequent rastering of the microbeam via electrostatic or magnetic forces. The final achievable spot size is usually in the order of 1 μm [88]. In both methods, a vacuum environment is mandatory in order to preserve the range of the ions and also to reduce beam spreading through air scattering. The advantage of this test method is the ability to confine the heavy ion interaction volume to very small and localized regions. The rastering of the microbeam allows the injection of heavy ion in a very precise and confined manner. The drawback of this technique lies in the requirement for a heavy ion particle accelerator to produce the initial broad beam of heavy ion. Also, as the microbeam injects heavy ion in a small localized area, the deposited dose has to be carefully monitored [90] in order to avoid damage artifacts.

Pulsed laser SEE test method

D.H. Habing, from Sandia National Laboratories, was the first to demonstrate the use of lasers in radiation testing back in 1965 [91]. Two decades later in 1987, significant improvement in resolution was demonstrated by two separate research groups; one led by S.P. Buchner [92] and the other by A.K. Richter [93]. Buchner collaborated with Naval Research Laboratory (NRL) and his research showed that a pulsed picosecond laser can be used to efficiently measure the sensitivity of a commercial bipolar logic circuit to SEU. The SEU data, from the pulsed laser SEE test, showed relatively good agreement when compared to that from an ion beam. More importantly, due to the small size and controlled positioning of the laser spot, sensitive transistor junctions can be identified. Following these encouraging results, research gained traction and the laser technique has gained more recognition. There are two main laser techniques used in radiation testing and these are Single Photon Absorption (SPA) and Two Photon Absorption (TPA). SPA will be reviewed in detail while TPA will be briefly discussed. In general, using pulsed laser in SEE testing offers the benefits as follow:

1. Ability to control the position and time of laser hit on device
2. Ability to investigate transient effects by clock synchronization
3. No permanent damages such as TID or DD on device
4. Repeated irradiation on a single spot

5. Ease of accessibility to test equipment
6. Can be conducted in ambient condition
7. Low cost

In pulsed laser SEE testing, a pulse of focused laser traverses through a semiconductor material and induces localized generation of electron-hole pairs. These electron-hole pairs are generated due to the photoelectric effect and occur only when the incident photon energy is greater than the semiconductor's bandgap energy. The incident photon interacts with the outermost electron and if the energy absorbed is larger than the electron binding energy, the electron will gain enough energy to move from the valence band to the conduction band, leaving a hole behind in the valence band. Through this process, electron-hole pairs are generated.

The generation rate of the laser is largely affected by the lateral profile of the Gaussian laser beam and its incident energy. Neglecting second-order effects like non-linear absorption and wavefront curvature, the laser generation rate can be modelled by equation (6) [23]:

$$g_{las}(r, z, t) = \frac{2\alpha T E_L}{\pi^2 \omega_0^2 E_\gamma \tau_{las}} \frac{\omega_0^2}{\omega(z)^2} e^{-\frac{2r^2}{\omega(z)^2}} e^{-\alpha z} e^{-\frac{t^2}{\tau_{las}^2}} \quad (6)$$

$$\omega(z) = \omega_0 \sqrt{1 + \left(\frac{z}{z_{sc}}\right)^2} \quad (7)$$

where w_0 is the beam waist on the surface of the semiconductor material, z_{sc} is the laser confocal length, α is the linear absorption coefficient of the material, E_L is the incident laser energy, E_γ is the energy of a single photon and T is the energy transmission coefficient. The temporal profile, τ_{las} , of the laser beam is assumed to be Gaussian with 1 ps width. Extending from equation (6), Figure 2.13 illustrates the plot of carrier density generated when a pulse of laser traverses through a semiconductor material. As compared to Figure 2.8, the width of the charge track induced by a laser is indeed larger than that of an ion. Despite this difference, research results since the late 1980s have

shown that the laser is a valuable complementary tool to conventional heavy-ion radiation testing. Melinger and co-workers [94] have shown that the initial difference in charge tracks of heavy-ion and laser will be mitigated by the evolution of charge distribution and in an ultrafast time scale (< 10 ps), the charge distribution was found to be qualitatively similar.

Figure 2.13 Carrier density generated in silicon using a laser pulse of 8 pJ at 800 nm [23]

The SPA technique involves the focusing of laser beam on an area of semiconductor material and generating charges in a precise location (x, y) at a specific time. A single electron-hole pair is generated per photon and hence the nomenclature. In performing SPA, it is critical to work in the linear optical absorption regime where the laser intensity is sufficiently small to allow linear optics to accurately describe the light-material interaction. Optical absorption in the SPA technique is primarily governed by Beer Lambert's law, as shown in equation (8):

$$I(z) = I_0 \exp(-\alpha z) \quad (8)$$

where I_0 is the intensity of the incident laser beam, α is the linear absorption coefficient of the material and z is the penetration depth of the laser. Beer's law describes the exponential decrease in the electromagnetic radiation (light in this case) intensity as it propagates through an absorbing material. As the laser is highly tunable, extra precautions are needed to ensure that the appropriate parameters of interest are selected.

Parameters such as beam radius, wavelength, material absorption coefficient and surface reflections will directly affect the generation of charge density profile. Figure 2.14 illustrates the wide range of wavelength to be chosen for various substrate materials.

Figure 2.14 Absorption coefficient of various substrate materials at different wavelength [95]. 1064 nm laser wavelength yields a penetration depth of 676 μm in silicon devices.

As illustrated in Figure 2.14, the different choice of wavelength will affect the absorption coefficient and ultimately the penetration depth of the laser beam. This will affect the charge generation depth and the ability of the laser to probe transistors at different depths. For example, the use of laser wavelength at 590 nm yields a penetration depth of approximately 1.7 μm while 1064 nm laser wavelength will achieve a penetration depth of 676 μm for silicon devices [96]. In addition, as microelectronic devices advance to more complicated architectures, the number of metal layers on the front side of the devices increases. The presence of these metal layers poses a major limitation to the application of the laser in inducing radiation effects. In view of these limitations, several different techniques have been developed over the years. Backside SPA laser testing has been demonstrated by F. Darracq [97], D. Lewis [98] and co-workers via the use of laser to induce SEE in devices with multiple front-side metal layers.

More recently in 2002, D. McMorow and co-workers demonstrated a new laser-based technique in generating carriers via TPA [99-101]. Huge efforts have been devoted in the study of TPA by comparison against SPA [102, 103] and heavy ion [104, 105] in recent years. The TPA technique is an extension to the above-mentioned SPA technique. This extended technique utilizes a wavelength which is lower than the bandgap energy of the semiconductor material. TPA operates in the nonlinear optical absorption regime whereby optical absorption depends on the square of the laser intensity. Thus, under normal laser intensity, no electron-hole pairs will be generated. At sufficiently high intensity, the semiconductor material will be able to absorb two photons simultaneously and a single electron-hole pair will be generated. In this case, a single electron-hole pair is generated by two photons and hence the nomenclature. As the material is transparent to the wavelength at which TPA is usually conducted, carrier injection can be locally achieved at any depth, depending on the high-intensity focal region of the laser beam. This allows charge generation through the backside of the device and also subsequent 3D mapping of SEE sensitivity.

The advantages of pulsed laser SEE testing lies in its relatively simpler setup as compared to heavy ion particle accelerators. This is a lab bench equipment and thus, significant savings in land space can be attained. Through the precise positioning of the laser spot, irradiation can be targeted at specific structures and thus, this technique provides additional spatial information as compared to broad beam heavy ion test method. Through the synchronization of the pulsed laser trigger, the timing of laser irradiation can be controlled and thus, providing additional temporal information as compared to broad beam heavy ion test method.

Some limitations in existing pulsed laser SEE setups are related to the laser coverage of the entire device under test through movement of the stage. In order to obtain the SEE sensitivity assessment of the entire die area, existing pulsed laser SEE setups rely on the movement of the stage to complete the laser irradiation in a step-wise manner. This not only limits the stability of the system (due to mechanical movements of the stage) but also limits the speed of the result acquisition. These limitations in existing pulsed laser SEE test method form the basis of focus in the engineering need of this thesis and thus, aiming to provide improvements in this area.

2.4 PhD in Context of Literature

This PhD thesis is built around investigation of the limitations identified in section 2.2 and section 2.3. Section 2.3 highlighted the limitations of the current ‘gold’ standard of SEE testing via the broad beam heavy ion test method and reviewed various alternative (or complementary) test methods for suitability to efficiently conduct SEE evaluation on advanced microelectronic devices. In view of the recent industry’s move towards use of more COTS components, there is a need for other SEE test methods. Reviews of proton, neutron and ion microbeam concluded that such methods still required the use of particle accelerators and thus, requiring large area of land and startup capital. This is especially impractical in consideration of the land constraints faced in Singapore. Californium-252 offers a relatively compact and cheap solution but it also suffers from drawbacks such as limited range to penetrate advanced microelectronic devices and also requiring specific radiation licenses for the handling, storage and operation of the radioactive source. Eventually, pulsed laser SEE test method was reviewed and the combination of a lab bench equipment and ability to offer additional information (spatial and temporal) as compared to broad beam heavy ion test stood out. In context of existing literatures, this thesis contributes to the research community through the proposal of a laser scan methodology for efficient SEE evaluation on advanced microelectronic devices. This methodology will be realized in an industrial laser scanning microscope and will also be coupled with optical failure analysis techniques in order to provide more capabilities to functionally reverse-engineer COTS components. These features enable users to better understand the origin of SEEs in COTS components which are often ‘black boxes’ where users would have limited information on the physical layout and locations of functional blocks. The laser scan methodology also provides better stability, repeatability and higher throughput as compared to existing pulsed laser SEE setups which rely on stage movement.

Section 2.2 highlighted on the limitations of the current ‘gold’ standard of SEE testing via the broad beam heavy ion test method to study effects of ageing on SEE response. This was primarily due to the limited beam time in heavy ion test facilities and thus, effects of ageing are commonly investigated separately from radiation tests. Reviews of studies on cross-interactions involving TID were made and shown that impacts on TID sensitivity were significant. Also, literatures were relatively abundant and this is

most likely due to the easier access to TID test facilities and test slots, as compared to that of heavy ion particle accelerators. In view of the shrinking reliability margins and useful lifetime of advanced microelectronic devices, there is scientific interest in investigating the effects of ageing on SEE response. Reviews of studies investigating the influence of NBTI and TDDB on SEE had been made. However, conflicting results were obtained by several research groups. In context of existing literatures, this thesis contributes to the research community through the use of the proposed pulsed laser SEE scan methodology to study the effects of ageing on SEE response. Results showed that the proposed pulsed laser SEE scan methodology is a convenient and efficient method to conduct such studies. The evolution of the impact of ageing on SEE response can also be monitored over several time points of ageing stress.

In addition to the two contributions mentioned above, further studies will be carried out to evaluate the implementation of the proposed methodology. This will be demonstrated through investigations on two advantages and two concerns of the proposed methodology. Firstly, the methodology provides advantages in the assessment of the effects of device configuration on SEE response. In consideration of the increasing popularity of advanced field programmable gate array (FPGA) device which operates in multiple configurations, there is a need for alternate SEE test methods to study these effects. Another advantage will be demonstrated through the capability of the proposed pulsed laser scan methodology to localize SEE-sensitive structures and in combination with the optical failure analysis techniques of the system, to identify the root cause and apply mitigation techniques. This is especially important in gaining better understanding of COTS components which are commonly ‘black boxes’ to end-users. On the other hand, the proposed pulsed laser scan methodology is not without vulnerabilities too. Complications of test board configuration on the replication of SEE (as observed during previous heavy ion test) using the proposed pulsed laser scan methodology will be presented. Last but not least, complications of laser-induced damage in microelectronic devices fabricated with advanced technology nodes will be presented. This provides serious caution to the research community (both radiation and failure analysis) in the application of such technique on advanced microelectronic devices where new materials and architectures are frequently introduced and the invasiveness of the laser has to be considered. It also highlights the importance of

establishing a safe operating region to ensure that laser energies used during these tests do not induce undesired artifacts.

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Chapter 3

Experimental Methodology

Various experimental techniques were employed in this thesis and the principles and processes of these techniques are explained in this chapter. The chapter begins with an introduction to the general principles and procedures of the heavy ion broad beam test method and moves into the proposed pulsed laser SEE test method as a complementary tool. The pulsed laser SEE test method involves both scanning and point modes of operation, which are further described. Next, principles and procedures for characterization of laser parameters such as laser energy and spot size are elaborated. Sample preparation methods such as x-ray inspection, laser pre-decapsulation and selected area milling and polishing allowed the unimpeded penetration of the pulsed laser into the active volumes of the microelectronic samples. Electrical characterizations of several device parameters were carried out to monitor the device's degradation due to thermal or voltage stress. In addition, principles and processes of optical failure localization techniques are explained and utilization of these techniques enabled the analysis of possible laser-induced damages on devices fabricated with 65 nm CMOS process technology. Material analysis techniques such as focused ion beam, transmission electron microscopy and energy dispersive x-ray spectroscopy were employed to conduct physical failure analysis of these laser-induced damages.

3.1 Heavy Ion Broad Beam SEE Qualification

In this thesis work, heavy ion broad beam SEE qualification tests were conducted at the Texas A&M University (TAMU) radiation effects facility located in the United States of America (USA). As elaborated in section 2.1.2, heavy ion broad beam test technique is the current ‘gold’ standard for ground-level SEE qualification of space electronic components. The physics of ion-material interaction has also been deeply covered in section 2.1.2 and thus, in this section, the focus is to explain the process of using this test method. This technique is mostly based on the use of cyclotrons to accelerate ions to high energies in an outward spiral path. In such a setup, ions are held in orbit between the poles of superconducting magnets and the acceleration of the ions is achieved by high-speed alternating electric fields. Towards the end of the spiral path, deflection plates are placed to ‘attract’ the beamline away from its circular path and thus forming distinct beamlines for various applications. Figure 3.1 shows the cyclotron facility and beamline for radiation studies at TAMU.

Figure 3.1 (a) K500 Cyclotron at TAMU, USA [1] and (b) Beamline dedicated to studies of radiation effects in components.

At TAMU’s radiation effects facility, users will be able to choose a wide range of ions with various LET and penetration depths in order to suit their needs for radiation tests. LET is defined as the amount of energy transferred to the sample per unit length as an ionizing particle (e.g. heavy ion or proton) travels through a material. In the space radiation community, the common unit for this parameter is MeVcm^2/mg (after normalizing LET with the density of the material) as the particle’s energy transfer is

proportional to the density of the medium in which it travels in. At TAMU's radiation effects facility, the heavy ion beamline consists of a broad beam of ions impinging on the target uniformly over a circular cross sectional area of one-inch diameter. As the ions impinging on the sample is random and statistical in nature, the common parameter to define the number of particles in a unit area is fluence (units of particles/cm²) while the flux (units of particles/cm²-s) defines the fluence per unit time. Table 3.1 presents a selection of various ion species, LET (at normal incidence) and ion range provided at TAMU's radiation effects facility. If intermediate LET is desired, either the ion species or the angle of incidence can be changed.

Table 3.1 Representative selection of ion species, LET levels and range provided by the 15 MeV/u ion beam at TAMU, USA.

Ion Species	Initial LET in air (MeVcm ² /mg)	Range in Silicon (μm)
⁴ He	0.11	1423
²⁰ Ne	2.6	316
⁶³ Cu	18.7	172
⁸⁴ Kr	26.6	170
¹²⁹ Xe	49.3	156
¹⁴¹ Pr	56.0	154
¹⁹⁷ Au	82.8	155

Ions in TAMU's radiation effects facility are accelerated to higher energies and thus, the facility offers radiation tests in air as compared to the vacuum chambers offered by other radiation test facilities. This facilitates the ease of electrical set-up, use of larger samples/test boards and also reduce the time needed to depressurize the vacuum chamber. Ion requirements and generic test plan have to be communicated with the facility in order to allow sufficient time for the change of ion species during the test.

Prior to the start of the radiation test, the sample will be mounted on the test board and placed at the end of the beamline. The sample will then be centered and the tilt of the test board adjusted to be perpendicular to the beamline. Electrical cables will be connected between the test board and monitoring instruments such as power supply units, oscilloscope, function generators, etc. Long cables will be used to connect these instruments to the user control interface located in a separate room due to radiation safety protocols (which necessitates users to be isolated by thick concrete slabs from the radiation chamber during "beam on" time). In the case of TAMU's radiation effects

facility, users will move to the data room above the beamline room after the experiment has been fully set up. The sample will be powered up and verification will be done on all monitoring channels to make sure that the setup is ready to capture SEE during the irradiation window.

Irradiation will start when the users notify TAMU's radiation effects facility's staff that the experiment is ready for the beam. Users will also have access to the beam dosimetry data (such as the type of beamline, beam energy, ion fluence, ion flux and beam uniformity) and this allows them to control the duration of radiation exposure on the sample. As the broad beam of ions impinge on the sample, charges will be generated via Coulombic interactions. These charges will be swept by the electric field in the active region of the device and collected by the transistor terminals. This will generate a current transient which may lead to a SEE being captured by the monitoring setup. For each radiation exposure, SEE events will be monitored, counted and recorded. The radiation exposure will stop when the required fluence has been reached and the LET of the ion beam will be changed in order to commence the next round of radiation exposure.

3.2 Pulsed Laser SEE Test Technique

In this thesis work, pulsed laser SEE tests were conducted and an overview of the proposed pulsed laser SEE scanning microscope system (which had been set up at Nanyang Technological University or NTU) is shown in Figure 3.2. Briefly, the system consists of an InGaAs sensor in order to conduct backside imaging of the device's internal structures and allow navigation across the backside of the die. The system consists of three continuous wave laser sources of 1064 nm, 1319 nm and 1340 nm wavelength in order to conduct various optical failure analysis techniques on the device under test. An external pulsed laser of 1064 nm was integrated to the system in order to conduct SEE test or other fault injection techniques. Details of the setup and integration will be further covered in Chapter 4 but in this current section, the main purpose is to give an elaboration of the methodology of the pulsed laser SEE scan technique.

Figure 3.2 Overview of the proposed pulsed laser SEE scanning microscope system at NTU. System consists of InGaAs sensor, three continuous wave lasers to conduct various optical failure analysis techniques (OBIC¹, LIVA², OBIRCH³, TIVA⁴, LTP⁵) and a 1064 nm pulsed laser to conduct SEE tests. ¹ OBIC = Optical Beam Induced Current, ² LIVA = Light Induced Voltage Alteration, ³ OBIRCH = Optical Beam Induced Resistance Change, ⁴ TIVA = Thermal Induced Voltage Alteration, ⁵ LTP = Laser Timing Probe. PEM = Photon Emission Microscopy.

This system configuration allows the laser to be operated in scanning or point modes and the principles for these modes of operations are explained in the following sub-sections according to: (1) Scanning mode for SEE mapping and (2) Point mode for SEE waveform. In each sub-section, details of the laser SEE scan procedures and recording of SEE occurrences will be elaborated.

3.2.1 Scanning Mode – SEE Mapping

In this thesis, laser scanning mode was performed by both the DCG Meridian II system in Centre National d'Etudes Spatiales (CNES) and the Semicaps LTP1100 system in NTU. In the scanning operation mode of the pulsed laser SEE system, the pulsed laser is scanned across the sample surface via the coordinated functions of two precision-aligned galvo mirrors. The galvo motors rotate the mirrors (and thus deflecting the beam) through the precise control of current supplied to the galvo motors. A detector simultaneously reads back the positional information of the mirrors to the system and this ensures accurate and highly precise targeting of the laser beam on the device. The

currents and movements of the galvo mirrors are accurately controlled by the system while the user determines the area and resolution of scan. The resolution of the scanned image determines the pitch between two adjacent pixels. Figure 3.3 demonstrates the raster scan of the laser across the sample as the laser moves from one pixel to the subsequent ones until the end of the scan line. The galvo mirrors then snap the laser position back to the next line and continue moving from pixel to pixel, thereby generating a sawtooth wave pattern.

Figure 3.3 Simple schematic showing the raster scanning of laser across the sample surface according to the image resolution (in pixels) determined by the user.

During this raster scan across the sample surface, the device response is simultaneously fed through a preamplifier into the analog-to-digital converter of the system. The signal of this analog-to-digital converter forms an auxiliary channel where the intensities of the signals are simultaneously mapped according to the exact position of the laser scan. Any anomalies in the device voltage will be captured by the system and scaled accordingly in 8-bit (0 to 255) grayscale values. Figure 3.4 demonstrates the simultaneous scan of the laser image of the device shown in (a) and mapping of auxiliary channel shown in (b). In this case, the device (LM124) was biased with a static voltage and anomalies in the device voltage (as shown by white/black areas in Figure 3.4b) arise from the SET induced by the pulsed laser at sensitive transistors. An overlay of these images is shown in Figure 3.4c and allows the user to locate and identify SET-sensitive structures in the device.

Figure 3.4 (a) Laser scan image of device, (b) Simultaneous mapping of auxiliary channel which denotes anomalies in device response, and (c) Overlay of images (a) and (b) revealing SET-sensitive regions in the LM124 device used in this example.

3.2.2 Point Mode – SEE Waveform

Similarly, laser point mode was performed by both the DCG Meridian II system in CNES and the Semicaps LTP1100 system in NTU. The use of the galvo motors and mirrors allows the precise control over the position of the laser spot and this gives rise to another capability of the system: Point mode irradiation. First, the laser is scanned across the device surface in order to obtain a laser image of the device. This laser image reveals the structures of the device and allows easy navigation to the structures or transistors of interest. Once these structures of interest have been identified, the scan can be stopped and the laser image saved to the system. Subsequently, the point mode irradiation function can be activated by the user and the laser irradiation point will be denoted by a crosshair. The user can place this crosshair at any position within the previously obtained laser image. The laser spot will stay at the position of the crosshair and SEE can be repeatedly triggered. In a basic form of application, the SEE waveform can be obtained on an oscilloscope for deep analysis in future. In extension, this point mode is particularly useful in studying rare SEE occurrences and opens the door to studies involving clock synchronization or temporal manipulations.

Figure 3.5 shows a case where the laser system was operated in point mode with the laser positioned on a SEL-sensitive structure. The pulsed laser was configured to operate at 80 Hz while the device was protected by an anti-latchup module (to limit the current peak and avoid catastrophic failure of the device). It can be observed from

Figure 3.5 that the SEL can be repeatedly triggered at a stable frequency of 80 Hz (or time period of 12.5 ms) and the SEL waveform can be recorded for future analysis of its characteristics (rise time, amplitude, etc.).

Figure 3.5 80 Hz laser inducing "on-demand" SEL (i.e, high current state) in AD8629 device. Laser system was operated in point mode which allows repeated laser irradiation at any single position as determined by the user. As expected, the second laser pulse did not induce a SEL as the device was still in shut-down mode after SEL protection was activated.

3.3 Characterization of Laser Parameters

After integration of the external pulsed laser to the scanning microscope system, it is critical to fully characterize the capabilities of the system in terms of the laser energy being delivered to the device under test and also the laser spot size which defines the zone of energy deposition on the device. The methods used to characterize these two parameters are explained in the following sub-sections.

3.3.1 Energy Measurement – Detector Principles

Laser energy measurements were conducted using the Coherent J-10GE-LE energy sensor and Coherent LabMax-TOP energy meter. For laser energy measurement of a pulsed laser, two general approaches can be considered. The first approach is to use a power meter to measure the average power of a pulsed laser system and thereafter, using the repetition rate of the laser, derive at the pulsed laser energy. The second

approach (the preferred and employed approach in this thesis) is to use an energy meter to directly measure the per-pulse energy of the pulsed laser. In this approach, an energy sensor (J-10GE-LE from Coherent) was utilized to collect the laser pulses arriving at the sensor after the objective lens of the microscope system. This will give the reading of the actual energy arriving at the device under test. The sensor is based on a germanium photodiode with a 10 mm aperture. Due to the optical properties of germanium, the sensor is capable of detection in the spectral range from 800 to 1700 nm, which encompasses the 1064 nm wavelength of the target pulsed laser.

The operating principle of the photodiode follows that of a pn junction and in this case, photons with energy greater than the germanium bandgap is absorbed to produce electron-hole pairs in the space charge region. Figure 3.6 illustrates the energy band diagram of a pn junction under reverse bias condition. Under reverse bias, the electric field across the space charge region accelerates the electrons towards the n -region while the holes move towards the p -region. To improve the efficiency of the pn junction, $p-i-n$ photodiodes are commonly adopted. This includes an intrinsic region between the p and n regions, forming a high electric field region. This accelerates the separation and movement of the carriers, giving rise to efficient generation of photocurrent in the external circuit which is ultimately used to derive the energy of each laser pulse.

Figure 3.6 Energy band diagram of a pn junction operated under reverse bias voltage.

3.3.2 Spot Size Measurement – Knife-Edge Principles

Knife-edge measurements were conducted on a Coherent J-10GE-LE energy sensor which is connected to a Coherent LabMax-TOP energy meter. There are several methods, such as the use of a pin-hole [2], narrow slit scan [3], direct CMOS imaging [4] or translating knife edge [5], to determine the spot size of a laser beam. The knife edge (the preferred and employed approach) technique involves the use of a knife or razor blade to progressively chop the laser beam in a direction perpendicular to its propagation. The laser will be directed towards a photo detector (which will collect the light intensity being deposited onto the sensor) and its output will be monitored by an oscilloscope or power meter. Figure 3.7 shows an example of a laser set up for characterization of spot size via the knife-edge method.

Figure 3.7 Illustration of the knife edge methodology reproduced from [6]. The translating knife edge progressively chops across the laser beam and the light signal collected at the photo detector was used to construct the spot size profile of the laser.

With the knife edge initially blocking the entire laser spot and as the knife edge translates away from the center of the beam axis, a larger portion of the laser will be exposed and thus, the output signal of the photo detector will increase. Figure 3.8 illustrates an example of the results from a knife edge scan which starts with the knife fully blocking the laser and ultimately translating to a position which fully exposes the laser to the photo detector. Since the laser is a Gaussian beam, the measured response from the photo detector will follow a Gauss error function curve and subsequent

differentiation of this curve will give the Gaussian spot profile of the laser. The spot size can thus be determined from this Gaussian distribution.

Figure 3.8 Example of photo detector's response (left axis) following a Gauss error function curve (sigmoid 'S' shape) and the differentiated data (right axis) following a Gaussian distribution reproduced from [7].

3.4 Sample Preparation for Backside Optical Analysis

Prior to pulsed laser SEE tests, the microelectronic devices (often packaged in full molding compound) have to be exposed on the backside of the silicon die in order to avoid any obstruction of the laser beam through the front-side metal layers. The following sub-sections explain the various methods used to prepare the sample's backside surface to a state of mirror polish, rendering it suitable for pulsed laser backside SEE test.

3.4.1 X-ray Initial Inspection

In this thesis, x-ray inspection was conducted using the Shimadzu SMX-2000 Microfocus X-Ray Fluoroscopy system. Microelectronic devices can be packaged in metal can, hermetic ceramic or most commonly plastic molding compound. These compounds are opaque to the human eye and thus, x-ray imaging is used to conduct the

initial inspection of the device in order to locate the position of the silicon die. Figure 3.9 demonstrates the position of the x-ray source and detector in a typical x-ray imaging equipment.

Figure 3.9 Schematic showing the inverted column of the x-ray imaging equipment and positions of x-ray source and detector.

The x-ray imaging equipment is based on the operating principle of utilizing an x-ray source to radiate the sample while the detector collects the resultant transmitted x-rays. Either the stage or detector can offer the flexibility of imaging at various tilt angles in order to expand the range of view angles. The transmitted x-rays arriving on the detector will determine the contrast of the final image and thus, the x-ray absorption of different materials and layers within the sample will be crucial. In general, the lighter the atomic weight of the element, the less absorptive the material is. In the case of microelectronic devices, the plastic or ceramic packaging compound will be less absorptive and thus, allows more x-rays to transmit to the detector. Metal leads, grounding pads or copper paddles will be more absorptive and thus, appear darker in the x-ray image. Figure 3.10 shows an example of the ability of x-ray image to reveal the silicon die through an opaque package. Wire bonds which connect the metal leads to the silicon die can be easily seen. This helps the user to confidently identify the location of the silicon die and mark out the area of interest in subsequent laser pre-decapsulation step.

Figure 3.10 (a) Microelectronic device packaged in plastic molding compound and (b) x-ray imaging of the same device revealing the position of the silicon die of interest.

3.4.2 Laser Pre-Decapsulation

Laser pre-decapsulation [8, 9] was conducted using the Digit-Concept SESAME 1000 laser decapsulation system. Laser pre-decapsulation equipment was used to remove the molding compound on the backside of the device. Figure 3.11 shows the direction of laser pre-decapsulation through the backside of a device packaged in plastic molding compound. This technique operates based on the absorption of the laser wavelength in the target material. Commonly, a high power laser of 1064 nm will be utilized. As this wavelength is in the infrared spectrum, the epoxy (plastic molding compound) absorbs the laser energy which eventually causes the molding compound to vaporize. The laser is controlled with a scanning galvo head which enables the user to confine the ablation to a very localized area. This prevents damage to the metal leads which are ultimately needed for connection to the electrical test board.

Figure 3.11 Typical silicon die packaged in dual-in-line plastic molding compound with indication of direction of laser decapsulation through the backside of the device.

The pre-decapsulation process starts by placing the device on the stage and then superimposing the x-ray image over the physical device in order to accurately determine the position of the die. The intended ablation area is marked out around the die and copper paddle. Laser power is selected and the ablation process starts with layer-by-layer removal of the molding compound. The ablation process stops when the copper paddle at the backside of the device is exposed.

3.4.3 Selected Area Milling and Polishing

After decapsulation, selected area milling was conducted using the Ultratec ASAP-1 IPS system. Selected area milling was utilized to remove the copper paddle, thin and polish the remaining silicon substrate on the backside of the die. This technique involves the use of basic milling movement of the tool to mechanically remove material. However, particularly important for preparation on a silicon die, this equipment is empowered by a force feedback mechanism in order to limit the amount of force or pressure being asserted on the silicon die during the entire process. This prevents the undesired cracking of the silicon die during the milling process. Figure 3.12 shows the Ultratec ASAP-1 IPS system at NTU with the sample mounted on the tilt-stage and milling tool floating above the sample.

Figure 3.12 Ultratec ASAP-1 IPS system at NTU to carry out selected area milling and polishing.

After the removal of the copper paddle, either polishing or thinning (depending on remaining silicon thickness) of the silicon substrate will be conducted. This is to ensure that the silicon substrate is thin and smooth enough for the 1064 nm pulsed laser to penetrate. This usually demands a polished mirror surface on the backside of the die and is accomplished by various steps of thinning and polishing using the same equipment. Figure 3.13 illustrates these steps which involve: (1) Substrate thinning, (2) Rough polishing, (3) Moderate polishing and (4) Fine polishing. Each step is accomplished by specific thinning/polishing tools and polishing slurry of different particle sizes.

Figure 3.13 Schematic of die substrate thickness, indicating various steps involved in polishing and its corresponding reduction in die thickness (extent of which can be controlled by polishing parameters).

Ultimately, the backside of the die must be mirror finished in order to avoid unwanted diffraction of the pulsed laser during SEE tests. Figure 3.14 illustrates the sample's surface finish after various steps of the polishing process. It is evident that each polishing step improves the die's surface condition and ultimately, the entire integrated circuit can be clearly seen through the backside of the die.

Figure 3.14 IR micrographs of backside surface finish of LM124 sample after (a) Step 2 Rough Polishing, (b) Step 3 Moderate Polishing and (c) Step 4 Fine Polishing.

3.4.4 IR Microscope Verification

In this thesis, infrared (IR) microscopy was conducted using the Olympus BX51M microscope equipped with IR objective lenses of 5X, 20X and 50X. In order to verify that the sample is suitable for pulsed laser SEE test, the backside surface of the die is not only visually inspected for mirror surface finishing but also inspected under the IR microscope. This technique relies on the transparency of silicon in the near-infrared spectrum. Various IR objective lenses are equipped to enable users to view samples under different magnification. Also, these lenses are coupled with an adjustment ring to conduct silicon-thickness corrections. Figure 3.15 shows the IR micrograph of a device (LM124) imaged under 5X and 20X objective lenses. As the surface was well polished, defects or scratch lines were not impeding the IR transmission and thus, the integrated circuit can be clearly seen through the silicon substrate.

Figure 3.15 IR micrograph of (a) Entire die of LM124 under 5X objective lens and (b) Zoom-2in view on one of the amplifier in LM124 under 20X objective lens.

3.5 Electrical Characterization

Electrical characterizations were conducted on the LM124 operational amplifier, chain of flip flops and chain of inverters. This was to monitor the shift in electrical parameters after various hours of ageing. Characterization procedures of these parameters will be explained in the following sub-sections.

3.5.1 Frequency

The frequency or bandwidth of the device was determined using a Tektronix DPO4054 4-channel 500 MHz oscilloscope. The frequency of the device gives an indication on the overall response speed of the internal structures or transistors. Degradation of this response speed can have an impact on the duration of SET and thus, affect the radiation sensitivity of the device after ageing. Figure 3.16 shows the circuit diagram of the setup used for the characterization of the device's bandwidth/frequency response.

Figure 3.16 Electrical circuit diagram of the setup used during characterization of the device's bandwidth.

The operational amplifier was connected in an inverting configuration with a gain of 100. Power supply of ± 15 V and an input sine wave signal of 100 mV (peak-to-peak) at 500 Hz was supplied to the device. As the bandwidth of an operational amplifier is defined as the frequency range where the amplifier's voltage gain is above -3 dB, the input frequency was progressively increased until the output voltage is 70.7% of its original value. This new input frequency was thus specified as the bandwidth of the device.

3.5.2 Power Supply Current

The power supply current of the device was measured using a Hewlett Packard 3457A bench digital multi-meter. The power supply current gives an indication on the degradation of the device upon ageing and can potentially have an impact on the radiation sensitivity of the device. The operational amplifier was connected in an inverting configuration of gain 100 according to Figure 3.16. Power supply of ± 15 V

and an input sine wave signal of 100 mV (peak-to-peak) at 500 Hz was supplied to the device. The power supply current was determined via the Hewlett Packard 3457A bench digital multi-meter with a Number of Power Line Cycles setting of 10, in order to reduce unwanted noise from the power lines.

3.5.3 Voltage Transfer Curve

The voltage transfer curve (VTC) was obtained using a Keithley 4200 parameter analyzer and Keithley 2612b source-measure meter. The VTC was characterized for the sample consisting of single or chain of inverters fabricated with 65 nm CMOS process technology. VTC gives the output response of the inverter as a function of its input voltage. A shift in the VTC after ageing gives an indication of a shift in the threshold voltage of the inverter. This may potentially have an impact on the radiation response of the device. When a low voltage is supplied to the input of an inverter, the PMOS will be turned on and thus, resulting in a high output voltage. Conversely, a high input voltage to an inverter will cause the NMOS to be turned on and thus, resulting in a low output voltage. Figure 3.17 shows an example of the VTC obtained from a single inverter which was biased with a power supply of 1.2 V. During the characterization, the power supply voltage was held constant while the input voltage was progressively increased from 0.45 V to 0.70 V. Simultaneously, the output voltage of the inverter was monitored and this gave rise to the VTC as observed.

Figure 3.17 Voltage transfer curve of a single inverter fabricated with 65 nm CMOS process technology and biased with power supply of 1.2 V.

3.5.4 I_{DD} - V_{IN}

In this thesis, the I_{DD} - V_{IN} curve was obtained using a Keithley 4200 parameter analyzer and Keithley 2612b source-measure meter. The I_{DD} versus V_{IN} curve was characterized for the sample consisting of single or chain of inverters fabricated with 65 nm CMOS process technology. This curve gives an indication of the short circuit current when the inverter is switching from one state to another and also the input voltage where this transition takes place. During the characterization, a constant power supply voltage was supplied to the device while the V_{IN} was progressively increased. The I_{DD} was simultaneously monitored and this gave rise to the curve as observed in Figure 3.18.

Figure 3.18 I_{DD} against V_{IN} curve of a single inverter fabricated with 65 nm CMOS process technology and biased with power supply of 1.2 V.

3.6 Optical Fault Localization Techniques

Optical fault localization techniques are commonly employed as non-destructive methods to analyze and locate damaged regions in integrated circuits before further destructive physical failure analysis can be conducted. The sample has to be de-capsulated while maintaining the full functionality of the device. In this work, mainly three different techniques have been employed and will be explained in the following sub-sections.

3.6.1 Laser Frequency Mapping

In this thesis, laser frequency mapping (also known as electro-optical frequency mapping or laser voltage imaging) was performed by both the Hamamatsu TriPHEMOS system in CNES and also the Semicaps LTP1100 system in NTU. Laser frequency mapping is based on the analysis of the reflected light signal which has been modulated by the device after an optical injection by a laser. Figure 3.19 presents the schematic of an optical setup for this technique.

Figure 3.19 Schematic of the laser frequency mapping configuration [10] in which a laser source injects an incident beam to the device and gets modulated by the device. The reflected light signal is collected by a photon detector and final analysis is conducted by a spectrum analyzer or oscilloscope.

Firstly, a square wave signal of a user-defined frequency is supplied to the device using a function generator. This will cause the modulation of free carriers in the active regions of the device. Next, the laser source will inject an optical pulse towards the device and as it reflects off the transistors, the intensity of the reflected light signal depends on the refractive index of the silicon (which in turn depends on the change in free carrier

concentration). Free carrier concentration in a junction varies according to the voltage across it and thus, the reflected light signal will be ultimately dependent on the modulation of the voltage signal imposed by the function generator. The modulation of the reflected light signal will be approximately synchronized with the square wave frequency of the device's input and thus, after the collection and Fourier transform of the reflected light signal by a spectrum analyzer, the resultant frequency of the reflected signal will be close to that of the input frequency. This allows the monitoring of the structures in the integrated circuits which are involved in the switching at the input frequency.

3.6.2 Laser Frequency Probing

In this study, laser frequency probing (also known as electro-optical probing or laser voltage probing) was performed by both the Hamamatsu TriPHEMOS system in CNES and also the Semicaps LTP1100 system in NTU. Laser frequency probing relies on the same principles as that described in section 3.6.1. The difference lies in the analysis of the reflected light signal. In the probing mode, the reflected light signal is analyzed by the oscilloscope which allows the visualization of the waveform of the reflected light signal.

3.6.3 Photon Emission Microscopy (PEM)

Similarly, PEM was performed by both the Hamamatsu TriPHEMOS system in CNES and also the Semicaps LTP1100 system in NTU. Photons are emitted due to the radiative emission of electromagnetic waves from the transition of carriers from a state of higher energy to one of lower energy. In the case of microelectronics failure analysis, this process is usually initiated by electrical bias and thus, the process is in fact electroluminescence. These radiative transitions can be broadly categorized into three groups: (1) Interband transitions, (2) Impurities, defects, traps transitions and (3) Intraband transitions. Figure 3.20 shows the configuration of a typical PEM with the detector at the end of the optical column to collect the emitted photons.

Figure 3.20 Schematic of a typical photon emission microscope [11]

The process of photon emission studies starts with the image acquisition of the layout of the device, usually with a IR camera such as an InGaAs detector. In the imaging mode, an illumination light source is turned on and the reflected image of the sample is taken at focus. Next, the light source is turned off and the background emission is taken without any electrical bias to the device. Lastly, electrical bias is supplied to the sample and the actual emission is integrated over a user-defined period of time. The background emission is subtracted from this integrated emission image and subsequently superimposed onto the reflected image of the device layout to reveal the emission sites in the integrated circuit.

3.7 Material Analysis

Material analysis was mainly conducted on the sample consisting of 65 nm CMOS chain of inverters. The intention was to conduct physical failure analysis on the suspected laser-induced damages on the chain of inverters. A combination of FIB, TEM and EDS was utilized and will be explained in the following sub-sections.

3.7.1 Focused Ion Beam (FIB)

FIB was conducted using the FEI Nova NanoLab 600 DualBeam (FIB/SEM) system. This technique is based on the use of highly accelerated ions directed at the sample in order to cause physical sputtering of the target material. The sputtering process is

caused by the momentum transfer (elastic collision) between the impinging ions and the atoms in the target material. If the target atom receives sufficient kinetic energy from the impinging ion to overcome its surface binding energy, the surface atom will be ejected from the material and thus achieving the goal of material milling in the nanoscale. Figure 3.21 shows a typical ion beam column of a FIB system.

Figure 3.21 Schematic of a typical ion beam column with liquid metal ion source at the top, followed by lenses for focusing, beam blanking and deflection octopole [12].

The ion beam is first generated by the liquid metal ion source of gallium which consists of a tungsten needle attached to a reservoir of gallium material. The heated gallium wets the tungsten tip and an electric field applied to the tip causes the molten gallium to form a point source of very small diameter (typically in the order of 2-5 nm) with a Taylor cone shape. Next, the potential difference between the tip and the extractor electrodes forces the extraction of the gallium ions by ionization through the field evaporation process. The extracted gallium ions are then accelerated down the ion column by potential difference controlled by the accelerating voltage. A series of lenses then focuses the beam of gallium ions at the sample surface. A series of fine tuning through the centering of apertures, adjustments to lenses, use of stigmators are employed to optimize the beam shape. Also, when the beam is not needed, it can be deflected by the use of beam blankers in order to avoid unnecessary degradation to the sample surface.

3.7.2 Scanning Electron Microscopy (SEM)

SEM was also carried out using the FEI Nova NanoLab 600 DualBeam (FIB/SEM) system. SEM is based on the use of highly accelerated electrons focused at the sample surface in order to induce electron-sample interactions. These interactions generate a wide variety of signals but most commonly, it allows the imaging of the sample surface via the detection of the generated secondary electrons. Imaging details like the topography and morphology of the sample surface can be revealed at high resolution with this technique. Figure 3.22(a) shows the dual beam configuration consisting of both an ion column for FIB application and electron column for SEM application in a typical dual beam FIB system. The two beams are positioned at an angular offset in order to allow simultaneous milling by the ion beam and imaging by the electron beam.

Figure 3.22 (a) Schematic of a dual beam FIB system where the electron and ion columns are at an angular offset to allow simultaneous milling via ion beam and imaging via electron beam [12] and (b) Schematic of a typical scanning electron microscope showing the electron gun as the source, condenser lenses for focusing, scan coils for beam deflection, specimen stage and detector [13].

The electron beam is generated at the top of the electron column as shown in Figure 3.22(b). Several methods for generation of electrons exist and the one employed in the FEI Nova NanoLab 600 DualBeam (FIB/SEM) system is via the field emission gun method. In this scheme, an emitter, made up of a single crystal of tungsten welded to a thin wire of tungsten, acts as the source of electron. A voltage is applied to the extractor

electrode to induce an electric field which causes the tunneling effect necessary to generate electrons. Another voltage applied to the accelerating electrode further extracts the electrons into a continuous beam which is subsequently focused by the condenser lens, and deflected by the scan coils for rastering motion of the beam on the sample surface.

When the highly accelerated electrons impinge on the sample surface, secondary electrons from the k shell of the sample's atoms can be generated by inelastic scattering. The energies of these secondary electrons are generally low (typically 50 eV or less) and thus, the secondary electrons available for collection/analysis is mainly from the surface of the sample. The ejected secondary electrons are subsequently collected by a detector which is commonly based on the scintillator design. The scintillator converts the electrons to light, which then passes through a photomultiplier tube to generate outputs in the form of electrical signals. These electrical signals are subsequently passed to an analog-to-digital converter to display the constructed image in two-dimensional grayscale values.

3.7.3 Transmission Electron Microscopy (TEM) and Energy Dispersive X-ray Spectroscopy (EDS)

TEM was carried out using the JEOL JEM-2100F-UHR system. TEM is based on the use of highly accelerated electrons directed at very thin sample (typically < 100 nm) in order to induce electron-sample interactions such as scattering or penetration. After a series of lenses, these electrons will eventually arrive on a surface (fluorescent screen, film or CCD) where users can view the resultant image of the analysis. The intensity of electrons exiting the sample and finally arriving on the surface depends on the absorption and scattering properties of the material. Figure 3.23(a) shows the schematic of a typical TEM column which consists of three broad groups of components: (1) Illumination sub-system, (2) Objective lens with stage and (3) Imaging sub-system. The illumination sub-system is involved in the generation of the electron beam and thus, is positioned at the top of the TEM column. As shown in Figure 3.23(b), it consists of the electron gun, accelerating tube and condenser lens which in combination, generate either a parallel or convergent electron beam. The parallel beam is commonly used during imaging mode while the convergent beam is used during the EDS mode.

The objective lens and stage assembly acts as a chamber for the specimen and the objective lens collects the information (image or diffraction pattern) from the electron-sample interactions. Thus, this is also the most important lens in the TEM column as it is the primary lens which determines the fundamental quality of the TEM results. The imaging sub-system is involved in the magnification of the information collected after the objective lens and functions through several lenses (intermediate and projection lens in Figure 3.23(b)) to finally focus this information on a viewing screen or camera assembly.

Figure 3.23 (a) Schematic of TEM column [14] and (b) Ray diagram showing imaging and diffraction mode of typical TEM [15]

In addition to the electrons which penetrate or are scattered by the material, the high-energy electron beam also generate x-rays due to electron-sample interaction. These x-rays are characteristic of the element due to specific energy levels in the inner-shell of the atom. An EDS detector (commonly based on silicon or germanium) is fitted into the TEM column in order to collect these characteristically emitted x-rays. The x-rays arriving at the EDS detector generates electron-hole pairs with its intensity proportional to the x-ray quantum energy. The application of a reverse bias on the EDS detector accelerates the separation of electron-hole pairs and results in a voltage pulse which is

processed by an analog-to-digital converter before being sorted and stored in a multichannel analyzer. The multichannel analyzer counts the number of pulses at each x-ray quantum energy and displays the results as a spectrum with photon energy at the x-axis and number of photons at the y-axis. Since the TEM is operated with a convergent beam during the EDS mode, an elemental mapping of the surface can be achieved through scanning of the beam spot across the sample surface.

3.8 Simulation

Simulation of radiation effects is commonly conducted on several levels of integration such as particle-matter interaction, device physical modelling, electrical circuit modelling or mixed-mode simulations. In electrical circuit modelling, several models have been proposed to describe the transient current induced by radiation sources. Douin and co-workers [16] proposed a laser-induced electrical current model based on two stages of charge collection. More importantly, the transient current in the model follows a double exponential pulse shape, which is typically used in the radiation research community. Alternatively, Champeix and co-workers [17] proposed an electrical model based on a current source which is parallel with a test structure (*pn* junction) in order to model the transient current induced by a laser.

In this thesis, electrical circuit simulation was conducted in the Cadence Spectre Circuit Simulator environment and a double exponential pulse shape was adopted for the modelling of the transient current. This was conducted on a chain of flip flops fabricated with 65 nm CMOS process technology in order to understand the influence of a change in threshold voltage of the device on its radiation sensitivity. The simulator is based on SPICE level simulation which does not take into account 3-dimensional properties of the simulated device architecture. In this way, the total simulation duration can be more efficient in order to give a quick indication of the trends resulting from a change in device parameters. Also, the use of SPICE simulation is closer to the real-life application situation where most users have no access to the details of the 3-dimensional fabrication process (heavily guarded by the semiconductor foundries in terms of trade secrets or intellectual properties). In place of the 3-dimensional properties of the device architecture, a set of device electrical parameters are included to describe the response of the device. In this study, there is access to the electrical circuit layout and process

design kit of the chain of flip flops fabricated with 65 nm CMOS process technology and thus, this knowledge was used to define the electrical response of the device in the simulator.

As the single inverter is the fundamental building block of a flip flop, this was the targeted test subject during the simulation. The inverter was supplied with power supply and input voltages which were similar to the conditions used during the pulsed laser SEU tests. During the experiment, the flip flop was stressed by higher operating voltage to monitor the change in radiation sensitivity as a function of voltage stress duration and thus, in the Cadence Spectre environment, this was simulated by a change in threshold voltage of the PMOS transistor (which has been a dominant reliability concern in recent semiconductor technology nodes). The threshold voltage of the PMOS was progressively shifted and the power supply current and SEU threshold energy were simultaneously monitored. The SEU threshold energy was simulated by the injection of laser pulses which was in turn represented by an electrical model describing the transient current originating from the photocurrent generation of electron-hole pairs in the semiconductor upon laser irradiation. This electrical model is characterized by a double exponential current source injected at the drain of the most sensitive transistor where the minimum energy needed to cause a SEU was monitored to give an indication of the shift in SEU sensitivity as a function of the shift in PMOS's threshold voltage.

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Chapter 4 *

Development of Pulsed Laser SEE Scanning Microscope System

In addressing the engineering needs identified in section 1.2, this chapter presents the results for the set-up and subsequent validation of the proposed pulsed laser scanning microscope system to induce SEE in microelectronic devices. In contrast to existing conventional radiation test method, this proposed pulsed laser SEE scanning microscope system aims not only to be more efficient, but also to provide additional information (both spatially and temporally) on the induced SEE. Ultimately, these advantages target to offer a radiation test methodology in land-scarce Singapore, in order to reduce the satellite design feedback loop time and also to provide satellite engineers with more information on SEE to facilitate analysis of complex advanced microelectronics. In this chapter, details of the setting up of the proposed pulsed laser scanning microscope system are explained via reporting on the choice of laser source configuration, laser delivery fibers and connectors. Characterization results of laser parameters (like pulsed laser energy and laser spot size) are also presented. To validate this setup, further benchmarking of pulsed laser SEE test results were conducted on two devices of dissimilar technology processes/architectures and results are reported in this chapter.

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4.1 Introduction and Motivation

Currently in land-scarce Singapore, there is no available radiation test facility for qualification of space microelectronic components. As a result, the current practice is to send teams of satellite engineers to overseas radiation test facility in order to conduct the necessary qualification tests. The motivation of this thesis is thus to first set up an alternative method in Singapore to conduct SEE tests on microelectronic components.

Survey on limitations of existing methods

In order to achieve this target, a review (presented in section 2.3) on existing methods were conducted and the pulsed laser methodology is deemed to be the most suitable in Singapore's context due to its compact footprint while at the same time, avoid any public concerns on particle radiation safety. However, this pulsed laser methodology is not without its own inadequacies. Current existing pulsed laser SEE setups across the globe are custom systems built on optical bench which generally consists of a pulsed laser source, mirrors, objective lenses and movable x-y-z sample stage. The pulsed laser source is fixed on the optical bench to prevent positional shifts while the movement of the x-y sample stage allows irradiation of the pulsed laser at various positions of the sample. The movement of x-y sample stage can impose limitations via: (1) The mechanical speed of movement thereby limiting efficiency, and (2) The mechanical stability or repeatability of the movement thereby limiting positional accuracy in advanced microelectronics with very small and dense structures. Although these setups allow a lot of freedom for customization and flexibility, it requires an experienced and trained user a few hours to fully align the laser optical path and validate the exact energy output at the sample position before commencement of the actual testing. In overall, this limits the efficiency and operational availability of the system, even to trained but inexperienced users.

Survey on proposed methodology: Pulsed laser SEE scanning microscope system

In view of the above-mentioned inadequacies to meet this thesis's motivation/target of setting up a methodology to provide efficient, easy-to-use, additional SEE information and capabilities to test on advanced microelectronics, efforts were devoted to look into other scientific domains for solutions. Ultimately, efforts were focused in the microelectronic failure analysis domain where scanning microscope systems are

utilized to analyze microelectronic devices fabricated with the most advanced technology nodes. The proposed laser scan methodology potentially improves the limitations imposed by the x-y stage movement, thereby improving both efficiency and positional accuracy. Also, the proposed integration of the pulsed laser source to the system via an optical fiber avoids the time spent on alignment of the laser optical path, thereby improving operational availability and ease-of-use. Details of the setup, pulsed laser energy measurement, pulsed laser spot size measurement and benchmarking results will be elaborated in the following sections.

4.2 Experimental Details

The experimental details section is divided into three sub-sections reporting on: (1) Characterization procedure of pulsed laser energy, (2) Characterization procedure of pulsed laser spot size, and (3) Device descriptions of LM124 and LMC6484 for benchmarking tests.

4.2.1 Characterization of Pulsed Laser Energy

The pulsed laser energy was measured using the Coherent J10-GE detector with its principles already explained in section 3.3.1. With the pulsed laser operating in the laser-scanning irradiation mode, imaging was first performed on the energy sensor using the 5X objective lens in order to find the z position of the optimum focus at the X-Y center location of the sensor. Irradiation at the center of the sensor is important in order to fully maximize the sensor area and thus, offsetting potential beam energy losses due to any defocusing effects which will enlarge the laser spot size at the device under test (DUT).

The pulsed laser was then operated in the single-point irradiation mode to conduct the actual energy measurement of the pulsed laser. Laser pulse repetition rate, sensor measurement range and energy trigger level were modified to obtain the most accurate measurement. These conditions were recorded and kept constant (for subsequent measurements across different days). Laser energy was progressively increased by modifying the preamp current of the pulsed laser source. For each preamp current, 60 measured laser energy values were taken and the average of these values were recorded.

The standard deviation of these values were also recorded to monitor the spread and validity of data points. The preamp current was later increased from 1.6 A to a maximum of 6 A in order to obtain the full range of energy measurement for the pulsed laser source. This procedure was then repeated for the 20X and 50X objective lenses.

In extension of the pulsed laser energy measurement experiments, the same procedures were repeated on a total of eight different days (across a period of 8 months) in order to monitor the longer-term energy stability of the system.

4.2.2 Characterization of Pulsed Laser Spot Size

The pulsed laser spot size was determined through the differentiation and Gaussian fitting of laser energy measurements obtained using the Coherent J10-GE detector at various z focal positions. A knife edge was inserted between the objective lens and the detector, as according to the knife-edge methodology which was explained in section 3.3.2. With the pulsed laser operating in the laser-scanning irradiation mode, imaging was first performed on the knife edge using the 5X objective lens in order to find the z position of the optimum focus and to align the knife edge at the center of the field of view.

The pulsed laser was then operated in the single-point irradiation mode to conduct the actual energy measurement of the unblocked portion of the pulsed laser. Laser pulse repetition rate was kept at 5 Hz, the laser source's preamp current at 3.8 A and scan image resolution at a maximum of 2048 pixels. As shown in Figure 4.1, the knife edge and detector were both stationary, with the laser spot being first placed on the surface of the knife. In this initial position, the laser was entirely blocked by the knife and thus, the laser energy measured by the sensor was zero. The movement of the laser spot was subsequently achieved through the pixel-to-pixel scan of the microscope system and thus, increasing portion of the laser spot falls onto the sensor and results in larger values of measured laser energy.

Figure 4.1 Plan and side views of the experimental setup used for the characterization of laser spot size

The line scan across the knife edge yields a sigmoid ‘S’ curve of laser energy measurement, as expected from the Gaussian distribution of a laser spot. Differentiation and Gaussian fitting were conducted on the laser energy measurements in order to obtain the value for the laser spot size. This procedure was repeated for various z positions in order to determine the minimum spot size for the 5X objective lens. This procedure was then repeated for the 20X and 50X objective lenses.

4.2.3 Device Descriptions of LM124 and LMC6484 for Benchmarking

LM124:

The LM124 is a bipolar analog device consisting of four identical and independent operational amplifiers assembled in a single dual-in-line plastic package. Figure 4.2 illustrates the representative cross section schematic of a device fabricated with the bipolar process technology.

Figure 4.2 Cross section schematic representative of a device (p^+np) fabricated with the bipolar process technology [1]

For benchmarking purposes, this device was chosen as it is one of the most widely tested device by other research groups over the world. Thus, there are many available literatures [2-5] and data on this device for comparisons and benchmarking purposes. There is also a wide base of knowledge on the device topology, circuit elements and its corresponding response to SET.

For the benchmarking test on LM124, the proposed pulsed laser SEE scanning microscope system was utilized to assess the SET response of the device and comparisons were made with previous heavy ion test results reported in literature [2]. Figure 4.3(a) shows the four identical and independent operational amplifiers packaged in LM124 while Figure 4.3(b) shows the amplifier operating in the voltage follower configuration with corresponding biases during the benchmarking test.

Figure 4.3 (a) Four identical and independent operational amplifiers in a single LM124 device and (b) Voltage follower mode and bias conditions during benchmarking test

As shown in Figure 4.3(b), the amplifier was configured as a voltage follower with power supply voltages of ± 15 V and input voltage of 1 V. The output of the amplifier was connected to an oscilloscope to capture any SET induced by the laser pulse. In the first part of this experiment, the pulsed laser was first scanned across the sample surface in order to locate all the SET-sensitive transistors. In the second part of this experiment, the pulsed laser was operated in the single-point irradiation mode at specific sensitive transistors and the pulsed laser energy was progressively increased to induce SETs of higher amplitude and longer duration. The pulsed laser energy was increased to a point where the SET amplitude matches that obtained from heavy ion test in literatures (i.e.,

the benchmark reference). This SET waveform was recorded and its pulse duration/shape/polarity was finally compared with the previous data from literature.

LMC6484:

The LMC6484 is a CMOS analog device consisting of four identical and independent operational amplifiers assembled in a single dual-in-line plastic package. Figure 4.4 illustrates the representative cross section schematic of a device fabricated in the CMOS technological process.

Figure 4.4 Cross section schematic representative of a device (NMOS) fabricated in the CMOS technological process

For benchmarking purposes, this device was chosen as there are available pulsed laser test data in the literatures. More importantly, it provides similar functionality as the above-mentioned LM124 but the interest is that it is fabricated in more recent CMOS process technology. In extension of the previous benchmarking test, validity of this approach can be demonstrated in more recent process technology.

For the benchmarking test on LMC6484, the proposed pulsed laser SEE scanning microscope system was utilized to assess the SET response of the device and comparisons were made with previous pulsed laser test results reported in literature [6]. Figure 4.5(a) shows the four identical and independent operational amplifiers packaged in LMC6484 while Figure 4.5(b) shows the amplifier operating in the voltage follower configuration with corresponding biases during the benchmarking test.

Figure 4.5 (a) Four identical and independent operational amplifiers in a single LMC6484 device and (b) Voltage follower mode and bias conditions during benchmarking test

As shown in Figure 4.5(b), the amplifier was configured as a voltage follower with power supply voltage of 10 V and input voltage of 8 V. The output of the amplifier was connected to an oscilloscope to capture any SET induced by the laser pulse. In the first part of this experiment, the pulsed laser was first scanned across the sample surface in order to locate all the SET-sensitive transistors. In the second part of this experiment, the pulsed laser was operated in the single-point irradiation mode at specific sensitive transistors and the pulsed laser energy was progressively increased to induce SET of higher amplitude and longer duration. This generates a family of SET waveforms which was recorded and finally compared with the previous pulsed laser data from literature.

4.3 Results and Discussions

With the experimental details section of this chapter covered, the results and discussions section will be presented next. This will be reported in six sub-sections covering: (1) Set up of scanning microscope system, (2) Choice of laser source and optical components, (3) Pulsed laser energy characterization, (4) Pulsed laser spot size characterization, (5) Benchmarking via LM124 and (6) Benchmarking via LMC6484.

4.3.1 Set Up of Pulsed Laser SEE Scanning Microscope System

Figure 4.6 shows the overview schematic of the proposed pulsed laser SEE scanning microscope system while Figure 4.7 shows the actual system (with laser safety enclosure) located at the Microelectronic Failure Analysis Laboratory 2, NTU. This entire setup was realized in collaboration with a local university's spin-off company, Semicaps Pte Ltd. The system consists of two laser ports to handle laser sources at two different input positions with its respective optical paths. Next, the laser passes to the laser scanner and is then focused by the objective lens to finally arrive at the DUT itself.

Figure 4.6 Overview schematic of proposed pulsed laser SEE scanning microscope system showing capabilities to handle laser scanning from two laser sources

Figure 4.7 Proposed pulsed laser SEE scanning microscope system located at Microelectronic Failure Analysis Laboratory 2, NTU

To empower the capability of inducing SEE in silicon-based microelectronic devices, a specific pulsed laser (1064 nm, 10 ps) was installed on the position of “Laser Source 1” in Figure 4.6. This pulsed laser is delivered via a laser delivery fiber and connector to the system’s collimator lens, where it later passes to the laser scanner, is subsequently focused by the objective lens and arrives ultimately at the DUT. This pulsed laser source is capable of delivering laser energies up to 11 nJ (measured at source) at repetition rates of single shot to 50 MHz. Table 4.1 shows the details of the objective lenses available in the current setup.

Table 4.1 Details of all the objective lenses installed on the current scanning microscope system

Objective Lens	Numerical Aperture	Observed resolution with 1064 nm laser (μm)
1X	0.40	-
5X	0.16	-
20X	0.40	-
50X	0.40	1.00
RSIL*	3.00	0.12

*RSIL stands for Refractive Solid Immersion Lens

In addition to the pulsed laser source, there are three other laser sources installed in the system in order to conduct optical failure analysis techniques via a single platform. The details of these other laser sources with their associated optical techniques (some of which will be utilized in subsequent chapters of this thesis) are elaborated in Table 4.2.

Table 4.2 Details of three other laser sources (in addition to pulsed laser) installed on the current scanning microscope system

Laser Wavelength (nm)	Lasing Type	Possible techniques
1064	Continuous wave	OBIC ¹ , LIVA ²
1340	Continuous wave	OBIRCH ³ , TIVA ⁴
1319	Continuous wave	LTP ⁵

¹OBIC = Optical Beam Induced Current, ²LIVA = Light Induced Voltage Alteration, ³OBIRCH = Optical Beam Induced Resistance Change, ⁴TIVA = Thermal Induced Voltage Alteration, ⁵LTP = Laser Timing Probe

For imaging purposes, the system is equipped with a charge-coupled device (CCD) and InGaAs camera in order to perform both optical and through-silicon imaging respectively. This allows real-time imaging of the device during the laser scan process. The InGaAs camera also provides the capability to do PEM (which will be utilized in later chapters of this thesis) studies.

For stability purposes, the system is placed on the ground floor of the building. In addition, the stage and laser scanning head are placed on a heavy-weight granite table in order to dampen any minute acoustic/mechanical vibration (i.e., from turret rotation, motors, stage movements) generated within the system enclosure. This granite table is further suspended by an anti-vibration system installed on all four supports of the system in order to isolate effects of any remaining inherent ground vibration or external vibration sources. This is a very critical enabler to provide repeatable and accurate testing on very advanced microelectronic devices with very small feature sizes.

For navigation purposes, the system is equipped with linear servo and linear encoder stages capable of moving the laser scanning head by X and Y axis movements of up to 50 mm by 150 mm, with 20 nm resolution and repeatability better than 0.5 μm .

Moreover, the sample is mounted on a movable circular base stage which can be freely positioned within the system, thereby nulling any concerns on maximum travel distance of sample placement. These features combined allow accurate and repeatable positioning of sample and laser spot.

4.3.2 Choice of Laser Source, Fiber and Connectors

Choice of laser source:

This sub-section reports on the results for the choice of laser source. It is mandatory for the laser setup to be able to perform single shot and thus, exploration was carried out on two possible solutions being: (1) Pulse picker placed outside of the laser source or (2) Pulse picker fully integrated inside the laser source. For solution 1, it is mandatory to place the laser source on an optical table with a free space optical path directed towards the input of a pulse picker. The pulse picker will select the desired laser pulses from the input and only allow the desired pulses to propagate to the output. After the output, it is mandatory to collimate the free space laser beam into an optical fiber for laser delivery to the main microscope system. Solution 1 provides advantages such as more flexibility in the choice of pulse picker (thereby allowing pulse laser sources of higher energy or repetition rates), modularity for future upgrades and straightforwardness of troubleshooting in case of anomaly. To evaluate the possible limitations of such a solution, experiments were set up at a collaborator's laboratory in CNES and interfacing was done with existing equipment. From the experiments, two possible limitations of this solution were identified: (1) "Beam spill" phenomenon resulting in very poor extinction ratio and (2) Optical misalignment which can significantly decrease the laser energy delivered to the DUT.

Limitation 1: "Beam spill" phenomenon resulting in very poor extinction ratio

Figure 4.8 presents the schematic of the experimental setup. A laser source (1064 nm, 7.5 ps, 80 MHz) was placed before the electro-optic deflector (i.e., pulse picker) which selects the true desired laser pulses and deflects the unwanted ones. Two different photodiodes were placed at the position of "dumped laser pulses" and at the end of the "fiber" in order to monitor the respective magnitude of incident laser pulses.

Figure 4.8 Schematic of free-space pulse picker (electro-optic deflector) experimental setup. Two different photodiodes were each placed at the position of “dumped laser pulses” and at the end of the “fiber” in order to monitor the incident laser energy.

Figure 4.9 shows the amplitude of transient voltage generated in these two different photodiodes (“PD fiber” was positioned at the end of the fiber while “PD EOD” was positioned at the end of the dumped laser pulses of the electro-optic deflector) as incident laser power increases.

Figure 4.9 Oscilloscope trace diagram showing the voltage transients generated by incident laser pulses at 40 MHz. Top trace shows the arrival of laser trigger, middle trace shows voltage transient of the photodiode at the end of “fiber” and bottom trace shows voltage transient of another photodiode at the “dumped laser pulses” of the electro-optic deflector (EOD). Scale of the diagram is 50 mV/div on the vertical axis and 20 ns/div on the horizontal axis. Diagram shows issue of vast portion of true pulses being dumped at high laser power.

As the electro-optic deflector serves as a pulse picker, the true desired pulses will propagate to the photodiode positioned at the end of the “fiber” while the unwanted pulses will be deflected to the photodiode at the position of “dumped laser pulses”. With reference to Figure 4.9, it can be observed from the middle trace of PD fiber that the amplitude of true pulses was increasingly overshadowed by dumped pulses as laser power increased. This is in-line with the bottom trace of PD EOD whereby increasing amplitude of true pulses was being deflected/dumped at high laser power. This experiment was conducted at 40 MHz, half the natural lasing frequency (80 MHz) of the laser source. Under normal pulsed laser SEE test conditions, a typical frequency of 1 kHz will be utilized and it can be easily understood that many more of the 80 MHz pulses will be deflected/dumped than the scenario presented in Figure 4.9. In this case, at high laser power, the dumped laser pulses will form a very strong background pulse train at 80 MHz while the desired 1 kHz laser pulses will be greatly overshadowed. This is identified as a “beam spill” phenomenon and a major limitation that should preferably be avoided in the proposed system. Although this phenomenon can be greatly improved by proper optical alignment and fine tuning of voltage bias to the electro-optic deflector, an alternative solution will be better.

Limitation 2: Optical misalignment significantly decreasing the delivered laser energy

Figure 4.10 shows the effect of optical misalignment on the laser energy arriving at the PD fiber. This verified that the free-space setup is very vulnerable to vibrations and optical misalignment can greatly affect not only the amplitude of laser energy but also its linearity response to increase in laser power. This linearity is broken when the optical beam is misaligned (as seen in Figure 4.10a) and reasons (large portion of true pulses being dumped) were already explained in the discussions above.

Figure 4.10 Amplitude of voltage transient observed at PD fiber with increasing laser power (a) before alignment and (b) after alignment. Notice the almost 30X increase in observed amplitude after alignment. The non-linearity observed in (a) is largely due to excessive portion of the true desired pulses being dumped away by the electro-optic deflector.

In view of the above limitations and vulnerability to optical misalignment, it was conceived that the proposed setup at NTU is to adopt solution 2 of laser source implementation (i.e., pulse picker fully integrated into laser source). As such, the final laser source was chosen to be a customized Genki 10 HP model from Swiss manufacturer Onefive. Figure 4.11 shows the actual pulsed laser source with its 3U rack mount installed. The pulse picker was fully integrated into the pulsed laser source and there were no free-space elements outside of the radiation safety enclosure of the unit.

Figure 4.11 Pulsed laser source unit with integrated pulse picker installed at NTU's pulsed laser SEE scanning microscope system. No free-space elements outside of the unit's radiation safety enclosure.

This was a pulsed laser of 1064 nm wavelength and 10 ps pulse duration, capable of delivering laser pulses up to 11 nJ (measured at source) of laser energy at natural lasing frequency of 50 MHz. A pulse picker (based on acoustic-optic modulator) was fully

integrated in the laser source, thereby enabling repetition rates down to single shot. Working with the manufacturer, Figure 4.12 shows the spectral width and autocorrelation function of the pulsed laser source, thereby verifying the centering of wavelength at 1064 nm and pulse duration of approximately 10 ps.

Figure 4.12 Verification of pulsed laser source specifications showing centering around (a) 1064 nm wavelength and approximately (b) 10 ps pulse duration

Choice of laser delivery fiber:

This sub-section reports on the results for the choice of laser delivery fiber. Working with the microscope manufacturer, the laser delivery fiber was designed with a 6 μm core diameter. Moreover, due to space constraints and practical reasons, the length of delivery fiber had to be at least 1.5 meters. Working with the laser source manufacturer, simulations were conducted to understand the spectral broadening tradeoff in the choice of delivery fiber of such a small fiber core diameter. Figure 4.13 shows that as the core diameter of the delivery fiber decreases, the amount of spectral broadening will be larger. It was decided that a broadening of 1 nm (comparison between 6 μm and 25 μm core diameter at maximum 10 nJ) was acceptable in the proposed system at NTU. This tradeoff in spectral broadening was counter-minimized via the definition of pulse duration at 10 ps which is shown in Figure 4.14 that the extent of spectral broadening was reduced with a larger pulse duration.

Figure 4.13 Simulation conducted for 1.5 m of delivery fiber, showing spectral broadening tradeoff against pulsed laser energy for delivery fiber of various core diameters. Small fiber core diameter results in large spectral broadening.

Figure 4.14 Simulation conducted for 1.5 m of delivery fiber, showing spectral broadening tradeoff against pulsed laser energy for delivery fiber of various core diameters and pulse durations. Larger pulse duration results in smaller spectral broadening.

Choice of optical fiber connector:

This sub-section reports on the results for the choice of optical fiber connector. Working with the microscope manufacturer, understanding was reached that the fiber-interfacing connector had to be a ferrule connector (FC). At the end of the FC, there were two main types of finishing polish being physical contact (PC) or angled physical contact (APC).

As the fiber connector was interfacing between the laser delivery fiber and the collimator lens of the microscope system, this choice would significantly affect the collection of beam and correspondingly determine the laser energy arriving at the DUT. Figure 4.15 shows a simplified diagram illustrating the impact of the two different connectors. It can be seen that with an incorrect connector, there can be a risk of improper collimation of the laser beam and thus, leading to beam misalignment or laser energy loss.

Figure 4.15 Simplified diagram showing impact of (a) FC/PC and (b) FC/APC connectors on the proper filling of the collimator lens into the optical path of the microscope system

To verify the above-mentioned impact of the different connectors, an experiment was set up to evaluate the laser energy arriving at the DUT (Coherent J10-GE energy sensor in this case) for the two different connector types. The results are presented in Figure 4.16 where the pulsed laser energy was plotted against increasing values of laser source preamp current for FC/PC and FC/APC fiber connectors. It can be seen that across the entire range of laser source preamp current, the laser energy was always higher with the use of FC/PC fiber connector. This fiber connector was thus the final configuration decided for the proposed system at NTU.

Figure 4.16 Pulsed laser energy measurement on Coherent J10-GE energy sensor with increase in laser source preamp current using different FC fiber connectors. Higher laser energy achieved with FC/PC connectors throughout entire range of laser source preamp current.

Last but not least, this connector was coupled with a narrow key design in order to prevent rotation of the delivery fiber when the connector plug was screwed into the system's receptacle. This ensures that the polarization of the laser was maintained properly from the laser source, through the laser delivery fiber to the microscope optics.

4.3.3 Measured Results of Pulsed Laser Energy

This sub-section reports on the results of the pulsed laser energy measurement conducted on the Coherent J10-GE energy sensor with Coherent LabMax TOP energy meter. Conditions of the measurement were as per described in section 4.2.1 and results are reported in Figure 4.17 for a total of eight different days (across a period of eight months) in order to monitor the longer-term energy stability of the system.

Figure 4.17 Pulsed laser energy measurement on Coherent J10-GE energy sensor for (a) 5X, (b) 20X and (c) 50X objective lenses over a period of eight months. Results showed good laser energy stability of the pulse laser SEE scanning microscope system at NTU.

The above data was further analyzed and even with the highest magnification lens of 50X (where conditions for laser energy stability were more stringent), standard deviation of the laser energy stability was below 1.2% across the entire range of laser source preamp current from 1.6 A to 6 A. This result demonstrated the stability of the laser system with all the objective lenses installed.

4.3.4 Measured Results of Pulsed Laser Spot Size

This sub-section reports on the results of the pulsed laser's full-width-half-maximum (FWHM) spot size measurement conducted using the Coherent J10-GE energy sensor with Coherent LabMax TOP energy meter. Conditions of the measurement were as per described in section 4.2.2 and results are reported in Figure 4.18 for the 5X, 20X and 50X objective lenses installed on the laser system at NTU. As observed from the blue-cross data points in Figure 4.18, the measured laser energy was initially low (knife blocks the laser) but increases exponentially to a saturation value as the laser spot scans across the knife edge and deposit majority of the laser energy onto the sensor. The laser energy data was processed to obtain the first derivative (green-dots in Figure 4.18) and then fitted with a Gaussian function (red line in Figure 4.18) in order to obtain the FWHM spot size of 6.22 μm , 2.04 μm and 1.85 μm for 5X, 20X and 50X objective lenses respectively.

Figure 4.18 Pulsed laser spot size measurement for: (a) 5X, (b) 20X and (c) 50X objective lenses. Blue crosses represent raw data from laser energy measurement using energy sensor while red line represent the Gaussian fit to the green dots in order to obtain the FWHM spot size of the laser system at NTU.

Figure 4.19 shows the results obtained for various positions in the z-axis, in order to determine the minimum spot size for each objective lens. As expected, the laser spot size reaches a minimum value near to the focal position and broadens out with increased extent of defocusing in the z-axis.

Figure 4.19 Laser spot size (FWHM) as a function of z position. Minimum spot sizes of 6.22 μm, 2.04 μm and 1.85 μm are obtained for 5X, 20X and 50X objective lenses respectively.

4.3.5 Benchmarking Results of LM124

This sub-section reports on the results for the benchmarking of the proposed laser scanning system, via tests conducted on LM124. Bias conditions of LM124 in this set of experiments were as per described in section 4.2.3. In this bias condition, the normal operating output would be a static 1 V signal. However, when a laser pulse arrives at the DUT, electron-hole pairs would be generated and a current transient would form. This would propagate to the output of the device and appear as a voltage transient pulse on the oscilloscope, thereby signifying occurrence of SET. Based on the purpose and procedures of the first part of this experiment already explained in section 4.2.3, the pulsed laser was scanned (with 20X objective lens) across the sample surface to locate all the SET-sensitive transistors. Figure 4.20 shows the SET mapping with increasing laser energy. At low laser energy, only the most SET-sensitive transistors appear on the SET mapping. However, at higher laser energies, more electron-hole pairs were generated, thereby inducing larger transient currents at other sensitive transistors and

ultimately leading to more sensitive regions being observed on the SET mapping in Figure 4.20.

Figure 4.20 Localization of SET-sensitive areas in LM124 operational amplifier. Increase in SET-sensitive area as laser energy increases from (a) to (g). Laser energies used were: (a) 0 nJ, (b) 0.20 nJ, (c) 0.26 nJ, (d) 0.42 nJ, (e) 0.82 nJ, (f) 1.55 nJ and (g) 2.79 nJ.

With knowledge of the exact location of these SET-sensitive transistors, part two of the experiment could commence. The pulse laser was then operated in the single-irradiation mode and targeted at specific transistors with the 50X objective lens. Figure 4.21 shows the results obtained at Q9 transistor of LM124. The pulsed laser energy was progressively increased to induce more electron-hole pairs and consequentially, SET of higher amplitude and longer duration. The pulsed laser energy was increased to a point where the SET amplitude matches that obtained from heavy ion test in literatures (i.e., the benchmark reference). The laser-induced SET waveform was then compared to the heavy ion test results and good similarity in pulse polarity, shape and duration was observed.

Figure 4.21 SET waveform induced by NTU pulsed laser at Q9 transistor of LM124. Results showed good correlation with benchmark reference (heavy ion test result reproduced from [2]). Laser energy used in this case was 0.12 nJ.

Figure 4.22 shows the results obtained at another transistor, Q20, of LM124. This transistor was chosen as it produces a positive SET, unlike the case of Q9 which was negative SET. Laser-induced SET was once again compared to heavy ion test results and good similarity was observed. Also, this transistor was much less sensitive than Q9, thus requiring a larger laser energy in order to induce a SET. The similarity in SET waveform verified the validity of this technique even at high laser energies.

Figure 4.22 SET waveform induced by NTU pulsed laser at Q20 transistor of LM124. Results showed good correlation with benchmark reference (heavy ion test result reproduced from [2]). Laser energy used in this case was 2.14 nJ.

This sub-section showed that the proposed pulsed laser SEE scanning microscope system at NTU was capable of inducing SET which correlates well with previous

published data from heavy ion tests. This was a critical step in order to validate the technique and form the baseline for comparison in future tests.

4.3.6 Benchmarking Results of LMC6484

This sub-section reports on the results for the benchmarking of the proposed laser scanning system, via tests conducted on LMC6484. Bias conditions of LMC6484 in this set of experiments were as per described in section 4.2.3. In this bias condition, the normal operating output would be a static 8 V signal. When a laser pulse arrives at the DUT, electron-hole pairs would be generated and when a SET was induced, a voltage transient pulse would be observed on the oscilloscope. According to procedures already outlined in section 4.2.3, the first part of this experiment involved scanning the pulsed laser across the sample surface to locate all the SET-sensitive transistors. Result of the SET mapping (with 2.5X objective) is presented in Figure 4.23(a). These regions were clearly identified and marked out on a high resolution IR micrograph of LMC6484 as shown in Figure 4.23(b). Deeper investigation was conducted on region A and SET mapping of sensitive regions were obtained under 50X objective lens. These results are presented in Figure 4.23(c).

Figure 4.23 (a) SET mapping (with 2.5X objective lens) of LMC6484 with red regions showing SET-sensitive structures, (b) Identification of SET-sensitive area, regions A and B, superimposed on a high resolution IR micrograph of LMC6484 and (c) Identification of SET-sensitive structure in region A of LMC6484 with 50X objective lens.

With knowledge of the exact location of these SET-sensitive transistors, part two of the experiment could commence. The pulse laser was operated in the single-irradiation mode and targeted at the structure marked by the yellow cross in Figure 4.23(c). Pulsed

laser energy was subsequently increased, inducing SETs of larger amplitude and longer duration. As a result, a “family of SET curves” were obtained from each facility and compared against available literatures [6]. This comparison involved three different pulsed laser SEE facilities and is presented in Figure 4.24 with the x and y axis of all graphs being scaled to the same dimensions in order to facilitate comparison. Additional verification was also conducted by superimposition of the graphs and results showed good agreement across all facilities.

Figure 4.24 Family of SET curves obtained from LMC6484 at three different pulsed laser SEE facilities: (a) CNES facility via 1064 nm, 7.5 ps laser, (b) NRL facility via 590 nm, 1 ps laser reproduced from [6] and (c) NTU facility via 1064 nm, 10 ps laser. Laser energies were increased from 20% to 80% at CNES facility while laser energies were increased from 2.5 A to 6 A of laser source preamp current at NTU facility. Results showed good agreement (similar SET polarity, shape, pulse duration and recovery slope) across all facilities while the CNES and NTU laser seemed to be able to induce larger SETs than those available in the NRL literature. This was expected as laser sources with different maximum laser energies were used at each facility.

This sub-section showed that the proposed pulsed laser SEE scanning microscope system at NTU is capable of inducing SET which correlates well with data from two other pulsed laser facilities. In addition, this was demonstrated on LMC6484, a device fabricated in CMOS technology, which was more recent and relevant in today’s vast variety of microelectronic devices.

4.4 Conclusions

In this chapter, details regarding the setting up of the proposed pulsed laser scanning microscope system were described. The choice of the scanning microscope configuration was unique from the current existing pulsed laser SEE setups across the globe. Current existing pulsed laser SEE setups are customized systems generally consisting of pulsed laser source, mirrors, objective lenses and movable x-y-z sample stage built on an optical bench. The x-y sample stage was moved to control the irradiation of pulsed laser at various positions of the sample. This movement can impose limitations on efficiency (mechanical speed constraints) and positional accuracy (mechanical stability or repeatability constraints), thereby limiting the accuracy of tests conducted on advanced microelectronics of very small and dense structures. The pulsed laser scan methodology proposed in this chapter therefore seeks to improve on these limitations. In this methodology, the laser was scanned across the sample surface and thus, avoids mechanical movements of the stage. This improves the positional accuracy which is especially important during testing of advanced microelectronic devices with small and dense structures.

In addition, evaluation studies were conducted on the various configurations of laser source, laser delivery fibers and connectors. These were crucial decisions to be made in ensuring compatibility to the microscope system. Following the setting up of the system, characterization results of laser parameters (pulsed laser energy and laser spot size) were presented. Laser energy stability was verified for up to a period of eight months and gives strong confidence for repeatable test results to follow. To validate this setup, further benchmarking of pulsed laser SEE test results were conducted on two devices of dissimilar technology processes/architectures and reported in this chapter.

With the details and validation of the proposed pulsed laser scanning microscope covered, the effects of ageing on devices fabricated with old and advanced process technologies would be evaluated in the following chapter.

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Chapter 5 *

Effects of Ageing on Radiation Sensitivity

The proposed pulsed laser SEE scan methodology (as described in the previous chapter) was applied to investigate the scientific hypothesis (identified in section 1.2) that the effects of ageing on SEE response will be more severe in advanced microelectronic devices. Reliability margins are getting thinner with each advancement in technology node but currently, radiation tests are commonly conducted only on pristine devices and not on aged devices. The results for this study not only raise concerns to the space radiation community to take into account of device ageing during radiation qualification process but also highlight the efficient feedback loop that the proposed pulsed laser scan methodology could offer. In this chapter, ageing tests were conducted on LM124 (old technology) and chain of flip flops fabricated in advanced 65 nm CMOS process technology. Changes in electrical parameters for each device type are reported. After ageing, little change in SEE sensitivity was observed for LM124 (old technology) while significant change in SEE sensitivity was observed for the chain of flip flops in advanced 65 nm technology. Further simulation results on the change in threshold voltage and SEE sensitivity are also reported to provide insights into the vulnerability of advanced microelectronics to ageing effects.

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5.1 Introduction and Motivation

Currently, SEE radiation qualification via the ‘gold’ standard of heavy ion test methodology is commonly conducted on pristine devices. Sample sizes for these qualifications are normally quite small (but sufficient to arrive at a confident assessment) due to the expensive and limited amount of accelerators’ beam time. Satellite engineers often work in shifts (around the clock) which consists of different teams in order to fully utilize the allocated time slot. Difficulty in accessing these facilities further aggravates the satellite’s design feedback loop time and development cycle.

The recent boom in the interest of using COTS in space arises partly from the desire to utilize state-of-the-art, high frequency, high processing speed and low power advanced microelectronic devices to improve the performance of satellites. These advanced devices were not originally intended for space applications and therefore, reliability of these components has to be carefully assessed to ensure space mission success. Moreover, reliability margins of advanced microelectronic devices have been getting thinner over the years and will continue to be so. These issues pose growing concern on whether ageing of advanced microelectronic devices in space would have an increasing impact on its SEE response. Studies on these cross-interactions (between ageing and SEE) would be extremely difficult in heavy ion test facility, considering the global status of inadequate beam time, as discussed in the preceding paragraph.

The motivation is therefore to utilize the pulsed laser SEE scan methodology, as described in Chapter 4, to study the impact of ageing on SEE response of old and advanced microelectronic devices. Potentially, this method offers two main advantages. The first advantage being, this method does not require the use of heavy ion test facility and therefore, potential time and cost savings on accelerators’ beam time can be attained. This is especially important to small-satellite engineers who face short satellite development cycle or to circuit designers who can benefit from the shorter satellite’s design feedback loop time. Secondly, this method also potentially offers the user with additional spatial information to identify where or which are the structures that are becoming more sensitive after ageing, so that additional mitigation schemes can be applied to improve its hardness. These advantages work in tandem to provide an alternative SEE methodology which complements the ‘gold’ standard of heavy ion SEE

test. Details of the use of this pulsed laser SEE scan methodology to study the effects of ageing on LM124 and 65 nm chain of flip flops, changes in device electrical parameters, changes in SEE sensitivity, and simulation results will be elaborated in the following sections.

5.2 Effects of Ageing on LM124 Bipolar Operational Amplifier

This section is divided into two sub-sections reporting on: (1) Experimental details and (2) Experimental results of the ageing conducted on LM124 bipolar operational amplifier. In each sub-section, details of the device descriptions, device stressing or ageing conditions, device electrical parameter characterizations, and laser SEE test procedures will be elaborated.

5.2.1 Experimental Details

This sub-section reports on the ageing procedures for LM124. Briefly, the experimental flow cycle for the ageing of LM124 began with preparation of the sample for backside optical access. The sample was then subjected to repeated cycles of (1) electrical characterization, (2) high temperature and current stress, and (3) laser SET test, for various time points of stress duration up to 1002 hours. Experimental details for each of these procedure will be explained below.

Device description and stress/ageing conditions

The device under test was LM124 bipolar operational amplifier which consisted of four identical and independent amplifiers packaged in a single device. Figure 5.1 illustrates the schematic of this sample while specifying the various transistors, resistors and capacitors involved in the input, gain and output stages during the operation of the amplifier.

Figure 5.1 Schematic of LM124 with various transistors, capacitors and resistors [1]. Q1 to Q4 are involved in the input stage, Q10 to 12 are involved in the gain stage and Q5, Q6 and Q13 are involved in the output stage of the amplifier.

The sample was then milled and polished on the backside of the silicon die in order to allow for laser optical access during pulsed laser SET tests. Figure 5.2 shows the sample before and after preparation.

Figure 5.2 Images of LM124 sample (a) before and (b) after preparation. Backside of the silicon die (red arrow) was exposed to allow optical access during subsequent pulsed laser SET tests.

During ageing, the LM124 was subjected to high temperature and current stress. Figure 5.3 illustrates the bias conditions during the ageing in which Figure 5.3(a) represents the low power supply voltage (V_{DD}) case of ± 5 V while Figure 5.3(b) represents the high V_{DD} case of ± 15 V. In each case, the four independent amplifiers of LM124 were biased differently. Using different load resistor values, amplifiers 1 and 2 were stressed

at high current while amplifiers 3 and 4 were stressed at low current. Also, the amplitude and polarities of the input voltage were different for each amplifier.

Figure 5.3 Bias conditions of LM124 during ageing for (a) low V_{DD} and (b) high V_{DD} cases. Amplifier 1 was stressed with small input voltage of 0.05 V, amplifier 2 was stressed with high current (via use of small load resistor of 4.7 Ω), amplifier 3 was stressed with low current (high load resistor of 100 k Ω) while amplifier 4 was stressed at low current with negative input voltage applied at the positive terminal.

The ageing was carried out in an oven being set to a temperature of 125 °C. Thermocouples were placed on the samples in order to verify the actual ageing temperature and output voltages of each amplifier were verified to ensure that bias conditions were accurate. Dedicated test boards were fabricated for the ageing experiments in order to prevent effects of ageing on passive components to be spilled over to subsequent electrical characterization and laser SET tests. For these subsequent characterization tests, a new set of test boards were used. Electrical biases were provided during the ageing experiments to the test boards. At time points of 0 h, 334 h, 668 h and 1002 h, the samples were taken out from the oven in order to conduct electrical characterizations and laser SET test stages of the entire experiment flow cycle.

Device electrical parameter characterizations

A total of seven different electrical parameters were monitored during this set of experiments. These parameters were: (1) power supply current, (2) input bias current, (3) output current, (4) output voltage, (5) bandwidth, (6) slew rate and (7) noise. Figure 5.4 illustrates the various device configurations being utilized for characterization of these electrical parameters. Each parameter required a specific device configuration in order to obtain the maximum resolution or sensitivity for the measurement. These

device configurations were prepared on various test boards and to maintain consistency for each parameter measurement, the same test boards were used for characterization across the different ageing time points of 0 h, 334 h, 668 h and 1002 h.

Figure 5.4 Device configurations utilized during electrical characterization of (a) bandwidth, (b) slew rate, (c) noise and (d) input offset voltage. In addition, power supply current, input bias current, output voltage were also characterized using the configuration as depicted in (a).

Laser SEE test procedure

Pulsed laser SEE tests were conducted using the proposed scan methodology at a pulse repetition rate of 40 kHz to induce SET in the LM124 amplifiers. This was performed at three different time points, each time after ageing duration of 0 h, 334 h and 668 h. An objective lens of 20X was utilized during this set of experiments in order to permit adequate field of view to scan the entire amplifier.

During these pulsed laser SET tests, the LM124 was operated in the voltage follower mode and supplied with V_{DD} of $\pm 5\ V$ and V_{IN} of 100 mV. As a consequence of this biasing condition, the normal operating output voltage was at a static 100 mV state. As the pulsed laser scans across the sample, energy would be deposited into the sensitive nodes of the integrated circuit, thereby generating transient currents. As the laser energy increases, SET of higher amplitudes and duration will be generated. The laser SET threshold is defined as the first laser power to induce a SET. In this experiment, the LM124 was capable of displaying negative and positive SET and thus, there were two

different values for laser SET thresholds. Figure 5.5 presents the laser SET mapping and superimposed micrograph image obtained under 1% and 3% laser power for negative and positive SET, respectively. Since these were the laser power which induced the first negative and positive SET, these were defined as the negative and positive SET laser thresholds respectively. The laser SET threshold gives an indication of the sensitivity of the device to SET. A lower laser SET threshold will signify that less laser power is needed to induce a SET and thus, the device had become more sensitive.

Figure 5.5 Superimposed image of laser SET mapping and device micrograph showing the SET sensitive regions for (a) Negative SET, denoted in dull red, obtained at negative SET laser threshold of 1% laser power and (b) Mixture of negative and positive SET, denoted in bright red, obtained at positive SET laser threshold of 3% laser power.

As the pulsed laser scans pixel by pixel across the sample surface, this SET occurrence would be registered as an error at the corresponding pixel on the SET mapping image. As SET are transient (or temporary) signals, the device output will automatically return to the nominal state after the event and wait for the arrival of the next laser pulse at the next pixel. Figure 5.6 presents an example of the waveform of a single SET induced at one position of an amplifier in LM124. It can be observed that the device voltage returns back to the nominal 1 V level after the SET event.

Figure 5.6 Oscilloscope waveform of a single SET induced in LM124 via pulsed laser setup. The SET is a transient signal which ultimately returns back to the normal state of device voltage (1 V in this case).

This iterative process continued until the entire field of view of the sample surface was completely scanned and the superimposition of the SET mapping image with the device microscope image revealed the position of the SET-sensitive regions in the design.

5.2.2 Experimental Results and Discussions

With the experimental details covered, the next sub-sections will cover the experimental results for the monitoring of change in electrical parameter and SET sensitivity of LM124 after ageing.

5.2.2.1 Changes in Electrical Parameters of LM124

This section reports on the changes in the various types of electrical parameters of the amplifiers in LM124 after being monitored over a maximum duration of 1002 hours (almost 42 days). Figure 5.7 presents the results for the change in power supply current with ageing duration. It can be observed from Figure 5.7(a) that under the condition of low V_{DD} at ± 5 V, ageing resulted in a general increase in power supply current for all of the four independent amplifiers. A maximum of up to 5% change in power supply current was observed from amplifier 4. In the high V_{DD} condition of ± 15 V as shown in Figure 5.7(b), it can be observed that there is a general decrease in power supply

current for all of the four independent amplifiers. The extent of decrease is however relatively small, with the maximum change at 2% from amplifier 1.

Figure 5.7 Change in power supply current as a function of ageing duration for the four independent amplifiers of LM124 operated in (a) low V_{DD} of $\pm 5V$ and (b) high V_{DD} of $\pm 15V$ cases. Changes in power supply current were relatively small after considering the long duration of ageing imposed on the samples.

In all cases, the percentages of change in power supply current were relatively small after considering the long duration of ageing imposed on the samples. Moreover, it can be observed that even for the fresh samples (ageing duration of 0 h), there were already amplifier-to-amplifier variation in power supply current. Thus, the change in power supply current (5% and 2% for low and high V_{DD} cases respectively) after ageing was not considered very significant. This was in line with expectations and provided quick indication that devices fabricated in well-established bipolar processes are reliable and able to withstand harsh conditions for an extended period of time.

Figure 5.8 presents the results for the change in input bias current with ageing duration. This parameter was monitored to give indication of any leakage currents at the input transistors of the amplifiers. In both cases of low and high V_{DD} , it can be observed from the figure that input bias current had remained relatively flat even after 1002 hours of ageing and thus, showed that leakage currents at input transistors were not significantly affected.

Figure 5.8 Change in input bias current as a function of ageing duration for the four independent amplifiers of LM124 operated in (a) low V_{DD} of ± 5 V and (b) high V_{DD} of ± 15 V cases. Input bias current remained relatively flat even after 1002 h of ageing.

Figure 5.9 presents the results for the change in output current with ageing duration. This parameter was monitored to give indication of any increased current consumption at the output transistors of the amplifiers. In both cases of low and high V_{DD} , it can be observed from the figure that output current remained relatively flat, signifying that output transistors remained relatively unchanged after 1002 hours of ageing.

Figure 5.9 Change in output current as a function of ageing duration for the four independent amplifiers of LM124 operated in (a) low V_{DD} of ± 5 V and (b) high V_{DD} of ± 15 V cases. Output current remained relatively flat even after 1002 h of ageing.

Figure 5.10 presents the results for the change in output voltage with ageing duration. This parameter was monitored to give indication of any change in voltage gain of the amplifiers. A change in this parameter could affect the amplitude of the SET and thus, affect the SET sensitivity of the device. However, from the experiments conducted in both cases of low and high V_{DD} , it can be observed from the figure that output voltage remained relatively unchanged after 1002 hours of ageing. Even the maximum change

(0.5% from amplifier 4 of low V_{DD} case) was not considered significant for the long period of ageing.

Figure 5.10 Change in output voltage as a function of ageing duration for the four independent amplifiers of LM124 operated in (a) low V_{DD} of ± 5 V and (b) high V_{DD} of ± 15 V cases. Output voltage remained relatively flat even after 1002 h of ageing.

In monitoring the various electrical parameters of the LM124 as discussed in this section, devices fabricated in well-established bipolar processes are generally very reliable and capable of enduring severe conditions for long duration. Ageing has limited impact on the electrical parameters but checks on SET sensitivity were still dutifully carried out. Results of these checks on SET sensitivity as a function of ageing will be covered in the immediate section to follow.

5.2.2.2 Little Change in SET Sensitivity of LM124

This section reports on the changes in the SET sensitivity of LM124 after ageing. The SET sensitivity of LM124 was determined via the laser energy threshold parameter. This parameter defines the first pulsed laser energy needed to cause a positive or negative SET and was checked after ageing time points of 0 h, 334 h and 668h. Figure 5.11 presents the results for the laser energy threshold to trigger negative SET in LM124 as a function of ageing duration for amplifiers aged in both low V_{DD} and high V_{DD} cases. It can be observed from Figure 5.11 that there was little change in the SET sensitivity even after 668 hours of ageing. Unfortunately, SET tests were not conducted at the 1002 h time point as the laser system was unavailable. Nevertheless, this conclusion was consistent across all the amplifiers tested and was independent of the low or high current stress conditions.

Figure 5.11 Laser threshold of negative SET for LM124 amplifiers aged under (a) low V_{DD} and (b) high V_{DD} cases. Samples were operated in voltage follower mode during pulsed laser tests. Little change in SET sensitivity was observed even after 668 hours of ageing.

Figure 5.12 presents the results for the laser energy threshold to trigger positive SET in LM124 as a function of ageing duration for amplifiers aged in both low V_{DD} and high V_{DD} cases. It can be observed from Figure 5.12 that there was little change in the SET sensitivity even after 668 hours of ageing. In Figure 5.12(b), it may seem like there was a slight increase in laser threshold with ageing duration but since the change was relatively small, the general trend cannot be confidently affirmed. This conclusion was consistent across all the amplifiers tested and was independent of the low or high current stress conditions.

Figure 5.12 Laser threshold of positive SET for LM124 amplifiers aged under (a) low V_{DD} and (b) high V_{DD} cases. Samples were operated in voltage follower mode during pulsed laser tests. Little change in SET sensitivity was observed even after 668 hours of ageing.

In view of the results presented in this section, there was little change in the SET sensitivity of the amplifiers in LM124 even after being subjected to a maximum ageing

duration of 668 hours, under various conditions of low or high current and low or high V_{DD} . This was in line with expectation that devices fabricated with old process technology (bipolar junction transistors in LM124) are generally more robust and reliable, thus requiring much longer stress or ageing duration to induce any significant change.

5.3 Effects of Ageing on 65 nm CMOS Chain of Flip Flops

With the experimental details and results of the ageing of LM124 covered, this section reports on the details and results of the ageing conducted on 65 nm CMOS chain of flip flops.

5.3.1 Experimental Details

This sub-section reports on the ageing procedures for 65 nm chain of flip flops. Briefly, the experimental flow for the ageing of 65 nm chain of flip flops began with preparation of the sample for backside optical access. The sample was then subjected to repeated cycles of (1) electrical characterization, (2) voltage stress, (3) electrical characterization and (4) laser SEU test, for various time points of stress duration at 0 h, 10 h, 30 h and 130 h. Experimental details for each of these procedures will be explained below.

Device description and stress/ageing conditions

The chain consisted of 100-stage flip flops manufactured in 65 nm low power bulk CMOS process technology by GlobalFoundries, Singapore. For this structure, the nominal operating voltage was 1.2 V. Figure 5.13(a) illustrates the schematic of this chain of 100 flip flops with input, clock and output terminals. Also shown in Figure 5.13(b), each flip flop was made up of various internal transistors and pass gates which were controlled by the clock signal. In order to mimic as closely to the randomized layout commonly encountered in real-life application, these individual flip flops were intentionally dispersed among structures of other designs in a single silicon die.

Figure 5.13 Schematic diagram of (a) chain of 100 flip flops and (b) internal transistors of a single D flip flop.

The sample was then milled and polished on the backside of the silicon die in order to allow for laser optical access during pulsed laser SEU tests. Figure 5.14 shows the sample before and after preparation.

Figure 5.14 Images of 65 nm chain of 100 flip-flops sample (a) before and (b) after preparation. Backside of the silicon die (red arrow) was exposed to allow optical access during subsequent pulsed laser SET tests.

During ageing, the chain of flip flops was subjected to voltage stress of 12.5% above nominal (i.e., V_{DD} is 1.35 V), with clock and input signals being held at a HIGH state (1.35 V). All of the voltage signals were delivered at static conditions with the aim to segregate complications from dynamic stress and recovery phenomenon. To further isolate the cause of ageing degradation, only voltage stress and no temperature stress was applied. The sample was stressed for a total of four different time points at 0 h, 10 h, 30 h and 130 h. At the end of each time point, the sample was subjected to characterizations of electrical parameters, laser SEU test and then a second round of

electrical characterizations (to monitor if there were any impact of the laser on electrical parameters), before the ageing continues again.

Device electrical parameter characterizations

Characterization of the device's electrical parameters were conducted twice for each ageing time point. This was done before and after the ageing. The aim was to monitor the effects of ageing on the electrical parameters and also to ensure that the pulsed laser tests do not induce significant changes to the electrical parameters. Various electrical parameters such as static power supply current, dynamic power supply current and slew rate were monitored. These electrical parameters were prudently chosen as they impose direct impacts on the electrical performance (correspondingly, radiation performance) of the chain of flip flops.

Static power supply current was measured when the device was biased at V_{DD} of 1.2 V, with both input and clock signals at LOW state. Dynamic power supply was measured at V_{DD} of 1.2 V, with clock frequency of 1 MHz while input was held at LOW state. Slew rate was measured at V_{DD} of 1.2 V, with clock frequency of 1 MHz while input transited from HIGH to LOW state.

Laser SEE test procedure

Pulsed laser SEE tests were conducted using the proposed scanning microscope methodology at a pulse repetition rate of 1 kHz to induce SEU in the chain of 100 flip flops. This was performed at four different time points, each time after ageing duration of 0 h, 10 h, 30 h and 130 h. An objective lens of 20X was utilized during this set of experiments in order to permit adequate field of view to scan the entire chain of flip flop. Also, laser energies used in this set of experiments did not exceed 1 nJ to minimize any possible thermal effects to the sample.

During these pulsed laser SEU tests, the chain of 100 flip flops was supplied with V_{DD} of 0.9 V while the clock frequency was at 1 MHz and input terminal held at a LOW state (0 V). As a consequence of this biasing condition, the normal operating output voltage was at a LOW state. As the pulsed laser scans across the sample, energy would be deposited into the sensitive nodes of the integrated circuit, thereby generating transient currents. As the laser energy increases, there would be a point where

sufficiently large transient current would be generated and thus causing an alteration in the internal state of the flip flop. At this point, a SEU (observed as a conversion of the output state from LOW to HIGH) would have occurred. As the pulsed laser scans pixel by pixel across the sample surface, this SEU occurrence would be registered as an error at the corresponding pixel on the SEU mapping image. Subsequently, the 1 MHz clock signal would reset the state of the chain of 100 flip flops back to the nominal output at the LOW state while waiting for the arrival of the next laser pulse at the next pixel. Figure 5.15 presents the waveform of a single SEU induced in the 65 nm chain of 100 flip-flops. It can be observed that the device voltage returns back to the nominal 0 V level after the SEU event.

Figure 5.15 Oscilloscope waveform of a single SEU induced in the 65 nm chain of 100 flip-flops via pulsed laser setup. The SEU was being reset by the device clock signal which ultimately returned the device to the nominal state (0 V in this case). X-axis scale of 10 $\mu\text{s}/\text{div}$ and y-axis scale of 500 mV/div (yellow trace) and 5 V/div (pink trace) were used.

This iterative process continued until the entire field of view of the sample surface was completely scanned and the superimposition of the SEU mapping image with the device microscope image revealed the position of the SEU-sensitive regions in the design. Figure 5.16 presents the laser SEU mapping and superimposed micrograph image obtained at 28% laser power. This superimposed image was then compared against the designer layout and verified to match with the actual flip flop locations of the chain.

Figure 5.16 (a) Laser SEU mapping obtained at 28% laser power and (b) Superimposed image of laser SEU mapping on device micrograph. Red regions indicate SEU-sensitive structures.

5.3.2 Experimental Results and Discussions

With the experimental details covered, the next sub-sections will cover the experimental results for the monitoring of change in electrical parameter and SEU sensitivity of the 65 nm CMOS chain of flip flops after ageing.

5.3.2.1 Changes in Electrical Parameters of 65 nm CMOS Chain of Flip Flops

This section reports on the monitoring of changes in the various electrical parameters of the chain of flip flops and are hereby presented in Figure 5.17. It can be observed that the voltage stress impacted the electrical parameters and caused two different phases of variation: (1) The early phase consisting of a rise in power supply currents and slew rate and (2) The late phase consisting of a drop in power supply currents and slew rate.

Figure 5.17 Impact of voltage stress on changes in: (a) Static power supply current, (b) dynamic power supply current and (c) slew rate of chain of flip flop, for stress duration up to 130 hours.

In the early phase of stressing, several mechanisms such as redistribution of defects [2] or recovery of intrinsic traps [3] were involved and would inevitably lead to variations in electrical parameters. Interactions between these mechanisms are non-trivial and require deep investigations to fully understand some of these short-timeframe mechanisms. Nevertheless, in the late phase of longer term stressing, the dominant mechanisms would prevail and thus, variations in electrical parameters could be better comprehended. The drop in power supply currents results in the lowering of current drive in the transistors of the flip flop. This current drive is a determining factor in defining the amplitude and rate of charge or discharge in the internal nodes of the flip flop. Accordingly, the temporal and amplitude properties of a transient current during radiation impact (pulse laser in this case) would be modified. Moreover, the drop in slew rate gives an indication that the chain of flip flops was slower in responding to a change of state. This could cause an increase in the duration of transient current which would increase the probability of SEU-capture at any clock frequency, thereby increasing SEU-sensitive cross-section area.

Ageing has been shown to impact the electrical performance of the chain of flip flops and checks on SEU sensitivity were also carried out. Results of these checks on SEU sensitivity as a function of ageing will be covered in the immediate section to follow.

5.3.2.2 Changes in SEU Sensitivity of 65 nm CMOS Chain of Flip Flops

This section reports on the changes in the SEU sensitivity of the chain of flip flops after ageing. The pulsed laser SEE scan methodology was employed to assess the SEU-sensitivity of the chain of flip flops. The aim was to monitor the global representation (not just a single flip flop) of SEU sensitivity of the entire chain of flip flops and thus, the scan methodology allowed these experiments to be carried out in an efficient manner. Laser power was sequentially increased to induce more SEUs and these events were recorded. Figure 5.18 shows one series of such superimposed images of a fresh sample. In line with expectation, the SEU-sensitive regions enlarged as more laser power was delivered. In addition, regions which are sensitive at low laser power remained even at high laser power, thereby validating the reliability of this method.

Figure 5.18 Superimposed images of laser SEU mapping on micrograph of sample across various laser power. Denoted in red were SEU-sensitive regions which was found to increase with laser power.

This process of laser SEU mapping was reiterated at several time points of voltage stress in order to evaluate the change in SEU sensitivity of the chain of flip flops. These results are illustrated in Figure 5.19. It can be observed that with the increase in duration of voltage stress, the SEU-sensitive area also increased.

Figure 5.19 Laser SEU mapping conducted at various time points of voltage stress. A constant laser power of 20% was utilized and SEU-sensitive area (denoted as black pixels) was found to increase with duration of voltage stress.

These laser SEU mappings were later processed to obtain the SEU cross-section versus laser power curve as shown in Figure 5.20. This cross-section area was in fact the ratio

of the number of SEU-sensitive pixels to the number of pixels of the entire micrograph. It represents the global SEU response of the entire chain of flip flops, and thus minimize any localized effects which may arise if evaluation was conducted on a single flip flop. It can be observed that after voltage stress of 130 hours, a left-shift in the SEU cross-section curve of the flip flop chain had occurred. This reflected the increase in SEU sensitivity of the chain of flip flops. This was supported by the observation that the saturation cross-section area, at a constant laser power, increased with duration of voltage stress.

Figure 5.20 SEU cross-section area versus laser power curve for various stress durations of 0 h, 10 h, 30 h and 130 h conducted on sample containing chain of 100 flip flops.

5.3.2.3 Simulation Results on 65 nm CMOS Chain of Flip Flops

In view of the complexity of transistor design in a single flip flop, electrical circuit simulations (by means of Cadence Spectre) was employed to better comprehend the fundamental modifications in electrical parameters and SEU response of the chain of flip flops. As mentioned in section 3.8, the electrical circuit layout and process design kit of the 65 nm CMOS chain of flip flops were used to define the electrical response of the device in the simulator. As the fundamental building block of a flip flop was a single inverter, this was targeted as the test subject during the simulation. The inverter was supplied with a V_{DD} of 0.9 V and input was held LOW to keep conditions similar to that used during the pulsed laser SEU tests.

To simulate the effects of ageing on the transistor, the drain current (a function of the threshold voltage, V_{th}) was the primary factor that had been considered as several past studies and evidences [4-6] had shown it to be the dominant concern in long term stress. Following this, focus was placed on the V_{th} shift in the PMOS transistor of the inverter. Figure 5.21 illustrates the simulation results where a decrease of up to 1.4% of the static power supply current (blue square markers) was obtained when the V_{th} of the PMOS shifted by a maximum of 10% (a commonly defined failure criterion).

Figure 5.21 Impact of change in V_{th} of PMOS transistor on static power supply current (denoted as blue squares) and SEU threshold (denoted as red crosses) obtained from simulation studies.

Simulation was also conducted to study the SEU sensitivity of the same inverter. Fundamentally, the SEU response of an inverter is caused by the transient current (which is influenced by the drain current) being generated by a radiation event. In the proposed pulsed laser scan methodology, the laser creates electron-hole pairs in the semiconductor and since the laser pulse duration was short, an electrical model from A. Douin [7], as presented in Figure 5.22, was appropriately implemented.

Figure 5.22 Electrical model for generation of transient current by short laser pulse [7].

For the determination of SEU sensitivity, the SEU threshold (representing the minimum energy required to generate a transient which exceeds the 0.45 V level (50% of V_{DD}) was targeted. For this minimum energy (or SEU threshold), the NMOS (most sensitive transistor with high carrier mobility [8, 9]) was naturally targeted. A double exponential current source, with rise time of 25 ps, was introduced at the drain terminal of the ‘off’ NMOS transistor to simulate the transient current which was generated by a laser pulse. This rise time is slightly longer than the pulse width of the laser source (10 ps) in order to account for delays in circuit response.

Figure 5.21 illustrates the shift in SEU threshold (red cross markers) against the shift in V_{th} of the PMOS. It can be observed that a decrease of up to 38% was obtained on the SEU threshold with a 10% shift in V_{th} . This decrease meant that a lower amount of energy was required to cause an SEU and thus, signifying increased SEU sensitivity. Moreover, another observation was that the extent of SEU threshold shift was much larger than the change in static power supply current, a trend also observed in the experimental results.

5.4 Conclusions

In this chapter, experimental details, results and discussions of the effect of ageing on SEE sensitivity of microelectronic devices were described. This was accomplished through reporting of tests conducted on two devices which were fabricated with vastly different process technologies. The aim was to investigate the scientific hypothesis if device ageing will have significant impact on the SEE response of advanced microelectronic devices. In the presented work, the pulsed laser SEE scan methodology was utilized to assess the SEE sensitivity of both types of devices (LM124 fabricated with old bipolar process technology and chain of 100 flip-flops fabricated with advanced 65 nm CMOS process technology).

In the case of LM124, four individual amplifiers were stressed under various high current and high temperature conditions (125 °C), up to a maximum duration of 1002 hours. Samples were taken out of stress conditions at periodic time points in order to conduct SEE sensitivity assessment via pulsed laser SET tests. The pulsed laser SET energy threshold parameter was taken as a gauge on the shift in SET sensitivity. It was

found that there was little change in SET sensitivity for both positive and negative SETs. This was in line with expectation that devices fabricated with old bipolar process technology are generally more robust and reliable, thereby requiring much longer hours of ageing to induce any significant degradation in the device.

In the case of chain of 100 flip flops, only voltage stress (without high temperature stress) was imposed on the sample, up to a maximum of 130 hours. Despite the shorter stress duration, through monitoring of the SEU mapping of the sample, voltage stress (12.5% above the nominal voltage) was found to significantly increase the SEU sensitivity of such structures. This was clearly evident from the plotting of the SEU cross-section versus laser power curve, which shows that the laser SEU threshold parameter shifted to lower values and the saturation cross-section area increased significantly after the voltage stress. This shift to increased SEU sensitivity was found to be associated with the degradation of electrical parameters and additional SPICE simulations were conducted to achieve better comprehension of the observed trends.

In addition to the above-mentioned results, this chapter also clearly illustrates two benefits of the pulsed laser scan methodology. The first benefit is in providing an efficient means of radiation testing (in addition to conventional heavy ion test methodology) through offering the capability to conduct numerous SEE evaluation tests at various time points during ageing tests. The cost and time savings can be very crucial to small-satellite engineers. Secondly, the pulsed laser scan methodology allows small-satellite engineers to identify structures which had become more sensitive after ageing and thus, presents the possibility to apply mitigation schemes and improve its SEE radiation hardness. These results showed that the pulsed laser SEE scan methodology can be a very useful complementary technique to conventional heavy ion test methodology.

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Chapter 6 *

Applications of Pulsed Laser SEE Scan Methodology

The proposed pulsed laser SEE scan methodology was applied on commercial and custom-designed devices to evaluate its benefits and possible areas of concern. The recent rise in small satellites and increased use of COTS components in space systems provide a fertile application ground for pulsed laser SEE tests which can provide more spatial and temporal information of the device, as compared to conventional heavy ion tests. The results of this chapter not only demonstrate the unique benefits of the pulsed laser SEE scanning microscope system (coupled with optical failure analysis techniques) at NTU but also presents the possible areas of concern in the use of pulsed laser on devices fabricated with advanced process technology, which utilize many new materials (of which, the reliability is not yet fully understood). In this chapter, the applications of the pulsed laser SEE scan methodology will be presented. This will be accomplished through four different studies which involved: (1) Assessing the effects of device configuration on SEE sensitivity, (2) Synergy of optical failure analysis techniques with pulsed laser SEE test methodology, (3) Test board complexity on SEE qualification process and (4) Laser-induced damage in advanced microelectronic devices.

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6.1 Introduction and Motivation

The pulsed laser SEE scan methodology was conceived to alleviate the high demand in heavy ion beam time by providing a quick test method and at the same time, offering users with additional information on SEE radiation response as compared to traditional heavy ion tests. In addition, the scan methodology was conceived to offer better stability and repeatability as compared to stage movement methods and thus, rendering added potential in SEE testing on small structures of microelectronic devices fabricated with advanced process technologies. With the set-up of the pulsed laser SEE scanning microscope system in NTU, this chapter demonstrates applications of this methodology while evaluating some of its advantages and possible areas of concern. These will be presented in this chapter according to four different studies.

Pulsed laser SEE scan methodology was employed to demonstrate the influence of device's bias configuration on its sensitivity to SET and benefits of pulsed laser SEE methodology in alleviating any increased demand for heavy ion radiation tests. Another advantage of the pulsed laser SEE scanning microscope system in NTU is that the system is also equipped with three other laser sources to conduct various optical failure analysis techniques. Several of these techniques were used in tandem for investigations on a PIC16 microcontroller and benefits of this system setup will be elaborated in this chapter.

Although offering multiple advantages as compared to traditional heavy ion test method, the pulsed laser SEE scan methodology is not without its own vulnerabilities. One of the application of the methodology is to reproduce rare SEE events encountered during heavy ion test so that the origins for these rare SEE events can be better understood. This requires the replication of the test conditions used during heavy ion test. However, complete replication can be a challenge due to several factors such as the complications of getting access to the actual test board used during the heavy ion test (if it is designed by third-party radiation test service providers), difference in cable lengths and influence of signal noise between different electrical setups in separate locations. This can pose limitations to the application of the pulsed laser SEE scan methodology and details of these investigations are presented using chain of inverters fabricated with 65 nm CMOS process technology. Last but not least, the potential of pulsed laser SEE scan

methodology in testing on advanced microelectronic devices was evaluated using chain of inverters fabricated with 65 nm CMOS process technology. Laser-induced damages were observed and reported in this chapter. This highlights caution to the application of the technique and demands the definition of the safe operating area for the laser energies used in future pulsed laser SEE test campaigns (especially on advanced microelectronic devices).

With the chapter introduced and motivation explained, the following sections describe the four different studies according to: (1) Assessing the importance of device configuration on SEE sensitivity, (2) Synergy of optical failure analysis techniques with pulsed laser SEE test methodology, (3) Test board complexity on SEE qualification process and (4) Laser-induced damage in advanced microelectronic devices. Experimental details, results and discussions will be covered for each study.

6.2 Importance of Device Configuration on SEE Sensitivity

This section reports on the study which assesses the influence of device configuration on SEE sensitivity, demonstrated via LM124 operational amplifier. Pulsed laser SEE scan methodology was applied on LM124 which was operated under different bias conditions and the respective SET-sensitive mappings (and cross-section curves) were compared. Experimental details, results and discussions are elaborated in the following two sub-sections.

6.2.1 Experimental Details

Briefly, the experimental flow for the LM124 operational amplifier began with preparation of the sample for backside optical access. The sample was configured in voltage follower mode and subjected to pulsed laser SEE test to determine its sensitivity to SET. The amplifier was then configured in comparator mode and its sensitivity to SET analyzed using the pulsed laser SEE scan methodology again. Experimental details for each of these procedures will be described below.

Device description

As the LM124 is an operational amplifier, this type of device is commonly configured in different electrical bias conditions according to the actual application needs. The device under test was the LM124 bipolar operational amplifier which consisted of four identical and independent amplifiers packaged in a single device. The schematic of the sample with its internal transistors, resistors and capacitors had previously been detailed in section 5.2.1. More importantly for this chapter, Figure 6.1 illustrates some of the possible operation modes of a typical operational amplifier.

Figure 6.1 Some possible configurations of an operational amplifier operating in: (a) Open-loop, (b) Inverting and (c) Non-inverting modes [1]

The sample was originally packaged in dual-in-line plastic molding compound. Laser pre-decapsulation was employed to remove the molding compound and subsequent milling and polishing steps were conducted on the backside of the silicon die in order to allow for laser optical access during pulsed laser SET tests. An example of such a prepared sample had previously been shown in section 5.2.1.

Laser SEE test procedure

Next, we set up the LM124 by connecting external power supplies (± 5 V) and providing the desired input signal (100 mV or 200 mV) to the device. During pulsed laser SEE test, the device was operated in two discrete modes and these biasing conditions are shown in Figure 6.2. As a consequence of these biasing conditions, the normal operating output voltage of the device was at a static 100 mV and 3.8 V in the voltage follower (VF) and comparator (COM) modes, respectively.

Figure 6.2 Configuration and biasing conditions of LM124 in (a) comparator and (b) voltage follower modes during pulsed laser SEE tests. $R1 = R2 = R3 = 220 \text{ k}\Omega$.

The device was first configured in voltage follower mode and its SET sensitivity was assessed using the pulsed laser SEE scan methodology. The device was then configured in comparator mode and its sensitivity assessed via the same method. In both cases, the output of the device was connected to the auxiliary channel of the microscope system in order to capture SET occurrences and to mark these SET-sensitive positions on the SET mapping image. For this evaluation, the CNES pulsed laser setup with a wavelength of 1064 nm and 7.5 ps pulse width was utilized. Irradiation was performed through the back side of the die with optical pulses being focused onto the DUT via the 20X microscope objective. This objective lens was utilized in order to permit adequate field of view to scan the entire amplifier. Pulsed laser SEE tests were conducted using the proposed laser scan methodology at a pulse repetition rate of 40 kHz to induce SET in the LM124 amplifiers. As the pulsed laser scanned across the sample pixel-by-pixel, energy would be deposited into the sensitive nodes of the integrated circuit, thereby generating transient currents. When the laser energy exceeded the SET threshold of a particular node of the device, a sufficiently large transient current could be generated and would cause a SET to propagate to the device's output. This event would be subsequently denoted as a SET-sensitive position on the SET mapping image. The laser energy was progressively increased and as this proceeded, more nodes would appear sensitive in the SET mapping image and result in an increase in the total SET-sensitive cross-sectional area. Results for this set of study will be presented in the immediate subsection to follow.

6.2.2 Experimental Results and Discussions

This sub-section reports on the results for the study on the influence of device configuration on the SET sensitivity of LM124 operational amplifier. The device was operated in two distinct configurations consisting of the voltage follower and comparator modes. In both cases, the SET sensitivity was evaluated using the proposed pulsed laser scan methodology. Figure 6.3 presents the laser SET mappings for both the voltage follower and comparator modes obtained using various amount of laser energies.

Figure 6.3 Superimposed laser SET mappings showing areas of SET-sensitive regions against device micrograph of LM124 at different laser energies. (a)-(d) shows mappings for device configured in voltage follower mode while (e)-(h) shows the case for comparator mode. Laser energy for each mapping is indicated in terms of percentage while bright red regions represent positive SETs and dull red regions represent negative SETs.

It could be observed that as expected, the area of SET-sensitive regions increased with laser energy when the device was operating in both operation modes. Comparing the SET mappings of the two different modes, it could be seen that the SET-sensitive structures were different. For example, at 4% laser energy, the SET-sensitive structures at the center of the amplifier (as observed in Figure 6.3(b)) when operated in the voltage follower mode was not sensitive when operated in the comparator mode (as observed in Figure 6.3(f)). This could be explained as different transistors were activated during

the two different modes of operation and thus, the SET-sensitivity of the transistors could differ.

Another observation was that the total cross-sectional area of SET-sensitive regions were higher when the device was operated in the voltage follower mode as compared to the comparator mode. This could be evidently observed when comparing Figure 6.3(d) against Figure 6.3(h). The difference in total SET response (in different operating modes) of the entire amplifier was further represented in a SET cross sectional area versus laser energy curve. This SET cross sectional area is represented by normalizing the total SET-sensitive area against the device area at each laser energy. As shown in Figure 6.4, as the laser energy increases, the SET cross sectional area increases until saturation. The curves clearly showed that the SET saturation cross sectional area of the amplifier in voltage follower mode was higher than that in comparator mode. This signified that the device exhibited more sensitive areas in voltage follower mode and subsequent care should be taken by system engineers in assessing the device radiation response in different operating modes.

Figure 6.4 SET cross sectional area versus laser energy curve for LM124 operated in voltage follower and comparator modes. The SET mappings at the top represent the evolution in SET-sensitive area when the device was operated in voltage follower mode at increasing laser energies.

The significance of this study highlighted the need for a large amount of radiation testing to fully qualify a microelectronic device for space application. As the SEE sensitivity of a device changes according to its configuration and bias conditions, the demand for traditional SEE qualification via heavy ion test method would be high. The proposed pulsed laser SEE scan methodology offers the advantage of investigating these configurations or bias dependencies without additional requirement of heavy ion beam time. In addition, this methodology provides additional spatial information to satellite engineers in order to identify the SEE-sensitive structures in different operating conditions.

This finalizes the section reporting on the study which highlights the importance of device configuration on SEE sensitivity. In the next section, the second study involving synergy of optical failure analysis techniques with pulsed laser SEE test methodology will be presented.

6.3 Synergy with Optical Failure Analysis Techniques

This section reports on the study which highlights the synergistic benefits between optical failure analysis techniques and pulsed laser SEE test method, demonstrated via PIC16 microcontroller. Optical failure analysis techniques such as PEM and laser frequency mapping were conducted on the PIC16 microcontroller in order to better understand the origin of SEL. Laser frequency mapping was also conducted to locate the physical location of a single bit in the SRAM functional block of the device and pulsed laser SEE scan methodology was subsequently applied to induce SEU at the bit of interest. Experimental details, results and discussions are elaborated in the following two sub-sections.

6.3.1 Experimental Details

Briefly, the experimental flow for the PIC16 microcontroller began with preparation of the sample for backside optical access. The sample's memory block was first configured with hexadecimal value of 0xFF and then subjected to pulsed laser SEE test to determine its sensitivity to SEE. SEL was first observed at low laser energy and subsequent combination of two optical failure analysis techniques (PEM and laser

frequency mapping) located the SEL-sensitive regions and determined the root cause of this effect. Mitigation was implemented by substituting the external clock signal (originally provided by a function generator) with internal oscillator and this implementation successfully eliminated the occurrence of SEL at low laser energy. Further experiments proceeded at higher laser energy and localization of the memory bits of the SRAM was attained via laser frequency mapping technique. Combined with subsequent pulsed laser irradiation, this enabled triggering of SEU at precise locations of the commercial PIC16 device (a ‘black box’ where users normally do not have information on the structures within the device). Experimental details for each of these procedures will be described below.

Device description

The device under test was a PIC16F688 8-bit microcontroller from Microchip. Microcontrollers have multiple embedded functional blocks which enable multiple variations of configuration possibilities and thus is a popular choice for use in electronic systems. On the flip side, the increased complexities of such devices complicate the interpretation of SEE results and thwart the efforts to identify root causes to the problem. Basic understanding of the device could first be attained from the device’s datasheet with its pinout diagram shown in Figure 6.5(a) and the backside surface of the prepared sample of 14-pin plastic dual-in-line package shown in Figure 6.5(b).

Figure 6.5 (a) Pinout diagram of PIC16 consisting of V_{DD} , V_{SS} and 12 other Input/Output (I/O) pins and (b) Backside-prepared sample of PIC16.

Briefly, the device consisted of one pin for power supply (pin 1 for V_{DD}), one pin for ground (pin 14 for V_{SS}) and 12 pins for configurable I/Os. The clock signal to the device could be externally supplied (up to 20 MHz) or internally sourced (up to 8 MHz). The device’s data memory consisted of 256 bytes of SRAM dedicated as file registers. Other

memory blocks, consisting of Flash and Electrically Erasable Programmable Read-Only Memory (EEPROM), were present in the device but were not targeted during this set of experiments.

Laser SEL test procedure

Pulsed laser SEE tests were conducted using the proposed pulsed laser scan methodology to induce SEE in the PIC16 microcontroller. During the SEL tests, the device was provided with 5 V at the power supply pin by a source-measure unit (SMU) with current compliance of 10 mA and the memory was written with a hexadecimal value of 0xFF. This data was subsequently read and re-directed to the output pin of the device in order to record any occurrences of SEE. An external clock signal at 20 MHz was supplied to the 'clock in' pin of the device by a function generator. In this configuration, the nominal power supply current was around 3.3 mA.

Pulsed laser was scanned across the device's backside surface using a 50X objective lens with one pulse being delivered per pixel of the scanned image. The pulsed laser energy was progressively increased after each complete scan until SEE was observed. Firstly, when a SEL was triggered, the pulsed laser scan was stopped and imaging of the device was made with the infrared camera which was installed on the same system. This technique relies on the infrared reflection of the illuminated sample and strong photon emission spots appear as bright regions which saturate the camera. Secondly, the data of the SRAM was monitored at the output pin of the device to provide more information on the impact of the SEL on the device response. Thirdly, laser frequency mapping was performed on the sample during its latched-up state to investigate the origin of the signal at the output pin of the device. Fourthly, confirmation of the root cause of the SEL was conducted by swapping the source of the clock signal from a function generator to a SMU with current-limiting capabilities. With the root cause of the SEL determined, the fifth and also the last procedure for the pulsed laser SEL test involved mitigation of SEL sensitivity of the device by replacing the external clock signal with the internal oscillator of the device.

Laser SEU test procedure

With the SEL sensitivity of the device mitigated as elaborated in the preceding section, further experiments were carried out to trigger SEU in the SRAM region of the device. During the SEU tests, the device was provided with 3.3 V at the power supply pin and the internal oscillator was utilized to provide a clock signal of 1 MHz to the device. The memory was written with a hexadecimal value of 0xFF. Writing of these data were confined to the bounds of the first 16 addresses (0x20 to 0x2F) with each address being made up of 8 bits. One of the devices' I/O was toggled to provide a constant indication of normal device operation during laser irradiation. After each irradiation, the data (written to the first 16 addresses) were verified by sending an interruption signal which triggered the microcontroller to compare each bit with a reference value (logic '1' in this case). If the stored value had changed, a pulse would be sent to the output pin and to signify the occurrence of a SEU. This output pin was connected to an oscilloscope which recorded and compiled the number of such pulses (equivalent to the number of SEU) for each interrupt cycle.

After SEU had been observed (i.e., the device was verified to be sensitive to SEU), laser frequency mapping was employed to locate the physical location of the bits in the SRAM region. As this technique relied on the periodic activities of the transistors, the SRAM cell was toggled at a periodic frequency of 500 kHz when the clock was at a frequency of 20 MHz. The localization of the bits allowed subsequent pulsed laser irradiation to be conducted at a single point (precise targeting of the bit) to trigger SEU.

With the experimental details covered, the next sub-section will elaborate on the results for this study.

6.3.2 Experimental Results and Discussions

This section reports on the experimental results of the study which highlights the synergistic impact of utilizing optical failure analysis techniques with pulsed laser SEE laser methodology. This is unique to the laser system at NTU as other existing pulsed laser SEE facilities across the globe do not incorporate these optical failure analysis techniques in a single platform. In this section, two sets of experimental results from pulsed laser SEL and pulsed laser SEU tests would be presented. In pulsed laser SEL

test, PEM, laser frequency mapping and pulsed laser were employed to mitigate the SEL sensitivity of the device. In pulsed laser SEU test, laser frequency mapping was employed to pinpoint the physical location of the bit in the SRAM and subsequent pulsed laser irradiation was conducted to induce SEU at the bit. These experiments show the benefits of the setup at NTU to investigate COTS components which are often ‘black-boxes’ where users would have no information on the sensitive structures in the device and thus, causing pulsed laser SEE test results to be difficult to obtain or interpret.

Pulsed laser SEL test results

Pulsed laser scan methodology was conducted on the PIC16 microcontroller to investigate its sensitivity to SEL. Prior to pulsed laser irradiation, the device’s nominal power supply current was around 3.3 mA. Pulsed laser energy was progressively increased and when the device was scanned with a pulsed laser energy of 90 pJ, the power supply current surged and hit the compliance limit of 10 mA enforced by the SMU. Due to the limitation in current drive, the power supply voltage of the device fell to 2.1 V. The high current state could not be removed until a power cycle was conducted and thus, this surge in power supply current indicated the occurrence of SEL. While the device was still in the latched-up state, infrared imaging of the device was conducted. Figure 6.6(a) shows the infrared image with the red arrow pointing to the site of strong photon emission. The image was obtained over a short integration time of 50 ms and this signified that the emission signal was very strong. Also, it should be noted that prior to pulsed laser irradiation and occurrence of SEL, this emission spot was not present. Next, it was observed that the output of the device after latch up showed a signal toggling at 20 MHz (which was previously absent during normal device operation). Laser frequency mapping was subsequently carried out at the clock frequency of 20 MHz and Figure 6.6(b) shows the obtained results with strong 20 MHz signal at the same site of strong photon emission. As the internal oscillator of the device could only operate up to a maximum of 8 MHz, the immediate suspicion of the root cause of the SEL pointed to current sinking from the external function generator which was the only source of this 20 MHz signal.

Figure 6.6 (a) Infrared imaging of PIC16 device with red arrow pointing to the site of strong photon emission and (b) Laser frequency mapping of PIC16 at 20 MHz (also the frequency of the external clock signal). Both images were obtained while the device was still in the latched-up state.

With the root cause of the SEL identified with PEM and laser frequency mapping, further confirmation of the proposition that the device was sinking current from the function generator was attained via the replacement of the function generator with a SMU to deliver the square wave signal of the clock. Pulsed laser irradiation was repeated and the SMU indeed hit the current compliance and thereby confirming that the device was sinking current from the ‘clock in’ I/O. Final mitigation of the device’s sensitivity to SEL was achieved by removing all external clock signals and using the internal oscillator of the device instead. Pulsed laser irradiation was repeated and no SEL was observed. It should be noted that in both cases, the device was designed to allow the provision of clock signal via either an external source or the internal oscillator. Although the use of the internal oscillator limits the clock frequency to a maximum of 8 MHz (compared to 20 MHz from an external source), SEL was mitigated.

Pulsed laser SEU test results

After the device’s sensitivity to SEL had been mitigated, pulsed laser scan methodology was further conducted to investigate the device’s sensitivity to SEU. The device’s memory was initially written with a hexadecimal value of 0xFF at the first 16 addresses. Pulsed laser scan methodology was conducted across the device’s surface and after SEU had been confirmed, laser frequency mapping was conducted to pinpoint the

physical locations of the bits in the SRAM region. Figure 6.7(a) shows the localization of the bits of the 0x20 address in the SRAM via laser frequency mapping using the 50X objective lens. Eight distinct clusters of bright spots could be observed in the figure and was postulated to correspond to the eight pairs of cross-coupled inverters of a SRAM cell. With this spatial information of bit 0 of the 0x20 address, pulsed laser was operated in the single point mode and irradiated at the bit location.

Figure 6.7 (a) Laser frequency mapping of PIC16 at 500 kHz which enabled the localization of the 8 bits (bit 0 circled in red) of 0x20 address in the SRAM and (b) Oscilloscope waveform of SEU induced by pulsed laser (480 pJ at 1 kHz repetition rate) at bit 0 of 0x20. Oscilloscope diagram's vertical scale is 2 V/div and horizontal scale is 5 ms/div.

Figure 6.7(b) shows the SEU induced at bit 0 with a pulsed laser energy of 480 pJ and a repetition rate of 1 kHz. The induced SEU followed a periodic signal repeating at 1 kHz with several missing spikes. These missing spikes could be explained by the period of dead time in the program of the microcontroller where SEU cannot be detected. As the clock signal was not fully synchronized with the pulsed laser for this experiment, it was possible that some laser pulses will arrive at the device during this dead time and thus, accounting for the missing spikes. Nevertheless, the conclusion for this set of experiments was not affected.

In this set of experiment, PEM, laser frequency mapping and pulsed laser were used in a single platform to induce SEL and also to mitigate SEL sensitivity in the PIC16 device. Furthermore, laser frequency mapping was utilized to identify the bit locations in the SRAM and subsequent single point pulsed laser irradiation was conducted at selected bit location in order to induce SEU. These results demonstrate the advantage of the pulsed laser SEE scanning microscope system at NTU which coupled optical failure

analysis capabilities in a single platform. This is unique from the other existing pulsed laser SEE setups across the globe which do not have such optical failure analysis capabilities.

This finalizes the section reporting on the study which highlights the synergistic effect between optical failure analysis techniques and pulsed laser SEE test methodology. In the next section, the third study involving the influence of test board complexity on SEE qualification process will be presented.

6.4 Test Board Complexity on SEE Qualification Process

This section reports on the study which presents the influence of test board complexity on the SEE qualification process, demonstrated via test structure consisting of inverter chains fabricated with 65 nm CMOS process technology. With the industry shift towards smaller satellites, more corporations and small nation entities are increasingly involved in the radiation test process. Unlike established space agencies with standardized main boards and daughter boards for radiation test campaigns, these small entities often rely on third-party radiation test service providers to design test boards for radiation test campaigns. These test board designs are often proprietary and thus, in the attempt to conduct pulsed laser tests after heavy ion test campaign, separate test boards often have to be designed.

In this study, heavy ion and pulsed laser tests were conducted on the test structures. SEEs were observed during heavy ion tests but not during pulsed laser tests. Deeper investigations using laser frequency mapping and active oscilloscope probes (lower capacitive impedance) identified the insufficient implementation of on-chip output buffer as the root cause. Following this identification, two new versions of test boards were re-designed in order to reduce the impedance of the copper traces (via reduction in trace width, placement of output pin headers closer to the test structure, use of voltage translators). Although no SEEs were observed during pulsed laser tests, this set of experiments served as a caution that both test boards and electrical instruments could affect SEE test results. This would be very crucial in future correlation studies (a recurring need among other researchers, satellite engineers and executives from small, medium enterprises) between heavy ion and pulsed laser tests.

6.4.1 Experimental Details

Briefly, the experimental flow for the SEE tests on 65 nm chain of inverters involved the use of two different methods of test: (1) Heavy ion tests conducted at the radiation effects facility of TAMU, USA and (2) Pulsed laser SEE tests conducted at NTU. SETs and SEUs were observed during the heavy ion tests but not during pulsed laser SEE tests. Primary suspicion for this difference points to the different test boards used for both tests as the ones used during the heavy ion tests were proprietarily designed by the radiation test provider and could not be easily replicated for subsequent pulsed laser tests. Pulsed laser tests enabled deeper investigation and it was later discovered that the insufficient implementation of on-chip output buffers might have led to issues of impedance mismatching when connection was made between test boards and electrical instruments. Experimental details for both test methods will be described below.

Device description

The test structure consisted of chains of inverters fabricated with GlobalFoundries 65 nm low power bulk CMOS process technology. The chains of inverters varied according to lengths of 1, 100 and 600 inverters and within each chain, there were two outputs. Figure 6.8 illustrates the schematic of an inverter chain with one output (OUTx) located at the end of the chain and another output (OUTy) located at the end of the latch after the chain. These two outputs allow the monitoring of SET and SEU respectively. In addition, for each chain, transistors were designed in two different sizes while maintaining the same gate lengths.

Figure 6.8 Schematic of inverter chain with two outputs, OUTx and OUTy. The length of the various chains of inverters differed between 1, 100 and 600 inverters.

Under normal operation, the value or state of output X of an even-numbered chain of inverters should follow the device's input. In the event of a radiation ion strike, electron-hole pairs would be generated in the active volume of the transistors and subsequent charge collection would result in a transient current. This induces a change in voltage or SET being observed at output X. In the event that the SET satisfies the latching conditions (according to the clock signal), a SEU would be observed at output Y.

In the case of heavy ion test, the sample was intentionally packaged without any front-side encapsulation in order to allow the heavy ion beam to penetrate the device via the front-side of the silicon die. This was to ensure that the LET of the heavy ions will remain relatively high as there was no need to penetrate the thick silicon substrate (typically 200 μm and above) through the backside of the die. Figure 6.9 shows the image of the sample used during heavy ion tests.

Figure 6.9 Test structure consisting of chain of inverters fabricated with 65 nm CMOS process technology for heavy ion SEE tests. The silicon die was packaged without any front-side encapsulation to allow direct heavy ion irradiation via the top-side of the sample.

In the case of pulsed laser test, the sample was packaged with front-side encapsulation to allow laser irradiation through the backside of the die. The sample was subsequently milled and polished on the backside of the die and Figure 6.10 shows the sample before and after preparation for pulsed laser SEE tests. The polished backside surface allowed laser to deposit energy into the active volume of the device without any obstruction from the metallization on the front-side of the die.

Figure 6.10 Test structure consisting of chain of inverters fabricated with 65 nm CMOS process technology (a) before and (b) after backside sample preparation for pulsed laser SEE tests.

Heavy ion test procedure

Heavy ion test was conducted at the radiation test facility situated in TAMU, USA, with the help from Radiation Test Solutions Inc. in providing the logistics support for beam time arrangement, instrument delivery and design support for test boards. Details of the facility had already been covered in section 3.1 and to briefly highlight, the heavy ion test campaign involved several months of planning and waiting before finally being allocated with six hours of beam time. Heavy ion tests were conducted via irradiation in air with fluxes experienced during the test ranging from 2×10^4 to 1×10^5 particles/cm²/s while fluences were from 2×10^6 to 1×10^7 ions/cm². Table 6.1 shows the types of ions used during the heavy ion test.

Table 6.1 Types of ions used during heavy ion test conducted at TAMU. USA.

Ion Type	Effective LET (MeVcm ² /mg)	Effective range (μm)
Cu	19.6	135.5
Cu	29.8	86.6
Cu	39.9	64.7
Xe	51.5	119.7
Pr	58.3	117.5
Pr	69.6	98.5

Figure 6.11 shows the general configuration of the beamline at TAMU's cyclotron while Figure 6.12 shows the DUT mounted onto the test board designed by Radiation Test Solutions Inc. During the heavy ion test campaign, the device was provided with power supply of 0.9 V and a clock signal of 1 MHz for the latch situated after the end of each inverter chain. The inputs of the chains of inverters were varied during the test.

Figure 6.11 TAMU's heavy ion test showing: (a) Beamline apparatus, (b) End of beamline and test board containing DUT, (c) Cables connecting DUT to computer controls in another shielded room.

Figure 6.12 DUT mounted on the test board which was proprietarily designed by the radiation test provider. The heavy ion beamline was aligned to the DUT.

The test board used in the heavy ion experiments was proprietarily designed by Radiation Test Solutions Inc. Voltage translators were soldered close to the DUT in order to act as buffers for the input and output signals. A FPGA was employed to provide the input signals and also to record the outputs of the DUT. The sampling rate of the FPGA was set at 50 MHz and an error was recorded when the device output deviated from the nominal value by 30%.

The entire heavy ion test was limited to a beam time of six hours, including time for set up of equipment, test boards, changing of heavy ion LET and capturing of test data. After setting up of electrical instruments and connections, the normal functionality of the entire experimental setup and SEE monitoring scheme was checked. Next, the heavy ion beam was centered on the die and heavy ion irradiation began. At each heavy ion LET level, the inputs to the inverter chains were first set at a logical state of '0' and the number of SEEs (SETs on output X and SEUs on output Y) were recorded. This was repeated for the case where the inputs to the inverter chains were set at a logical state of '1' before changing to another heavy ion LET level. This process was repeated for the range of heavy ion LET levels shown in Table 6.1. A second sample was then tested to provide verification of results from the first sample. The beam time of six hours was barely sufficient to cover the tests conducted on these samples and thus, any further investigations had to be fulfilled via pulsed laser testing.

Pulsed laser test procedure

Pulsed laser SEE tests were conducted using the proposed pulsed laser scan methodology at a pulse repetition rate of 1 kHz to induce SET or SEU in the chains of inverters. During the pulsed laser tests, conditions were kept similar to the ones used during heavy ion tests (i.e., the chains of inverters were supplied with V_{DD} of 0.9 V while the clock frequency was at 1 MHz and inputs of the inverter chains held at a logical state of '0'). As a consequence of this biasing condition, the normal operating output of the device was at a logical state of '0'. A simple test board (here forth referred as 'invTBsimple') was designed and fabricated to allow connections between electrical instruments (such as SMU, function generator and oscilloscope) and the pins of the packaged device. Figure 6.13 shows this basic version of the test board.

Figure 6.13 Basic version ‘invTBsimple’ of test board for pulsed laser SEE tests on 65 nm chain of inverters. To avoid complications, no additional components were implemented on this version of test board. Copper traces of 0.41 mm were used.

This test board consisted of printed circuit board (PCB) traces which connects the pins of the packaged device to pin headers on the test board. To avoid complications, no other components were implemented on the test board. Pulsed laser SEE scan was conducted in a localized manner through limiting the laser scan area to a single chain of inverter at a time. The outputs of the inverter chain under investigation were connected to an oscilloscope for observance and capture of any SET or SEU. Pulsed laser scans were repeated on various inverter chains under different conditions of V_{DD} , clock frequencies and input logical states.

It was re-affirmed after several trials on various chains of inverters of different sizes and bias (V_{DD} , input and clock frequency) conditions that no SET or SEU were observed under pulsed laser SEE tests. In these trials, the suspicion of too-low laser energy to induce SET or SEU was eliminated as laser energy was progressively incremented until the chains of inverters became non-functional. This led to the upper energy limit of the pulsed laser test on this device and also the discovery of laser-induced damages which will be covered in more details in the last study of this chapter. The failure to observe any SET or SEU was cross-verified with pulsed laser tests using both the CNES and NTU pulsed laser setups.

With previous experience and success in inducing SEU in test structures consisting chain of 100 flip flops fabricated with GlobalFoundries 65 nm low power bulk CMOS process technology, this failure to observe SEE from pulsed laser tests on the chains of inverters was surprising. Immediate attention was paid towards verifying the fabrication process variation and circuit design of the test structures in order to look for clues which could potentially impede the frequency response of the device. It was suspected that fast SETs in 65 nm technology node might not have successfully propagated to the outputs of the device and thus, resulting in the failure to capture these events during pulsed laser SEE tests.

Deeper investigation of the device performance was conducted via trials involving the use of active oscilloscope probes (Lecroy D600A-AT) for lower capacitive impedance (as compared to high-impedance passive oscilloscope probes) and use of laser frequency mapping in order to quantify the high frequency response of the chain of inverters. Several V_{DD} , input and clock frequencies conditions were tested. Laser frequency mapping was successfully conducted at frequencies of up to 50 MHz (which is the limit of the function generator available at the point of test). In any case, laser frequency mapping proved that the internal structures of the chain of inverters were capable of operating at 50 MHz but on the output of the device, the signal integrity of the device dropped after 1 MHz. This prompted further investigations and was later verified that the output buffers of the chain of inverters were not sufficiently implemented. This would cause the issue of impedance mismatch between the output of the device and external electrical instruments such as the oscilloscope.

With this suspected root cause in mind, several versions of customized test boards were designed in the attempt to capture SET or SEU. In the first improved version (hence forth referred as 'invTBthinc'), the test board was designed with thinner copper PCB traces (0.17 mm) and pin headers were placed closer to the sample. Figure 6.14(a) shows the first improved version of test board. The thinner and closely-placed copper traces and pin headers to the sample were expected to reduce resistive impedance and thus, improve the propagation of fast transient signals to the pin headers and subsequently to the oscilloscope.

Figure 6.14 Two improved versions of test boards for pulsed laser SEE tests on 65 nm chain of inverters: (a) Version ‘invTBthinc’ which consisted of thin copper traces (0.17 mm) and pin headers placed close to the sample and (b) Version ‘invTBvtrans’ which consisted of voltage translators connected via thin copper traces (0.17 mm) and placed close to the sample.

In the second improved version (hence forth referred as ‘invTBvtrans’), on top of the thin copper PCB traces, the test board was designed with voltage translators (same model as those used during heavy ion tests) placed close to the sample. Figure 6.14(b) shows the second improved version of the test board. The placement of voltage translators close to the sample were expected to act as input and output buffers to provide sufficient current drive and impedance matching from the pins of the packaged device to external electrical instruments.

Pulsed laser SEE scan methodology was repeated on new samples which were mounted on these two improved versions of the test boards. Pulsed laser SEE scan was conducted in a localized manner through limiting the laser scan area to a single chain of inverter at a time. The outputs of the inverter chain under investigation were connected to an oscilloscope for observance and capture of any SET or SEU. This was repeated on various inverter chains under different conditions of V_{DD} , clock frequencies and input logical states.

6.4.2 Experimental Results and Discussions

This section reports on the results from the use of two different methods for SEE qualification: (1) Heavy ion test and (2) Pulsed laser SEE test. SEEs were observed during the heavy ion tests but not during pulsed laser SEE tests. Primary suspicion for this disparity pointed to the different test boards used for both tests and was further complicated by the insufficient implementation of on-chip output buffers in the test structure design.

6.4.2.1 Heavy Ion Test Results

Figure 6.15 presents the heavy ion cross-section versus LET curves derived from normalizing the total number of SEE errors by the fluence level at each LET level for two pristine samples (Samples 3 and 5). Each set of data represented the total number of errors of all the different designs of inverter chains in the test structure. During the heavy ion test, SET and SEU had been successfully induced and no permanent damage such as SEL was observed.

It can be observed from Figure 6.15 that results from both samples were consistent. With an input equivalent to a logical state of '1', the SET threshold LET (indicated by LET value where blue down arrow occurred) was found to be between 20-30 MeVcm²/mg while the SEU threshold LET (LET value where purple down arrow occurred) was 30-40 MeVcm²/mg. In comparison, when the input was changed to logical state of '0', the SET threshold LET (LET value where red down arrow occurred) was found to be higher (above 30 MeVcm²/mg) while the SEU threshold LET (LET value where green down arrow occurred) was below 40 MeVcm²/mg. From the comparison of SET and SEU threshold LET, although it may appear that the device was more sensitive when supplied with an input logical state of '1', this set of comparisons were insufficient and deeper analysis was needed to draw any meaningful conclusions.

Figure 6.15 Heavy ion SEE cross-section versus LET curve of (a) Sample 3 and (b) Sample 5. In the figure legend, I1 and I0 signified the logical input state ('1' and '0' respectively) of the chains while X and Y signified the errors observed at the X and Y outputs of the inverter chain, respectively. Down arrow represented the lowest LET tested with no observable errors under each bias condition. Blue curves act solely as guidance to the eye and do not represent the actual Weibull fits.

Deeper comparisons were done by assessing the SEE saturation cross sectional area of the device to SET and SEU. From Figure 6.15, the lowest saturation cross-section was found to be obtained from the SET errors when the input was equivalent to a logical state of '0' while the highest saturation cross-section was found to be obtained from the SET errors when the input was equivalent to a logical state of '1'. Although this comparison seemed to suggest that the device was more sensitive when supplied with an input logical state of '1', it should be noted also that the saturation cross-section for SEU errors suggested otherwise. When comparing SEU saturation cross-section, it was found that the device was more sensitive when supplied with an input logical state of '0' instead. The reason for this higher SEU (than SET) saturation cross-section remained unclear but pulsed laser tests could provide deeper and repeated investigations. The occurrence of SEU depends on the amplitude and duration of the preceding SET

within the latching window. These factors could potentially affect the eventual number of SEUs that was being captured.

Comparisons were also drawn between inverter chains of different transistor sizes and results are shown in Table 6.2. When the input was at a logical state of '0', it was found that more SEU were observed on inverter chains of larger transistor size. The same trend was observed in both chain of 100 and 600 inverters. Since heavy ion test involved random bombardment of ions across the field of view of the beam, we were unable to accurately conclude if the obtained results were a consequence of larger sensitive volume of the larger transistors. Pulsed laser testing could provide more information by scanning the device surface, determining the sensitive area pixel by pixel and finally computing the total sensitive area.

Table 6.2 Number of SEU errors in chain of inverters consisting of large and small inverter sizes when input was at logical '0'.

Ion Type	Effective LET (MeVcm ² /mg)	Number of SEU errors			
		Chain of 600 inverters		Chain of 100 inverters	
		Large inverters	Small inverters	Large inverters	Small inverters
Xe	51.5	31	18	60	19
Pr	58.3	44	27	44	24

6.4.2.2 Pulsed Laser Test Results

Pulsed laser SEE tests were first conducted using the 'invTBsimple' test board. This was the simplest version (out of the 3 versions used in this set of pulsed laser SEE experiments) which served its basic function of fanning out leads of the packaged device to pin headers for connection to external electrical instruments. Table 6.3 summarizes the various test results obtained using the 'invTBsimple' test board under different test conditions and verified via two independent pulsed laser setups at CNES and NTU. In all cases summarized in Table 6.3, no SET or SEU had been observed. For each test, the chain under investigation was provided with the desired bias conditions and pulsed laser scan was conducted only on the physical area of the specific

chain of interest. The outputs to the chain were monitored and pulsed laser energy was progressively increased until changes in the outputs were observed. These changes were recorded and the maximum pulsed laser energy used was also noted down.

Table 6.3 Summary of various tests conducted using the ‘invTBsimple’ test board under different test conditions and verified via two independent pulsed laser setups at CNES (laser energy shown in %) and NTU (laser energy shown in nJ).

Test Serial No.	Chain length	Transistor Size/Area	V _{DD} (V)	Input state	Clock (MHz)	Max Laser Energy (% or nJ)	Laser repetition rate (kHz)	Monitored Outputs
1	100	Medium	0.9	0	1	30%	1	XΔ 0→1 YΔ 1→0
2			No bias			46%		No outputs
3		Small	1.2	0	1	34%	1	XΔ 0→1 YΔ 1→0
4						1.09 nJ		YΔ 1→0
5	600	Medium	0.9	1	1	42%	1	YΔ 0→1
6			1.2	1	0.01	38%		XΔ 1→0 YΔ 0→1
7			1.2	0	1	2.60 nJ		YΔ 1→0
8		Small	0.9	1	1	2.30 nJ	1	No SEE, no damage
9			1.2	0	0.1	2.51 nJ	10	XΔ 0→1 YΔ 1→0
10			1.2	1	0.1	3.18 nJ	0.1	YΔ 0→1
11	1	Medium	1.2	0	1	1.44 nJ	1	XΔ 1.2V→0.7V
12		Large				2.99 nJ		XΔ 1.2V→0.6V

For example, test serial number 1 of Table 6.3 presents the case of pulsed laser SEE test on a chain of 100 inverters, biased with V_{DD} of 0.9 V, input logical state of ‘0’ and 1 MHz clock. At a laser repetition rate of 1 kHz, when the laser energy reaches 30% of the CNES laser setup, the X (and Y outputs) of the inverter chain changed from a logical state of ‘0’ to ‘1’ (and ‘1’ to ‘0’), as shown in Figure 6.16. In all cases summarized in Table 6.3, the change in X and Y outputs was similar to that of Figure 6.16 which do not recover after the event and thus, do not qualify as a SET or SEU. Instead, it was a permanent change in device response which did not recover even after power cycling of the device. From Table 6.3, test serial numbers 1 and 2 compared the cases whereby one was conducted with the device being biased while the other was not. In fact, test serial numbers 2 and 5 were conducted back-to-back on the same day and the laser energy needed to trigger a permanent change in output was very similar (42% while device was biased and 46% while device was unbiased). This gave a strong warning

that the permanent alteration to the device could be related to the effect of the laser and not that of the electric field of the device.

Next, test serial numbers 3 and 4 were conducted under the same bias conditions but using two independent pulsed laser setups located at CNES and NTU. In both locations, SET or SEU was not observed and instead, permanent alteration to the device was induced after pulsed laser SEE tests. The remaining of the test cases in Table 6.3 present results where the V_{DD} , input logical state, clock frequencies and laser repetition rates were modified and tested using the pulsed laser scan methodology. The possibility of a too-low laser energy to induce SET or SEU was eliminated as laser energy was progressively incremented until the chains of inverters became non-functional (i.e., the upper energy limit of the pulsed laser test on this device).

Figure 6.16 Oscilloscope diagram of the change in X (pink trace) and Y (green trace) outputs of the chain of inverter during pulsed laser SEE test. Horizontal axis was 1 ms/div while vertical axis was 500 mV/div for both traces. Laser repetition rate was 1 kHz and laser energy was 30% using the CNES pulsed laser setup.

Following the inability of both pulsed laser setups at CNES and NTU to trigger SET and SEU in the chains of inverters, a series of electrical tests were conducted to investigate if the chains of inverters were capable of allowing the propagation of fast transients and to evaluate its frequency response. Figure 6.17 shows the test results obtained using active oscilloscope probes under input signals of various frequencies. It

was found that the frequency response of the device started to degrade after 1 MHz (rounding of signal edges) while using passive probe and thus, pointing to possible issues of capacitive loading.

Figure 6.17 Frequency response of chain of 100 inverters obtained from square-wave input signals of 1 kHz, 1 MHz and 10 MHz. Comparison between output signals obtained via active and passive probes indicate that frequency response of the chain degrades after 1 MHz using the passive probe, pointing to possible issues of capacitive loading.

Figure 6.18 presents the results obtained from laser frequency mapping conducted on a chain of 100 inverters at 50 MHz. It was evident that the internal structures of the chain of inverters were capable of operating at 50 MHz but at the output of the device, the signal integrity of the device drops after 1 MHz. This prompted further investigations and was later verified that the output buffers of the chain of inverters were not sufficiently implemented. This would cause issues of impedance mismatch between the output of the device and external electrical instruments such as the oscilloscope.

Figure 6.18 Laser frequency mapping obtained from chain of 100 inverters with input signal of 50 MHz. Bright spots showed that the inverters were indeed capable of operating at 50 MHz.

With this suspected root cause in mind, pulsed laser SEE scan methodology was repeated on new samples mounted on the ‘invTBsimple’ test board but the passive oscilloscope probes were replaced with active ones. Pulsed laser SEE tests coupled with the use of active oscilloscope probes were conducted using both the CNES and NTU setup and in both cases, no SET or SEU were observed.

In addition, pulsed laser SEE scan methodology was repeated on new samples mounted on two improved versions (Version ‘invTBthinc’ and Version ‘invTBvtrans’) of the test boards using high-impedance passive oscilloscope probes. Figure 6.19 shows the improvement in output frequency response of the chain of inverters on the improved version of the test board. Despite these improvements, no SET or SEU were observed during pulsed laser SEE tests.

Figure 6.19 Frequency response obtained from square-wave input signals of 1 MHz, 10 MHz, 20 MHz and 50 MHz. Clear improvement in output frequency response could be seen with the use of the improved test board (version 'invTBvtrans').

The root cause in the failure to observe SET or SEU during pulsed laser tests was postulated to be fundamentally due to the insufficient implementation of on-chip output buffers for the test structure (consisting of chains of inverters). It should however be noted that despite these insufficiencies, SET and SEU were still observed during heavy ion tests which utilized intricate test boards designed proprietarily by experienced radiation test experts. Although full replication of the test board (which involved voltage translators and FPGA implementation) used during heavy ion test was impossible, efforts were undertaken to mimic as closely to the heavy ion case via several improved versions of the test board with thinner PCB traces and placement of voltage translators close to the device in order to reduce resistive impedance. The use of active oscilloscope probes did not enable the observance of SET or SEU too. From this set of experiments, the different test boards used during heavy ion test enabled the observance of SET and SEU as opposed to the non-observance during pulsed laser tests.

This finalizes the section reporting on the study which highlights the influence of test board complexity on SEE qualification process. In the next section, the fourth and last study involving complications of laser-induced damage during pulsed laser SEE tests will be presented.

6.5 Laser-induced Damage in Advanced Microelectronics

This section reports on the study which investigates the laser-induced damages by 1064 nm pulsed laser, demonstrated via test structures consisting of inverter chains fabricated with 65 nm CMOS process technology. Pulsed laser SEE scan methodology was applied on the test structures under typical laser energies used during pulsed laser SEE tests. Laser-induced damages were observed and verified using two independent pulsed laser SEE setups in CNES and NTU. Subsequently, optical failure analysis techniques were employed to localize the damaged structures and physical failure analysis was carried out to characterize the fault. It was found that nickel diffusion was the root cause of the laser-induced damage under 1064 nm pulsed laser.

6.5.1 Experimental Details

Briefly, the experimental flow for the study of laser-induced damage began with preparation of the sample (consisting chain of inverters) for backside optical access. The inverter chain of interest was then scanned with the pulsed laser while the chain's outputs were simultaneously monitored. Pulsed laser energy was progressively increased until permanent failure of the chain of inverters was observed. Fault localization in the sample was further attained from PEM which revealed locations of hot spots. Next, laser frequency mapping was employed to verify the propagation of signals in the chain of inverters and its site of termination. Laser frequency probing was conducted to investigate the signal at each inverter and results showed the disappearance of signal after the failure site.

The laser-induced damage was observed to be repeatable and verified to be replicable with two independent pulsed laser SEE systems at CNES and NTU. Physical failure analysis was conducted at the failure site via the use of FIB (for cross-sectioning) and SEM (for imaging). TEM was employed to obtain images of the damage in higher resolution and then coupled with EDS elemental analysis to study the diffusion species leading to the damage of the chain of inverters.

Device description and stress/ageing conditions

The test structure consisted of chains of inverters fabricated with GlobalFoundries 65 nm low power bulk CMOS process technology which had been previously covered in section 6.4.1 (or Figure 6.8). The test structure was packaged with front-side encapsulation and was subsequently milled and polished on the backside of the silicon die in order to allow for laser optical access during pulsed laser SEU tests. Image of a prepared sample had previously been shown in Figure 6.10.

Laser SEE test procedure

Pulsed laser SEE tests were conducted using the proposed pulsed laser scan methodology at a pulse repetition rate of 1 kHz to induce SET or SEU in the chains of inverters. During the pulsed laser tests, the chains of inverters were supplied with V_{DD} of 1.2 V while the clock frequency was at 1 MHz and inputs of the inverter chains held at a logical state of '0'. As a consequence of this biasing condition, the normal operating output of the device was at a logical state of '0'. Pulsed laser SEE scan was conducted in a localized manner through limiting the laser scan area to a single chain of inverter at a time. The outputs of the inverter chain under investigation were connected to an oscilloscope for observance and capture of any SET or SEU.

6.5.2 Experimental Results and Discussions

This section reports on the failure analysis of the damage induced on test structure containing chain of inverters during pulsed laser SEE tests. The damage was found to be repeatable using two independent pulsed laser setup at CNES and NTU.

Optical Failure Analysis

On the failed chain of inverters, PEM was conducted using the Hamamatsu TriPHEMOS system at 50X objective lens and 180 seconds of integration. Figure 6.20(a) presents the emission hot spots obtained from the InGaAs camera superimposed with the device micrograph of a chain of 100 inverters while Figure 6.20(b) presents the overlay of device layout with the previously pulsed laser scanned area. The strong photon emission spots within the previously laser scanned area aided in localizing the site of damage and also gave an indication that the damage was related to the pulsed laser scan.

Figure 6.20 Photon emission image (a) superimposed with device micrograph and (b) overlaid with design layout and laser scan area (indicated by yellow box). Results show photon emission hot spots within previously pulsed laser scanned area.

Next, laser frequency mapping was conducted to ascertain the propagation of signal and termination site in the chain of inverters. This was conducted using the Hamamatsu TriPHEMOS system and through “locking” of the system’s spectrum analyzer to the desired frequency, this technique enabled tracking of the frequency of the signal propagating in the device.

In this set of experiment, an AC electrical signal of 200 kHz was being delivered to the inputs of the failed chain and an adjacent fully-functional chain. Figure 6.21 presents the results for this set of experiments. For the adjacent fully-functional chain, we could see that the signal propagates through the entire chain, as shown by the vertically aligned bright spots spanning across both Figure 6.21(b) and (c). However, for the damaged chain which emitted the photon emission hot spot, we could see that the signal terminates (halfway through Figure 6.21) in the area previously irradiated by the pulsed laser. This finding reinforced our hypothesis that the pulsed laser had possibly induced damage in the scanned area and prevented the propagation of signal beyond this region.

Figure 6.21 Laser frequency mapping showing: (a) Device Micrograph, (b) amplitude and (c) phase images. Results show that the signal stopped propagating after the site of hot spot identified in the previous photon emission study.

Figure 6.22(a) shows the magnified version of the laser frequency mapping's amplitude superimposed with the device micrograph and layout. The red spot indicated the highest laser frequency mapping's amplitude and the arrows point to the respective inverters where laser frequency probing was subsequently carried out.

Figure 6.22 (a) Laser frequency mapping's amplitude image superimposed with device micrograph and layout. Various points (P1 to P4) indicated the various inverters where subsequent laser frequency probing was carried out and (b) Laser frequency probing waveforms at respective probing points of inverters. A clear edge was observed in the waveform obtained from the initial probing at P1. At P2, an unexpected phase of the signal was observed and subsequently at P3, the edge sharpness of the signal dropped off. Final verification was done at P4 whereby no signal was able to propagate to the chain's output.

Figure 6.22(b) shows the various waveforms obtained when laser frequency probing was conducted on the individual inverters. The direction of signal propagation in the inverter chain was from the top to bottom of the image and thus, at P1, we could see that the initial waveform had a clear and defined edge. As we probed at P2, the signal revealed an unexpected change in phase and thereafter at P3, the signal dropped off in edge sharpness. Ultimately, the signal failed to propagate to P4 and this explains the unexpected voltage level observed at the output of the chain after pulsed laser SEE test.

Physical Failure Analysis

The pulsed laser scan was repeated on several other inverter chains and laser-induced damages were consistently observed. Moreover, this was replicated using the laser system at NTU and in order to gain a deeper understanding of the damage, fault localization was conducted to identify the location for subsequent FIB cross-sectional cut. Figure 6.23 presents the photon emission micrograph taken after pulsed laser

irradiation of 1.44 nJ and 2.60 nJ. At 2.60 nJ of laser energy, the OUTx terminal of the device flipped from a logical state of '0' to '1'. However, power cycling or change in the input states did not manage to restore the device back to original functionality. Also in Figure 6.23, the overlay of device layout onto the micrograph allowed the identification of hot spots occurring on the V_{DD} rail of the inverter chain. This overlay also allowed the localization of hot spots at the 17th, 19th and 20th inverter of the chain.

Figure 6.23 Photon emission micrograph, with overlay of device layout, taken after pulsed laser irradiation at: (a) 1.44 nJ and (b) 2.60 nJ using the NTU pulsed laser SEE setup. Images show abnormal hot spot at the V_{DD} rail of the inverter chain, results which are consistent with those induced by CNES pulsed laser SEE setup.

With this localization of the defect site, FIB cross-sectional cuts were subsequently carried out. Figure 6.24(a) shows the device layout and the location of the two FIB cross-sectional cuts (A-A' and B-B') while Figure 6.24(b) shows the SEM images taken at these two locations. It can be observed that there was an abnormal extension of the suspected silicide layer (indicated by yellow arrows) at A-A', as compared to B-B'.

Figure 6.24 (a) Device layout of the PMOS transistor and V_{DD} rail of the inverter chain and (b) SEM imaging after progressive FIB cross-sectional cuts at two locations (A-A' and B-B') of the 17th inverter. Yellow arrows indicate abnormal extension of the suspected silicide layer at FIB cut of A-A', as compared to B-B'.

A high resolution SEM image of this A-A' cut at the PMOS of the 17th inverter is presented in Figure 6.25(a) and the extension of the suspected silicide layer towards the gate terminal can be clearly observed. Another FIB cross-sectional cut was made at the 19th inverter and Figure 6.25 (b) shows that this extension was consistent.

Figure 6.25 High resolution SEM images showing: (a) PMOS of the 17th inverter and (b) PMOS of the 19th inverter. Abnormal diffusion of the suspected silicide layer was observed in both inverters. Yellow arrows indicate abnormal diffusion of the suspected silicide layer towards the gate terminal.

After the localization of the defect site in the 19th inverter, TEM samples were prepared and EDS mapping was performed to confirm the suspicion of silicide diffusion. Figure 6.26 presents the TEM images and EDS elemental mappings centered around the two gate terminals of the 19th inverter. With reference to the TEM images, it can be clearly observed that the dark layer had extended under both gates. Subsequently, EDS elemental mappings confirmed that these dark layers were nickel diffusion.

Figure 6.26 TEM images and EDS elemental mappings centered on (a) left gate terminal of Figure 6.25(b) and (b) right gate of Figure 6.25(b). Green, red and blue traces were EDS elemental mappings of Nickel, Copper and Tungsten respectively. Nickel diffusion was identified to be the root cause of laser-induced damages in the test structure.

From the TEM images and EDS elemental mappings presented above, diffusion of nickel in the silicide layer towards the gate terminals was confirmed. The expanse of diffusion indicated that potential shorts between the drain-gate, source-gate, or source-drain-gate terminals could have been induced. As the test structure consists of an even-numbered chain of inverters, the OUTx terminal of the irradiated chain was originally expected to mimic the logical state of the input signal. In consideration of the electrical characteristic of the induced damage (whereby the OUTx terminals were stuck at a logical state of '1'), several failure paths could be proposed. In the case where the induced damage occurred at the PMOS of an odd-numbered inverter, a short between the gate (input of this stage of inverter) and the source (V_{DD}) would cause the NMOS to be permanently 'ON'. This would cause the test structure's OUTx terminal to be stuck at a logical state of '1'. In the case where the induced damage occurred at the PMOS of an even-numbered inverter, a short between the drain (input to the next stage of inverter) and source (V_{DD}) would cause the test structure's OUTx terminal to be stuck at a logical state of '1'. Lastly, in the case where the drain is shorted to the gate terminal, the phase of the test structure's OUTx terminal would be inverted. It should be noted that these paths of failure were probable and such electrical characteristics were indeed observed during the series of experiments which were conducted. Deeper investigations (via single-point pulsed laser irradiation) could limit the induced damage to a single inverter (be it odd or even) and potentially pin down the specific failure paths responsible for the observed electrical characteristic. Nevertheless, the observance and conclusions drawn from the laser-induced damages in this study remain valid.

Another discussion topic involves the practical relevance of laser energies used in this study. It had already been well known that high laser power would cause material degradation, modification or vaporization. In effect, this ability of the laser had been leveraged to conduct laser ablation of materials [2] using systems which require higher-powered lasers with longer pulse width duration. However, in the study presented in this section, the laser energy used during the experiments was not excessively damaging to the test structure. Using the same laser wavelength, several other pulsed laser SEE test facilities [3, 4] had been reported to utilize higher energies of up to 50 nJ (though it was unclear if these quoted laser energy values were measured at the source or DUT level). This also highlights the current challenge in the pulsed laser test research community in establishing common calibration standards or methods across various

pulsed laser SEE test facilities. With a unified method for specifying the pulsed laser energies across each pulsed laser SEE test facility, the community would gain from the formulation of a region of safe operating laser energies to conduct SEE tests on advanced microelectronic devices.

The last discussion topic for this study involves the role of electric field on the damages induced by laser. In the failure analysis domain, the 1064 nm laser has been commonly used as this wavelength possesses photons with energy above the bandgap of silicon. Thus, the dominant light-material interaction mechanism is electron-hole pair generation (as compared to thermal effects). In contrast, the 1340 nm laser, with photon energy lesser than silicon bandgap, has been commonly used to induce thermal effects in target test structures. In the attempt to separate these effects, pulsed laser SEE tests were conducted without biasing of the device and yet, laser-induced damages were still observed. In the circumstances where electric field is absent, several research groups [5-7] had already validated that pulsed laser is capable of inducing annealing effects on layers of nickel silicide. However, of note, these demonstrations were conducted using pulsed laser with shorter wavelengths (higher photon energy) of less than 355 nm and longer pulse duration (10 to 150 ns) than the pulsed laser (1064 nm and 10 ps) utilized in this study. In addition, these research groups reported that the pulsed laser induced annealing effects which impacted the nickel silicide layer after 0.3 to 0.6 J/cm² of laser fluence. In comparison, a maximum 0.06 J/cm² of laser fluence was utilized during this study and impacts on nickel silicide layer were already evident. Deeper investigations are needed to fully establish the mechanism(s) driving the influence of 1064 nm picosecond pulsed laser on layers of nickel silicide. Nevertheless, this study provided clues on the laser fluence required to induce such impacts and could form the foundation to establish the safe operating area for future pulsed laser SEE tests on advanced microelectronic devices.

6.4 Conclusions

In this chapter, experimental details, results and discussions of the advantages and possible areas of concern of the proposed pulsed laser SEE scan methodology were presented. This was accomplished through application of the methodology on four different case studies which involved: (1) Assessing the effects of device configuration

on SEE sensitivity, (2) Localizing SEE-sensitive regions and applying mitigation schemes, (3) Test board complexity on SEE qualification process and (4) Study on laser-induced damage in advanced microelectronic devices.

In the first study involving the assessment of effects of device configuration on SEE sensitivity, the device (LM124 operational amplifier) was operated in different device configurations (voltage follower and comparator modes) and the sensitivity of the device to SET was evaluated using the pulsed laser scan methodology. It was found that under different device configuration, the structures which were sensitive to SET were also different. This could be explained as specific structures would have been activated under different device configuration and thus, the sensitivity of the node would be dissimilar. In order to compare the sensitivities of the device under different configuration, the total cross-sectional area of SET-sensitive regions was computed and results showed that the voltage follower mode was more prone to SET than the comparator mode. The significance of this study lies in highlighting the need for large amount of heavy testing in order to fully assess a device's sensitivity to SEE under different device configuration or bias conditions. The proposed pulsed laser SEE scan methodology offers the benefit of assessing such dependencies without additional heavy ion beam time requirement and also provides additional spatial information to satellite engineers on the structures responsible of the device's SEE sensitivity.

In the second study involving localization of SEE-sensitive regions and application of mitigation schemes, the device (PIC16 microcontroller) was initially found to be sensitive to SEL at low laser energy. PEM and laser frequency mapping localized the origin of the SEL sensitivity and mitigation was achieved by replacing the external function generator with the internal oscillator of the device. Although this had limited the maximum clock frequency of the device, it enabled the SEL sensitivity of the device to be greatly reduced. This mitigation allowed subsequent investigation of SEU at higher laser energy. This was achieved by locating the bits of the SRAM by laser frequency mapping. These precise locations of the bit are the target for pulsed laser SEU irradiation. The significance of this study lies in highlighting the advantages of the proposed pulsed laser SEE scanning microscope system at NTU which combines pulsed laser SEE tests with optical failure analysis techniques in a single platform. This allowed localization of functional blocks and structures in a commercial device (usually

a ‘black box’ to consumers) and allowed pulsed laser SEE tests to be conducted in an informed and precise manner.

In the third study involving the complications of test board design on SEE qualification process, heavy ion tests were performed at the radiation effects facility in TAMU, USA and pulsed laser tests were performed at both CNES and NTU. Using the test boards proprietarily designed by the radiation test provider, SEUs and SETs were both observed and captured during heavy ion test on test structures consisting of chains of inverters. No SEL or permanent failure of the device was observed throughout the entire heavy ion test. However, during pulsed laser SEE tests, no SET or SEU was observed. This was verified using two independent pulsed laser SEE systems at CNES and NTU. Primary suspicion pointed to the different test boards used for both pulsed laser tests as compared to the ones used during heavy ion. Although efforts (thinner PCB traces and placing voltage translators close to sample) were made to mimic as closely to the heavy ion test boards, no SEUs or SETs were eventually observed. Deeper investigation narrowed down the fundamental cause to the insufficient implementation of on-chip output buffers which might have led to issues of impedance mismatch between the device and external electrical instruments (such as oscilloscope). The significance of this study lies in highlighting the possible limitations of the pulsed laser SEE scan methodology in replicating results obtained from heavy ion tests. Although it was always preferable to use the same test boards for all tests, it may not always be possible. This is especially true for Singapore or other small satellite entities whereby there are no base for standardized main boards and daughter boards to be used in radiation test campaigns; a situation unlike those of established space agencies. Heavy ion test conducted abroad would also require engaging radiation test providers for logistics support. Results from this study also serve as a heavy caution in future correlation studies between heavy ion and pulsed laser test results to consider the impact of test board designs on the final test results.

In the fourth and final study involving the complications of laser-induced damages in advanced microelectronic devices, pulsed laser SEE scan methodology was conducted on test structures consisting of chains of inverters. Pulsed laser parameters were kept to typical SEE test norms and laser energy was progressively increased until permanent failure of the chain of inverters was observed. PEM found the site of strong emission

and laser frequency mapping confirmed the termination site of the signal propagation in the inverter chain. Laser frequency probing was conducted at individual inverters and results showed the disappearance of signal after the failure site. Subsequent physical failure analysis was conducted via FIB and imaging was achieved with both SEM and TEM. The significance of this study lies in highlighting the potential of laser-induced damage in advanced microelectronic devices. This could potentially be worse when objective lenses of high numerical apertures were used to achieve smaller laser spot sizes in order to target smaller device structures of advanced technology nodes. There is a need to establish the safe operating region of the pulsed laser SEE technique in order to avoid unwanted artifacts during pulsed laser SEE tests.

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Chapter 7

Discussion and Future Work

The proposed pulsed laser SEE scan methodology was realized in the pulsed laser SEE scanning microscope system at NTU. Previous chapters described the set-up, benchmarking, characterization, applications, advantages and possible concerns of this proposed methodology. In this chapter, discussions will be made with respect to key outputs from this thesis. The advantages, disadvantages and perspectives of the pulsed laser scan methodology will be discussed. Effects of ageing on test structures and limitations of the pulsed laser SEE technique will be deliberated. Some auxiliary works (temporal advantage of laser scan methodology and limitations of conducting ageing on commercial samples) undertaken during the PhD but not included in the main chapters will also be presented. Outstanding questions from this thesis with respect to inclusion of electrical degradation models to improve SEE error rate predictions and establishment of safe operating area for laser energies to be used during future pulsed laser SEE tests will be presented. These topics present opportunities for interested readers to pursue further investigations and to improve the state of research in the field.

7.1 General Discussion

The proposed pulsed laser SEE scan methodology has been realized through the setting up of the pulsed laser SEE scanning microscope system at NTU. In this thesis, efforts were undertaken to characterize the pulsed laser parameters, benchmark SEE results against existing literatures, study the effects of ageing on SEE response and evaluation of further advantages and limitations of this technique. The following sections discuss some of the implications of this proposed methodology and also highlight some of the outstanding questions which are worth building on for future investigations.

7.1.1 Pulsed laser SEE Scanning Microscope – Advantages, Disadvantages and Perspectives

Unlike existing pulsed laser SEE setups across the globe which utilize stage movement, the proposed pulsed laser SEE scanning microscope relies on the scanning of the laser in order to fulfil the full area scan of the entire die of a microelectronic device. In addition, an external pulsed laser was integrated to a laser scanning microscope equipped with other optical failure analysis and imaging techniques. The following section discusses some of the advantages, disadvantages and perspectives of this proposed methodology.

Advantages

The proposed laser scan methodology aims to improve the stability and repeatability of this technique in order to accurately and precisely target small structures in advanced microelectronic devices. An experiment was set up to briefly investigate this advantage. Figure 7.1 shows the results on the change in laser power as the laser spot was moved across a knife blade according to the knife-edge method.

Figure 7.1 Change in laser power as system's native 1064 nm continuous wave laser was moved in steps of 0.1 μm across the knife edge using: (a) Laser scan method and (b) Stage movement method. Data was collected from a Coherent PM30 power sensor. Larger spread in data was observed for stage movement method (leading to more errors in Gaussian fitting) while Gaussian distribution fits well with experimental data obtained via laser scan method.

From Figure 7.1(a), it can be observed that with the laser scan method, the change in laser power for each increment in laser position follows closely to the Gaussian distribution and thus, the Gaussian fitting was a good match. However, when the experiment was repeated using the movement of the stage (Figure 7.1(b)), there was a wider spread in the change in laser power for each increment in laser position. This reinforces the fine precision and repeatability of the laser scan methodology as compared to mechanical movement of the stage. More experiments to prove this point is part of future works as precise resolution targets or test structures will need to be procured to make a conclusive study. The choice of a pulsed laser source with fully integrated pulse picker allows highly stable pulsed laser energies to be delivered to the microscope system. This is especially important as the critical charge decreases for advanced microelectronic devices and the impact of variation in laser energy during SEE test will be larger. A stable system will thus ensure that results are consistent and reliable.

Secondly, the system at NTU encompasses several capabilities of optical failure analysis and imaging techniques in a single platform. The imaging techniques allow the in-situ navigation and localization of small features in advanced microelectronic devices. More importantly, three other laser sources equipped on the system allows

several optical failure analysis techniques to be conducted. In combination, these techniques fulfil certain degree of functional reverse engineering on the tested device and allow either precise localization of structures to conduct subsequent pulsed laser SEE tests or better understanding on the origin of the induced SEE. This is very important for evaluation of SEE in advanced COTS components which are usually ‘black boxes’ to end users as the physical layout and functional blocks on the silicon die are often proprietary information to the manufacturers. A case study illustrating the advantages of utilizing these techniques in a single platform had already been covered in section 6.3. These techniques, working in tandem, is expected to be a major advantage of this system, especially for investigation of COTS components.

Thirdly, the proposed pulsed laser SEE scan methodology provides additional information as compared to traditional broad beam heavy ion test. Through the deflection scan of the laser beam, precise spatial targeting can be achieved. This allows localized investigation of SEE and precise information on the location of the laser hit. This is not possible with broad beam heavy ion test method which is based on a statistical bombardment of heavy ions in the entire area of the beam. The spatial and timing information of the arrival of the heavy ions on the sample is also unknown to the user. On the contrary, with the synchronization of the pulsed laser trigger, it is possible to control the timing of laser hit on the sample. This is expected to be very useful in studying the effects of timing, clock frequency and irradiation hits on advanced microelectronic devices which are operating at increasingly high frequencies.

Last but not least, the proposed pulsed laser SEE scanning microscope system offers greater ease of use and convenience as compared to particle accelerators. It is a lab bench equipment which is much easier to set up and requires smaller land space. These are very critical advantages for land-constraint Singapore as it provides a quick mean to conduct SEE screening tests on microelectronic devices. Greater ease of use results from the reduced amount of time spent on calibration or alignment of the laser optical path, as the laser source and pulse picker are fully integrated and connections are made via optical fiber.

Disadvantages

A possible limitation of the proposed pulsed laser scan methodology relates to the limited field of view of the scan area when objective lenses of high numerical aperture or magnification are used. As the user move towards investigating smaller feature sizes in advanced microelectronic devices, objective lens with higher numerical aperture has to be utilized and this will limit the scan area. At the current stage, this has not been much of a problem since the test structures investigated are relatively small in die size. However, as technology scales to smaller nodes and integration efforts intensify, larger die size is expected (or in fact, is already the case for FPGA or memory devices) and will pose a limitation in the near future. This issue is also encountered by laser systems which relies on stage movement and is not an exclusive limitation faced by the proposed laser scan methodology. A possible future work is in the area of developing stitching software algorithms to automate the process such that successive scans of the die surface can be combined to form a unified result.

Perspectives

With the apparent benefits of the pulsed laser SEE test method, increased adoption of the technique is highly expected. As more pulsed laser SEE test setups are established across the globe, there will be a greater need for the standardization of laser setup characterization for possible cross-calibration efforts. Multiple methods were utilized for determination of laser spot size and pulse energy as detailed in Table 7.1. Moreover, these collected data can be processed using various methods such as differentiation [1, 2], custom algorithms [3] or error function fitting [4]. To complicate matters further, laser wavelength and pulse width of most setups are different and thus, the required efforts to set up a reasonably good cross-calibration between different laser setups is huge.

Table 7.1 Various methods available for reporting of laser spot size and pulse energy.

Laser spot size data collection methods	Laser spot size definition methods	Laser energy definition methods
1. Knife-edge [5] 2. Beam Profiler [6] 3. Pinhole [7] 4. CMOS imaging [8]	1. Theoretical approximations [9] 2. FWHM [10] 3. $1/e^2$ [11] 4. 10-90% [12]	1. At the laser source 2. Delivered to the device

At the current state, pulsed laser SEE test method is mostly used as a qualitative test method. Although quantitative correlation studies against heavy ion LET had already been carried out for quite some time, the consensus in the community is that this correlation factor changes for each process technology. More experimental results and a larger database of pulsed laser tests are required to establish a reasonable correlation factor for a general class of devices or process technologies. Nevertheless, with the inherent industry shift towards small satellites and large inflow of COTS components to be tested, it is expected that pulsed laser SEE test method will offer a good alternative to small satellite integrators. This is mostly due to the shorter mission duration of small satellites and shorter development cycles which demand a more efficient manner to conduct SEE qualification tests.

Laser but not least, the RSIL equipped on the NTU pulsed laser SEE scanning microscope was not utilized in this thesis. There is great potential in the use of this exceptionally high numerical aperture lens (3.0 for SIL as compared to 0.4 for the 50X lens) which allows incredibly small spot size. It will be very interesting to investigate SEE using this lens and the effects of spot size on advanced microelectronic devices could be studied. This is particularly important when structures are getting smaller than the laser spot size and charge sharing phenomenon is imposing a larger influence on SEE response of advanced microelectronic devices. Also, in using this lens, caution has to be taken into studying the effects of high optical density on inducing possible laser damage in the tested devices.

7.1.2 Effect of Ageing on Chain of Inverters

High voltage and high temperature ageing stress was conducted on 65 nm chain of inverters. Electrical characterization was conducted on the fresh sample and also at intermittent time points throughout the stress duration. Samples were stressed at 2.4 V and 125°C for a maximum duration of 96 hours and significant shift in threshold voltage was observed. Figure 7.2 shows the voltage transfer curves for two representative design of inverters. Characterization was also conducted on other chains of inverters of various lengths and the same trend (left shift in voltage transfer curve) was obtained.

Figure 7.2 Voltage transfer curves of two representative designs of inverters consisting of: (a) Single inverter and (b) Chain of 100 inverters, taken at various time points of up to 96 hours of ageing

It can be observed from Figure 7.2 that as ageing duration increases, there is a left shift in the voltage transfer curve. This is in line with expectation from NBTI stress whereby the threshold voltage of the transistors will be shifted due to the stress conditions. It should also be noted that under such stress conditions, significant changes can be observed within relatively reasonable duration of stress. From the experimental results, it seems that there is an initial big change in threshold voltage from 0 to 10 hours of ageing stress. Thereafter, the rate of shift in threshold voltage slows and saturates. Through the use of test structures, ageing can be accurately enforced on the test structures as the users have precise control on the device biasing. This is in contrast to the case of commercial devices where the users will have limited information on the physical layout and circuits of the devices. Moreover, commercial devices often consist of protection diodes or circuits and this can impede the maximum amount of ageing

stress to be imposed on the device. More illustration of this limitation will be covered in section 7.2.2.

7.1.3 Pulsed Laser and Its Limitations on Advanced Microelectronics

As reported in section 6.5 of this thesis, laser-induced damages on test structures fabricated with 65 nm bulk CMOS process technology were observed. Penzes and co-workers [13] have previously reported on the observation of 1340 nm continuous wave laser invasiveness on 28 nm FDSOI and bulk transistors. As the 1340 nm laser has a photon energy which is above the energy bandgap of the silicon substrate, it is unable to induce electron-hole pairs and thus, majority of its effect is thermally based. Platinum and nickel silicide was found to diffuse vertically within the gate structure. Further simulation studies [14] supported the increase in internal temperature of the gate structure when increasing energies of 1340 nm continuous wave laser pulses were delivered to the device. In another study by Chen and co-workers [15], persistent error was observed in 20 nm phase-locked loop devices after scans were made with 1260 nm pulsed laser. Additional tests were conducted on 28 nm single transistors and it was found that the 1260 nm pulsed laser caused an increase in drain leakage current. In the study, no characterization on the material changes in the structures was conducted but it was suggested that changes in junction doping profile or diffusion of junction contact atoms could be the cause of the damages.

In the studies carried out in this thesis, damages to the 65 nm bulk CMOS transistors were induced by a 1064 nm pulsed laser. The root cause was found to be related to nickel diffusion from the silicide layer. This material continues to be used in advanced microelectronic devices and it remains unclear if the same damages will be induced in future devices. A complete understanding on the mechanism of nickel diffusion induced by the pulsed laser requires a vast amount of investigation and thus, forms part of future work beyond this thesis. Laser damage was observed even when no electrical bias was provided to the device and thus, several studies could be set up to investigate this phenomenon. With the spot size measurements already conducted on the system at NTU, it is possible to calculate the divergence of the laser spot size, measure the laser spot size at different focus positions and investigate the effects of defocusing (or optical fluence) on the laser-induced damage. In addition, the system at NTU is equipped with

a RSIL which offers even smaller spot size. With the laser energy and spot size characterization already conducted on the system, it is possible to set up studies to calculate the optical density and possibly establish a safe operating region for laser energies to be used in future pulsed laser SEE tests. Not solely limited to the radiation test domain, the repercussion of these future works can also be highly relevant to the research community in failure analysis of microelectronic devices as recent trend indicates the move towards modulated or pulsed lasers to improve resolution of obtained results. In such domain, it is immensely important to avoid inducing artifacts or undesired damages to the DUT.

7.2 Reconnaissance Work Not Included in Main Chapters

Other auxiliary works have been carried out during the PhD study but were not included in the main chapters. However, these works remain important to demonstrate the capabilities of the proposed pulsed laser SEE scan methodology and thus will be briefly covered in the following sub-sections. These works report on the temporal advantage that the pulsed laser SEE scan methodology provides and also on the limitations of conducting ageing on commercial samples.

7.2.1 Temporal Advantage of Pulsed Laser SEE Scan Methodology

Figure 7.3 illustrates the repetitive capabilities of the pulsed laser technique conducted on a AD8629 CMOS operational amplifier. The laser was set to pulse at a frequency of 80 Hz (or 12.5 ms per pulse) on a single position of the device. The arrival time of these laser pulses were represented by the red lines while the blue line represents the power supply current being monitored during the experiment. It can be observed that the SEL was triggered in sync with the arrival of laser pulses at the designated frequency. At 258 ms, the laser pulse expectedly did not trigger a SEL as the device was in a shut-down mode (SEL protection provided by external anti-latch circuits).

Figure 7.3 80 Hz laser inducing "on-demand" SEL (i.e, high current state) in AD8629 CMOS operational amplifier. Control of laser repetition rate and synchronization allows user to induce SEE at specific time or phase in a test pattern.

As the pulsed laser can be tuned to pulse at user-defined frequencies, it is possible to repeatedly irradiate at a single position and reproduce SELs for investigative studies. This can also be applied to investigate rare SEE events and provide in-depth understanding to sporadic occurrences (in which test engineers are unable to fully understand) encountered during limited test duration of heavy ion test campaign. In-depth studies on the rise time of the SEL current can enable satellite engineers to design specific anti-latchup circuits to mitigate SEL sensitivity in the intended satellite system before catastrophic damage is induced.

7.2.2 Limitations of Conducting Ageing on Commercial Samples

Ageing stress was trialed on the LMC6484 CMOS operational amplifier by attempting to apply a voltage overstress on the device. This is a commercial device with four independent operational amplifiers packaged in a single dual-in-line plastic molding compound. From the device's datasheet, the maximum rating for its power supply voltage is 16 V. Ageing stress was initially conducted at a voltage overstress of 20 V and after 20 days of ageing, there was no significant changes in the electrical parameters. In an attempt to further accelerate the ageing degradation without complications from elevated temperature, the power supply and input voltages were further increased. Figure 7.4 shows the PEM studies conducted on LMC6484 at various values of power supply and input voltages.

Figure 7.4 Photon emission mapping of LMC6484 biased with power supply and input voltages of: (a) 10 V, (b) 16 V, (c) 28 V and (d) 28 V with activation of current compliance limit. Yellow arrows point to strong photon emission hotspots which indicate high current flow and thus limiting the amount of overstress that users can impose on these commercial devices.

It can be observed from Figure 7.4 that as the voltage increases, the protection diodes of the device set in and thus, strong photon emission hotspots (indicated by the yellow arrows) were observed. This analysis revealed that there is a limit to the amount of voltage overstress that users can impose on commercial devices which are often designed with protection diodes or circuits. This confines the amount of acceleration that users can impose on ageing campaigns involving commercial devices and thus, a long duration stress is to be expected. As an alternative, users can look into fabricating test structures which allow direct access to the source, drain and gate terminals of the design. In this way, higher acceleration in ageing can be achieved through application of more aggressive ageing parameters. However, this alternative suffers from the high cost and long waiting time for planning a semiconductor foundry's tapeout. Also, the number of samples available for such ageing campaigns can be highly limited as compared to commercial samples which can be easily purchased off the market.

7.3 Outstanding Questions

This thesis marks the end of this PhD study but also the start of a new period of testing capabilities in Singapore. The pulsed laser SEE scan methodology was proposed with the industry's shift to small satellites in vision and the need for more radiation testing on COTS components in mind. Pulsed laser SEE scanning microscope with several optical failure analysis techniques was successfully set up at NTU. Due to the integration of the pulsed laser to the scanning microscope system, massive efforts were undertaken to fully characterize the laser parameters of the system. In addition,

benchmarking campaigns were carried out to make sure that the system is capable of inducing SEE in the correct manner as compared to published literatures. Studies on the effect of ageing on SEU response were conducted on 65 nm chain of flip flops and were reported in Chapter 5. Applications (advantages and possible areas of concern) of this methodology had also been evaluated and reported in Chapter 6.

However, there are several remaining questions which had not been fully addressed in this thesis and could pose as potential future works for interested readers. The big question in the investigation of effects of ageing on SEE response is ultimately: “Can electrical degradation models be included to improve SEE error rate predictions?”. Traditional reliability models are already relatively well studied and although models are still being debated, relatively accurate models have already been proposed and shown to provide good predictability to device lifetime. Through the monitoring of ageing degradation of electrical parameters in microelectronic devices, it could be possible to link these degradations (reduction in current drive or threshold voltage shift in the transistors) and thus, predict the impact on SEE error rates. The degradation of electrical parameters due to ageing can be modeled and this can be taken into account during SEE rate prediction. This will ensure that the device is fully qualified over the entire duration of its operational lifetime. This need is getting more important as reliability margins and device useful lifetime decreases with technology scaling. Also, investigations of such nature involves inter-disciplinary research from the field of microelectronic reliability and space radiation studies. Accurate modeling and statistical studies are non-trivial.

The next big question that arises from the laser-induced damage observed in this thesis is if there is a safe operating area for laser energies during pulsed laser SEE tests on advanced technology nodes? Although some phenomenon (diffusion of nickel from silicide layer, damage even without electrical bias) were observed in this thesis, there are many questions which require deeper investigations. The mechanism of 1064 nm pulsed laser inducing nickel diffusion has yet to be fully investigated. The effect of spot size and consequently optical density on laser-induced damage has yet to be studied. In the push towards even smaller laser spot size and better spatial resolution, could there be a laser damage threshold that limits the application of pulsed laser SEE tests on advanced microelectronic devices? With the scaling down in technology node and

critical charge, perhaps less laser energy is required to induce SEE in more advanced microelectronic devices and thus, this technique could still be applied? In the event that a safe operating area for pulsed laser energies to be used during SEE tests is established, the learning can also be applied to the field of optical failure analysis as recent trend is to move into modulated and pulsed lasers to achieve higher resolution results.

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