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Etching-free patterning method for electrical characterizations of atomically thin CVD-grown MoSe₂ film

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Patterning two-dimensional materials into specific spatial arrangement and geometry is essential for both fundamental materials studies and applications in electronics. However, the patterning methods that are currently available generally involve etching steps that rely on complicated and expensive procedures.

Here we report a facile patterning method of atomically thin MoSe₂ film by means of stripping with EBL-exposed SU-8 negative resist layer. Additional steps of chemical and physical etching were not necessary in SU-8 patterning method. The SU-8 patterning was used to define a ribbon channel from field effect transistor of CVD-grown MoSe₂ film. Notably, the narrowing of conduction channel area with SU-8 patterning was crucial to suppress leakage current within the device, thereby allowing a more accurate interpretation of electrical characterization results from the sample. Electrical transport study, which was enabled by the SU-8 patterning, revealed variable range hopping behaviour at high temperature.

1. Introduction

Layered two-dimensional (2D) materials such as graphene and transition metal dichalcogenides (TMDs, *e.g.*, MoS₂, WS₂, WSe₂) have attracted significant interest due to their interesting electronic and optical properties.¹⁻³ To harvest those unique material properties for practical applications, it is necessary to have the capability in producing the materials in scalable manner. In that aspect, chemical vapor deposition (CVD)⁴⁻⁷ and liquid exfoliation⁸ have been reported to produce layered TMD film samples in promisingly large area and high production rate. To enable the manufacturing of these 2D materials into devices and systems for various electrical studies and applications, the next crucial step is the patterning of the film into specific spatial arrangement and geometry. However, the absence of dangling bonds on the surface of 2D TMDs results in the inertness of the (0001) cleavage plane, making these materials difficult to be removed by conventional wet etchant (*e.g.*, Aqua Regia, HF, KOH) at room temperature (Fig. S1 in ESI†).

There have been varieties of experimental procedures that can be used to pattern TMDs, which were predominantly demonstrated on MoS₂.⁹⁻¹³ At present, the patterning of TMDs is commonly done *via* lithography and dry etching process with reactive ion (*e.g.*, SF₆ and XeF₄).^{9, 14} However, reactive ion etching requires multi-step procedures (including both lithography and the etching process itself) which involve highly specialized equipments. Plasma etching that sputters the 2D materials with ion bombardment was also reported,¹⁰ but the sample removal might not be thorough because the process does not produce volatile byproducts and is prone to re-deposition.

While thinning method by laser has been introduced,¹¹ the method may not be potentially scalable considering that direct laser writing is a prerequisite. Other thinning methods such as by thermal annealing is ineffective for patterning targeted only at a confined area.^{15, 16} There are also reports on top-down patterning which incorporate stamping approaches,¹² although ordered pattern can be achieved, the sample may have large variability in the layer thickness, unlike CVD synthesis which may controllably produce very thin layers.

Here we report a patterning method on layered 2D film by utilizing SU-8 negative resist as a stripping layer. By first spincoating the 2D film with SU-8, the region of SU-8 that is then exposed with electron beam lithography (EBL) can be used to strip the film beneath it. The patterning method with SU-8 requires neither chemical nor physical etching steps. The SU-8 patterning is thus attractively simpler than the available patterning methods on 2D material, incurring potential economic advantages for industrial fabrication processing. Our approach also minimizes the possibility of affecting the pre-existing structure or device on the sample as compared with other ion etching methods.

As a case study, we demonstrate the SU-8 patterning on molybdenum diselenide (MoSe₂) film grown by CVD.¹⁷ The patterning is effective for atomically thin samples that we produce, which can be controlled to thickness primarily within 1-6 layers. We have also fabricated devices from patterned CVD-MoSe₂ ribbon channel as a field effect transistor (FET) for the study of electrical transport properties of CVD-MoSe₂. Despite being a member to the family of layered TMDs crystal, the relatively lower natural abundance of MoSe₂ causes the studies on MoSe₂ to be less common than that on MoS₂. With the

emergence of CVD synthesis method to produce atomically thin MoSe₂ in large area very recently,¹⁷⁻²⁰ it becomes compelling to investigate accordingly the electrical transport properties of MoSe₂. The SU-8 patterning enables the fabrication of well-defined channel from the MoSe₂ film that minimizes the leakage current, thus allowing the electrical characterization results to be interpreted accurately.

2. Experimental

2.1 Sample preparation

Large area atomically thin MoSe₂ films (~1 cm²) were synthesized with CVD on highly p-doped Si substrates with 100 nm thick SiO₂ (University Wafers, Prime grade).¹⁷ MoSe₂ devices fabrication and patterning were performed with EBL (JEOL JSM-7001F equipped with Deben beam blanker and Nanometer Pattern Generation System) at 30 kV acceleration voltage. In all devices, the contact was 50 nm of Ni. Negative epoxy-based SU-8 2002 (MicroChem) was used in all SU-8 patterning. SU-8 was spincoated on the sample at 4000 rpm for 40 s, and soft-baked on a hotplate at 65°C for 1 min, followed by another 95°C for 1 min. After EBL exposure, the sample was immersed in SU-8 developer (MicroChem) for 1 min, post-exposure baked at 95°C for 1 min, immersed in Remover PG (MicroChem) at ~65°C for 10-30 min to remove the SU-8 pattern, and blowdried with N₂ flow.

2.2 Characterizations

The samples were characterized by scanning electron microscopy (SEM, JEOL JSM-7001F) and tapping mode atomic force microscopy (AFM, Veeco Dimension V). SEM was performed with 5 kV acceleration voltage in top view by detecting the secondary electron emission from the sample. Raman spectra were obtained on a triple-grating micro-Raman spectrometer (Horiba-JY T64000). All samples were excited with 532 nm laser. The signal was collected through a 100× objective, dispersed with a 1,800 g/mm grating, and detected by a liquid

N₂ cooled charge-coupled device. Raman mapping was performed with Renishaw InVia Raman system using 532 nm laser excitation. Device measurements were performed on probe station (Lakeshore) connected to a current preamplifier and controlled by Semiconductor Device Analyzer (Keithley). Electrical measurements were performed at temperature between 350 to 83 K at pressure below 10⁻⁵ mBar.

3. Results and discussion

3.1 Patterning of atomically thin MoSe₂ film with SU-8

Fig. 1 Schematic diagram of the patterning process

Fig. 1 illustrates schematically the process of patterning with SU-8, whose procedure is described in details in the experimental section. Briefly, after the synthesis of large area and atomically thin MoSe₂ film with CVD on SiO₂/Si substrate, SU-8 solution was spincoated and soft-baked on top of the sample. As SU-8 is a negative resist, EBL was used to expose the area of SU-8 layer in a certain shape and size that will remain on the sample after the resist development step. Finally, the developed SU-8 structure carries along the MoSe₂ layer beneath it upon the removal of the SU-8 layer in Remover PG solvent. Thus, the MoSe₂ film is removed in an area whose shape corresponds to the exposed SU-8 area during the EBL process.

Fig. 2 Characterizations of patterning on MoSe₂. Optical micrograph of MoSe₂ sample (a) with developed SU-8 layer, and (b) after the removal of SU-8 layer, thus also removing MoSe₂ in an array of hexagonal area. (c) SEM image of the sample after the patterning. (d) Raman spectra collected at the area of MoSe₂ and the area whose MoSe₂ layer was removed by SU-8. The wavenumber of the identified modes is given in the plot. (e) Raman mapping of the sample at the A_{1g} mode. (f) A typical AFM image at the boundary of a patterned area. *Inset*: Height profile from the image.

As a demonstration, we show in Fig. 2a and b the fabrication process of an array of hexagons opening from CVD-grown MoSe₂ as seen from optical microscope. Due to the thickness of the MoSe₂ film which was within a few nanometer range, the contrast between MoSe₂ and bared SiO₂ substrate is not immediately distinguishable. Fig. 2c shows the same sample area under SEM, where the difference in the yield of secondary electron emission signal from the MoSe₂ film and SiO₂ substrate is beneficial to produce image with visible contrast difference. Meanwhile, MoSe₂ under SU-8 regions that are unexposed by EBL is left without noticeable changes before and after the patterning (Fig. S2 in ESI†).

To corroborate the success of SU-8 patterning, we compare the Raman spectra collected from the removed MoSe₂ area and that from the remaining MoSe₂ layer (Fig. 2d). Raman spectroscopy is a reliable tool to characterize the presence of atomically thin TMDs since phonon frequencies are not only sensitive to the materials being studied, but are also rich in informations to probe interlayer coupling and layer thickness.^{21, 22} The micro-Raman setup also allows signal collection only from the local area where the MoSe₂ film has been removed. Raman signatures of MoSe₂ were identified from the remaining layer, where the signal from the out-of-plane A_{1g} mode was particularly intense. Meanwhile, those Raman modes disappeared in the spectrum from the removed MoSe₂ area. The mapping of Raman intensity of the A_{1g} mode (241 cm⁻¹, Fig. 2e) shows that MoSe₂ layer was removed with the SU-8 patterning method. Furthermore, atomic force microscopy (AFM, Fig. 2f) at the boundary of the removed area on similar patterned sample verifies that patterning could produce a clean removal of 2D materials with a relatively sharp edge. Interestingly, we do not observe redeposition issues with SU-8 patterning unlike etching methods relying on purely physical means (*e.g.*, Fig. S3 in ESI†).

We attribute the mechanism behind the MoSe₂ removal with SU-8 patterning to the adhesion between the exposed SU-8 and the MoSe₂ film. As long as the adhesion between MoSe₂ and SU-8 is sufficiently stronger than the adhesion between the MoSe₂ film and the SiO₂ substrate, the MoSe₂ can be removed when the SU-8 is dissolved. Additionally, adhesion of films to SiO₂ layer is generally difficult; an intermediate layer which can be oxidized (*e.g.*, Cr, Ti) is needed to block the transportation of oxygen from within the SiO₂ to the interface to achieve good adhesion. Since MoSe₂ does not oxidize rapidly in air, the adhesion between MoSe₂ and SiO₂ is relatively weak such that SU-8 layer can be used to peel off MoSe₂ film from SiO₂.²³

Typical to most other negative resists, EBL exposure and post-exposure baking cause the SU-8 polymer to be highly cross-linked and more rigid. The rigidity of the exposed SU-8 structure helps to improve the conformal contact with the MoSe₂ area below the SU-8, ensuring that the MoSe₂ layer is stripped from the substrate as a single unity uniformly—as opposed to being dissolved in smaller patches—for the complete removal of the MoSe₂ with the stripping of SU-8. Given the inertness of the (0001) plane of MoSe₂, we do not assume any unique chemical

bonds between SU-8 and MoSe₂ to allow the patterning.

Consistent with our assumption, we observed that the patterning approach is not unique to SU-8: we found that patterning can be done by using metal sacrificial layer which strip the MoSe₂ film upon the etching of the metal (Fig. S1 in ESI†). On the other hand, SU-8 patterning can also be used to remove MoS₂ flakes that were produced by exfoliation method on SiO₂ (Fig. S4 in ESI†). It is conceivable that similar methods can be performed with other lithography resist polymers. Meanwhile, the inability of some other EBL resists, such as poly(methyl methacrylate) (PMMA), to be used as the stripping layer for patterning was attributed to the poorer adhesion between PMMA and MoSe₂.

Considering the adhesion mechanism of the removal, we believe that the SU-8 patterning method will be especially useful to be employed in layered material samples with small grains. When the grain size of MoSe₂ is smaller than the feature size of the SU-8 pattern, the presence of the grains will help to ensure that the film will break following the shape of SU-8. Thus, we believe that the SU-8 patterning method will have strong applications in layered materials films produced from processes such as liquid phase exfoliation⁸ and certain CVD synthesis approaches.^{6, 17}

3.2 Device application

An immediate application of the SU-8 patterning is to define a conduction channel for electrical characterizations. Here, we patterned a ribbon channel from MoSe₂ film in a back-gated FET device (Fig. 3a,b). Two 80×80 μm² Ni pads were used as the device electrodes. By constraining the current flow into the channel, it is possible to avoid defect structures existing on the substrate that may hamper the performance of the device. For example, in a MoSe₂ film FET prior to patterning, we noticed a significant amount of gate leakage current (~nA, Fig. 3c). A typical signature of gate leakage is exhibited: the current direction is inverted when the gate voltage polarity is switched, implying that there is conduction between the source-drain electrodes to the back gate. By narrowing the area of MoSe₂ conduction channel into a ribbon, the gate leakage level can be suppressed by two orders of magnitude (Fig. 3c inset) and is now nearly independent of the gate voltage sweep. As a direct benefit of such gate leakage suppression, device performance such as I-V characteristics (Fig. S5a in ESI†) and electrical transport properties (section 3.3) can be measured more accurately.

Fig. 3 SU-8 patterning for device application. All scale bars in the image correspond to 10 μm . (a,b) A typical example of optical micrograph of MoSe₂ back-gated FET (a) before and (b) after patterning process into a ribbon channel. (c) Gate leakage current measured on a MoSe₂ device before and after patterning. *Inset*: The same data plotted in semi-log scale. (d) Schematic explanation on the reduction of leakage current with device patterning. (e) Process in cutting the channel to create an open circuit. *Inset*: SEM image of the cut channel. (f) I-V plot of a MoSe₂ device before (red) and after (blue) channel cutting. *Inset*: the plot of cut channel in semi-log scale.

Our hypothesis regarding the mechanism of gate leakage reduction with the device patterning is explained schematically in Fig. 3d. Defects on the substrate such as pinholes in gate oxide may form due to the imperfection of the substrate production, the high temperature during the sample synthesis (as was also observed for CVD-grown MoSe₂ FET),²⁴ or device fabrication and processing steps. The creation of oxide defects is particularly problematic since it generally creates reliability issues, such as short circuit of the back gate with the top electrodes. Prior to patterning, the MoSe₂ film may have

electrical connection to these defects, which results in appreciable gate leakage. The current leakage issue is exacerbated due to the large area ($\sim 1 \text{ cm}^2$) of the as-grown film,¹⁷ which causes the connection between the device to existing oxide defects somewhere on the substrate. By reducing the area of the active conduction channel with the SU-8 patterning, it is possible to avoid electrical connection from the MoSe₂ layer to such oxide defects, thus eliminating the gate leakage current.

Consistent with our hypothesis that SU-8 patterning may break electrical connection between a device to oxide defects, we show that SU-8 patterning can also be used to electrically isolate the device. By performing SU-8 patterning on the conduction channel (Fig. 3e), the channel can be cut to produce an open circuit. Prior to channel cut, drain current flows in response to the application of bias voltage (Fig. 3f). However, the drain current becomes insensitive to bias voltage after channel cut, dropping to $\sim \text{pA}$ level, which corresponds to the noise level of the measurement (Fig. 3f inset). This result confirms that the removal of MoSe₂ from the channel was indeed completed.

3.3 Electrical transport measurements

The SU-8 patterning method enables a more in-depth characterization of transport properties of the CVD-grown MoSe₂. Temperature-dependent electrical characterizations were performed on the sample (Fig. 4a). The MoSe₂ channel had a high resistance at tens of $\text{M}\Omega$ at room temperature, multiple orders higher than that of the contact resistance between MoSe₂ and Ni that reaches only hundreds of $\text{k}\Omega$ at 35 V gate overdrive.²⁵ The drain current was also strongly dependent on temperature, showing an insulating behaviour where the conductance decreases with decreasing temperature. Moreover, the current level at temperature $< 80 \text{ K}$ was beyond our measurement noise level. This suggests that the CVD-grown MoSe₂ is highly disordered, where electron localization and thermally-activated hopping conduction may play important roles in the electronic transport within CVD-MoSe₂. We also noted that the temperature-dependent conductance data exhibit nonlinearity when graphed in Arrhenius plot (Fig. 4b). The nonlinearity of the curve indicates that simple thermally activated model transport, where $\sigma \propto \exp(-E_a/k_B T)$, does not explain the temperature-dependence of our sample properly. Thus, we attempt to explain the transport behaviour in terms of variable range hopping (VRH) mechanism.

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Fig. 4 Electrical transport properties of patterned CVD-MoSe₂ ribbon channel. (a) I-V characteristics of two-probe device at various temperatures. The channel length was 0.5 μm. *Inset*: Optical micrograph of a typical patterned ribbon device. Scale bars: 100 μm (left) and 10 μm (right). (b) Arrhenius plot of the width-normalized conductance data. Black, dashed straight line is a guide to the eye. (c) Temperature dependence of width-normalized conductance in semilog scale plotted with respect to $T^{-1/3}$. *Inset*: Fitting parameter T_0 as a function of carrier density. (d) Temperature dependence of the field-effect mobility of electrons. *Inset*: Simplified band diagram, showing the position of localized states.

VRH transport has been observed in monolayer and few layered 2D materials samples such as MoS₂.^{26–30} Likewise, VRH in bulk MoSe₂ has also been reported.³¹ However, the transport behavior in ultrathin MoSe₂ samples remains elusive. Previous experimental data on few-layers MoSe₂ exfoliated from powder seemed to display a phonon-limited transport, where the device mobility decreases with increasing temperature.²⁵ In exfoliated MoS₂ and bulk MoSe₂, VRH behaviour started only in temperature range below 200 K. In contrast, our CVD-MoSe₂ devices exhibit VRH at high temperature (350 K), similar to previous work on reduced graphene oxide.³²

In VRH, the electrons occupy localized states which have a distribution of energy and position in real space. Hopping occurs due to mutual overlap of eigenfunctions of neighbouring states. The conductance of electron is proportional to the probability per unit time of hopping to happen which is given by $P(r) \propto \exp[-2r/\xi - \Delta E(r)/k_B T]$, where r is the hopping distance, ξ is the localization length, and ΔE is the activation energy.³³ For Mott-VRH in 2D material, it is assumed that density of states $N(E)$ is constant near the Fermi level. The most likely hopping maximizes $P(r)$ by circumscribing $dP/dr = 0$. This results in the VRH conductivity that can be written as

$$\sigma(T) = \sigma_0 \exp(-T_0/T)^{1/3}, \quad (1)$$

where T_0 is a fitting parameter.³³ We remark that there have been different accounts on the temperature-dependence of the exponential prefactor, σ_0 , in 2D Mott-VRH. Ghatak *et al.*²⁶ reported that $\sigma_0 \propto T^{0.8}$, as backed by a theoretical study.³⁴ Meanwhile, other previous experimental and theoretical works report σ_0 that is T -independent^{32, 33, 35} to yet other forms of T -dependence.^{36, 37} For our experiments, we notice that the T -dependence of σ_0 does not affect our conclusion dramatically and hence we shall assume that σ_0 is constant in the following discussions.

We then extract the temperature-dependent conductance of the sample at the quasi-Ohmic regime near $V_{ds} = 0$ V. Fig. 4c shows that the data can be fitted adequately with the Mott-VRH model from equation (1), giving coefficient of determination (R^2) value > 0.995 for all V_g . The inset shows the T_0 fitting parameter with respect to the carrier concentration, $n = C_g(V_g - V_{th})$, where $C_g = 3.45 \times 10^{-4}$ Fm⁻² is the gate capacitance and V_{th} is the threshold voltage. In support to our conclusion toward a hopping transport, we find that the mobility of the sample increases with temperature (Fig. 4d). This observation is in contrast to the band-like diffusion transport, as observed in MoS₂ and MoSe₂ flakes from exfoliation.^{29, 25} Moreover, the mobility also follows an $\exp(-T_0^*/T)^{1/3}$ trend, in agreement with a Mott-VRH in 2D sample.^{26, 37}

In MoS₂, Qiu *et al.* attributed the carrier localization

responsible for VRH to the sulfur vacancies, which is also the electron donor of the sample.²⁷ Analogously, we have also observed that Se vacancies exist in our sample, as verified from scanning transmission electron microscopy.¹⁷ Thus, it is reasonable to suggest that similar mechanism also contributes to the VRH in MoSe₂. Meanwhile, we observed that the fitting parameter T_0 in MoSe₂ to be one order higher than that in MoS₂. For 2D Mott-VRH, T_0 is given by

$$T_0 = \frac{13.8}{k_B N(E_F) \xi^2}, \quad (2)$$

where $N(E_F)$ is the density of states near the Fermi level.³⁸ Given that equation (1) in Mott-VRH is derived by assuming a nearly constant $N(E_F)$ within the range of several $k_B T$, then one may write that $\partial n / \partial T = N(E_F) k_B$ at temperature approaching 0 K. As a rough order-of-magnitude approximation,³⁵ we may take $\partial n / \partial T \approx n(100 \text{ K}) / 100 \text{ K}$ in order to calculate $N(E_F)$, which is about $3 \times 10^{14} \text{ eV}^{-1} \text{ cm}^{-2}$. Thus, using equation (2), we obtain that $\xi \approx 1 \text{ \AA}$, lower than that assumed in MoS₂ exfoliated flakes (6 \AA) in the literature.²⁷

A shorter ξ suggests that it is more difficult for charge carriers to hop across localized states that is distantly separated in space. This point is consistent with the relatively low conductance and mobility of CVD-MoSe₂ film (electron mobility¹⁷ reaching only $0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 300 K). While the MoSe₂ film mobility seems low, we remark that such mobility is within the typical values reported from previously CVD-grown MoS₂ film which also contain numerous grains ($\sim 0.003\text{--}0.8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$).^{4,6, 39} The occurrence of VRH behavior at room temperature can also explain the performance of MoSe₂ FET which has on-off ratio of only 10^2 at 37.5 V gate overdrive: considering that carrier localization induces states at the bandgap (see inset of Fig. 4d), it is possible for charge carriers to still contribute toward the electrical conduction across the device although the gate voltage was tuned to position the Fermi level within the bandgap of MoS₂. Meanwhile, the decrease of T_0 at higher carrier concentration is attributable to the increased screening effect, thus extending the localization length.

Conclusions

In conclusion, we have demonstrated the patterning of 2D materials with SU-8 on CVD-grown MoSe₂. The success of the patterning was characterized optically and electronically. The patterning enables further study and applications of the CVD-MoSe₂ in electronics, where the narrowing of conduction channel area with SU-8 patterning is beneficial in reducing leakage current significantly. We found that the film exhibited variable range hopping transport behavior.

The SU-8 patterning method can be used as an alternative for etching process with a preexisting structure on the sample. For instance, it is possible to benefit from the patterning method to create array of opening on the sample for further fabrication steps, such as by performing another growth step of 2D material to stitch additional material into the patterned area. In that way, lateral heterostructures with more complex arrangements can be realized.^{40, 41}

Although EBL was used in this study, we believe that it is also

possible to use UV photolithography to perform the SU-8 patterning since the method could also create similar cross-linking to induce stronger adhesion of SU-8 to the 2D film. The use of photolithography will also help to improve the throughput of the patterning.

Concerning the materials involved in the patterning, it is likely that other lithography resist can be used for similar patterning approach, subject to adequate adhesion with the material to be patterned. On the other hand, considering that the patterning depends only on strong adhesion of SU-8 to MoSe₂ after exposure with EBL, with no unique chemical reaction and binding being assumed, we also believe that the method should be general and applicable to other 2D materials as well, including graphene, h-BN, MoS₂, and WSe₂.

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