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Demonstration of Submicron-gate AlGaIn/GaN High-Electron-Mobility Transistors on Silicon with CMOS-compatible Non-Gold Metal Stack

Subramaniam Arulkumar¹, Geok Ing Ng², Salmuganathan Vicknesh¹, Hong Wang², Kian Siong Ang¹, Chandramohan Manoj Kumar¹, Khoon Leng Teo¹ and Kumud Ranjan¹

¹Temasek Laboratories@NTU, Nanyang Technological University, Singapore, 637553.

²School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore, 639798.

We have demonstrated 0.15- μm gate-length AlGaIn/GaN high-electron-mobility transistors (HEMTs) with direct-current (DC) and microwave performance for the first time using complementary metal-oxide-semiconductor (CMOS)-compatible non-gold metal stack. Si/Ta-based ohmic contacts with low contact resistance value ($R_c=0.24 \Omega\cdot\text{mm}$) and with smooth surface morphology. The fabricated GaN HEMTs exhibited $g_{m\text{max}}=250 \text{ mS/mm}$, $f_T/f_{\text{max}}=39/39 \text{ GHz}$, $BV_{\text{gd}}=90\text{V}$ and drain current collapse $<10\%$. The device Johnson's Figure of Merit (J-FOM $=f_T \times BV_{\text{gd}}$) is in the range between 3.51 THz.V to 3.83 THz.V which are comparable to the other reported GaN HEMTs on Si with conventional III-V gold-based ohmic contact process. Our results demonstrate the feasibility of realizing high performance submicron GaN-on-Silicon HEMTs using Si CMOS-compatible metal stack.

GaN High-Electron-Mobility Transistors (HEMTs) have achieved record-high cut-off frequencies ($f_T \sim 370$ GHz),¹⁾ microwave power density ($P_{out} \sim 2.5$ W/mm) @40 GHz,²⁾ which exceeded the existing Si-based device technology limits. Most reported GaN devices with impressive performance were fabricated using non complementary metal-oxide-semiconductor (CMOS)-compatible gold-based metal stacks.¹⁻⁸⁾ Now, many industries including existing silicon semiconductor manufacturers are showing increased interests to develop GaN HEMT technology on large diameter Si substrates.^{3,8,9)} In order to utilize the existing Si fabrication line, non-gold ohmic contacts with low contact resistance, R_c is essential. To date, most of the ohmic contacts with low R_c values make use of gold-based metal schemes. Table I summarizes some of the best reported R_c values for “gold” and “non-gold” based ohmic contacts for AlGaIn/GaN HEMTs on Si. The lowest R_c of 0.49 $\Omega \cdot \text{mm}$ so far achieved is with non-gold ohmic contact annealed at 870 °C.¹⁰⁾ Till now, researchers have only reported >1.5 μm -gate-length AlGaIn/GaN HEMTs using “non-gold” ohmic contacts for low-cost high-power electronics.⁸⁻¹⁰⁾ However, for high frequency applications, submicron gate-length HEMTs are necessary. Thus far, to the best of our knowledge, no report exists on the DC and microwave characteristics of sub-micron gate-length AlGaIn/GaN HEMTs using CMOS-compatible non-gold metal stack. In this letter, we report for the first time the DC and microwave characteristics of sub-micron gate-length AlGaIn/GaN HEMTs using CMOS-compatible non-gold metal stack.

The GaN HEMT structure was grown by metal-organic chemical vapor deposition with 2nm-thick GaN cap-layer, 18nm-thick $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier, 800-nm-thick GaN buffer and 1.4 μm -thick transition layer on a 4-in silicon (111) (resistivity >6000 $\Omega \cdot \text{cm}$).⁶⁾ The grown structure exhibited room temperature 2-Dimensional Electron Gas mobility of 1450 $\text{cm}^2/\text{V}\cdot\text{s}$ and sheet carrier density of 1.1×10^{13} cm^{-2} . This HEMT structure is chosen for this study to benchmark with our HEMTs using standard gold-based process.¹¹⁾ After the mesa isolation

was formed using dry etching by BCl_3/Cl_2 plasma, Ta/Si/Ti/Al/Ni/Ta (8/2/15/140/30/25 nm) ohmic metal was deposited and annealed at 800°C for 30s in a N_2 environment with a rapid thermal annealing system. Typical R_c of $0.24 \Omega\cdot\text{mm}$ (standard deviation of $0.07 \Omega\cdot\text{mm}$) is achieved out of 3 separate runs with an average specific contact resistivity (ρ_c) of $1.25 \times 10^{-6} \Omega\text{cm}^2$. The achieved R_c is believed to be the lowest ever reported for non-gold ohmic contacts for conventional GaN HEMTs on Si and it is also lower than the recessed ohmic contacts¹⁰⁾ as shown in Table I. This ohmic metal stack also provides smooth surface morphology [see Fig.1(a) and (b)] and good edge-definition. This simple ohmic scheme also avoids the need to use other complicated techniques such as ohmic-recess¹⁰⁾ or re-grown ohmic contact¹⁾ which will further introduce complication in the manufacturing process. The ohmic contact details will be published elsewhere.

To form the T-gate, a first layer of 120-nm thick SiN was deposited by plasma enhanced chemical vapour deposition (PECVD) after the ammonium sulphide $[(\text{NH}_4)_2\text{S}_x]$ treatment for about 30 min.¹¹⁾ The $0.15\mu\text{m}$ foot-print was opened and etched the SiN by CF_4/O_2 plasma. Then $1.0\text{-}\mu\text{m}$ gate-head was subsequently formed with CMOS-compatible non-gold metal stack of Ni/Al/Ta (100/400/30 nm). Finally, the non-gold metal-stack Ti/Al/Ta (50/800/30 nm) as a inter-connect metal was deposited followed by final passivation with 120-nm thick PECVD grown SiN. The metal schemes used for this study (i.e. ohmic-contact, Schottky-contact and interconnect metal lines) are commonly used in the silicon fabrication process line and hence it will not introduce any cross-contamination in the manufacturing lines. The device dimensions used for this study are $L_{\text{sg}}/L_g/L_{\text{gd}}/W_g = 0.8/0.15/1.7/(2 \times 75) \mu\text{m}$. The fabricated device DC and pulsed I-V characteristics of the HEMTs were measured using Agilent B1500 semiconductor parameter analyzer and Accent Diva D265, respectively. The microwave small signal (from 6 to 40 GHz) measurements

were also carried out using HP 8510C vector network analyzer (VNA).

Figure 1 (c) shows the typical I_{DS} - V_{DS} characteristics of 0.15- μm gate-length GaN HEMTs with CMOS compatible non-gold metal scheme. The devices exhibited -maximum drain current density ($I_{D\text{max}}$) of 830 mA/mm, maximum extrinsic transconductance ($g_{m\text{max}}$) of 250 mS/mm and threshold voltage (V_{th}) of -3.75 V. The Ni/Al/Ta Schottky gate exhibited a barrier height of 0.88 eV and a reverse gate-leakage current (-20 V) of 3.8×10^{-3} mA/mm.

Figure 2 (a) shows the small signal gain versus frequency for the HEMT with CMOS compatible non-gold metal stack. The devices exhibited a unit current gain cut-off frequency f_T of 39 GHz and maximum oscillation frequencies f_{max} of 39 GHz. This is believed to be the first reported microwave performance of submicron AlGaN/GaN HEMTs using CMOS-compatible non-gold metal stack ohmic contacts. Figure 2 (b) shows the pulsed I-V characteristics (pulse width = 200 ns; pulse period=1ms) of AlGaN/GaN HEMTs with CMOS-compatible non-gold metal stack. Very little current collapse (<10%) was observed for the gate- and drain-quiescent biases ($V_{\text{gs0}}=-8$ V, $V_{\text{ds0}}=10$ V). Three terminal OFF-state breakdown voltage (BV_{gd}) of AlGaN/GaN HEMTs is 90 V which is measured by drain current injection method (see Fig 3).¹²⁾ The J-FOM^{13,14)} ($= f_T \times BV_{\text{gd}}$) of HEMTs are in the range between 3.51 THz.V to 3.83 THz.V for different gate-drain spacing devices ($L_{\text{gd}}=1.7$ to 3.5 μm). The obtained values are comparable to the J-FOM of 3.3 THz.V for 0.15- μm gate-length GaN HEMTs on Si(111) fabricated using non-CMOS comparable gold metal stack.¹⁵⁾

In summary, we have demonstrated for the first time a sub-micron gate-length AlGaN/GaN HEMT on high-resistivity Si substrate with DC and microwave performance using CMOS-compatible non-gold metal stack. After annealing at 800 °C, ohmic contact exhibited smooth surface morphology with a low R_c value of 0.24 $\Omega \cdot \text{mm}$. The fabricated 0.15- μm -gate GaN HEMTs exhibited $g_{m\text{max}}=250\text{mS/mm}$, $f_T/f_{\text{max}}=39/39\text{GHz}$, $BV_{\text{gd}}=90\text{V}$ and

drain current collapse <10%. The device Johnson's figure of merit (J-FOM = $f_T \times BV_{gd}$) is in range between 3.51 THz.V to 3.83 THz.V which are comparable to the other reported GaN HEMTs on Si with gold-based metal scheme (3.3 THz.V). These results demonstrate the feasibility of non-gold metallization process to achieve sub-micron gate AlGaN/GaN HEMTs on Si substrate for high-frequency applications.

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References:

- 1) Y. Yue, Z. Hu, J. Guo, B. S. Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena and H. Xing: IEEE Electron Device Lett., **33** (2012) 988.
- 2) F. Medjdoub, M. Zegaoui, B. Grimbert, D. Ducatteau, N. Rolland, and P. A. Rolland: IEEE Electron Device Lett., **33** (2012) 1168.
- 3) S. Arulkumaran, G.I. Ng, S. Vicknesh, W. Hong, K.S. Ang, J.P.Y. Tan, V.K. Lin, S. Todd, G.-Q. Lo and S. Tripathy: in Int. Workshop on Nitride Semiconductors, 14-19 Oct 2012, Sapporo, Japan.
- 4) J. W. Johnson, E. L. Piner, A. Vescan, R. Therrien, P. Rajagopal, J. C. Roberts, J. D. Brown, S. Singhal, and K. J. Linthicum: IEEE Electron Device Lett., **25** (2004) 459.
- 5) S. Arulkumaran, S. Vicknesh, G.I. Ng, S.L.Selvaraj and T. Egawa: Applied Physics Express, **4** (2011) 08410.
- 6) H.F. Sun, A.R. Alt, H. Benedickter and C.R. Bolognesi: Electron. Lett., **45** (2009) 376.
- 7) D. Ducatteau, A. Minko, V. Hoel, E. Morvan, E. Delos, B. Grimbert, H. Lahreche, P. Bove, C. Gaquiere, J. C. De Jaeger, and S. Delage: IEEE Electron Device Letters, **27** (2006) 7.
- 8) M. V. Hove, S. Boulay, S. R. Bahl, S. Stoffels, X. Kang, D. Wellekens, K. Geens, A. Delabie, and S. Decoutere: IEEE Electron Device Lett., **33** (2012) 667.
- 9) B. De Jaeger, M. Van Hove, D. Wellekens, X. Kang, H. Liang, G. Mannaert, K. Geens, and S. Decoutere, in 24th Int. Sym. Power Semicon. Devices (ISPSD), 3-7 Jun. 2012, pp.49-52.
- 10) H. S. Lee, D. S. Lee, and T. Palacios: IEEE Electron Device Lett., **32** (2011) 623.

- 11) S. Vicknesh, S. Arulkumaran and G.I. Ng: in Proc. IEEE MTT-S Inter. Microw. Symp. Dig., pp.1-3, Jun 2012.
- 12) J. A. Del Alamo and M. H. Somerville: IEEE J. Solid-State Circuits, **34** (1999) 1204.
- 13) F. A. Marino, N. Faralli, D. K. Ferry, S. M. Goodnick and M. Saraniti: J. Phys. Conf. Series, **193** (2009) 012040.
- 14) M. J. Rosker, J. D. Albrecht, E. Cohent, J. Hodiaktt, T.-H Changtt: in Proc. IEEE MTT-S Inter. Microw. Symp. Dig., pp.1214-1217, May 2010.
- 15) S. Yoshida, M. Tanomura, Y. Murase, K. Yamanoguchi, K. Ota, K. Matsunaga, and H. Shimawaki: in Proc. IEEE MTT-S Inter. Microw. Symp. Dig., pp. 665-668, Jun 2009.

Figure Captions:

Figure 1. Surface morphology of (a) non-CMOS compatible gold-based (b) CMOS compatible non-gold ohmic contact and (c) I_{DS} - V_{DS} characteristics of 0.15 μ m-gate AlGaIn/GaN HEMTs with CMOS-compatible non-gold metal stack.

Figure 2. (a) Small signal characteristics of AlGaIn/GaN HEMTs with CMOS compatible non-gold metal stack. Bias points: $V_d=6V$, $V_g=-2.7V$. (b) Pulse I_{DS} - V_{DS} characteristics of 0.15- μ m-gate AlGaIn/GaN HEMTs with CMOS compatible non-gold metal stack. $V_g= +1$ to -5 V, step $-1V$.

Figure 3. Three terminal OFF-state breakdown voltage characteristics of HEMT with CMOS compatible non-gold metal stack. The device is with dimensions of $L_{sg}=0.8$ μ m, $L_g=0.15$ μ m, $L_{gd}=1.7$ μ m and $W_g=2\times 75$ μ m.

Table I. Contact resistance values for different GaN HEMT structures on Si substrate using III-V compatible gold and CMOS compatible non-gold ohmic contacts.

Research Group	HEMT on Si	Metal Stack	Annealing Temperature [°C]	R_c [$\Omega \cdot \text{mm}$]	
				Gold	Non-Gold
Nitronex [4]	AlGaIn/GaN	Ti/Al/Ni/Au	825	0.45 (Rough Surface)	-
NTU [5]	AlGaIn/GaN	Ti/Al/Ni/Au	825	0.18 (Rough Surface)	-
ETH-Z[6]	AlGaIn/GaN	Ti/Al/Ni/Au	850	0.45 (Rough Surface)	-
IEMN [7]	AlGaIn/GaN	Ti/Al/Ni/Au	900	0.50 (Rough Surface)	-
MIT [10]	AlGaIn/GaN	Ti/Al/W	870 (Ohmic-Recess)	-	0.49 (Smooth Surface)
IMEC [8]	AlGaIn/GaN/AlGaIn	Ti/Al/W	800	-	0.65
IMEC [9]	AlGaIn/GaN/AlGaIn	Ti/Al/Ti/TiN	550 (Ohmic-Recess)	-	1.25
This Work	AlGaIn/GaN	Ta/Si/Ti/Al/Ni/Ta	800	-	0.24 (Smooth Surface)

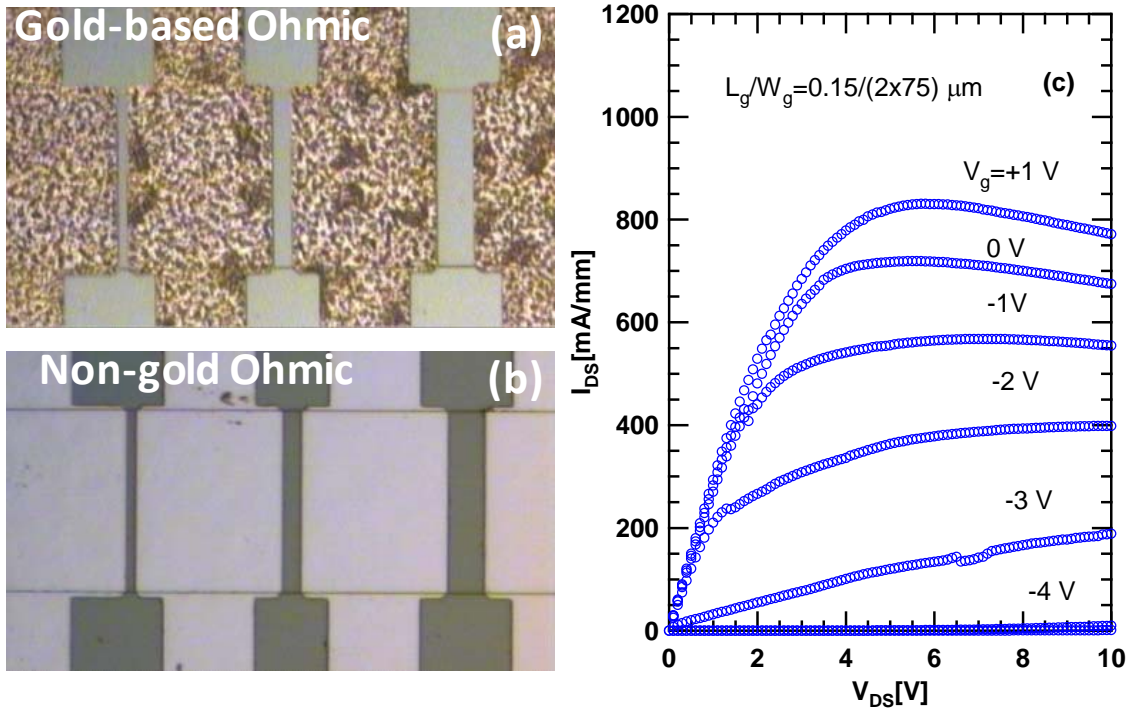


Figure 1. S. Arulkumaran et al.,

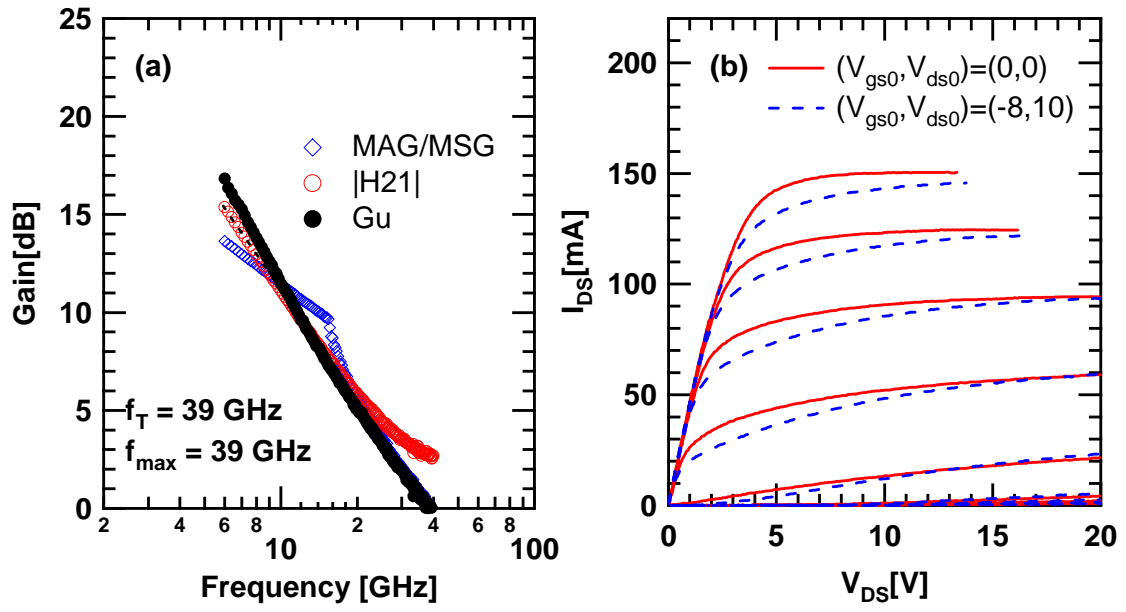


Figure. 2. S. Arulkumaran et al.

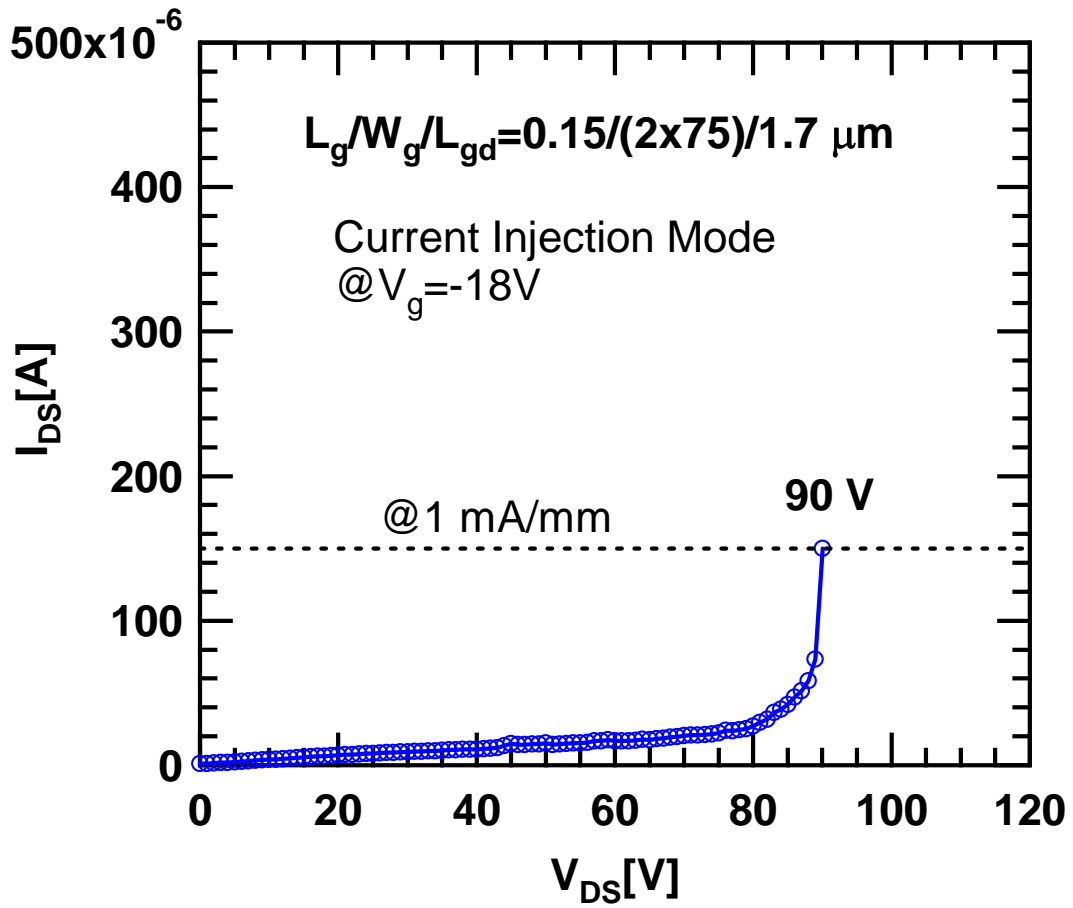


Figure 3. S. Arulkumaran et al.