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Tunneling field-effect transistor with Ge/In_{0.53}Ga_{0.47}As heterostructure as tunneling junction

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High quality epitaxial germanium (Ge) was successfully grown on In_{0.53}Ga_{0.47}As substrate using a metal-organic chemical vapor deposition tool. The valence band offset ΔE_V between the Ge layer and In_{0.53}Ga_{0.47}As determined by high-resolution x-ray photoelectron spectroscopy was found to be 0.5 ± 0.1 eV, suggesting the Ge/In_{0.53}Ga_{0.47}As heterojunction has a staggered band alignment at the interface. This makes the Ge/In_{0.53}Ga_{0.47}As heterojunction a promising tunneling junction for application in tunneling field-effect transistor (TFET). Lateral TFET with *in situ* doped p⁺ Ge-source In_{0.53}Ga_{0.47}As-channel using a gate-last process was demonstrated for the first time. The temperature dependence of the TFET transfer characteristics was investigated. The TFET with gate length (L_G) of 8 μm exhibits an on-state tunneling current (I_{ON}) of 380 nA/ μm at $V_{GS} = V_{DS} = 2$ V. The subthreshold swing (S) at the steepest part of the transfer characteristics of this device is ~ 177 mV/decade. It was found that the off-state leakage current (I_{OFF}) was determined by the Shockley-Read-Hall generation-recombination current in the Ge-source region. The temperature dependence of I_{ON} was mainly due to the change of the band gap with temperature. Furthermore, S was found to be limited by the trap-assisted tunneling at the Ge/In_{0.53}Ga_{0.47}As tunneling junction. The low I_{ON} and poor S can be enhanced by improving the source/channel profile and optimizing Ge epitaxial growth process. © 2013 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4794010>]

I. INTRODUCTION

High static power consumption due to off-state leakage current is a serious issue as complementary metal-oxide-semiconductor (CMOS) technology scales down. To reduce off-state leakage current, the subthreshold swing (S) of a metal-oxide-semiconductor field-effect transistor (MOSFET) has to be lowered. However, S is limited by Fermi-Dirac distribution of carriers for a MOSFET and cannot be reduced below 60 mV/decade at room temperature. The tunneling field-effect transistor (TFET) is a promising candidate to replace the MOSFET for its excellent off-state and subthreshold characteristics, which allows significant reduction of supply voltage and power consumption.^{1–36}

The TFET is fundamentally a gated p-i-n diode, which works on the principle of gate controlled band-to-band tunneling. An abrupt source doping profile is required to achieve a low S and a high on-state current (I_{ON}). Source dopant steepening implantation and dopant segregation techniques have been demonstrated for silicon (Si) TFET.^{19,20} However, the large band gap (E_G) of Si limits its application in TFET as the band-to-band-tunneling generation rate (G_{BTBT}) decreases rapidly with increasing E_G . To achieve a high G_{BTBT} and I_{ON} , small band gap materials such as germanium (Ge) and III-V

materials with E_G less than ~ 0.7 eV should be employed. Research effort is now focused on III-V TFET.^{16,22–24,26,27,29,31–33,35,36} Another approach to achieve high I_{ON} is by using heterostructures with a staggered band alignment at the tunneling junction. With the staggered band alignment, the length of tunneling path is effectively reduced, increasing G_{BTBT} and, therefore, I_{ON} . It was reported that TFET with In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As heterostructure outperforms In_{0.53}Ga_{0.47}As homostructure TFET in terms of I_{ON} and S .³¹ Recently, TFET with a high I_{ON} of ~ 190 $\mu\text{A}/\mu\text{m}$ at a drain bias V_{DS} of 0.75 V was achieved using GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As heterostructure tunneling junction.³² TFET with InAs/Al_{0.45}Ga_{0.55}Sb tunneling junction having a staggered band alignment was also experimentally demonstrated.³³

In this work, we experimentally realized lateral TFET with Ge/In_{0.53}Ga_{0.47}As tunneling junction for the first time. To fabricate such TFET, the process module of Ge growth on In_{0.53}Ga_{0.47}As substrate is needed. Ge growth on In_{0.53}Ga_{0.47}As is an interesting topic because of its potential application in high mobility channel MOS and optical devices.^{37–40} However, it remains a challenge to grow high quality Ge on In_{0.53}Ga_{0.47}As substrate due to the large lattice mismatch of $\sim 3.7\%$ between them. High quality Ge was successfully grown on In_{0.53}Ga_{0.47}As using a metal-organic chemical vapor deposition (MOCVD) tool in this work. In Sec. II, the device concept and design are discussed. The experimental details are documented in Sec. III. Section IV presents the

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FIG. 1. (a) Schematic showing the key features of a TFET with Ge/In_{0.53}Ga_{0.47}As tunneling junction. (b) Energy band diagrams illustrating the tunneling junction regions in two TFETs. The first TFET has a homostructure where the tunneling path length is $L_{T,1}$. The second TFET has a heterojunction with type II or staggered band alignment, and the tunneling path length $L_{T,2}$ is smaller than $L_{T,1}$ under the same bias condition.

material analysis of the epitaxially grown Ge film and electrical characterization of the fabricated Ge/In_{0.53}Ga_{0.47}As TFET. Section V highlights the main conclusions of this work.

II. DEVICE CONCEPT AND DESIGN

Fig. 1(a) shows a schematic of a TFET with Ge/In_{0.53}Ga_{0.47}As tunneling junction. This structure has several advantages. First, the Ge/In_{0.53}Ga_{0.47}As interface has a staggered band alignment. The valence band energy of Ge is higher than that of In_{0.53}Ga_{0.47}As, which can help to reduce the length of tunneling path as illustrated in Fig. 1(b). In TFET, the tunneling current is exponentially dependent on the length of tunneling path. With a shorter tunneling path as compared to a homostructure under the same bias condition, a heterostructure tunneling junction with a staggered band alignment can achieve a higher I_{ON} . Second, an abrupt p-type dopant profile at the Ge/In_{0.53}Ga_{0.47}As can be formed. The p-type dopant (Ga) in Ge is not a dopant in In_{0.53}Ga_{0.47}As; therefore, it is not a problem even if the Ga atoms diffuse from Ge into In_{0.53}Ga_{0.47}As. In addition, the diffusion of Ge into In_{0.53}Ga_{0.47}As can result in an n-type In_{0.53}Ga_{0.47}As layer at the tunneling junction since the diffused Ge atoms are n-type dopants in In_{0.53}Ga_{0.47}As. The presence of n-type In_{0.53}Ga_{0.47}As layer adjacent to the p⁺ Ge source can boost the electric field at the tunneling junction and lead to a high I_{ON} .^{9,20} Third, the tunneling current in this structure is determined by direct band-to-band tunneling, where electrons tunnel from the Γ point of the valence band in Ge to the Γ point of the conduction band in In_{0.53}Ga_{0.47}As. This is because In_{0.53}Ga_{0.47}As in the channel is a direct band gap material. This direct Γ -to- Γ point tunneling does not require the assistance of phonons and is expected to have a higher tunneling probability than indirect tunneling.⁴¹ Finally, the epitaxial Ge grown on In_{0.53}Ga_{0.47}As can be *in situ* doped to form p⁺ Ge. The *in situ* doping contributes to a high doping concentration in the Ge source region, which can also help to increase the device drive current. Fig. 1(a) summarizes the key features of the device design in this work.

Fig. 2 compares the I_{DS} - V_{GS} characteristics of a homostructure In_{0.53}Ga_{0.47}As TFET and a TFET with Ge/In_{0.53}Ga_{0.47}As

heterojunction at $V_{DS} = 0.5$ V. In this simulation, the simulator used implements a non-local algorithm for accurate calculation of the band-to-band-tunneling (BTBT) current across a heterojunction. The details of the simulator can be found elsewhere.^{42,43} For this simulation, the device parameters used were: source doping $N_A = 1 \times 10^{20} \text{ cm}^{-3}$, drain doping $N_D = 1 \times 10^{19} \text{ cm}^{-3}$ with a profile of 10 nm/decade into the channel, body doping $N_A = 1 \times 10^{16} \text{ cm}^{-3}$, equivalent oxide thickness (EOT) = 0.8 nm, gate length = 200 nm, the length of gate-to-source overlap ($L_{OV,GS}$), and gate-to-drain overlap ($L_{OV,GD}$) = 10 nm. A 5 nm thick n-type In_{0.53}Ga_{0.47}As layer ($N_D = 1 \times 10^{18} \text{ cm}^{-3}$) with an abrupt doping profile was inserted at the tunneling junction. An In_{0.53}Ga_{0.47}As TFET was simulated as reference using the same set of parameters without the n-type layer at the tunneling junction.

The S of the TFET with Ge/In_{0.53}Ga_{0.47}As tunneling junction is much smaller than that of the In_{0.53}Ga_{0.47}As TFET. We

FIG. 2. I_{DS} - V_{GS} curves for In_{0.53}Ga_{0.47}As TFET and TFET with Ge/In_{0.53}Ga_{0.47}As tunneling junction at $V_{DS} = 0.5$ V. I_{ON} and S of TFET are improved by employing Ge/In_{0.53}Ga_{0.47}As heterojunction as tunneling junction.

FIG. 3. Process steps used in the fabrication of Ge-source $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -channel TFET: (a) deposition of a 20 nm thick sacrificial ALD Al_2O_3 ; (b) Si^+ implantation to form n^+ doped drain region; (c) recess etching into $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ followed by selective growth of p^+ Ge by MOCVD; (d) formation of gate stack comprising TaN on Al_2O_3 .

define $V_{\text{leak_floor}}$ to be the maximum gate voltage in the off-state leakage floor region of the $I_{\text{DS}}-V_{\text{GS}}$ curve, i.e., just before I_{DS} rises sharply with increasing V_{GS} . For a fair comparison, the gate work functions for these two TFETs were adjusted so that $V_{\text{leak_floor}}$ are the same. It can be observed that TFET with Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ tunneling junction can achieve a higher I_{ON} as compared to the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ TFET.

III. EXPERIMENT

Fig. 3 illustrates some of the process steps for the fabrication of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -channel TFET with lateral Ge source using a gate-last process. A 2-in. (100)-oriented semi-insulating InP wafer with an overlying 500 nm thick epitaxial p-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer ($N_A \sim 5 \times 10^{16} \text{ cm}^{-3}$) was used as the starting substrate. After degreasing in acetone, isopropanol, and de-ionized water, a 20 nm thick sacrificial aluminum oxide (Al_2O_3) was deposited using atomic layer deposition (ALD) tool to protect the wafer surface during subsequent processing steps [Fig. 3(a)]. Drain was formed by a masked Si^+ implantation at an energy of 40 keV and a dose of

$1 \times 10^{14} \text{ cm}^{-2}$ [Fig. 3(b)]. The dopants would be subsequently activated during a Ge epitaxial growth at 650°C . A layer of 200 nm thick silicon dioxide (SiO_2) was then deposited by a plasma-enhanced chemical vapor deposition (PECVD) and patterned to expose the source region. This SiO_2 layer acts as a mask for recess etch of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ by a chlorine (Cl_2)-based plasma process. The wafer was then treated in diluted sulfuric peroxide mixture (SPM) solution for 10 s to remove a thin layer of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ that was damaged during plasma etching. Pre-epitaxial cleaning using concentrated sulfuric acid (H_2SO_4 96%) for 1 min was performed before the wafer was loaded into a MOCVD system for Ge epitaxial growth. A blanket $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ sample was also included for characterization of the epitaxial Ge film.

After loading the samples into the MOCVD system, the substrate temperature was ramped up to about 380°C when arsine (AsH_3) was flowed to suppress arsenic (As) out-diffusion. The wafers were then baked at 650°C for 3.5 min to remove residual native oxide before Ge growth. Germane (GeH_4) with a flow rate of 20 sccm was used for Ge epitaxial growth. 10 sccm of trimethylgallium (TMGa) was introduced for *in situ* Ga-doping to form p^+ Ge. The pressure of the chamber was 100 mbar during growth [Fig. 3(c)].

After Ge epitaxial growth, the wafers were treated in diluted NH_4OH (31% by weight): H_2O_2 (28% by weight): H_2O (1:2:160) for 10 s before the sacrificial Al_2O_3 and SiO_2 on the channel and drain regions were removed using diluted hydrofluoric acid (HF). The final thickness of the epitaxial Ge layer on the source region was 29 nm. Pre-gate cleaning using hydrochloric acid (HCl), ammonium hydroxide (NH_4OH), and ammonium sulfide [$(\text{NH}_4)_2\text{S}$] was then performed. Gate stack comprising of 5.6 nm of ALD Al_2O_3 and 120 nm of reactive-sputtered tantalum nitride (TaN) was formed. A Cl_2 -based plasma was used to define the gate electrode [Fig. 3(d)]. Finally, a 10 nm thick nickel (Ni) layer was deposited and annealed at 350°C for 30 s using a lift-off process to form the contact. This completed the device fabrication process.

IV. RESULTS AND DISCUSSION

A. Material analysis

X-ray diffraction (XRD) characterization was performed on a blanket Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample. Fig. 4(a) shows the

FIG. 4. (a) High-resolution XRD curve of a blanket Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample. The Ge peak was clearly observed. The peaks from $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InP substrate appear at the same Bragg angle due to the same lattice constant. (b) The RMS surface roughness for a $5 \mu\text{m} \times 5 \mu\text{m}$ area is 0.54 nm, indicating that a smooth Ge surface was obtained.

FIG. 5. (a) High-resolution TEM image of 50 nm thick Ge epitaxially grown on In_{0.53}Ga_{0.47}As substrate. (b) TEM image at the Ge/In_{0.53}Ga_{0.47}As interface indicated by the dashed box in (a). High quality Ge film was formed and defects were only observed at the interface.

XRD results. The well-defined Ge peak indicates the good quality of the epitaxial Ge film. Fig. 4(b) shows the surface roughness measured using atomic force microscopy (AFM). The Ge surface has a low surface roughness with a root mean square (RMS) value of 0.54 nm over a $5 \mu\text{m} \times 5 \mu\text{m}$ scan area. Fig. 5 shows the high-resolution transmission electron microscope (TEM) images of a 50 nm thick epitaxial Ge film grown on In_{0.53}Ga_{0.47}As substrate. Fig. 5(b) is a zoomed-in view of the Ge/In_{0.53}Ga_{0.47}As interface. High quality Ge with no observable defects was successfully grown. However, some defects were observed at the Ge/In_{0.53}Ga_{0.47}As interface due to the large lattice mismatch between Ge and In_{0.53}Ga_{0.47}As. As a result, the Ge film is almost fully relaxed as analyzed using Raman spectroscopy. Fig. 6 shows the Raman spectra for the In_{0.53}Ga_{0.47}As sample with 50 nm thick epitaxial Ge layer and for a bulk Ge reference sample obtained using 532 nm laser. The amount of strain in the epitaxial Ge layer can be calculated from the Raman shift ($\Delta\omega$) relative to the bulk Ge peak using

$$\Delta\omega = b\varepsilon_{//}, \quad (1)$$

where $\varepsilon_{//}$ is the biaxial tensile strain and $b = -(415 \pm 40) \text{ cm}^{-1}$.^{40,44} The small $\Delta\omega$ of -0.85 cm^{-1} corresponds to a tensile strain of only $\sim 0.2\%$, indicating that the Ge film is almost fully relaxed.

Secondary ion mass spectrometry (SIMS) was performed to examine the Ge profile at the Ge/In_{0.53}Ga_{0.47}As interface, as shown in Fig. 7. Low energy Ar⁺ beam was used in the SIMS analysis to improve the depth resolution of the Ge profile. It is clearly observed that Ge atoms profile decays gradually into the In_{0.53}Ga_{0.47}As layer. It is well known that inter-diffusion of Ge, Ga, and As atoms occurs easily at the Ge/GaAs interface.^{45–47} As the growth temperature for Ge on In_{0.53}Ga_{0.47}As used in this work is 650 °C, it

FIG. 6. Raman spectra of a bulk Ge sample and an In_{0.53}Ga_{0.47}As sample topped by 50 nm thick Ge film. Lorentzian functions were fitted to the spectra. The small shift of the Ge peak with respect to that of bulk Ge indicates the epitaxial Ge film is almost fully relaxed.

FIG. 7. SIMS analysis of the Ge/In_{0.53}Ga_{0.47}As sample indicates that Ge atoms diffuse into In_{0.53}Ga_{0.47}As. As a result, an n-type In_{0.53}Ga_{0.47}As layer is formed at the Ge/In_{0.53}Ga_{0.47}As interface. This n-type layer enhances the lateral electric field at the tunneling junction, which can contribute to a higher TFET drive current.

FIG. 8. (a) Top-view SEM image of a fabricated TFET. (b) Zoomed-in view of the same device in (a). The gate-to-source overlap $L_{OV,GS}$ of $5\ \mu\text{m}$ is clearly observed. The channel length L_{CH} is $8\ \mu\text{m}$. (c) TEM image of a fabricated TFET device showing the tunneling junction region.

is expected that Ge atoms will diffuse into $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate. Since Ge atoms are n-type dopants in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, a $\text{p}^+\text{Ge}/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{n}^+\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (p^+nnp^+) structure is formed, which can contribute to improved TFET performance. Hall measurement was carried out on a blanket $\text{Ge}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample. A hole concentration as high as $3 \times 10^{20}\text{ cm}^{-3}$ was achieved in the Ge layer. This high doping concentration shortens the tunneling distance and helps to increase the tunneling rate in a TFET.

Fig. 8(a) is a top-view scanning electron microscope (SEM) image of a fabricated Ge-source $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -channel TFET. The SEM image in Fig. 8(b) clearly shows the gate-to-source overlap region. The channel length L_{CH} of the device is $8\ \mu\text{m}$. Fig. 8(c) is a TEM image of a TFET device showing the tunneling junction region. The thickness of the Al_2O_3 gate dielectric layer is $\sim 5.6\text{ nm}$. The rough Ge surface in the tunneling junction region may cause a high gate leakage current as the surface roughness can enhance the average electric field inside the gate dielectric.^{48,49} However, it should not have a large impact on the tunneling current of the device.

B. Band alignment study

The band alignment between Ge and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is an important device design consideration. However, the band alignment at the $\text{Ge}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface has not been reported. In this work, the band alignment at the $\text{Ge}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface was investigated using high-resolution x-ray photoelectron spectroscopy (XPS). Two samples were used to measure the valence band offset ΔE_V between Ge and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. The first comprises 50 nm thick Ge grown on 500 nm thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. The second is a 500 nm thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ reference sample.

The core-level spectra of Ge $3d$ from top Ge film and As $3d_{5/2}$ from $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ were used for the calculation of band offset because of their large information depth (lower binding energy). Therefore, strong signals from the interface and less experimental error are expected. The technique proposed by Kraut *et al.* has been widely used to study the

valence band offset for heterojunction systems.^{50–56} In this technique, the valence band offset ΔE_V can be obtained from

$$\Delta E_V = (E_{CL}^{Ge\ 3d} - E_V)^{Ge} - (E_{CL}^{As\ 3d_{5/2}} - E_V)^{InGaAs} + \Delta E_{CL}^i, \quad (2)$$

where E_{CL} and E_V are the binding energies of the core-level electron and valence band edge, respectively; ΔE_{CL}^i is the core-level binding energy difference between the two materials at the interface and it can be found using $\Delta E_{CL}^i = E_{CL}^{Ge\ 3d} - E_{CL}^{As\ 3d_{5/2}}$ from the Ge $3d$ and As $3d_{5/2}$ spectra obtained at the $\text{Ge}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface.

Fig. 9 shows the valence band and core-level spectra obtained from the Ge film grown on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [(Fig. 9(a))] and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ reference sample [(Fig. 9(b))]. In Fig. 9(a), the valence band edge of the Ge film was determined by the intersection of the regression determined line segments defining the edge and the flat energy distribution curve in the energy gap region. It was found to be around 0 eV as the Ge film has a high concentration of holes. After careful curve fitting, the energy difference between valence band edge and the Ge $3d$ peak was found to be 29.56 eV . The valence band and core-level As $3d$ spectra of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ are shown in Fig. 9(b). The As $3d_{5/2}$ and $3d_{3/2}$ doublets were determined to be 40.67 eV and 41.36 eV , respectively. The valence band edge of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ was found to be 0.11 eV . Based on the doping concentration of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($N_A \sim 5 \times 10^{16}\text{ cm}^{-3}$), the valence band maximum is calculated to be 0.13 eV below the Fermi-level, which agrees well with the XPS results. The energy difference between valence band edge and the As $3d_{5/2}$ peak from $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ was determined to be 40.56 eV as indicated in Fig. 9(b).

To calculate the valence band offset, the interfacial core-level binding energy difference ΔE_{CL}^i between Ge and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is needed. The 50 nm thick Ge on the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample was thinned down using Ar ion. ΔE_{CL}^i was obtained when the Ge layer was thin enough so that signals from both Ge and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ were obtained. The value of ΔE_{CL}^i was found to be 11.50 eV as shown in Fig. 9(c).

FIG. 9. (a) The Ge 3d core-level and valence band spectra for 50 nm thick Ge on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. (b) The As 3d core-level and valence band spectra for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ reference sample. The valence band maximum is extrapolated from the intersection point between the leading edge of the valence band spectrum and the base line. (c) The Ge 3d and As 3d core-level spectra from the Ge on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample after Ge was thinned down by Ar ion. Energy difference between the two core-levels is shown. (d) The energy band alignment between Ge and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is illustrated, showing the conduction band offset of 0.2 ± 0.1 eV and valence band offset of 0.5 ± 0.1 eV. The band gap narrowing effect due to high doping concentration in Ge was taken into consideration.

Therefore, the ΔE_V between Ge and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ was calculated to be 0.5 ± 0.1 eV. The error was due to the system limitations of the XPS tool. It is worthy to note that there is a small accumulation region in the p^+ Ge film. However, the measured valence band edge of Ge is in fact from the charge neutral region in Ge. This causes the obtained valence band offset to be very slightly underestimated by the amount of band bending in Ge, which is very small (~ 0.02 eV) compared to the error due to tool limitation. The conduction band offset can be determined to be 0.2 ± 0.1 eV by taking consideration of the band gap narrowing effect in Ge.⁵⁷ Fig. 9(d) illustrates the band alignment at the Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface.

C. Electrical characterization of TFETs

The staggered band alignment between Ge and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ makes this heterostructure a suitable candidate for the tunneling junction in a TFET. The large valence band offset contributes to a small tunneling path length, which is beneficial for the drive current of TFET. Fig. 10(a) shows the measured transfer characteristics $I_{DS}-V_{GS}$ of a fabricated TFET device with L_{CH} of $8 \mu\text{m}$. The $L_{OV,GS}$ and $L_{OV,GD}$ are $9 \mu\text{m}$ and $2 \mu\text{m}$, respectively. The S of this device is ~ 177 mV/decade. All the S in this work was found at the steepest part of the $I_{DS}-V_{GS}$ curve at $V_{DS} = 0.2$ V. The output

FIG. 10. $I_{DS}-V_{GS}$ characteristics of a Ge-source $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -channel TFET with L_{CH} of $8 \mu\text{m}$. The $L_{OV,GS}$ and $L_{OV,GD}$ are $9 \mu\text{m}$ and $2 \mu\text{m}$, respectively. The minimum point S is ~ 177 mV/decade. (b) $I_{DS}-V_{DS}$ characteristics of the same device in (a). The device performance can be further improved by optimizing the Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ tunneling junction.

FIG. 11. I_{DS} - V_{GS} characteristics of a fabricated TFET under various temperatures ranging from 240 K to 330 K in steps of 30 K.

characteristics I_{DS} - V_{DS} of the same device are shown in Fig. 10(b). Fig. 11 shows the I_{DS} - V_{GS} characteristics of a TFET device measured under various temperatures ranging from 240 K to 330 K in steps of 30 K at V_{DS} of 0.2 V.

When V_{GS} is less than ~ 0.25 V, the device is in the off-state. The leakage current I_{OFF} of the device was defined as the drain current I_{DS} at $V_{GS} = -1.0$ V. Fig. 12(a) is a Arrhenius plot of $\ln(I_{OFF}/T^{3/2})$ versus $1/kT$, where k is the Boltzmann constant and T is the temperature. The linear relationship between $\ln(I_{OFF}/T^{3/2})$ and $1/kT$ indicates that the I_{OFF} is mainly due to Shockley-Read-Hall (SRH) generation-recombination current. SRH-dominated leakage current floor is a function of the intrinsic carrier concentration n_i , which is proportional to $e^{-E_g/2kT}$. The slope of the fitted curve is 0.27 eV, which is about half the band gap of Ga doped Ge, considering the band gap narrowing effect. This indicates that the leakage current is dominated by the SRH current from the source side. Furthermore, it is observed that the leakage current is insensitive to the gate voltage, which also suggests the leakage current is dominated by the source-side leakage.

Fig. 12(b) plots the I_{DS} at $V_{GS} = 1.0$ V and $V_{DS} = 0.2$ V as a function of temperature. The device is in the on-state

under this bias condition, and the I_{DS} is determined by the band-to-band tunneling current. In TFET, the G_{BTBT} is modeled using Kane's model⁵⁸

$$G_{BTBT} = A \frac{\xi^2}{E_G^{1/2}} \exp\left(-B \frac{E_G^{1/2}}{\xi}\right), \quad (3)$$

where E_G is the energy band gap of the material in the tunneling region and ξ is the magnitude of the electric field. Parameters A and B are adjustable depending on the properties of the material used and are functions of carrier effective mass. As temperature increases from 240 K to 330 K, there is a monotonic increase in I_{ON} , which is mainly due to the reduction of band gap. From 240 K to 330 K, the band gap of both Ge and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is reduced by ~ 33 meV. This amount of band gap reduction causes the increase in the G_{BTBT} , leading to an increase in the I_{ON} . The temperature dependence of the minimum point S characteristics was also depicted in Fig. 12(b). S increases from 133 mV/decade to 228 mV/decade when temperature increases from 240 K to 300 K. The positive temperature dependence of S could be caused by the trap-assisted tunneling current.^{22,59–61} As reported in Ref. 22, the trap-assisted tunneling has a strong positive temperature dependence and causes degradation in S . The large lattice mismatch between Ge and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ gives rise to defects at the Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface, leading to the formation of trap states in the band gap. Electrons can tunnel from the Ge source region to the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel via these trap states, causing the degradation of the S . Interface trap densities at $\text{Al}_2\text{O}_3/\text{Ge}$ and $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interfaces in the tunneling junction region may also increase the S of the TFET due to trap assisted tunneling. There is a sharp increase in S when temperature reaches 330 K, which is because S was determined at the relatively large I_{DS} due to the high leakage floor.

Despite the various advantages of the Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ heterostructure, the fabricated TFET suffers from low I_{ON} . Based on the reported contact resistance values of NiGe and Ni- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ formed under similar experimental conditions as this work, we estimated the total resistance in the source and drain regions to be $\sim 140 \Omega$.^{62,63} However, the

FIG. 12. (a) Arrhenius plot of $\ln(I_{OFF}/T^{3/2})$ versus $1/kT$. The slope of the fitted line is ~ 0.27 eV, which corresponds to the half band gap of Ge, indicating the off-state leakage current floor is determined by the SRH generation-recombination current in the source side. (b) Plot of I_{ON} and S as a function of temperature. The I_{ON} increases as temperature changing from 240 K to 330 K, which is mainly due to the band gap reduction. Due to the trap assisted tunneling, S has a positive temperature dependence. The discrepancy of the S at room temperature between this transistor and the one in Fig. 10 was due to device-to-device variation.

total resistance of the TFET in Fig. 10 is $\sim 2 \times 10^4 \Omega$ at $V_{DS} = 0.2$ V. Therefore, the low I_{ON} was mainly caused by the high resistance associated with the tunneling junction and the channel region of the transistor. The device performance can be further improved. From the TEM image of the tunneling junction region in Fig. 8(c), we found the Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface under the gate inclines to the source side, which is detrimental to the performance of the TFET. Both simulation and experiment have demonstrated that an extended source structure, i.e., the source/channel interface inclining to the channel, would lead to the establishment of more tunneling paths with shorter lengths, which increases the tunneling current and reduces S of the device.^{19,64} Therefore, the source geometry has to be improved to enhance the device performance.

In addition, the Ge growth process can also be further improved to reduce the defect density at the Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface, which will suppress the current due to trap-assisted tunneling and contribute to a steeper S . The Ge growth conditions can be adjusted, such as reducing the growth temperature and the Ge layer thickness, to achieve a strained Ge layer with lower the defect density at the interface.

V. CONCLUSION

High quality Ge was successfully grown by metal-organic chemical vapor deposition on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. Based on X-ray photoemission spectroscopy, it was found that Ge/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface has a staggered band alignment and the valence band energy of Ge is higher than that of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ by 0.5 ± 0.1 eV. Such a staggered band alignment is useful for application in an n-channel TFET. An $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -channel TFET with p^+ Ge-source was fabricated and characterized. Its electrical performance was investigated and the dominant conduction mechanisms in both on- and off-states were studied using multi-temperature measurement. The performance of the fabricated TFET can be further enhanced by improving the source/channel profile and optimizing Ge epitaxial growth process.

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