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Micellar poly(styrene-*b*-4-vinylpyridine)-nanoparticle hybrid system for non-volatile organic transistor memory†

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We present organic field-effect transistor (OFET) memories where *in-situ* synthesized gold (Au) nanoparticles in self-assembled polystyrene-*block*-poly-4-vinylpyridine (PS-*b*-P4VP) block copolymer nanodomains successfully functioned as charge storage elements. Both *p*-type (pentacene) and *n*-type (perfluorinated copper phthalocyanine) OFET based memories are reported, which have stable large charge capacity and programmable-erasable properties due to charge confinement in the embedded Au nanoparticles. Optical excitation has been utilized to demonstrate photogenerated minority carrier trapping in the Au nanoparticles for efficient erasing operations. The memory devices can hence be written and read electrically and erased optically, resulting in large memory windows (~9–11 V), high on/off ratio between memory states (10^3–10^5) and long retention times (>1000 s). The results clearly indicate the utility of the block copolymer-nanoparticle approach for OFET based memories.

Introduction

Block copolymers have unique associative properties that facilitate self-assembly into nanostructures determined by the solvent type, volume fraction of each block as well as the total molecular weight of the block copolymer.[1–4] The kinetic control over block copolymer film morphology to produce well defined arrays of nanoparticles has emerged as a powerful method for the production of nanostructured hybrid materials.[5–10] The general approach involves the binding of the nanoparticle precursor to specific (hydrophilic) domains of the block copolymer micelles followed by chemical reduction. The main advantages of this block copolymer approach are obvious: (1) the wide variability of the block copolymer chemistry enables the modification of the binding block for stabilization of different types of nanoparticles,[11–13] (2) the size of the nanoparticles can be controlled by varying the volume fraction of each block or the loading ratio of the precursor to the binding block,[5] (3) the utilization of high molecular weight polymers can solve the problem of colloidal stabilization as compared to the classical stabilization systems by surfactants or in microemulsions.[14,15]

These self-organized nanoparticles in a block copolymer template are considered excellent candidates for applications such as biological assays, magnetic storage, and electrical memory devices. Nonvolatile organic memory represents an ideal application to take advantage of this block copolymer approach since the nanoparticles represent huge ensembles of ordered electronic traps to enable the memory functionality. Nanoparticle based organic memories (akin to present day Flash memories) are especially attractive due to reduced charge loss from defects in the underlying dielectric, and the capability of multiple bit storage.[16–18] In particular, the memory characteristics can be simply tuned by using a mixture of metal and/or metal oxide nanoparticles with different electron affinities, hence creating multi-state levels. An advantage this system has over the pure polymeric memories[19–21] is the ability to preserve the primary dielectric/semiconductor interface while at the same time tuning the trap densities.

Organic field-effect transistor (OFET) based memories also allow a direct integration of the memory element with the transistor for integrated circuit applications. But degradation of device properties and variation in device-to-device performance are often observed due to multiple process steps – nanoparticle deposition, tunnel and control dielectrics formation and/or post annealing making it more prone to interface trap generation. Therefore, it is desirable to find a simple and low-temperature method able to produce homogeneous high density nanoparticle arrays as charge storage elements that can be reliably incorporated into organic transistors. The block copolymer-nanoparticle hybrid system offers such a great potential and its solution processability is especially suitable for low-cost large-area processing on flexible substrates, which may be considered to be the cornerstone of organic electronics applications.

Previously, we reported the memory potential of a block copolymer system of poly(styrene-*block*-4-vinylpyridine) (PS-*b*-P4VP) where arrays of discrete gold (Au) nanoparticles were *in-situ* synthesized (Fig. 1a) and acted as charge storage centers, within the dielectric layer in a Metal-Pentacene-Insulator-Silicon (MPIS) capacitor structure.[22] The charging mechanism is attributed to hole tunneling from pentacene through the thin PS (*ca.* 2–3 nm) and P4VP layers into the Au nanoparticles. Since the memory element of a non-volatile OFET is based on such an extended MPIS type structure, this is the first step in demonstrating how the process of incorporation of metal nanoparticles in a block copolymer gate dielectric can be exploited in designing floating gate organic memory transistors. Herein, we extend the MPIS structure and present OFET

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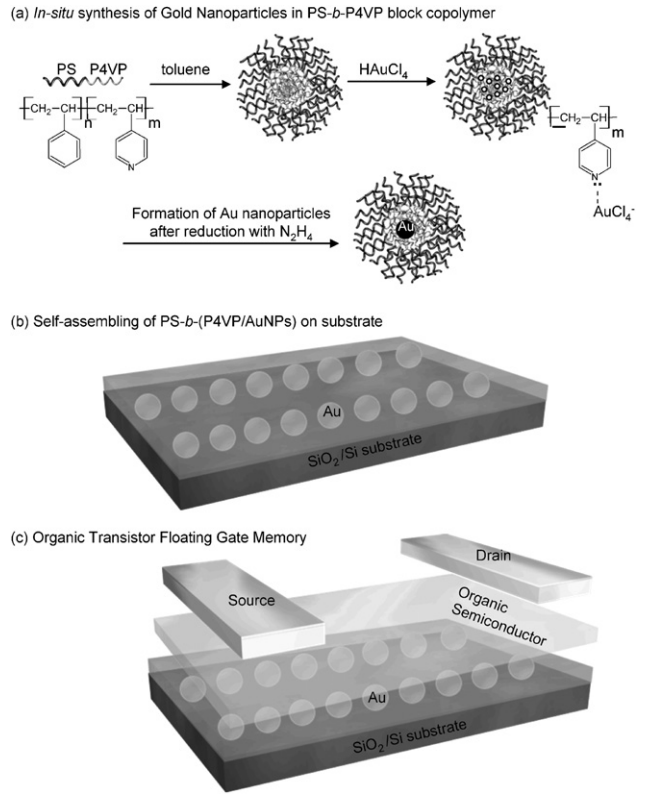

Fig. 1 Schematic illustration of (a) micellation process with *in-situ* synthesis of Au nanoparticles in PS-*b*-P4VP block copolymer; PS-*b*-(P4VP/AuNPs), (b) the self-assembling of PS-*b*-(P4VP/AuNPs) micellar film on substrate and (c) cross-section of an organic field-effect transistor (OFET) using PS-*b*-(P4VP/AuNPs) as floating gate memory elements.

memories that have large charge capacity, stable and programmable-erasable properties. Fig. 1 summarizes the block copolymer approach to realizing an OFET memory. The memory transistor is fabricated by sandwiching this block copolymer of PS-*b*-P4VP with Au nanoparticles; PS-*b*-(P4VP/AuNPs) between the organic semiconductor and a control thermal oxide layer. The active memory layer of PS-*b*-(P4VP/AuNPs) acts as a floating gate layer to trap charges while the purpose of the control thermal oxide layer is to prevent the leakage of stored charges. Both *p*-type (pentacene) and *n*-type (perfluorinated copper phthalocyanine) memory transistors have been realised and their charge trapping mechanisms are delineated.

Experimental

In-situ synthesis of Au nanoparticles in PS-*b*-P4VP micelles

Poly(styrene-*block*-4-vinylpyridine) (PS-*b*-P4VP) diblock copolymers (M_n^{PS} = 11 800 kg mol^{-1}, M_n^{P4VP} = 15 000 kg mol^{-1}, M_w/M_n = 1.04) were obtained from Polymer Source. Pentacene (sublimed), perfluorinated copper phthalocyanine ($F_{16}CuPc$) and tetrachloroauric acid ($HAuCl_4 \cdot 3H_2O$) were purchased from Sigma-Aldrich.

The block copolymer of PS-*b*-P4VP forms a micellar structure when dissolved in toluene due to the preferential solubility of the non-polar PS block in toluene while the P4VP block being insoluble collapses to form the core of the micelle (Fig. 1a). The block copolymer of PS-*b*-P4VP first underwent a solvent extraction process to remove any residual ionic impurities.[22,23] The purification process of the copolymer was done by dissolving the "as-purchased" PS-*b*-P4VP in toluene and washing the copolymer solution with de-ionized water. The water phase is then removed and the toluene phase containing the PS-*b*-P4VP was precipitated from hexane. The final precipitate was dried at 50 °C under vacuum for 48 h.

The "cleaned" PS-*b*-P4VP precipitate was re-dissolved in toluene (5mg ml^{-1}). Tetrachloroauric acid ($HAuCl_4 \cdot 3H_2O$) was added to the block copolymer solution in the required amounts given in molar relation to the P4VP units. $AuCl_4^-$ ions were bound as counterions in the polar core of the micelles by protonating the pyridine units, resulting in the formation of polyionic blocks. The molar ratio of $HAuCl_4$/pyridine units in the final solution is 1:4. The solution was subsequently stirred for 24 h and then treated with hydrazine monohydrate (ratio of $N_2H_4 \cdot H_2O$: Au^{3+} = 1:1). Due to its polar character, hydrazine is taken up preferentially in the core of the micelles where Au^{3+} ions were reduced and nucleated to form elemental gold particles in micelle cores (Fig. 1a).

Characterization of PS-*b*-(P4VP/AuNPs) miceller film

Fig. 2a presents the phase image (from atomic force microscopy, Digital Instruments Dimension 3000) of the assembled micelles containing Au nanoparticles after transfer onto substrate by spin coating. The micelles retained their integrity and the diameter of the micelle is around 50 nm. The measured thickness (using atomic force microscopy) of the layer is consistent with the diameter of the micelle, indicating the formation of a monolayer.

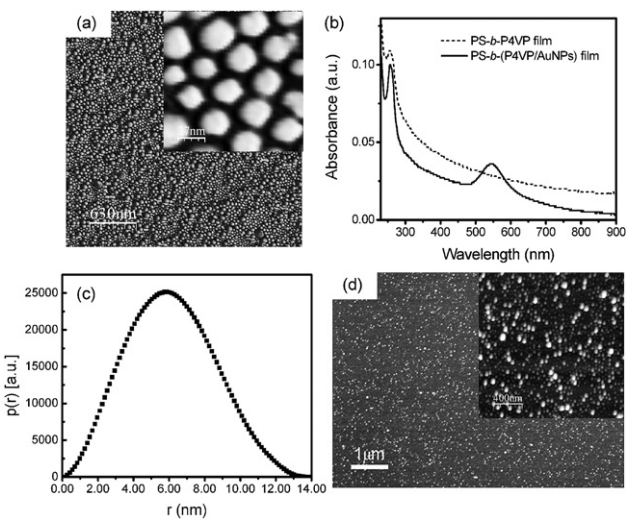

Fig. 2 (a) Phase image (from atomic force microscopy) of a micellar film of PS-*b*-(P4VP/AuNPs). Two different scanned sizes are presented to show local and long-range order. (b) UV-vis absorption spectra of PS-*b*-P4VP (with or without Au nanoparticles) thin films. (c) Pair distance distribution function for PS-*b*-(P4VP/AuNPs) thin film. The molar ratio of $HAuCl_4$:P4VP is 1:4. The size (r) of the gold nanoparticle is 14 nm. (d) Scanning electron microscopy and topography images of Au nanoparticles arrays on the SiO_2–Si substrates after removal of the PS-*b*-P4VP micelles by oxygen plasma treatment.

Fig. 2b shows the UV-vis absorption spectra of PS-*b*-(P4VP/AuNPs) thin film. The absorption band with a maximum at *ca.* 545 nm can be ascribed to the surface plasma (SP) band of Au nanoparticles, confirming the formation of Au nanoparticles.

The size distribution of the Au nanoparticles has been characterized using small angle X-ray scattering (SAXS) measurements (deposited on mica substrate). The experimentally measured SAXS curve is used to calculate the pair distance distribution function (PDDF), $p(r)$, which can be used to determine the overall shape and size of the scattering particles. The SAXS measurements were performed using a SAXSess camera (Anton-Paar, Graz, Austria) with a stand alone X-Ray generator (PANalytical, PW3830) operating at 40 kV and 50 mV with a sealed-tube Cu anode. Fig. 2c shows the PDDF of the scattering which is symmetrical, indicating that the particles are monodispersed and spherical.[24] The average diameter of each particle is determined to be 14 nm which is in agreement with the average size observed using the transmission electron microscopy.[22] Considering the size of the Au nanoparticles, loading of the Au precursors and total number of micelles in the system, the areal density of the Au nanoparticles is calculated to be around 6×10^{10} cm^{-2}.

To reflect the arrangement of the nanoparticles on substrate, field emission scanning electron microscopy (Jeol JSM 6340F) and topography (from atomic force microscopy) images are presented (Fig. 2d), where oxygen plasma treatment was performed on the PS-*b*-(P4VP/AuNPs) micellar film. After the oxygen plasma process, the block copolymer was completely removed and revealed reasonably good order of the nanoparticles.

Device characterization

The pentacene OFET memory devices were fabricated on *n*-type silicon wafer with 100 nm thermally grown silicon dioxide (SiO_2) on top. For perfluorinated copper phthalocyanine ($F_{16}CuPc$) memory devices, the SiO_2 layer has a thickness of 50 nm. A micellar film of PS-*b*-P4VP (~30 nm thick) or PS-*b*-(P4VP/AuNPs) (~50 nm thick) was spun coat on top of the SiO_2–silicon substrate. After spin-coating, the copolymer film was annealed at 110 °C in a vacuum for 72 h. The pentacene (sublimed grade) and $F_{16}CuPc$ (used without purification) were thermally evaporated, at a deposition rate of 0.1 nm s^{-1} and a pressure of 10^{-7} torr, to form a 45 nm and 40 nm thick film respectively. Finally, the gold source and drain contacts (thickness of 40 nm) were evaporated through a shadow mask, thereby defining a channel length of 75–150 μm and width of 500–4000 μm. Reference devices have a control SiO_2 only, or dielectric stack of pure PS-*b*-P4VP and SiO_2.

The output and transfer characteristics of the memory transistors were measured under vacuum (1×10^{-4} torr) in the dark at room temperature using a Keithley 4200 semiconductor characterization system and a cryogenic probe station (TTP6, Lakeshore). For the optical study, the devices were illuminated under vacuum using a Xenon lamp and the optical power density was fixed at ~74.4 mW cm^{-2} using neutral density filters. The light was illuminated directly on to the semiconductor. The temperature of the device was monitored to avoid errors induced by the heating of the device during the illumination. Heating during illumination is minimized by positioning the light source far from the sample (~18 cm).

Results and discussion

Fig. 3a and b present the typical output and transfer characteristics of the floating gate pentacene based OFET memory device (channel length of 100 μm and width of 1000 μm). The observed transistor characteristics indicate reproducible, stable device performance, suggesting that the additional floating gate layer does not interfere with standard OFET performance. The deposited polycrystalline pentacene thin film on the floating gate layer consists of grain sizes of approximately 0.25 μm (inset of Fig. 3a). The measured values of the typical hole mobility (μ_{hole}) and on/off ratio ($I_{on/off}$) were 0.2 cm^2 V^{-1} s^{-1} (maximum of 0.5 cm^2 V s^{-1}) and 10^4 –10^6 respectively. The threshold voltage, V_T, ranged from −3.8 V to −4.4 V obtained from the *x*-intercept of the linear portion of the plot of $I_D^{0.5}$ *versus* V_G.[25] The control transistor utilizing pure PS-*b*-P4VP (without Au nanoparticles) yielded comparable device performance: $\mu_{hole} = 0.1$–0.3 cm^2 V^{-1} s^{-1}, $I_{on/off} = 10^5$–10^6, and $V_T = -2.7$ V to −3.3 V (Fig. S1, ESI†).

An informative measure of the memory effect is the hysteresis window of the transfer curve upon double sweeping. The anticlockwise I_D–V_G hysteresis loop ($\Delta V_T \approx 7$ V) further indicates that there is a net hole trapping effect (Fig. 3b). This is in contrast to the control pentacene transistor which displays a negligible trapping effect. During the forward sweep, holding a negative voltage across the gate dielectric ("writing") causes the injection of holes from the pentacene to gold nanoparticles. This

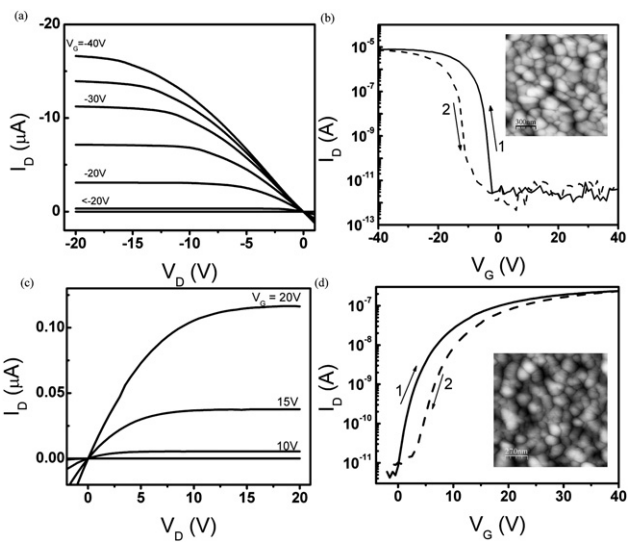

Fig. 3 (a) Output characteristics (I_D *versus* V_D) of a pentacene OFET memory utilizing PS-*b*-(P4VP/AuNPs), with a channel length of 100 μm and a width of 1000 μm. The gate voltage varies between 0 V to −40 V in steps of 5 V. (b) Double sweeping semilog plots of I_D–V_G transfer characteristics of the same pentacene memory device. The drain voltage (V_D) is −10 V. (c) Output characteristics of the $F_{16}CuPc$ OFET memory with channel length of 150 μm and channel width of 500 μm. (d) Double sweeping semilog plots of I_D–V_G transfer characteristics of the same $F_{16}CuPc$ memory device. The drain voltage is set at +5 V. The insets show the corresponding pentacene and $F_{16}CuPc$ morphology on the PS-*b*-(P4VP/AuNPs)/SiO_2 substrate.

phenomenon results in a shift in the electrical potential between the gate and semiconductor, and alters the charge distribution in the transistor. The positive charge stored in the Au nanoparticles "screens" the applied electric field and hence the threshold voltage shifts to a higher negative gate voltage during the reverse sweep. The number of stored charges (Δn) can be determined from the shift in V_T according to $\Delta n = (\Delta V_T * C_i/e) = 1.09 \times 10^{12}$ cm^{-2}, where C_i is the capacitance of the dielectric stack and e is the elementary charge.

We observed similar trapping phenomena in *n*-channel memory transistors based on perfluorinated copper phthalocyanine (F_{16}CuPc); Figs. 3c and d. The topography image of F_{16}CuPc thin film is shown in the inset of Fig. 3d, which has an average grain size of 0.19 μm. The electron mobility (μ_{elect}) and on/off ratio of F_{16}CuPc based memory transistor are determined to be 0.005–0.007 cm^2 V^{-1} s^{-1} and 10^3–10^4 respectively. The observed clockwise I_D–V_G hysteresis window indicates typical electron trapping behavior of the floating gate memory due to tunneling of the charge carriers from *n*-channel into the Au nanoparticles. At an operating voltage of 40 V, a positive threshold voltage shift of 3 V amounts to ~5.65 × 10^{11} cm^{-2} of stored electrons. The reference transistor with pure PS-*b*-P4VP exhibited no memory effects (see Fig. S2, ESI†); the μ_{elect} and $I_{on/off}$ are determined to be 0.003–0.0085 cm^2 V^{-1} s^{-1} and 10^3–10^4 respectively.

In comparing the memory performance between *p*-type and *n*-type transistors, it can be seen that there is a higher hole trapping effect in the Au nanoparticles from the pentacene channel as compared to electron trapping from the F_{16}CuPc channel. This may be attributed to differences in (1) the charge carrier density in the channel which affects the tunneling probability, and/or (2) the hole injection barrier (~0.5 eV between HOMOs of pentacene[26] and P4VP[27]) and the electron injection barrier (~1.3 eV between LUMOs of F_{16}CuPc[28] and P4VP). In particular, organic semiconductors with higher charge carrier densities may induce higher electric field coupling between the nanoparticle and the channel and hence a higher probability of tunneling. Further work is needed in order to have a better understanding and address the physical origins of the trapping.

The performance of the devices as electrically programmable and erasable memory cells was then evaluated. In general, the programming and erasing procedures of such devices consist of the application of voltage pulses of fixed duration. Depending on the polarity of the voltage pulses, holes or electrons can be injected into the floating gate. Such a modulation of the charge in the floating gate modifies the V_T of the memory transistor. During programming or erasing, the source and drain electrodes were grounded. After pulsing, the threshold voltage was determined by monitoring the I_D–V_G transfer characteristics. For the pentacene (or F_{16}CuPc) memory transistor, the programmed state can be defined when enough holes (electrons) are stored on the floating gate, shifting it to a higher V_T level. The erase state exists when trapped holes (electrons) are flushed out or electrons (holes) are stored on the floating gate, resulting in a lower V_T level. It should be noted that when pentacene or F_{16}CuPc OFET devices were fabricated with pure PS-*b*-P4VP (without Au nanoparticles), no significant shifts in V_T were observed under the same gate bias conditions that were used in the experiments. This device merely exhibited a degradation in OFET properties such as $I_{on/off}$, showing negligible shift in V_T (less than 1 V, see insets of Fig. 4) which may be attributable to bias-stress effects.[29]

Fig. 4a presents the transfer characteristics of the pentacene OFET memory upon application of a programming voltage ($V_{G,program} = -30$ V, 1 s). The entire transfer curve shifted towards negative voltages with a V_T shift of −6.7 V. The negative gate voltage pulses ($V_{G,program}$) cause negative shifts in V_T indicating holes are injected from the pentacene channel into the Au nanoparticles. This V_T shift was retained in subsequent voltage sweeps and increasing V_T shifts could be brought about by increasing $V_{G,program}$ (inset of Fig. 4a), further demonstrating the increasing hole trapping events. It should also be noted that the voltage values applied during the testing are too low for the electret mechanisms[19,20] to come into play. This is again illustrated by the inset of Fig.4a which displays no shift in the

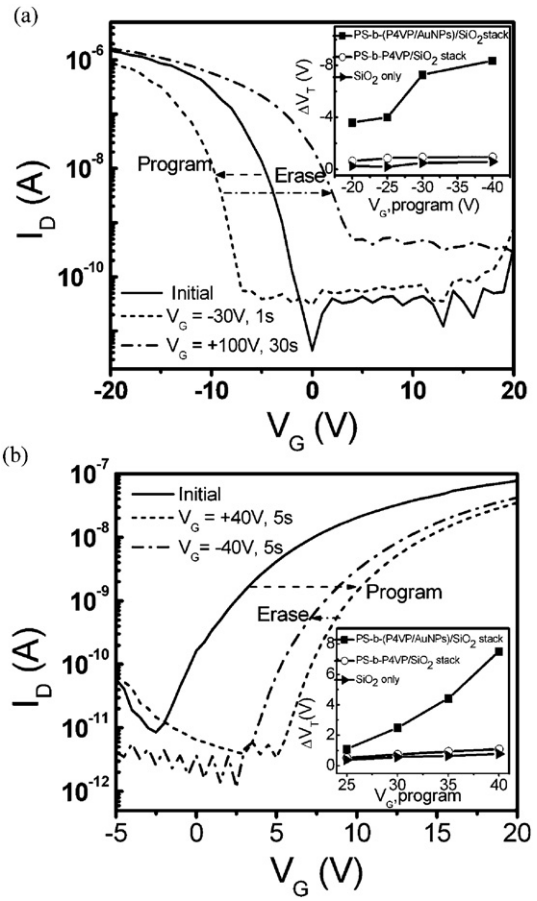

Fig. 4 Transfer characteristics obtained after different gate pulse conditions for (a) pentacene OFET memory with a channel length of 100 μm and a width of 1000 μm. The drain voltage, V_D, is −10 V. Programming: $V_G = -30$ V was applied for 1 s and erasing: $V_G = +100$ V was applied for 30 s. (b) F_{16}CuPc OFET memory with a channel length of 150 μm and a width of 500 μm. V_D is 5 V. Programming: $V_G = +40$ V was applied for 5 s and erasing: $V_G = -40$ V was applied for 5 s. $V_D = 0$ V during all programming and erasing operations. The insets show the corresponding shifts in V_T as a function of various programming voltages, $V_{G,program}$ for the memory and reference devices, at a charging time of 5 s. The reference devices have a control SiO_2 only, or dielectric stack of pure PS-*b*-P4VP and SiO_2.

threshold voltages on application of programming voltage to the OFET utilizing pure PS-*b*-P4VP layer.

On the other hand, the *erasing* operation could not be brought about even upon the application of a higher positive gate voltage. Repetitive erasing cycles ($V_{G,erase}$ = +40 V to ~+80 V, 30–300 s) also displayed little effect on the programmed state. This may be comprehended by considering that for V_G >0, the channel is depleted and the lifted channel potential reduces the effective electric field. Most of the potential drop also occurs in the 100 nm thick control thermal oxide layer. But the main reason is that the erasing efficiency is largely dependent on the presence of induced minority carriers in the organic semiconductor. The unipolar (hole-only) nature of transport across the pentacene, and the large work function difference between the Au electrode (~5.1 eV) and lowest unoccupied molecular orbital (LUMO) level of pentacene (~3 eV) prevents efficient electron injection and transport at positive gate voltages. Application of erasing voltages in excess of ~80 V (fields of > 5 MV cm^{-1}) finally brought about a positive shift in V_T (Fig. 4a). The positive shift in V_T was accompanied with a high gate leakage current (see Fig. S3a, ESI†) implying that the high erasing voltage brought about a possible breakdown in the dielectric and hence, the erasing operation occurred mainly through high field emission of holes from the floating gate and from the gate electrode through the control thermal oxide.

Charge programming was also performed on the F_{16}CuPc based memory transistor by pulsing the gate voltage at 40 V for 5 s (Fig. 4b). The transfer curve shifts to the positive voltage direction (V_T shift of 7.5 V) can be explained to be due to electron injection from the *n*-channel into the Au nanoparticles. The increasing electron trapping events can also be observed through the increase of V_T with increased $V_{G,program}$ (inset of Fig. 4b). Since most of the organic semiconductors exhibit only single carrier (electron or hole) operation mode, the efficiency of erasing in the F_{16}CuPc memory transistor is also low. This effect can again be seen in Fig. 4b, where we observed little V_T shift on the programmed curve after the erasing operation ($V_{G,erase}$ = −40 V for 5 s). Fig. 5 summarizes the various mechanisms that occurred with programming and erasing operations for each *p*- and *n*-channel memory transistor.

Data presented in the prior sections illustrate efficient programming operations enabled by direct tunneling of charge carriers from the channel to the floating gate. The effectiveness of the transistor memory is however compromised with the use of a high erase voltage and hence increased leakage currents. The high erase voltage is likely to degrade cell reliability and may interfere with subsequent read or programming operations. Although thinner control oxides may be utilized to lower the erasing voltages and improve the programming/erasing times, leakage and charge retention is likely to be compromised; necessitating the use of high-*k* dielectric layers.[30,31] It can also be envisioned that the fabrication of an organic memory transistor through the employment of ambipolar, bi-channel,[32] or a blend of *p* and *n*-type materials offers an effective programming-erasing approach for both hole and electron trappings. In addition, we have recently improved electron trapping in PS-*b*-(P4VP/AuNPs) through the use of an aluminum electrode which has a reduced electron injection barrier.[27] Hence, the utilization of asymmetric source–drain electrodes for efficient hole and electron injections offers an alternative approach.

The approach proposed herein to lower the erasing voltages is by utilization of a photoinduced charge transfer mechanism,[33–36] *i.e.* enabling minority charge carrier injection with the use of light. Transfer of nonequilibrium photoinduced charges from the

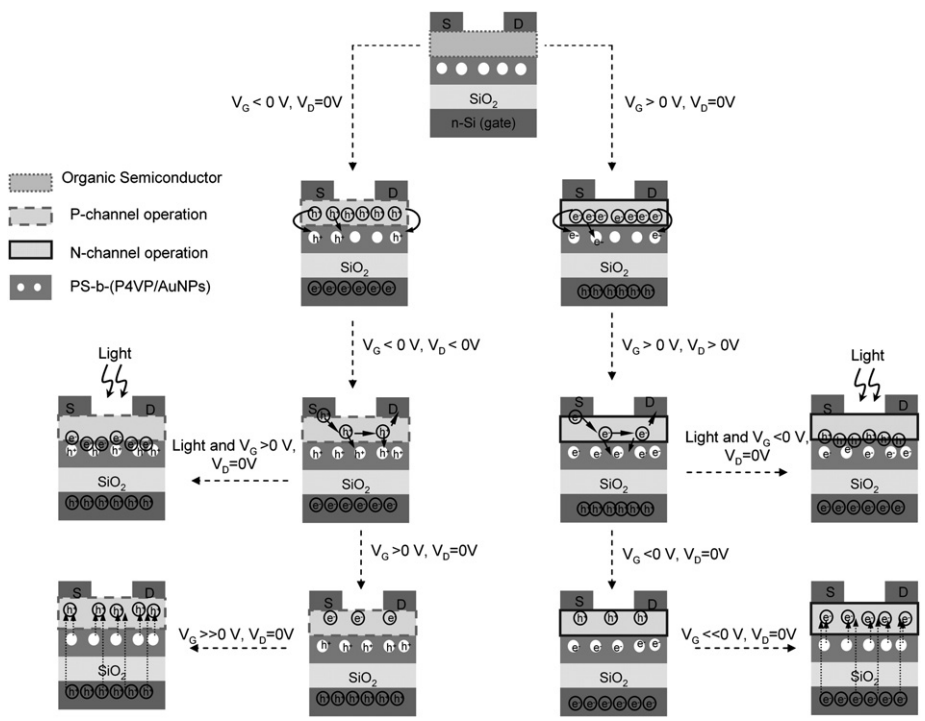

Fig. 5 Schematic of memory transistor (*p*- and *n*-channel) under various operations.

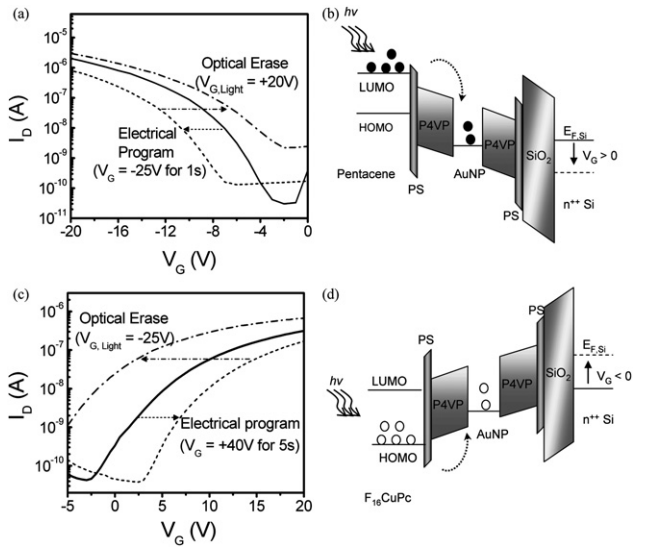

Fig. 6 (a) Semilog plots of transconductance characteristics of a pentacene OFET memory device, measured at a fixed $V_D = -20$ V in the dark, after programming operation ($V_G = -25$ V for 1 s) and after illumination of the device for 30 s. During illumination, a positive gate voltage of +20 V is applied. (b) Energy band diagram of the pentacene OFET memory under illumination and positive electric field. Electrons are represented by solid circles. The dotted arrows represent the flow of charge carriers. (c) Semilog plots of transconductance characteristics of a F_{16}CuPc OFET memory device, measured at a fixed $V_D = 10$ V in the dark, after programming operation ($V_G = +40$ V for 5 s) and after illumination of the device for 30 s. During illumination, a negative gate voltage of −25 V is applied. (d) Energy band diagram of the F_{16}CuPc OFET memory under illumination and negative electric field. Holes are represented by open circles.

organic semiconductor to the polymeric dielectric layer and localization of these charges by deep traps in the dielectric[37] and/or semiconductor-dielectric interface[33,38] have been reported. Illumination of the memory transistors thus provides a source of minority charge carriers for efficient erasing operations. Fig. 6a displays the transfer characteristics of pentacene OFET memory after programming ($V_G = -25$ V, 1 s) and illumination assisted erasing (under $V_G = +20$ V, 30 s). A shift of the dark transconductance characteristics toward lower V_G resulted and a large memory window of 11 V is attained. It should be noted that all the transfer characteristic measurements were done in the dark in order to exclude the effect of accumulation of photoelectrons under the source electrode.[39] The observed optical memory behavior that involves the charge transfer between the Au nanoparticles and pentacene are described hereafter. First, upon illumination, photoexcitation results in the generation of photoinduced charge carriers (electrons and holes). With the application of a positive electric field at the semiconductor–dielectric interface during illumination, the electron-hole pairs are separated; electrons are transferred and trapped into the Au nanoparticles and/or interfaces between pentacene–PS-*b*-P4VP (Fig. 6b). Upon switching off the photoexcitation, the OFET memory displays a characteristic governed by the stored charges in the Au nanoparticles. These stored electrons in the Au nanoparticles effectively provide a built-in potential across the channel, leading to a shift in V_T. It is also observed that higher positive gate voltages under illumination produced greater threshold voltage shifts since more electrons are transferred to pentacene and trapped into the Au nanoparticles and/or its interfaces. This effect is consistent with a model proposed in the literature wherein the gate electric field assists in the transfer of charge.[37] In particular, a significant difference in current output at $V_G = 0$ V (~5 orders of magnitude) was observed with a higher positive gate voltage of 40 V during optical erasing mode (Fig. S4, ESI†). This ability to read out the state of the memory system without the application of a gate voltage ensures a good retention performance because the de-trapping events induced on application of a reading voltage are avoided.

As in pentacene based memory transistor, optical erasing is implemented on F_{16}CuPc based memories to enable minority carriers (hole in this case) injection with the use of light. As shown in Fig. 6c, the increase of I_D is caused by the creation of a large number of charge carriers due to the photoinduced charge transfer between the F_{16}CuPc channel and the Au nanoparticles. The same explanations reported in an earlier section can be used: With the generation of photoinduced charge carriers and the application of a negative electric field during illumination, the electron-hole pairs are separated and holes are transferred and trapped into the AuNPs and/or its interfaces (Fig. 6d). Upon switching the photoexcitation off, the trapped holes in the AuNPs will lower the potential barrier between the source and the F_{16}CuPc channel, leading to a negative V_T shift of 9 V.

The high conductance state ("ON" state) induced by the optical erasing for both memory devices can be switched back to the 'programmed' or low conductance state ("OFF" state) using a single pulse of negative (for pentacene) or positive (for F_{16}CuPc) gate voltage, so that the channels are in the accumulation mode and provide the necessary charge carriers to recombine with the trapped electrons or holes. The insets of Fig. 7 present a series of program/erase cycles for both pentacene and F_{16}CuPc memory transistors, demonstrating that the responsivity of the OFET memory devices can be controlled using a combination of the gate voltage and the incident light source to perform the write, store and erase operations. Due to the lack of sophisticated systems to control the illumination and voltage simultaneously, the measurements could not be done at a finer time scale and did not allow measurement of the switching time between the electrical programming and optical erasing operations. Nevertheless these results are favourable and indicative of the potential of the system.

Next, we study the retention of the shifted characteristics after programming and erasing operations. A good retention property is the ability to maintain the ON/OFF ratio over time.[20,40] In the pentacene OFET memory, the OFF currents were measured every 10 s after an application of $V_G = -25$ V for 5 s, while the ON currents were measured after an application of $V_G = 40$ V for 30 s (under illumination) (Fig. 7a). In the initial OFF state, the current decreases slightly, suggesting that the reading gate voltage of −10 V is sufficient to 'write' the memory device. After which the drain current starts to increase gradually, indicating that the trapped holes are slowly discharged from the gold nanoparticles. In the ON state, a gradual discharge of the trapped electrons over 1000 s is also observed. The ON/OFF ratio was measured to be 10^4 at the beginning and decreased to 10^3 after 1000 s. Similarly for the F_{16}CuPc memory device, the

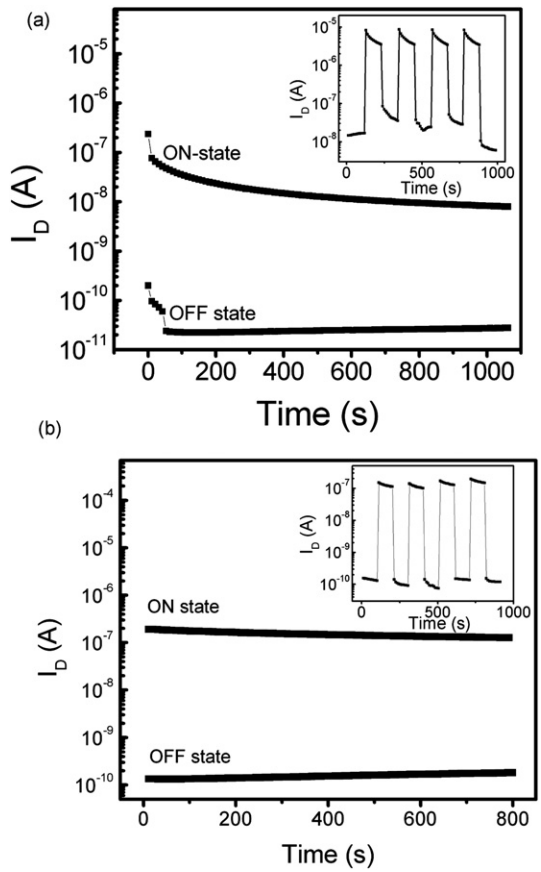

Fig. 7 (a) Time responses of the drain current at $V_G = -10$ V and $V_D = -20$ V, after programming ($V_G = -25$ V for 5 s) or erasing ($V_{G,Light} = +40$ V for 30 s) operation for the pentacene OFET memory. The channel width and length are 4000 μm and 125 μm respectively. The inset shows the dynamic responses after programming ($V_G = -40$ V for 5 s) and erasing ($V_{G,Light} = +40$ V for 30 s) of the pentacene OFET memory device (channel width is 4000 μm and length is 75 μm) at $V_G = -10$ V, $V_D = -20$ V. (b) Time responses of the drain current at $V_G = 3$ V and $V_D = 10$ V, after programming ($V_G = 40$ V for 5 s) or erasing ($V_{G,Light} = -25$ V for 30 s) operation for the F_{16}CuPc OFET memory. The channel width and length are 1000 μm and 100 μm respectively. The inset shows the dynamic responses after programming ($V_G = +40$ V for 5 s) and erasing $V_{G,Light} = -25$ V for 10 s) of the F_{16}CuPc OFET memory device at $V_G = +3$ V, $V_D = 10$ V.

individual OFF and ON states is monitored at time intervals of 10 s in the dark after applying programming and erasing bias of $V_G = 40$ V for 5 s and $V_G = -25$ V for 30 s (under illumination) respectively, Fig. 7b. In comparison to the pentacene memory, only a small amount of decay (rise) in the ON (OFF) state drain current is observed and the ON/OFF ratio was maintained at 10^3 over 1000 s. As an estimation, the time required for the ratio between ON-current and OFF-current states to decrease to at least two-orders of magnitude difference was found to be more than 10,000 s for the pentacene memory and 80,000 s for the F_{16}CuPc by extrapolation of the ON-current and OFF-current state curves. This difference in retention behavior between the two memories may be explained by the variation in barrier heights seen by the trapped charges, as explained previously. In strong contrast, the drain currents in the reference devices decayed rapidly after switching off the light source due to electron detrapping/recombination.[33,36,41]

Conclusion

In conclusion, we have demonstrated OFET memories where *in-situ* synthesized Au nanoparticles in block copolymer nanodomains functioned as charge storage elements. Both *p*-type pentacene and *n*-type F_{16}CuPc OFET based memories have been demonstrated, with large charge capacity, stable and programmable-erasable properties. The unipolar nature of transport across organic semiconductors prevents efficient erasing operations. Optical excitation is hence utilized to induce photogenerated charge carriers for the erasing operation. The responsivity of this OFET memory device can hence be controlled using a combination of the gate voltage and the incident light source to perform the write, store and erase operations. An enhanced performance, in terms of operating voltages and retention time can be expected on using ambipolar organic semiconductors and/or asymmetric source–drain electrodes (for example, gold and aluminum or calcium electrodes) for efficient hole and electron injections into the floating gate. Nevertheless, these results indicate the utility of the block copolymer-nanoparticle composite in organic transistor memories.

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