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Design of Non-destructive Single-sawtooth Pulse Based Readout for STT-RAM by NVM-SPICE

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Abstract—Spin-transfer torque random access memory (STT-RAM) is one promising candidate for future non-volatile memory based computing, because of its fast access time, high integration density and non-volatility. One major challenge of STT-RAM is to design robust readout circuit in the presence of large MTJ resistance variations. The lack of SPICE-like platform hinders the design validation for hybrid STT-MTJ and CMOS memory structure and readout circuits. In this paper, we have introduced the recently developed NVM-SPICE for the design of STT-RAM with large memory array and also non-destructive single-sawtooth pulse based STT-RAM readout. Compared to the simulation by equivalent circuit, the NVM-SPICE shows 117x faster simulation time for large-array STT-RAM. Moreover, validated by the NVM-SPICE, the proposed single-sawtooth pulse based readout shows 2x faster read latency with 8x larger sensing margin than the existing readout schemes.

I. INTRODUCTION

Featured with fast access speed, high density and zero standby power, the emerging non-volatile memories (NVM) at nano-scale such as spin-transfer torque magnetic tunnel junction (STT-MTJ) device, phase change memory (PCM) and etc. have introduced promising future for the new non-volatile computing [1], [2], [3], [4], [5], [6], [7], [8], [9]. Their tremendous advantages over the currently prevailing NVM (i.e. Flash memory) make the nano-scale NVMs not only the candidates to serve as the next-generation storage, but also replace DRAM and SRAM in conventional computing systems. Among those nano-scale NVM technologies, STT-MTJ based random-access memory (STT-RAM) has exhibited best potential due to its fast speed ($< 10ns$), high integration density ($6\sim 8 F^2$ where F is the feature size) and virtually unlimited endurance ($> 10^{15}$).

From the memory design perspective, reliability under the presence of large MTJ resistance variation becomes one critical issue to consider. One example is how to design robust sensing circuit for reliable readout. One destructive self-reference readout has been proposed in [2] to overcome the bit-to-bit resistance variation. However, the destructive nature of this approach requires a write-back operation after every readout, which slows down the read latency. Alternatively, a non-destructive readout scheme has been proposed in [3], which is faster and more power efficient but has limited sensing margin. Moreover, from the design validation perspective, the obstacle is the lack of SPICE-like simulator for hybrid STT-MTJ/CMOS circuit and system validation. The current

approach is to replace the STT-MTJ devices with complicated equivalent circuits for simulation, which is however very time-consuming for validation of the large-array STT-RAM. The newly introduced STT-MTJ needs to be included into a circuit simulator like SPICE by a similar fashion as we dealt with CMOS devices, which provides physics-based BSIM model with geometry-dependent parameters.

In this paper, one newly developed NVM-SPICE is reviewed for hybrid STT-MTJ and CMOS simulation, including validation of large-array STT-RAM. Then, a single-sawtooth pulse based readout design for STT-RAM has been proposed and also validated by NVM-SPICE. Compared to the previous work [2], [3], 2x faster read latency and larger sensing margin compared are observed. The rest of the paper is organized in the following manner. In Section II, the NVM-SPICE is discussed for large-array STT-RAM. In Section III, the previous readout schemes are reviewed and the single-sawtooth pulse based readout has been proposed. Experiment results are presented in Section IV with conclusions in Section V.

II. HYBRID STT-MTJ/CMOS SIMULATION

Design validation by simulation is one critical step in the circuit and system design flow, especially true for nano-scale NVMs. Unfortunately, current commercial tools lack the support for the nano-scale NVM devices. In this section, we will review the present approaches for hybrid STT-MTJ and CMOS design validation.

Fig. 1. Simplified diagram of equivalent circuit based STT-MTJ model proposed in [4]

TABLE I
A FULL LIST OF PARAMETERS FOR STT-MTJ MODEL

Name	Model parameter	Units	Default	Example
vcp	voltage-dependent coefficient for parallel state	-	0.01	0.1
vcap	voltage-dependent coefficient for anti-parallel state	-	0.9	0.65
p	pre-factor of the spin-transfer term and driving current ratio	-	6.37	6.37
gamma	electron gyro-magnetic ratio in Landau-Lifshitz-Gilbert equation	$(sA/m)^{-1}$	221k	221k
ms	saturation magnetization of material	kA/m	800k	800k
hk	effective anisotropy field	kA/m	29.05k	29.05k
rp	resistance value of parallel state	Ω	1230	1k
rap	resistance value of anti-parallel state	Ω	2650	5k
damping	damping constant in Landau-Lifshitz-Gilbert equation	-	0.01	0.005
Name	Instance parameter	Units	Default	Example
phi0	initial radian for internal state variable ϕ	rad	1	1
theta0	initial radian for internal state variable θ	rad	0.001	0.005

A. Simulation with equivalent circuit based SPICE macro-model

The STT-MTJ has been modeled by a number of subcircuits in [4], which has a simplified diagram shown in Figure 1. To emulate the electrical characteristics of an STT-MTJ, a two-terminal subcircuit that consists of dozens of additional devices has been proposed to produce the STT-MTJ behaviors like hysteresis loop, bias voltage dependence of the resistance and the critical switching current versus the critical switching time. Such a SPICE behavior is useful for early stage prototyping, however, is not suitable for the large scale designs where the accuracy and simulation speed are the main concern. Firstly, due to the complexity of equivalent circuit, the simulation is extremely time-consuming because each STT-RAM cell is modeled by a complicated equivalent circuit. Secondly, the missing of physical details such as geometry-dependent relations makes the model inaccurate or hard to scale.

B. Simulation with internal-state-variable based SPICE model

The intense researches on the physics of STT-MTJ can help build physics-based model by identifying the internal-state-variable [7], [8]. As such, one can implement physics-based model in SPICE for NVM devices similarly as we dealt with BSIM MOSFET model. For example, a STT-MTJ physics-based model with giant magnetoresistance effect, tunneling effect and spin-transfer torque effect has been proposed in the work [8]. Such model is based on the identification of internal-state-variables of magnetization angles, in addition to the conventional state variables of nodal voltages and branch currents. The proposed STT-RAM model with magnetization-angle state-variable is implemented in NVM-SPICE [10], which is a SPICE-extended simulator supporting many newly introduced nano-scale NVM devices. As one illustration example, all the supported parameters for STT-MTJ model are listed in the Table I. More examples of how to apply NVM-SPICE in NVM circuit and system design can be found in [10].

III. SINGLE-SAWTOOTH PULSE BASED READOUT

Existing STT-RAM readout schemes to avoid disturbance of large STT-MTJ resistance variation usually require several

steps, which slows down the read latency. We show that by applying a single-sawtooth pulse and exploiting the resistance roll-off of STT-MTJ, the robust readout can be achieved within one cycle.

A. Previous works for STT-RAM readout

Fig. 2. The existing schemes for STT-RAM readout: (a) basic STT-RAM readout (b) destructive self-reference readout in [2] (c) non-destructive self-reference readout in [3]

1) *Basic STT-RAM readout*: The basic voltage sensing scheme for the popular 1T-1MTJ structure STT-RAM is shown in Figure 2 (a). The reference voltage is set to satisfy

$$I_r \cdot (R_{AP} + R_t) > V_{ref} > I_r \cdot (R_P + R_t)$$

where I_r is the applied read current, R_{AP} , R_P and R_t are the MTJ anti-parallel state resistance, parallel state resistance and cell transistor on-state r_{ds} , respectively. However, in the presence of bit-to-bit MTJ resistance variation, the reference voltage has to fulfill

$$\text{Min}(V_{BL,AP}) > V_{ref} > \text{Max}(V_{BL,P})$$

where a satisfying V_{ref} may not exist when variation is large.

2) *Destructive self-reference readout*: In order to achieve reliable readout in the presence of large MTJ resistance variation, a self-reference readout is presented in [2], whose diagram is shown in Figure 2 (b). The read-operation is done in five phases:

- the read-current I_r is applied and its bit-line voltage is stored in C1;
- the “0” (parallel state) value is written to the target cell;
- the read-current I_r is applied again and its bit-line voltage is stored in C2;
- the sense amplifier is enabled and voltages of C1 and C2 are compared; and the output is “1” (anti-parallel state) if V_{C1} is greater than V_{C2} and “0” otherwise;
- the output value has to be written back to the destructed cell.

Therefore in terms of both speed and power, the overhead brought by write-back may be large for this scheme.

3) *Non-destructive self-reference readout*: The current-dependent resistance roll-off can be observed for STT-MTJ as shown in Figure 3. By exploiting the fact that the roll-off slope of the anti-parallel state is much greater than that of parallel state, a non-destructive self-reference readout is proposed in [3] with diagram shown in Figure 2 (c).

The read-operation is done in three phases:

- the read-current I_{r1} is applied to achieve its corresponding resistance R_1 ;
- the read-current I_{r2} is applied to achieve its corresponding resistance R_2 ;
- the sense amplifier is enabled and R_1 and R_2 are compared; The output is “1” if two values are significantly different and “0” otherwise.

As such, the non-destructive self-reference readout can improve the read latency by eliminating the two time-consuming write phases. However, this scheme still has limited performance in read latency and sensing margin as discussed below.

B. Single-sawtooth pulse based readout

Although the variation can be overcome by the two self-reference schemes above, they still involve several phases which slow down the read latency. A single-sawtooth pulse based readout is proposed in Figure 4 to reduce the read latency into one cycle. In the following, we will show that within one cycle, by applying a single-sawtooth pulse to bit-line and obtaining the second derivative of corresponding bit-line voltage, the variation disturbance during readout can be totally avoided.

Fig. 3. The measured R-I sweep curve of a typical MgO based MTJ in [2]

Fig. 4. Diagram of proposed single-sawtooth pulse based readout

Assume the applied sawtooth pulse to bit-line can be expressed as

$$i(t) = k_s \cdot t \quad (1)$$

where the k_s denotes the current rising rate. Also, the R-I curve slope in Figure 3 is assumed linear for simplification, thus the current-dependent resistance can be expressed as

$$\begin{aligned} R_{AP}(i) &= R_H - k_{AP} \cdot i \\ R_P(i) &= R_L - k_P \cdot i \end{aligned} \quad (2)$$

where R_H and R_L are the resistances of R_{AP} (anti-parallel) and R_P (parallel) when $i = 0$. Therefore, the bit-line voltage produced by the applied sawtooth pulse can be expressed as

$$\begin{aligned} V_{BL,AP}(t) &= i(t) \cdot R(i) = R_H \cdot k_s \cdot t - k_{AP} \cdot k_s^2 \cdot t^2 \\ V_{BL,P}(t) &= i(t) \cdot R(i) = R_L \cdot k_s \cdot t - k_P \cdot k_s^2 \cdot t^2 \end{aligned} \quad (3)$$

It can be observed that the bit-line voltage depends on the R_H and R_L , which will introduce readout errors in the presence of large variations. Nevertheless, the readout dependency on R_H and R_L can be eliminated if the second derivative of bit-line voltage can be obtained

$$\begin{aligned} \frac{d^2 V_{BL,AP}}{dt^2} &= -2 \cdot k_{AP} \cdot k_s^2 \\ \frac{d^2 V_{BL,P}}{dt^2} &= -2 \cdot k_P \cdot k_s^2 \end{aligned} \quad (4)$$

Note that the current-dependent resistance roll-off slopes k_{AP} and k_P are not fabrication-process sensitive, and k_P is a close-to-zero while k_{AP} is much larger as indicated in Figure 3, the robust readout can be easily achieved under the proposed scheme right after the sawtooth pulse is applied. Thus compared with previous work where several steps are required, the

proposed scheme can potentially reduce the read latency into one cycle time

The circuit to implement second-derivative operation can be designed as two differentiators in series, and each differentiator can be implemented as either an OPAMP-based feedback circuit or a RC-based high-pass filter. RC-based high-pass filter provides simple differentiation but has limited gain, while OPAMP-based one can generate output with significant sensing margin. Three different circuits to implement the second-derivative operations with trade-off between circuit complexity and readout sensing margin as follows:

- Pure OPAMP: two OPAMP-based in series;
- Hybrid: first-stage with OPAMP-based and second-stage with RC-based high-pass filter;
- Pure RC: two RC-based high-pass filters in series.

In this paper, the hybrid approach is deployed for the single-sawtooth pulse based readout as shown in Figure 4.

IV. NUMERICAL EXPERIMENTS

In this section, the simulation speed is first compared between circuit with equivalent subcircuit macromodel and physics-based model. Then the proposed single-sawtooth pulse based readout to avoid resistance variation for STT-RAM is validated. All the hybrid STT-MTJ/CMOS simulation are conducted using NVM-SPICE, and on the same work station with Intel Core i5 CPU and 8G RAM.

A. Simulation speed comparison

The 1T1MTJ structure STT-RAM array with transient analysis for a write operation is set as the test bench circuit. The circuit netlist is described in two versions which only differ in terms of STT-MTJ model, one using the equivalent circuit based SPICE macromodel in [4], and one using the intrinsic physics-based model in NVM-SPICE. Necessary modifications are made to port the HSPICE subcircuit netlist provided by [4] compatible with Berkeley SPICE styled NVM-SPICE. The simulation duration is set 20ns with time step of 0.1ns.

TABLE II
SIMULATION TIME COMPARISON FOR STT-RAM ARRAY USING
DIFFERENT SIMULATION APPROACHES (UNIT IN SECOND)

array size	Macromodel in [4]	NVM-SPICE	speedup
8×8	2.522	0.257	10x
16×16	98.131	1.87	52x
32×32	1119.99	11.533	97x
64×64	22188.8	189	117x

Table II shows the runtime comparison of the two different simulation approaches for different array sizes. It can be observed that the simulation using NVM-SPICE intrinsic physics-based model is 10x~117x faster than the equivalent circuit approach. The advantage will be even larger when the array size increases. For typical memory array size of hundreds by hundreds, the speedup can be expected more than 100x.

B. Single-sawtooth pulse based readout

The proposed single-sawtooth pulse based readout scheme in Figure 4 along with the STT-RAM array circuit are simulated together using NVM-SPICE intrinsic STT-MTJ model. The STT-MTJ model parameters are set with $cap = 0.9$, $cp = 0.1$, $rap = 2650$ and $rp = 1230$ with explanations for each parameter in Table I; the BSIM4.7 model is used for all the transistors with $L = 90nm$ and $W = 2\mu m$; the $I_w = \pm 900\mu A$ is used for write operation, and read current I_r rises from 0 to $200\mu A$ within 25ns, which produces a sawtooth pulse with $k_s = 8000A/s$.

The single-sawtooth pulse based readout with second derivative circuit achieved in all three ways are simulated with results shown in Figure 5. It can be observed that for the bit-line response to the applied sawtooth pulse current, the bit-line of AP state STT-MTJ exhibits some non-linearity while that of P state is almost linear. The first derivative of bit-line signals shows larger difference between AP state and P state cases, where the that of P state is almost constant while that of AP state has a considerable slope. The output difference in this stage still cannot avoid the readout fault caused by resistance variation according to Equation 3. The second derivation of bit-line voltage, which is variation tolerant according to Equation 4, shows separated voltage level for AP state and P state, which is also easy to distinguish by later sensing stage. The pure OPAMP based one can produce voltage levels separated by around 200mV between AP state and P state, and that of hybrid based one is around 30mV, and less than 0.2mV for pure RC based one. Table III shows the readout performance comparison between the proposed scheme and previous work.

TABLE III
COMPARISON OF DIFFERENT READOUT SCHEMES FOR STT-RAMS

Scheme	Read latency	Sense margin (mV)
destructive readout [2]	2 read cycles + 2 write cycles	76.6
non-destructive readout [3]	2 read cycles	12.1
proposed	1 read cycle	15 (hybrid) 100 (OPAMP)

V. CONCLUSION

In this paper, the newly developed hybrid NVM and CMOS simulator NVM-SPICE is illustrated with the support for STT-MTJ memory cell design. The STT-RAM model implemented in the simulator is all-physics-based-model similar to BSIM model for MOSFET. Compared to the equivalent circuit model based approach, the NVM-SPICE exhibits more than 117x faster simulation speed for large-array STT-RAM. Moreover, a single-sawtooth pulse based readout is proposed for STT-RAM, which is able to achieve reliable readout in the presence of large MTJ resistance variation. This scheme is non-destructive and is able to reduce the read latency into one cycle. Validated by the NVM-SPICE, the proposed scheme achieves about 2x faster read latency with similar sensing

Fig. 5. Transient response of bit-line voltage, first derivative, and second derivative to the applied sawtooth pulse for pure OPAMP, hybrid and pure RC based circuit, respectively

margin for hybrid scheme and 8x larger sensing margin for OPAMP scheme, when compared to the existing approaches.

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