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An improved inverter-based readout scheme for low-power ISFET sensing array

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Digital read-out scheme in ISFET sensing array is more advantageous when compared to the analog counterpart because of its lower power consumption, less area and less susceptible to environmental noise and parasitic. This work proposes an improved readout scheme in which each ISFET is stacked with a CMOS inverter to form a pH-to-time converter. pH level of the solution regulates the strength of the ISFET, which in turn modulates the delay of the stacked inverter and hence the pulse-width of the output signal. Simulation results using 0.18 $\mu\text{m}/2.5\text{V}$ CMOS process show that the modulated pulse width changes linearly over a wide range of pH. Our design achieves 5 orders of magnitude smaller leakage, 40% lower dynamic power consumption while requires only 50% of silicon area when compared to the conventional design. It is therefore more suitable for large ISFET array implemented in nano-scale CMOS technologies.

Introduction: Ion-sensitive field effect transistor (ISFET) is a versatile technology for measuring environmental, biomedical and chemical information. With recent advances in CMOS technology, ISFET devices can be integrated in analytical lab-on-chip for very large sensing array implementation [1, 2]. Unlike normal CMOS transistors, the gate of the ISFET device is left floating to interface with the chemical solution via a layer of insulator. In its most basic sensing form, ISFET translates the concentration of H^+ ion (and thus pH of the solution) to electrical signal by the means of threshold voltage shift of the underlying sensing device. Many research works [3-5] have exploited different readout schemes to translate the pH level of the solution to the corresponding output voltage signal, focusing on improving linearity and sensitivity. These circuits normally contain an analog front-end, followed by an on-chip ADC. [5] simplifies this analog front-end by using two ISFET devices to form a pH-to-time converter so that both on-chip ADC and other analog blocks such as op-amps can be eliminated. This approach offers the best compactness for large-scale implementation with a good ability to immune with environmental noises. In this letter, we propose a new design to improve the performance of the pH-to-time converter presented in [5], focusing on dynamic and leakage power consumption for large array implementation.

Power and leakage issues in the conventional pH-to-time converter: First, floating voltage (V_{FG}) at the gates of the ISFET devices in the conventional design [5] (Fig. 1a) leads to unwanted leakages in each sensing pixel. As ISFET is meant for large sensing array, this potentially high leakage will have a negative impact on the energy consumption of the whole system. For example, if potential of the reference electrode (V_{Ref}) is set so that V_{FG} is zero at pH = 12, this voltage will drift to 0.5 V when pH changes to 2 (assuming a sensitivity of -50 mV/pH). As a result, both devices are weakly turned on and thus its leakage current becomes substantial. In practice, this situation can be worst if V_{Ref} is set to a higher value or the floating gate voltage is shifted due to time or temperature drifting effect. Similarly during the sensing period, V_{FG} may never get to full swing due to the coupling effect and therefore can potentially draw a large DC current from the power supply. Second, the input ramp signal (V_{in}) is coupled directly to the floating gate of the sensing device and hence requires a large coupling capacitance (e.g 0.1 pF per pixel [5]), resulting in a high dynamic power and silicon area consumption.

Fig. 1 Schematic of the (a) conventional (b) proposed read-out scheme

Proposed design: From the above observations, our new sensing pixel (Fig. 1b) only needs one NMOS ISFET device stacked with a CMOS inverter, as shown in Fig. 1. The sizes of N_1 and P_1 are very small when compared to the size of the ISFET device. pH of the chemical solution will regulate the threshold voltage of the ISFET sensing device, which in turn will control the pull-down strength of the N_1 -ISFET path. As a result, the pulse width of the output signal (V_{out}) is modulated by the pH level of the solution. During standby, no signal is applied to the inverter and thus N_1 is completely off. During sensing, the ramp signal only needs to drive small devices P_1 and N_1 . In addition, our proposed design only requires one sensing device, leading to 50% area reduction when compared to the conventional design. More importantly, the ramp signal does not apply to the floating gate and thus does not affect the chemical solution interface. In an array implementation, the inverter P_1 - N_1 can also be shared by multiple ISFET devices to further suppress leakage and save area.

Simulation set-up and results: Both conventional and proposed designs were simulated using a 0.18 $\mu\text{m}/2.5\text{V}$ CMOS technology. Sizing of the ISFET devices were set to 50 $\mu\text{m} \times 50 \mu\text{m}$. Spice behavioural model of the ISFET device [6] was used to simulate the electronic-solution interface. Fig. 2 illustrates the output waveforms of the proposed design when pH level changes from 2 to 12, assuming a sensitivity of -50 mV/pH and the period of V_{in} is $T = 0.1$ ms. It can be seen from Fig. 3 and the zoomed in on the left of Fig. 2 that the width of the output pulse increases linearly with pH. To investigate the output response versus different V_{in} duration, we varies T from 0.1 ms to 1 ms and 10 ms. Interestingly, the proposed design is still able to maintain its linearity at different T , as shown in Fig. 3. It is therefore suitable for high throughput applications where output of each pixel must be quickly obtained with a faster clock frequency. The maximum clock frequency depends on the load capacitance and the conductivity of the transistors. In our set-up, maximum allowable ramp input frequency is 20 MHz, which is very high in bio-sensing applications.

Fig. 2 Simulation waveforms of the proposed read-out scheme.

Fig. 3 The proposed design achieves linearity over a wide range of pH and different period of the ramp input signal.

Regarding the width modulation, change in the pulse width of the conventional design is significant when compare to T [5] (10% of T per pH when $T = 33$ ms). Our pulse width response is only 1% T per pH. With input clock in the range of milliseconds, our design gives a resolution of a few tens of microseconds per pH. This time range can be easily resolved using on-chip counter. If a 20 MHz on-chip counter were used, ideally the proposed design will be able to achieve a sensitivity of 0.005pH, which is more than enough for most of pH sensing applications.

Fig. 4 compares the leakage and dynamic current of the proposed and the conventional designs. During standby, the input signal is

grounded and thus the CMOS inverter in the new design is strongly turned off. As a result, its leakage is only a few pA. Furthermore, this leakage is independent from the pH level. In contrast, the gates of the ISFETs are floating and their potentials are decided by both pH level and V_{ref} . If V_{ref} is set to the same value for both conventional and proposed design, the leakage from the conventional circuits is about $10^5\times$ higher than the new design and is close to a few hundred nA. For example, its leakage is 770 nA at pH equal to 6. This is significant when compared to the dynamic current, shown in Fig. 4b. In average, the new circuit consumes 6 μA while that of the conventional design is 10 μA .

Fig. 4 Leakage and dynamic current comparison of the proposed and the conventional design

Discussion: Linearity of both the proposed and conventional designs depends on the linear current respond of the ISFET device versus the pH level. A typical sensitivity of the CMOS-based sensor is about 40 mV/pH to 50 mV/pH and thus the gate voltage of the ISFET device will have a maximum change of about 400 mV to 500 mV over a pH range of 2 to 12. This poses a challenge to ISFET implementation in scaled CMOS technology where the supply voltage is reduced to 1.2 V or lower. At this low supply condition, the pH-to-time responses are not linear but still monotonic. Nonlinear time-to-digital will be needed to calculate back the pH level of the solution.

Conclusion: An improved pH-to-time readout scheme of pH sensing array was proposed with one ISFET stacked with one inverter per pixel. The proposed design is able to achieve good linearity over a wide range of pH. Its leakage and power consumption is $10^5\times$ and $1.7\times$ lower, respectively, when compared to the conventional design. It is therefore more suitable for future very large scale sensing applications implemented in nano-scale CMOS technology where both dynamic and leakage power are equally critical.

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