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Resilience of ultra-thin oxynitride films to percolative wear-out and reliability implications for high- κ stacks at low voltage stress

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Localized progressive wear-out and degradation of ultra-thin dielectrics around the oxygen vacancy percolation path formed during accelerated time dependent dielectric breakdown tests is a well-known phenomenon documented for silicon oxynitride (SiON) based gate stacks in metal oxide semiconductor field effect transistors. This progressive or post breakdown stage involves an initial phase characterized by “digital” random telegraph noise fluctuations followed by the wear-out of the percolation path, which results in an “analog” increase in the leakage current, culminating in a thermal runaway and hard breakdown. The relative contribution of the digital and analog phases of degradation at very low voltage stress in ultra-thin SiON (16 Å) is yet to be fully investigated, which represents the core of this study. We investigate the wear-out process by combining electrical and physical analysis evidences with modeling and simulation results using Kinetic Monte Carlo defect generation and multi-phonon trap assisted tunneling (PTAT) models. We show that the transition from the digital to the analog regime is governed by a critical voltage (V_{CRIT}), which determines the reliability margin in the post breakdown phase. Our results have a significant impact on the post-breakdown operational reliability of SiON and advanced high- κ -SiO_x interfacial layer gate stacks, wherein the SiO_x layer seems to be the weakest link for percolation event. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4819445>]

I. INTRODUCTION

Ultra-thin gate dielectric based metal-oxide-semiconductor (MOS) devices have been shown to exhibit a progressive phase of percolation path degradation and wear-out after the time dependent dielectric breakdown (TDDDB) event in both oxynitride^{1,2} and high- κ thin films.³ Recent studies have also revealed that MOS transistors with thin dielectric stacks operate correctly with good transfer characteristics even after the soft breakdown (SBD) event.⁴ Therefore, the definition of gate oxide reliability and time to failure has been modified to account for the post-SBD metal oxide semiconductor field effect transistors (MOSFET) operation, ensuring a relatively low gate leakage current. The post-SBD current evolution exhibits two distinct behaviors at moderate stress conditions consisting of initial random telegraph current fluctuations with discrete current levels (the average current is constant) followed by a monotonic increase in the current, which approaches the imposed current compliance of $\sim I_{gl} \sim 50\text{--}100\text{ }\mu\text{A}$ corresponding to the hard breakdown (HBD) occurrence. These two regimes are named digital (Di-BD) and analog breakdown (An-BD), respectively.^{5–7} While the transfer characteristics of the device are acceptably good in the digital regime, they are substantially degraded in the subsequent analog wear-out stage, making

the transistor no longer operational.⁵ It is therefore of interest to investigate the lifetime of the device in the digital regime and in the subsequent wear-out analog phase at the operating voltage ($V_{op} = 1\text{ V}$) to estimate the real MOSFET reliability margins from a transistor and circuit operation perspective. Although post-BD statistics has been sufficiently assessed in the past,^{3,8} the kinetics and the physical mechanisms governing the dielectric stack wear-out determining the digital to analog transition (DAT) need to be quantitatively explored from a physics point of view. The aim of this work is to address this point by presenting a detailed discussion of the physics of post-BD wear-out in silicon oxynitride (SiON) gate dielectric stacks by means of electrical/physical analysis and modeling-simulation results in order to estimate the enhancement in operation-related lifetime. The findings presented in this study have important implications also on the wear-out phenomenon in dual layer high- κ -SiO_x interfacial layer (HK-IL) thin films because the post-BD stage in these stacks involves dilation of the SiO_x interlayer which is the first to breakdown.^{9–17}

II. WEAR-OUT ELECTRICAL CHARACTERIZATION

All measurements in this study were carried out on NMOS devices with fixed SiON layer thickness ranging from $t_{ox} = 12\text{--}22\text{ }\text{\AA}$ at $T = 298\text{ K}$ with small area of $W \times L \sim 0.02\text{--}0.04\text{ }\mu\text{m}^2$. Fig. 1(a) shows the post-BD gate current evolution in three devices ($t_{ox} = 16\text{ }\text{\AA}$) subjected to a

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FIG. 1. Evolution of the gate current during a post-BD constant voltage stress at $V_g = 2.6$ V observed on a 16 Å SiON film, showing a clear transition from the digital to the analog regime for $I_{gl} > 5 \mu\text{A}$. (b)–(d) RTN fluctuations due to the stochastic capture/emission events in the percolation path at relatively low voltages of $V_g = 1.5, 1.8$, and 2.1 V. The initial SBD was triggered with a CVS-TDDB with low current compliance of $I_{gl} \sim 1 \mu\text{A}$.

constant voltage stress (CVS) of $V_g = 2.6$ V. Noisy digital fluctuations around a constant average value are observed in an initial phase, which is followed by a steady analog increase in the gate leakage with relatively low noise content. The random telegraph noise (RTN) fluctuations at lower $V_g = \{1.5, 1.8, 2.1\}$ V in one of the tested devices after SBD ($I_{gl} \sim 1 \mu\text{A}$) are shown in Figs. 1(b)–1(d). The number of discrete steps (2^N) is indicative of the number of traps (N) in the percolation path.

In order to illustrate the sensitivity of the digital to analog transition to V_g , the gate current noise pattern is measured using a multi-cycle step-stress test^{4,5,18,19} during which the stack is biased at a constant voltage that is subsequently increased by a constant value after a given time. Figure 2

FIG. 2. (a) Digital to analog gate current evolution observed during a two stage CVS test on 22 Å SiON with voltages starting from $V_{START} = 1.2$ V and incremented by $\Delta V = 0.2$ V until a drastic current jump is observed. (b) A clear difference in the gate current noise patterns and the evolution of the mean current levels is observed after the current spike at $V_g = 3.4$ V, which indicates the transition from the digital to analog mode. The low stress current levels and noise pattern shift drastically for $V_g < V_{CRIT} = 3.4$ V and $V_g > V_{CRIT}$.

shows the current measured on a $t_{ox} = 22$ Å stack biased at an initial voltage of 1.2 V (V_{START}), which is then incremented by steps of 200 mV for every 500 s until a significant current jump is observed reaching the current compliance of $10 \mu\text{A}$. After the large current jump observed at $V_g = 3.4$ V, a low voltage ramp stress starting from $V_g = 1.2$ V is applied (Fig. 2(b)) revealing a completely different pattern of noise and a drastic shift in the current level as well, indicative of the transition between the digital and analog phase. During the multiple-cycle CVS experiment, there is no significant degradation as far as the applied voltage is kept below V_{CRIT} , as confirmed by the fact that the same average current levels are measured during subsequent cycles of the multiple-stage CVS.¹⁸ In addition, the noise spectrum analysis (not shown here for brevity) of all the current signals in the first cycle (V_g ranging from 1.2 V to 3.2 V $< V_{CRIT}$), results in the same frequency power law exponent of $\alpha \rightarrow 2$ (Lorentzian). This indicates that there is no significant degradation of the SBD spot (and thus no changes in the physics of degradation) digital phase. Only after the sudden current jump observed at $V_g = 3.4$ V, all subsequent current-time data show purely $1/f$ noise ($\alpha \rightarrow 1$) indicating that the charge transport is dominated by a relatively large number of traps, consistent with a significant change in the driving forces and physical mechanisms causing wear-out and failure. Fig. 2 seems to indicate the existence of either a critical voltage ($V_{CRIT} = 3.4$ V for $t_{ox} = 22$ Å)¹⁸ or a critical field (ξ_{CRIT}) governing the DAT, which needs to be verified and its physical origin understood. Interestingly, the time taken for DAT to occur is very long for $V_g < V_{CRIT}$ and reasonably short for $V_g > V_{CRIT}$. Even after 30 000 s of stress on a 12.5 Å SiON device, we did not observe any DAT for a device tested at $V_g = 2$ V ($V_g < V_{CRIT}$), as shown in Fig. 3. It is worth noting that in the example shown in Fig. 3, the digital fluctuations tend to “quieten” down after ~ 22 500 s. This is a consequence of the Markovian nature of capture and emission processes wherein one of the conductive states (corresponding to a certain charge state of the oxygen vacancy (V_O)⁷) has a very high

FIG. 3. Example of a very long post-BD stress on 12.5 Å SiON film at $V_g = 2 \text{ V} < V_{\text{CRIT}}$. No clear signature of DAT is observed for as long as 30 000 s.

steady-state probability ($\sim 100\%$), whereas the other one has a very low occupancy due to high or low value (skewed ratio) of τ_c/τ_E .²⁰

The critical voltage V_{CRIT} was investigated on a statistical level using the above stress methodology. The tests were conducted on stacks with SiON thickness of $t_{\text{ox}} = \{16 \text{ Å}, 16.5 \text{ Å}, 20 \text{ Å}, 22 \text{ Å}\}$. The trend of the average V_{CRIT} is plotted versus t_{ox} in Fig. 4(a), whereas the $\xi_{\text{CRIT}}-t_{\text{ox}}$ relationship is shown in Fig. 4(b). Every data point was extracted by averaging the results obtained by testing 15–60 nominally identical devices. We observe a linear decrease in the V_{CRIT} value with t_{ox} , whereas ξ_{CRIT} remains roughly constant at the same value ~ 12.5 – 13 MV/cm (Fig. 4(b)), which is very close to the critical breakdown field of 15 MV/cm reported in the literature for SiO₂.²¹ When the linear trend in Fig. 4 is used to extrapolate the critical voltage of the typical interfacial SiO_x layer (5 – 8 Å thick) used in advanced high- κ stacks (assuming that SiO_x IL and SiON have similar material property), a

FIG. 4. (a) Minimum and maximum critical voltage (V_{CRIT}) extracted from the statistical tests performed on ultra-thin SiON are shown to decrease linearly with the oxide thickness. (b) The corresponding critical field (ξ_{CRIT}) derived from V_{CRIT} is shown to be approximately independent of the oxide thickness, indicating that the analog wear-out is a field-driven phenomenon.

V_{CRIT} lower than the operating voltage of $V_{\text{op}} = 1 \text{ V}$ is obtained. This finding indicates that in advanced HK-gate stacks, the thin IL layer could be susceptible to analog stage degradation. However, the voltage drop across the intact HK layer prevents the nucleation of a sudden analog phase, favoring an extremely long wear-out digital regime, as will be discussed in more detail in Sec. V.

III. WEAR-OUT PHYSICAL CHARACTERIZATION

The different current signatures shown in the post-BD digital and analog degradation regimes are investigated in this section by using physical characterization techniques in order to gain insights into the physical nature of the BD spot. For this purpose, we performed high resolution TEM (HRTEM) imaging of various devices subjected to different levels of breakdown hardness with compliance current I_{gl} ranging from $5 \mu\text{A}$ to $100 \mu\text{A}$. In Fig. 5, we examine the microstructure using HRTEM micrograph for three devices with (a) $I_{\text{gl}} \sim 100 \mu\text{A}$, (b) $I_{\text{gl}} \sim 50 \mu\text{A}$, and (c) $I_{\text{gl}} \sim 20 \mu\text{A}$. The location of BD here was electrically identified using the method proposed by Degraeve *et al.*²² As expected, the

FIG. 5. High resolution TEM micrograph of the post-BD SiON gate stack for (a) $I_{\text{gl}} \sim 100 \mu\text{A}$ with Si nano-cluster and severe DBIE, (b) $I_{\text{gl}} \sim 50 \mu\text{A}$ with moderate DBIE and (c) $I_{\text{gl}} \sim 20 \mu\text{A}$ with slight DBIE. The depletion of oxygen and the dilation of the breakdown path transform the central core of the BD region into a silicon-rich “nanowire” eventually shorting the gate and substrate. The gradual nano-cluster formation process leads to analog evolution of gate leakage current.

severity of oxide damage scales down with reducing I_{gl} . The darker contrast regions in the oxide represent the oxygen depleted clusters associated with higher vacancy concentration. In particular, Fig. 5(a) shows an almost fully oxygen depleted cylindrical core within the degradation spot, which we named as the “*Si nano-cluster*.” Additionally, we observe protrusions of the crystallographic Si from the substrate into the oxide BD site in Figs. 5(a)–5(c), which is referred to as the “*dielectric breakdown induced epitaxy* (DBIE).”²³ The nucleation of DBIE causes an effective thinning of the dielectric stack in the analog mode, which, together with the formation of Si nano-clusters²⁴ with high vacancy density, increases the current by establishing a positive feedback mechanism, where current and joule heating reinforce each other.²⁵ This leads to a continuous increase in the size and a reduction of the stoichiometry (SiO_x , $x \ll 2$) of the breakdown path,²⁶ which culminates into the HBD.

Note that these microstructural changes are only detected for current levels $> 5\text{--}10\ \mu\text{A}$, which correspond to the analog regime. In the digital mode, the gate stack does not show any clear physical/structural degradation: The DBIE is very small as shown in Fig. 5(c), and current fluctuations are due to the stochastic electron capture/emission events occurring at the oxygen vacancy traps along the percolation path. This seems to indicate that the post-SBD analog degradation phase (as well as reliability margin and V_{CRIT}) is associated with the creation of either a DBIE or a Si-nano-cluster, which is triggered by the localized current density and the temperature increase induced by related power dissipation.²⁵ In Sec. IV, we use a comprehensive physical model reproducing self-consistently the charge transport and defect generation within the dielectric stack to investigate the wear-out process following the creation of the SBD spot under different stress voltage conditions: $V_g < V_{CRIT}$ and $V_g > V_{CRIT}$ for a 16 Å SiON stack.

IV. WEAR-OUT MODELING AND SIMULATION

In order to shed some light on the role played by V_{CRIT} on the digital to analog transition occurring during the post-SBD degradation of the dielectric stack, we performed physics based degradation and breakdown simulations. We use a physical model,^{25,27,28} describing self-consistently the charge transport within the dielectric, as a multi-phonon trap-assisted tunneling (PTAT) process,^{27,28} and the stress- and temperature-induced defect generation, described by the thermochemical model for bond breaking.^{29,30} The model accounts for the temperature increase associated with the current-related power dissipation by solving the Fourier equation for heat dissipation.^{25,31} The physical parameters governing the defect generation (i.e., the bond polarization factor, $p_0 = 5.6\text{ eÅ}$ and the zero-field activation energy for Si-O, $E_a = 2.65\text{ eV}$) were extracted from TDDB measurements on 16 Å-thick SiON.^{12,33} Simulations have been performed considering a cylindrical simulation volume with a radius of 25 Å.

We first simulated the creation of the SBD spot during the initial $V_g = 3.2\text{ V}$ stress with $I_{gl} = 5\ \mu\text{A}$. Figures 6(a)–6(c) show the evolution of the current during the CVS stress as

well as the initial ($t_{stress} = 20\text{ s}$) and final defect and oxygen stoichiometry maps. The current increases monotonically until an abrupt jump is observed, which corresponds to the formation of the SBD spot, i.e., of a highly sub-stoichiometric region in the dielectric, see Fig. 6(c). The defect distribution map (i.e., the SBD spot) obtained from this initial simulation is then used as the starting condition for subsequent post-SBD stress simulations. For the 16 Å-thick SiON stack, the observed V_{CRIT} has an average value of $\sim 2.1\text{ V}$. In order to investigate the physical origin of V_{CRIT} , we simulate the post-SBD wear-out process by considering different post-SBD stress voltages, i.e., $V_g = 2.0\text{ V}$ (below V_{CRIT}) and $V_g = 2.5\text{ V}$ (above V_{CRIT}). Figures 6(e) and 6(f) show the simulation results obtained at $V_g = 2.5\text{ V}$ for the D and I current levels in the I_g - t graph of Fig. 6(d), respectively. The 3D and 2D (top view) oxygen sub-stoichiometry maps ($x \in [0, 2]$ in SiO_x) corresponding to these two current levels during the post-BD evolution are used to illustrate the progressive degradation of the stack. The thermo-chemical simulations clearly show a lateral dilation of the SBD spot, see Figs. 6(e) and 6(f), wherein the blue shaded (oxygen depleted) regions are getting wider. The simulated current-time trace in Fig. 6(d) shows that a duration of $\sim 2450\text{ s}$ is needed with applying $V_g = 2.5\text{ V}$ in the post-BD phase to reach the critical current level of $10\ \mu\text{A}$ (corresponding to analog degradation regime). The duration of the stress calculated from simulations agrees very well with the experimental stress time, whose distribution is plotted on a Weibull scale in Fig. 7 at different V_g .

It is worth noting in Fig. 7 that the Weibull Slope (β) gets steeper for lower V_g , thus indicating that the DAT process becomes increasingly determinate (less variant). This trend can be understood considering the thermochemical model^{29,30} in which the defect generation process is governed by the electric field and local SBD spot temperature. When the post-SBD stress is performed at a higher voltage, the current flowing through the SBD spot increases. As a consequence of the larger electron flow, the power dissipated at the trap sites of the SBD spot also increases, leading to a larger increase in the local temperature.²⁵ Our simulations show that this higher local temperature practically confines the defect generation process very close to the initial SBD spot. Therefore, fewer defects have to be generated to trigger the temperature-driven positive feedback leading to the final thermal runaway phase that determines the DAT transition.²⁵ This explains the reduction of the Weibull slope observed at higher stress voltages.

When the physical model simulation is run considering a constant voltage stress of $V_g = 2.0\text{ V} < V_{CRIT}$, the current compliance of $10\ \mu\text{A}$ is not reached even after $3 \times 10^8\text{ s}$ (10 years), see dashed line in Fig. 8(c), thus indicating a drastic prolongation of the DAT when the voltage is lower than the critical value. Typical current-time traces simulated at both $V_g = 2.0\text{ V}$ and 2.5 V in Fig. 8(c) are shown to have widely different time scales. In Fig. 9(a), we plot the diameter of the dilated SBD spot as a function of time for three stress voltages, i.e., $V_g < V_{CRIT}$, $V_g \sim V_{CRIT}$, and $V_g > V_{CRIT}$, which highlight the drastic (orders of magnitude) shift in the stress time. Interestingly, the dilation starts to show up only during

FIG. 6. (a) Current-time trace for one of the simulations of the initial SBD stage at $V_g = 3.2$ V. (b) Initial defect configuration at the initiation of device stress at 20 s and (c) TDDB stage defect map. (d) Current-time trace for the subsequent wear-out of the percolation path generated in Figs. 6(a)–6(c) at $V_g = 2.5$ V. (e) and (f) Post-SBD defect evolution at $V_g = 2.5$ V $> V_{CRIT}$, indicating the gradual dilation of the percolation path in a reasonably shorter frame of time. The two maps in (e) and (f) correspond to instants D and I in Fig. 6(d). Note that the size of the percolation path increases exponentially as a function of stress time, as evident later in Fig. 9(a). The legend in these figures refers to a value ranging between 0 and 2, corresponding to the oxygen sub-stoichiometry, x , in SiO_x . The red arrows in sub-plots (a) and (d) indicate the time instant at which the defect and sub-stoichiometry map is plotted.

the later phases of stressing when the increase in the defect generation rate becomes very steep because of a positive feedback process and interplay between the TAT conduction, field and temperature-assisted defect generation and “joule heating” phenomena.²⁵ Fig. 9(b) shows the maximum temperature inside the percolation path (T_{max}) as a function of the gate current as obtained from the simulations of a CVS at

3.2 V on two statistically different devices. As can be seen, whereas $T_{max} \sim 25$ – 40°C is close to the ambient one in the current range corresponding to the digital regime (i.e., below 3 – 5 μA), it increases steeply in the analog current range, indicating that V_{CRIT} could be related to a critical temperature that is required to activate positive feedback defect generation eventually ending with the hard/analog breakdown.

FIG. 7. Experimental Weibull plot of the DAT duration distribution at three different stress levels of $V_g = \{2.6, 2.8, 2.9\}$ V. The stress duration of 2450 s estimated from one of our simulation trials at $V_g = 2.5$ V is in good agreement with the experimental stress time (within same order of magnitude). This confirms that the thermochemical defect generation and charge transport model correctly describe the physics underlying the DAT process.

FIG. 8. (a) and (b) 2D defect spectroscopy map of the oxygen substoichiometry, $x \in [0, 2]$, for (a) $V_g = 2.5$ V and (b) $V_g = 2.0$ V with the corresponding time scales indicated. While the defect generation process is similar, the time scales are orders of magnitudes longer for $V_g < V_{CRIT}$. (c) Simulated current-time traces for the two cases further confirm the longer time scales for $V_g < V_{CRIT}$.

Probably, the DBIE we observe in the analog stage is driven also by thermally-assisted processes, such as atomic diffusion,²³ which requires a certain critical temperature for the epitaxial growth to effectively reduce the oxide thickness.

V. IMPLICATIONS FOR CIRCUIT RELIABILITY AND HIGH- κ DIELECTRIC STACKS

Using the physical model simulations, including defect generation and TAT charge transport to interpret results from electrical measurements and the in-depth physical analysis, allows proving that the reliability margin for the standard operating voltage $V_{op} = 1.0$ V $\ll V_{CRIT}$ is extremely good for the 16 Å SiON stack investigated in this work. Indeed, the digital regime is prolonged enough to ensure a lifetime of >10 years when the wear-out of a single percolation path is considered in a small area device. Therefore, the only possible way for attaining typical circuit failure criterion of $10 \mu\text{A}$ at $V_{op} = 1.0$ V is by means of multiple uncorrelated SBD events across the circuit comprising a billion transistors. Various statistical studies on multiple breakdown have

FIG. 9. (a) Diameter (lateral width) of the percolation path during the digital to analog stage wear-out for $V_g = \{2.0, 2.3, 2.5\}$ V in 16 Å SiON. (b) Trend of the maximum temperature (T_{max}) inside the percolation path during the digital and analog stages. It is worth noting that for current levels in the digital range, the temperature is around 25–40 °C, whereas it increases steeply in the case of analog evolution.

been proposed in the past³² and can be applied here to quantitatively understand how many breakdown spots are needed for circuit failure.

The results of our study can also be applied to investigate the post-BD resilience of high- κ dielectric stacks. As discussed in Sec. II, the value of V_{CRIT} reduces linearly as we move to thinner dielectrics, dropping below $V_{op} = 1$ V for $t_{ox} < 9$ Å, see Fig. 4(a). In typical advanced HK-IL gate stacks, the interfacial layer consists of a ~ 5 – 8 Å thick SiO_x film and is the first to breakdown.^{9–17,33} According to the results in Fig. 4(a) and assuming that the SiO_x IL and the SiON dielectric have similar material properties (which is an approximation), the critical voltage determining the DAT transition of the SBD spot formed in such a thin IL results to be lower than $V_{op} = 1$ V ($V_{CRIT} \sim 0.8$ V is estimated assuming a 6 Å-thick IL). Nevertheless, the voltage redistribution between the intact HK and the oxygen depleted SiO_x layer strongly reduces the voltage that is applied to the degraded IL, effectively preventing the DAT at normal operating conditions.

The different material properties of SiO_x compared with SiON lead to differences in its immunity towards wear-out and alters the scaling projections presented in Fig. 4(a). This is mainly due to the oxygen extracted from the interfacial SiO_x by high- κ layer during the fabrication, which induces a relatively high sub-stoichiometry and a high density of oxygen vacancy defects.³⁴ In particular, the SiO_x IL comprised

in high- κ stacks is typically highly sub-stoichiometric and thus characterized by a higher permittivity of $\kappa_{IL} \sim 7$ – 9 ³⁴ $\gg \kappa_{SiON} \sim 3.9$.²⁹ Additionally, the slightly higher thermal conductivity expected of SiO_x reduces the confinement of the heat generated during the thermal runaway culminating into the breakdown, thus reducing the maximum temperature and degradation at any reference current level when compared with the SiON.

Calculations performed using Gauss law³⁵ by considering $\kappa(\text{HfO}_2) \sim 25$, $t_{HK} \sim 2$ nm, $\kappa_{IL} \sim 9$ (because of the high post-percolation oxygen vacancy density) and $t_{IL} \sim 0.6$ nm, show that for the voltage drop across IL to be larger than $V_{CRIT} \sim 0.8$ V, the overall gate voltage has to be as high as 1.76 V $\gg V_{op} = 1$ V. This is much higher than 1.21 V calculated considering SiO_x and SiON with similar material properties. In short, the sub-stoichiometry of the IL layer provides additional immunity towards wear-out and improved scalability when compared with SiON. Even for very thin IL layers, the degraded region where the BD spot has been formed is not subjected to sufficient voltage stress to undergo substantial progressive wear-out within a 10-year life time. Therefore, this study helps in discarding the “wear-out” of a single SBD spot as one of the post-breakdown failure mechanisms in HK-IL stacks. This is an important conclusion as the quantitative post breakdown lifetime estimation strongly depends on the underlying mechanism assumed (multiple BDs or single percolation wear-out). This means that investigating circuit level reliability related to dielectric breakdown requires focusing only on the statistics of multiple soft breakdown events. The percolation path “wear-out” is only evident under accelerated stress conditions, where we intentionally over-stress the device to initiate the analog stage of degradation eventually leading to HBD. Predicting the post-BD reliability on the basis of pure “wear-out” considerations will give an overly-optimistic estimate of post-BD lifetime, as multiple SBD events dominate the post-BD reliability.

VI. CONCLUSIONS

In this study, a comprehensive understanding on the physics governing the digital-to-analog transition for post breakdown in ultra-thin SiON dielectrics has been achieved. We used electrical measurements, physical characterization, and model simulations, including defect generation and TAT charge transport to get an in-depth understanding of the wear-out phenomenon. Both experimental and simulation results point to the existence of the so-called critical voltage (V_{CRIT}), which is the minimum voltage needed to observe a significant dilation of the percolation path in a reasonable time-frame. If the value of $V_{op} < V_{CRIT}$ (which is true for most cases), we can conclude that the analog degradation phase leading to HBD are very remote events that has very low probability to occur. Thus, device and circuit failures are primarily determined by multiple SBD events. This is true also for HK-IL stacks wherein the intact high- κ reduces the effective voltage applied to the IL layer in the post-BD phase. The analog mode of degradation observed under accelerated stress conditions is not shown to occur at

nominal operating conditions. Therefore, it is worth noting that predicting thin film dielectric lifetime by extrapolating trends collected at high voltage stress using simple models can lead to wrong results, as the fundamental assumption of the same failure mechanism just accelerated by the higher voltage is no longer true.

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