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A 96×96 1V Ultra-low Power CMOS Image Sensor for Biomedical Application

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Abstract— An ultra-low power CMOS image sensor is designed for endomicroscope applications. The chip will be fabricated through Global Foundries 0.18 μ m standard CMOS process with 1V power supply. The total power consumption is 6 μ W for 96×96 array with 5fps frame rate, where global amplifier consumes 3.3 μ W, 10-bit SAR ADC consumes 900nW at 50kS/s, and on-chip digital processing further reduces IO power consumption down to 1.6 μ W.

I. INTRODUCTION

Recently, CMOS image sensors (CIS) are replacing Charge-coupled Device (CCD) in many biomedical applications with the benefit of low power, high speed and feasibility of system-on-chip (SoC) integration. These advantages become attractive especially for implantable medical system optimization [1, 2], which is more emphasis on low power consumption to enable standalone operation. For example, endomicroscope is a novel device to obtain noninvasive real-time diagnosis in clinic. Monitoring liver fibrosis progression by liver biopsy is important for disease treatment, however repeated biopsy is invasive for human being. Traditional noninvasive methods [3] use indirect marker to assess liver fibrosis but limited by the sensitivity, while endomicroscope provides better accuracy by transferring second harmonic generation (SHG) imaging into in vivo imaging and real-time monitoring the liver fibrosis directly [4]. The imaging acquisition device is the critical component to miniature endomicroscope system, and CIS is more suitable with low power consumption, low cost and small size. Moreover, sensitivity is an important parameter especially under low light internal environments. With the recent development of backside illumination (BSI) technology, the fill factor and quantum efficiency of CIS has been dramatically improved to achieve super low-light performance [5]. Finally, CIS technique enables on-chip image data analysis to achieve real-time imaging observation based on the compatible of standard CMOS process [6].

In this paper, we have designed an ultra-low power CMOS image sensor mainly targeted for endomicroscope application. The low power circuit design technique is explored within a global readout sensor architecture. What is

more, the proposed sensor array has dual operation mode towards self-powering. In other words, the pixel can be configured into solar cell to harvest the energy and further to support the sensor operation. The chip will be fabricated through Global Foundries 0.18 μ m standard CMOS process with 1V power supply. The total power consumption is 6 μ W for 96×96 array with 5fps frame rate, where global amplifier consumes 3.3 μ W, 10-bit SAR ADC consumes 900nW at 50kS/s, and on-chip digital processing further reduces IO power consumption down to 1.6 μ W. The rest of the paper is organized as follows. Section II describes the sensor architecture for the ultra-low power consumption. Section III describes the detail of block design. Then, the simulation result is shown in Section IV with conclusion in Section V.

II. ULTRA-LOW POWER IMAGE SENSOR ARCHITECTURE

The architecture of low-power image sensor is shown in Fig. 1. Global voltage readout is employed here to reduce the

Figure 1. Ultra-low power CMOS image sensor architecture

Figure 2. Dual-mode image pixel with energy harvesting ability: (a) schematic; (b) layout; and (c) A-B cross section

power consumption. The 96×96 pixel array is read out in sequence by controlling of row decoder. The pixel output from each row is sampled by column Sample/Hold circuit, then the correlated-double-sampling (CDS) signals are amplified by one shared global amplifier in serial and converted to 10-bit digital signal output by on-chip SAR ADC.

Note that this global readout architecture is similar as the one described in [1]. In this paper, a few more techniques are employed to further scale down the power. Firstly, a low supply voltage 1-V is deployed for all blocks to reduce the power consumption. Secondly, boosters are employed to increase the dynamic range of pixel so that the whole sensor system can work well under 1-V supply without sacrificing the performance of pixel. Last but not least, on-chip digital control is implemented to reduce the power dissipation from the additional IO pads. In the following section, the low-power design detail is illustrated from each component.

III. ULTRA-LOW POWER IMAGE SENSOR CIRCUIT DESIGN

A. Energy harvesting and imaging pixel

An energy harvesting and imaging (EHI) pixel is implemented as shown in figure 2. The EHI pixel is based on three-transistor (3T) standard active-pixel-sensor (APS) structure but with an additional photodiode and control-switch to switch between energy harvesting mode and imaging mode (shown in 2a). At imaging mode, the EHB_EN switch is turned off and energy harvesting bus (EHB) is connected to ground. Therefore, both photodiode-1 (PD1) and photodiode-2 (PD2) are reversely biased to work as image sensor. The signal at floating diffusion (FD) node generated from imaging PDs is amplified by source follow transistor and reset by reset-switch transistor as in the standard 3T APS pixel. At energy harvesting mode, the EHB_EN switch is turned on and disable PD1 by connecting FD node to the ground. Meanwhile the solar cell PD2 generates the current and sending it through energy harvesting bus (EHB) to on-chip power management circuit. The detail description of energy harvesting mode will be described in another paper.

As shown in figure 2(b), a novel layout structure by employing deep-N-well is proposed in order to reduce pixel fixed-pattern-noise (FPN) in standard CMOS technology. The pixel pitch is $23\mu\text{m}$ with 27.2% of fill-in factor. A-B cross section is illustrated in figure 2(c). The deep-well/P-substrate junction forms the PD1, and the N-plus/P-well junction forms the PD2. The N-type nodes of both of PDs are connected by N-well and metal to FD. The P-type node of PD1 is connected

Figure 3. Schematic of voltage booster for Reset & Select

Figure 4. Schematic of current-mirror OTA

to ground by P-substrate, and PD2 is connected to EHB by metal. The deep N-well is covered by N-well all around of it such that the PD2 in one pixel is totally isolated from its neighbors. Moreover, the deep-N-well/P-substrate junction provides better isolation between the pixel and its neighbors. As such, the deep-N-well pixel architecture achieves better FPN performance to avoid the crosstalk. It is an important design specification to achieve high-sensitivity endo-microscope application under low-light application.

B. Reset-and-select Voltage booster

With only 1-V power supply, the dynamic range of EHI pixel is limited. Boosting technique is the efficient method to extend the dynamic range of pixel [7], here the reset and select boosters are both employed, as shown in figure 3. The booster circuit is based on bootstrapping structure [8], including two inverters, a boosting capacitor and a PMOS transistor. Once the booster block is enabled, when clock input from IN port keeps at low, it will force the int2 output goes low and turn on the switch M0, therefore the OUT connects to VDD. When the input changes from low to high, the switch M0 is turned off so the bottom plate of CB is disconnected from VDD. Meanwhile the top-plate of CB is connected to VDD and force

the output boosted to voltage level between VDD to 2VDD. Note here, the booster efficiency is related to the ratio of loading capacitor CL and boosting capacitor CB, larger CB means better boosting efficiency.

C. Current-mirror OTA for global amplifier

Global amplifier is one of the most power hungry blocks in the readout chain. Here a gain-enhanced current-mirror OTA (shown in Fig.4) is employed in order to achieve low-power consumption under 1-V power supply. The OTA only needs two bias voltages, Vb1 and Vb2, to minimize the power dissipation of bias circuits. Note that a big-ratio (10:1) of current-mirror is adopted to increase the output driving capability. It is able to drive at least 10pF load at $(15 + 1.5) \times 200\text{nA}$ (3.3 μA) bias current, when considering that the amplifier needs to be output directly to testing board. The gain-enhancement is implemented by MN4 and MN5 to distribute the current through MN1 and MN2, which result in the increased resistance load of input-stage. The gain can be increased to $1/(1-k)$ times and is further adjusted by tuning the value of k [9].

D. 10-bit SAR ADC

A 1-V supplied 10-bit shift-register based standard

Figure 5. Low-power dynamic comparator in SAR ADC

Figure 6. Layout overview of the ultra-low power CMOS image sensor

successive approximation register (SAR) ADC [10, 11] is designed to convert the signal to digital output. Energy

efficient dynamic comparator [12] is employed to minimize power consumption of ADC as shown in figure 5. The comparator does not consume DC-bias current. The amplifier as first stage of comparator can suppress the kick-back noise and also make comparison faster. Note that the SAR ADC can achieve 100kS/s speed under 1-V supply. It meets the requirement of 10 fps full-speed of the image sensor system towards endomicroscope applications. The entire ADC only consumes 900nW when running at 50kS/s, which is fast enough for the targeted 5fps sensor speed.

E. On-Chip digital timing control

The digital timing control is also implemented on the same chip to ensure the chip operation. It generates control signals for each individual blocks, including row decoder, column decoder, amplifier and ADC. The total layout size is 0.14mm $\times$ 0.14mm. Compared to use off-chip IO digital inputs [1], this on-chip implementation of digital control can reduce power consumption 70% (5.6 μW to 1.6 μW).

IV. SIMULATION RESULTS

The proposed ultra-low power CMOS image sensor will be fabricated in 0.18 μm 1P6M Global Foundries standard CMOS process. The chip design spec is listed in Table 1. The entire chip occupies 3mm $\times$ 4mm and chip layout diagram is shown in figure 6. The sensor array is 96 $\times$ 96 with pixel pitch of 23 μm and fill factor of 27.2%. The total power consumption is 6 μW with 5fps readout speed.

A. The simulation results of OTA

The post-layout simulation results of open-loop of the current-mirror OTA used in global amplifier are shown in figure 7. The open-loop gain of the OTA is 60.5 dB, and the gain-bandwidth is 1.3MHz with 52.4 degree phase margin. The power consumption is 3.3 $\mu\text{A} \times 1\text{V} = 3.3\mu\text{W}$ with 10pF load. It can meet the 5fps speed requirement to read out the whole 96 $\times$ 96 image sensor array.

B. The simulation results of SAR ADC

Comparator is the critical component in SAR ADC, which determine the system speed and power consumption. The simulation result of the dynamic comparator in SAR ADC is shown in figure 8. With 1-V supply and 1.5MHz input clock, the comparator delay is 7ns after buffered output to achieve 5fps readout speed.

Moreover, the simulation result of SAR ADC is shown in figure 9. With 1-V power supply and 500mV input range, the conversion speed is 100kS/s, and the power consumption is only 2 μW . Note that we have designed the resolution of both 8-bit and 10-bit, which are configurable in order to further save power.

C. The simulation results of digital timing control

With external digital clock input, the on-chip digital timing block is able to generate all control signals internally as shown in Fig.10. Then the 10-bit digital sensor outputs along with frame_valid, line_valid and pixel_clk are sent off-chip to display the image alive. The total power consumption by reducing the IO pad is saved up 70%, from 5.6 μW down to 1.6 μW .

TABLE I. SPECIFICATION OF THE IMAGE SENSOR

Technology	0.18 μ m 1P6M CMOS
Chip area	3mm $\times$ 4mm
Pixel array size	96 $\times$ 96
Pixel pitch/fill factor	23 μ m/27.2%
Power consumption	6 μ W@1-V
Frame rate	5fps
ADC	10-bit SAR ADC

V. CONCLUSION

An ultra-low power CMOS image sensor is presented in this paper towards in vivo endomicroscope application. A number of low-power designing considerations have been introduced in this paper to optimize power performance in voltage booster, global amplifier, SAR ADC and on-chip digital timing control. With 96 $\times$ 96 sensor array under 1-V power supply, the power consumption is 6 μ W with 5fps speed when using 0.18 μ m 1P6M Global Foundries standard CMOS process.

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Figure 7. Frequency response of current-mirror OTA of global amplifier

Figure 8. Transient simulation results of the dynamic comparator employed in SAR ADC

Figure 9. Simulation results of SAR ADC

Figure 10. Simulation results of on-chip digital control