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Modulation of Capacitance Magnitude by Charging/Discharging in Silicon Nanocrystals Distributed Throughout the Gate Oxide in MOS Structures

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In this work, charge trapping in silicon nanocrystals (nc-Si) distributed throughout the gate oxide in a metal oxide semiconductor (MOS) structure has been studied. This situation is different from the conventional one with nc-Si confined in a narrow layer embedded in the gate oxide. In the latter, charge trapping in nc-Si leads to a shift in capacitance-voltage characteristic (*i.e.*, a change in the flat-band voltage). In contrast, in the former the charge trapping leads to a dramatic reduction in the MOS capacitance. The original capacitance could be recovered after the release of the trapped charges by a small bias, UV light illumination, or low-temperature thermal annealing.

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Silicon nanocrystals (nc-Si) embedded in gate oxide of metal oxide semiconductor (MOS) structures are expected to play an important role in memory devices due to the nanocrystals unique charging and discharging effect.¹⁻¹¹ Charging and discharging in nc-Si are indeed very important as they are directly related to data storage/retention in the memory cells. For memory applications, the nanocrystals are normally confined in a narrow layer embedded in the gate dielectrics near the Si substrate.⁹⁻¹¹ However, it would be interesting to examine the charging and discharging in the nc-Si that distributes throughout the gate dielectric specially with the nc-Si peak concentration located near the gate. For the MOS structures with such an nc-Si distribution, charging and discharging of the nc-Si are expected to occur easily and thus they will have a significant impact on the electrical characteristics of the MOS structures. Indeed, for such MOS structures, some interesting phenomena have been observed. In a previous study,¹² it was shown that charging in the nc-Si leads to a change in both the gate current and the MOS capacitance, and the change in the oxide conduction is explained by the change in the nc-Si tunneling paths due to charging/discharging in the nc-Si. In the present study, it will be shown that the capacitance can be reduced to an extremely low level by charging up the nc-Si with either a positive or a negative gate bias. Furthermore, the original capacitance can be recovered by discharging the nanocrystals with a small opposite gate bias, ultraviolet (UV) illumination, or even a low-temperature (100°C) heating. The modulation of the capacitance magnitude by charging/discharging in the nc-Si provides the possibility of memory devices application.

To fabricate the MOS structures with nc-Si distributed throughout the gate oxide with its peak concentration located near the gate, a 30 nm SiO₂ film was thermally grown on p-type (100) Si wafers in dry oxygen at 950°C. Then Si⁺ ions with the dose of $3 \times 10^{16} \text{ cm}^{-2}$ were implanted to the SiO₂ at 14 keV. From the transport and range of ions in matter (TRIM) simulations, the peak concentration was estimated to be at the depth of $\sim 20 \text{ nm}$. Thermal annealing was carried out at 1000°C in N₂ ambient for 1 h to induce nc-Si formation. The annealing can also eliminate the damage/defects caused by the ion implantation. Formation of nc-Si was clearly observed in transmission electron microscope (TEM) measurement. The mean size of the nc-Si is $\sim 4 \text{ nm}$ as determined from X-ray diffraction measurement.¹² The oxide layer was thinned in a HF solution of concentration of 50:1. An SiO₂ layer $\sim 17 \text{ nm}$ thick was removed such that the peak concentration of nc-Si is located close to the oxide surface. A 20 nm aluminum layer was then deposited to form the gate electrode. The wafer backside was coated with a layer of aluminum with the thickness of $\sim 1 \mu\text{m}$ after remov-

ing the backside oxide. Finally, metal alloy process was conducted at 425°C in N₂ ambient to form ohmic contacts. Figure 1 shows the secondary ion mass spectroscopy (SIMS) profile for the nc-Si in the gate oxide of the MOS structures. The peak concentration of nc-Si was found located near the gate, as predicted from the TRIMS simulation mentioned above. The experiment of charging/discharging the nc-Si by applying a constant voltage to the MOS structures was performed with a Keithley 4200 semiconductor characterization system, and capacitance-voltage (C-V) measurement was carried out with a HP4284A LCR meter at the frequency of 1 MHz. All experiments were carried out at room temperature. In the discharging experiment, the MOS structures were biased at a low voltage with polarity opposite to that of the charging voltage, or were exposed to UV light at the wavelength of 365 nm, or were annealed at a low temperature of 100°C.

For a MOS capacitor with a gate oxide thickness of 15 nm and a gate area of $100 \times 100 \mu\text{m}^2$, it has a capacitance of $\sim 24 \text{ pF}$ under strong accumulation at -3 V if there are no nanocrystals embedded in the gate oxide (Fig. 2c). However, as can be seen in Fig. 2a or b, with the nc-Si distributed throughout the gate oxide, the virgin capacitance (*i.e.*, the capacitance before charge trapping in the nc-Si) is much larger than this value (~ 45 times larger). This can be explained with the equivalent capacitance discussed below. Charge could be stored in the three elements of the MOS structures, *i.e.*, the nanocrystals, the remaining gate oxide capacitor, and the Si depletion layer. The corresponding capacitances of the elements are denoted by C_{nc} , C'_{ox} , and C_{D} , respectively. As discussed in Ref. 12, with a very large C_{D} under accumulation, the total capacitance C of the MOS structure is approximately equal to $(C_{\text{nc}} + C'_{\text{ox}})$. Due to the existence of a high concentration of nc-Si in the gate oxide close to the gate, the remaining gate oxide capacitance C'_{ox} should be much smaller than the conventional gate oxide capacitance (C_{ox}) without the nc-Si (C'_{ox} is found to be less than $\sim 700 \text{ fF}$). On the other hand, as the Si nanocrystals distribute throughout the gate oxide with their peak concentration located close to the gate, they easily respond to the small ac signal in the C-V measurement if they are uncharged or neutral (*i.e.*, no charges trapped in them). The virgin C_{nc} (*i.e.*, the nc-Si capacitance before charge trapping) should be very large due to the existence of a high concentration of nc-Si. Therefore, the MOS capacitance (C) is approximately equal to C_{nc} , and it will be very large when most of the nc-Si is uncharged.

However, applying a constant voltage of $+4$ or -4 V to the gate for 320 s reduces the MOS capacitance dramatically to a very low level ($< 700 \text{ fF}$), as shown in Fig. 2. The polarity of the gate voltage (either positive or negative) does not have a significant effect on the reduction of the capacitance. Obviously, the capacitance reduction can be explained in terms of the charge trapping in the nc-Si. With charge trapping in the nanocrystals, the nanocrystal capacitance C_{nc}

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Figure 1. Si SIMS profile for the MOS structures used in this study.

should decrease as the number of uncharged nanocrystals responding to the small ac signal in the C-V measurement is reduced. If all the chargeable nanocrystals are charged up, then C_{nc} should approach zero. Thus the MOS capacitance is very small as it is now determined by the remaining gate oxide capacitance C'_{ox} (<700 fF).

Note that the influence of charge trapping in the nanocrystals on C-V characteristics for the nc-Si distribution of this study is very different from the situation for nanocrystals being confined in a narrow layer embedded in the gate oxide (*i.e.*, the gate oxide has the structure of SiO_2 layer/nanocrystal layer/ SiO_2 layer). In the latter case, the charge trapping in the nanocrystals leads to a shift of the C-V curve (*i.e.*, a change in the flat-band voltage),^{1,9,11} but it does not change the capacitance magnitude under accumulation or inversion. In contrast, in our case, the charge trapping leads to a dramatic reduction in the capacitance magnitude, but no obvious flat-band voltage shift can be seen as the MOS capacitance is reduced to an extremely low level. The difference between the two cases highlights the importance of the nc-Si distribution.

On the other hand, if the charges trapped in the nc-Si are released, then C_{nc} should increase as the number of available electron states in the nc-Si that respond to the ac signal increases, and thus the MOS capacitance should increase. This has been confirmed in our experiment. As shown in Fig. 2, applying a low voltage of 2 V for 160 s with the polarity (either positive or negative) opposite to that of the charging voltage leads to the recovery of the MOS capacitance, indicating that most of the charges trapped in the nc-Si have been released during the application of the voltage. If the discharging voltage is increased, the recovery time will be shorter. However, if the voltage is further increased to 4 V or higher, the voltage may lead to discharging of nc-Si first but charging again later, corresponding to the first increase and then decrease in the MOS capacitance.

The charges trapped in the nc-Si can be also released by UV illumination or low temperature annealing. As shown in Fig. 3, the application of +4 V for 320 s reduces the MOS capacitance to an extremely low value (<700 fF); however, after 5 min of exposure to the UV light at the wavelength of 365 nm, the capacitance increases dramatically to a high level even larger than the virgin capacitance. This indicates that the UV illumination can release not only the charges that are trapped in the nc-Si during the application of the charging voltage but also the initial charges that are trapped in the nc-Si prior to the application of the voltage (note that the C-V measurement at -3 V may have already caused some charge trapping in the nc-Si). On the other hand, similar to the UV illumination, a low temperature annealing can also lead to the release of the trapped charges and thus a recovery of the MOS capacitance. Figure 4 shows the recovery of the MOS capacitance after the annealing at

Figure 2. Changes in MOS capacitance due to charging/discharging in nc-Si. (a) Charging at +4 V for 320 s and discharging at -2 V for 160 s; (b) charging at -4 V for 320 s and discharging at +2 V for 160 s; and (c) comparison of the MOS capacitance between the MOS structure without nc-Si and the MOS structures with nc-Si after charging (charging at either + or -4 V).

100°C for 10 min (a slight increase in the capacitance after the annealing indicates that some initial charges have been released also during the annealing).

We have also performed capacitance *vs.* time (C-t) measurements, and we found that the charge retention time is ~ 580 s if the capacitance is measured at -2 V with a measurement interval of 5 s and a measurement time <1 s. Note that the retention time obtained from the C-t measurement could be affected by the measurement conditions (such as at a large bias) because the charging/discharging could occur during the measurement. The fluctuation of the capacitance measurement at -2 V is within 15%, and the fluctuation is a random event. This suggests that some random charging and discharging occur during the capacitance measurement at -2 V.

Figure 3. Changes in MOS capacitance due to the charging at +4 V for 320 s and the discharging under UV illumination for 5 min.

In conclusion, in contrast to the conventional situation in which charge trapping in nc-Si confined in a narrow layer embedded in the gate oxide leads to a shift in C-V characteristic, charge trapping in nc-Si distributed throughout the gate oxide with its peak concentration located close to the gate leads to a dramatic reduction in the MOS capacitance. The capacitance could be recovered after the release of the trapped charges by a small bias, UV light illumination, or low temperature thermal annealing. The capacitance modulation by charging/discharging in the nc-Si provides the possibility of memory devices application.

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Figure 4. Changes in MOS capacitance due to the charging at +4 V for 320 s and the discharging under low temperature annealing at 100°C for 10 min.

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