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Simulation of Flash Memory Characteristics based on Discrete Nanoscale Silicon

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Abstract In this paper, we present a simulation study on the trapping properties of Flash memory device based on discrete nanoscale silicon embedded in silicon-dioxide (SiO₂). Taurus Suprem-4 and Taurus Medici are being used to carry out the simulations. The memory structure with a tunnel oxide of 3, 5 and 9 nm and a control oxide of 10, 20 and 40 nm have been simulated, respectively. The discrete nanoscale silicon with the size of 20 nm × 20 nm, 10 nm × 10 nm, and 5 nm × 5 nm have also been simulated, respectively.

I. INTRODUCTION

The concept of charge storage based on discrete nodes like the semiconductor nanocrystals embedded in the gate dielectric has drawn large attention for the past few years due to the possibilities of replacing the conventional floating-gate non-volatile memory devices [1,2]. Various nanocrystal materials (i.e., silicon, germanium, and metal) and fabrication techniques have been explored in the last few years [3,4]. To utilize the silicon nanocrystal (nc-Si) as charge storage node, understanding the dynamic behavior of programming and erasing in the nc-Si is important. Many characterization works have been carried out to understand the memory behavior of such devices [4,5]. Less work has been carried out to simulate the memory structure consisting of discrete nanoscale silicon or nc-Si as charge storage node and to predict the memory behavior with simulation methods.

In this paper, we present a simulation work on the trapping properties of memory device based on discrete nanoscale silicon as charge storage node. As a comparison, a layer of floating-gate silicon memory device is also being simulated. The threshold voltage (V_{th}) shift as a

function of programming voltage and programming time using channel hot electron (CHE) programming method are explored. The influence of control oxide thicknesses and tunnel oxide thicknesses on the memory behavior is being studied. Besides, the threshold voltage shift due to the programming of different dimension of discrete nanoscale silicon is also being simulated.

II. SIMULATION MODEL

Taurus Supreme-4 is being used to simulate the fabrication process of the Flash memory device with a layer of floating-gate and discrete nanoscale silicon embedded in the SiO₂ matrix, respectively. Taurus Medici is being used to simulate the memory behaviors. Medici solves three partial differential equations self consistently for electrostatic potential, and the electron and hole concentrations using Poisson equation and continuity equation. Parallel and perpendicular field are considered to specify the mobility of electron in Medici. Channel hot electron programming is carried out with a positive bias applied to both the gate and drain terminals ($V_g > 0$, $V_d > 0$), grounding other two terminals ($V_s = 0$, $V_b = 0$). The device dimension and doping concentration are given in Table I.

Table I Device dimension and doping concentration

Parameter	Value
Channel length (L)	0.25 - 1 μm
Control oxide thickness	20 - 40 nm
Tunnel oxide thickness	3 - 10 nm
Nanoscale silicon thickness	5 nm
Substrate doping	$1 \times 10^{15} \text{ cm}^{-3}$
Source / drain doping	$1 \times 10^{20} \text{ cm}^{-3}$

III. RESULTS AND DISCUSSION

Fig. 1a shows that the simulated Flash memory device with a layer of floating-gate (a) and discrete nanoscale silicon (b), sandwiched between two SiO_2 layers, respectively. The size of the discrete nanoscale silicon is $5 \text{ nm} \times 5 \text{ nm}$. As shown in this figure, the tunnel oxide is 3 nm and the control oxide is 10 nm for both memory devices. The transfer characteristics of the simulated Flash memory device with a layer of floating-gate and discrete nanoscale silicon are shown in Fig. 2. It is observed that there is a slight difference in the initial V_{th} between the two devices. This is mainly due to the work-function differences between the floating-gate and the discrete nanoscale silicon sandwiched between the control oxide and the tunnel oxide.

Fig. 1 Structure of the floating-gate (a) and discrete nanoscale silicon (b) memory devices simulated with Taurus Suprem-4.

Fig. 2 Transfer characteristics of floating-gate and discrete nanoscale silicon memory devices at $V_d = 0.1 \text{ V}$.

The effect of control oxide thicknesses on the trapping properties is simulated and is shown in Fig. 3. The charging was carried out with $V_g = 12 \text{ V}$ and $V_d = 5 \text{ V}$, respectively. Larger threshold voltage shift is observed for thinner control oxide. At a shorter programming time, more electrons can easily trap into the nanoscale silicon when the control oxide thickness reduces. Besides, it is observed that there is a left shift to the step-like behavior when the control oxide thickness reduces. For example, the V_{th} saturates at 20 V in 10^{-4} s when the control oxide thickness reduces to 20 nm , compared to that at 10^{-3} s for the 40 nm control oxide. At the same programming time, thinner control oxide leads to larger V_{th} shift compare to that of a thicker control oxide.

Fig. 3 Comparison of V_{th} shift for different control oxide thicknesses.

Fig. 4 V_{th} shift as a function of programming voltage. Programming transient was carried out with $V_d = 5.5$ V, V_s and $V_b = 0$ V.

Fig. 4 shows the threshold voltage shift as a function of programming voltages and programming time. The drain voltage is fixed at +5.5 V. When the gate voltage increases from +8 V to +9 V, the threshold voltage shift increases ~0.5 V at a programming time of 10^{-4} s. Larger threshold voltage shift can be observed at the time of 10^{-4} s when the programming voltage increases to +11 V. On the other hand, the step-like behaviors are observed for different programming voltages too. As shown in Fig. 4, saturation of V_{th} occurs at 10^{-1} s for both $V_g = +8$ and +9 V. When the V_g increases to +10 or +11 V, the saturation of V_{th} occurs at 10^{-2} s, which is one order earlier compared to $V_g = +8$ and +9 V. This shows that the step-like behavior which attributes to the parallel electric field that plays an important role during the trapping of charges in nanoscale silicon. When charge trapped into the discrete nanoscale silicon, the electric field at each of the nanoscale silicon will influence further charge trapping at itself as well as at the neighboring discrete nanoscale silicon. This effect will not be observed if the simulation is carried out without considering the parallel electric field among the discrete nanoscale silicon.

The effect of V_{th} shift as a function of programming time for different tunnel oxide thicknesses is shown in Fig. 5. The charging was carried out with $V_g = 12$ V and $V_d = 5$ V, respectively. Larger V_{th} shift is observed when the tunnel oxide thickness reduces. Besides, a step-like behavior is observed when the charging time increases from 10^{-4} s to 10^{-3} s and from 10^{-2} s to 10^{-1} s. The lateral electric field plays an

important role in the charge trapping process. When there are charges trapped in the nanoscale silicon, the induced lateral electric field can block further electron from trapping into the nanoscale silicon, thus reducing the amount of trapped electrons.

Fig. 5 Comparison of V_{th} shift for different tunnel oxide thicknesses.

Fig. 6 Charge distribution with different tunnel oxide thicknesses.

The charge distribution after the charging effect as a function of tunnel oxide thicknesses is shown in Fig. 6. The charging is carried out with $V_g = 12$ V, $V_d = 5.5$ V, grounding both the source and bulk terminals. The amount of charges is higher near the drain region since CHE programming is applied during in this study. It is observed that there are lateral charge diffusions to the neighboring discrete nanoscale silicon. When the tunnel oxide thickness reduces, the lateral charge diffusions become significant.

It will be interesting to examine the trapping properties when the dimension of the discrete nanoscale silicon is being reduced. Fig. 7 shows the threshold voltage shift as a function of

programming voltages when the dimension of the discrete nanoscale silicon reduces to $10\text{ nm} \times 10\text{ nm}$. As the V_g increases to $+11\text{ V}$, saturation of charge trapping occurs at 10^{-4} and at 10^{-2} s respectively. In contrast to the discrete nanoscale silicon with a dimension of $20\text{ nm} \times 20\text{ nm}$, saturation of charge trapping occurs only one time. This shows that the parallel electric field effect becomes dominant when the dimension of the discrete nanoscale silicon reduces.

Fig. 7 V_{th} shift as a function of programming voltages for dimension of $10\text{ nm} \times 10\text{ nm}$. Programming transient is carried out at $V_d = 5.5\text{ V}$, V_s and $V_b = 0\text{ V}$.

Fig. 8 V_{th} shift as a function of programming voltages for dimension of $5\text{ nm} \times 5\text{ nm}$. Programming transient is carried out at $V_d = 5.5\text{ V}$, V_s and $V_b = 0\text{ V}$.

On the other hand, it is observed that the charge trapping can occur at relatively shorter time when the dimension of the discrete nanoscale silicon reduces from $20\text{ nm} \times 20\text{ nm}$ to $10\text{ nm} \times 10\text{ nm}$. At $V_g = 11\text{ V}$ for 10^{-6} s , there is $\sim 2.8\text{ V}$ shift in V_{th} for the $10\text{ nm} \times 10\text{ nm}$ Flash memory compared to $\sim 0.2\text{ V}$ shift in the V_{th} for the $20\text{ nm} \times 20\text{ nm}$ Flash memory. The

difference is mainly due to the reduction of thickness of the discrete nanoscale silicon layer. Similarly as shown in Fig. 8, when the discrete nanoscale silicon dimensions reduced to $5\text{ nm} \times 5\text{ nm}$, charge trapping becomes more easily. Thus, the V_{th} shift becomes larger. For example, at $V_g = +9\text{ V}$ for 10^{-5} s , the V_{th} shift for the $10\text{ nm} \times 10\text{ nm}$ memory device is $\sim 2\text{ V}$. In contrast, the V_{th} shift for the $5\text{ nm} \times 5\text{ nm}$ memory devices is $\sim 4.4\text{ V}$, which is two times larger than that of a $10\text{ nm} \times 10\text{ nm}$ memory devices. This shows that larger V_{th} shift in the discrete nanoscale silicon with smaller dimension compared to that of a bigger dimension.

IV. CONCLUSION

Flash memory devices based on discrete nanoscale silicon with different dimensions are being simulated. It is observed that thinner the control oxide or tunnel oxide promotes easiness in charging up the discrete nanoscale silicon, thus producing bigger threshold voltage shift. On the other hand, it is observed that larger threshold voltage shift in the discrete nanoscale silicon for smaller dimension compared to that of the bigger dimension.

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