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PAPER

An Ultra-Low Voltage Analog Front End for Strain Gauge Sensory System Application in 0.18 μm CMOS

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SUMMARY This paper presents analysis and design of a new ultra-low voltage analog front end (AFE) dedicated to strain sensor applications. The AFE, designed in 0.18 μm CMOS process, features a chopper-stabilized instrumentation amplifier (IA), a balanced active MOSFET-C 2nd order low pass filter (LPF), a clock generator and a voltage booster which operate at supply voltage (V_{dd}) of 0.6 V. The designed IA achieves 30 dB of closed-loop gain, 101 dB of common-mode rejection ratio (CMRR) at 50 Hz, 80 dB of power-supply rejection ratio (PSRR) at 50 Hz, thermal noise floor of 53.4 nV/ $\sqrt{\text{Hz}}$, current consumption of 14 μA , and noise efficiency factor (NEF) of 9.7. The high CMRR and rail-to-rail output swing capability is attributed to a new low voltage realization of the active-bootstrapped technique using a pseudo-differential gain-boosting operational transconductance amplifier (OTA) and proposed current-driven bulk (CDB) biasing technique. An output capacitor-less low-dropout regulator (LDO), with a new fast start-up LPF technique, is used to regulate this 0.6 V supply from a 0.8–1.0 V energy harvesting power source. It achieves power supply rejection (PSR) of 42 dB at frequency of 1 MHz. A cascode compensated pseudo differential amplifier is used as the filter's building block for low power design. The filter's single-ended-to-balanced converter is implemented using a new low voltage amplifier with two-stage common-mode cancellation. The overall AFE was simulated to have 65.6 dB of signal-to-noise ratio (SNR), total harmonic distortion (THD) of less than 0.9% for a 100 Hz sinusoidal maximum input signal, bandwidth of 2 kHz, and power consumption of 51.2 μW . Spectre RF simulations were performed to validate the design using BSIM3V3 transistor models provided by GLOBALFOUNDRIES 0.18 μm CMOS process.

key words: active-bootstrapped, analog front end, chopper-stabilized amplifier, continuous-time filter, energy harvesting, instrumentation amplifier, low-dropout regulator, low voltage, strain gauge transducer

1. Introduction

Recent interest in energy harvesting systems has sparked research in low voltage analog ICs. For example, solar cells powered systems benefit directly in terms of reliability and compactness in view of the fact that solar cells are traditionally stacked in series with a significant number to provide a high V_{dd} . The commonly used energy harvesting design [1] uses a boost converter to provide a local boosted V_{dd} at the cost of switching noise at high frequency where most analog circuits have poor PSR. This paper, in contrast, provides a true low voltage analog solution in the design of low noise, low power, and high power supply/common-mode rejection energy harvesting sensory system that operates at only two stacked solar cells.

Conventional techniques such as cascoding and strong-inversion operation are a design concern in low V_{dd} operation. Use of weak-inversion operation [2] reduces designer's degree of freedom in optimizing amplifier's input-stage transistors' noise contribution. This unavoidably leads to a considerable increase of noise power spectral density (PSD). If the active load transistors are biased at the same inversion level with the input transistors, the PSD can be approximated to double compared to high V_{dd} design's noise PSD. In addition to the reduced signal swing in low V_{dd} design, this forces designer to increase circuit's current consumption so as to get satisfactory SNR.

Threshold voltage (V_t) reduction via forward-biased bulk [3] has been explored to increase amplifier's input common-mode range (ICMR). This technique also allows for transistor operation in slightly higher inversion level compared to transistor with grounded bulk connection for the same gate-source voltage bias and quiescent current. Excessive forward bias, however, can reduce reliability and increase chances of turning on parasitic BJT which can couple its noise to the circuit.

With V_{dd} of 0.6 V, the use of tail current source reduces the available headroom for the input and active load transistors. Tail current source-less design or pseudo-differential [4], although very attractive in low V_{dd} design, has poor common-mode rejection (CMR) which is not adequate for instrumentation application. Cascading fully differential amplifiers can solve this problem at the cost of higher power consumption. Triode tail current source [5], [6], which utilize feedback to suppress common-mode signal, can be used to retain the advantage of additional CMR capability of tail current source design. Nevertheless, the CMRR of a design using tail current source and current-mirror active load, which is approximately two-stage of gain, is still not adequate.

The objective of this work is to explore and to propose low voltage analog techniques applicable to the design of low noise instrumentation systems. Following this introduction, the AFE and its application are explained in Sect. 2.

The main highlight of the paper is a new differential difference amplifier (DDA) using the active-bootstrapped technique [7]. The OTA, which is the core building block of the technique, is implemented using the pseudo-differential technique suitable for low V_{dd} operation. New low voltage CDB bias circuit is also proposed to reduce the noise contribution of the input stage's active load transistors. Mathematical analysis, qualitative circuit description, and simulation

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results of the technique are discussed on Sect. 3.

Other supporting building blocks of the AFE: LDO, MOSFET-C filter, clock generator and voltage booster circuitry are qualitatively described in Sects. 4, 5, and 6 respectively including methods to reduce bandgap's PSR contribution in an LDO and to improve CMRR in a pseudo-differential two-stage amplifier. The overall system's simulation results and conclusion are given in Sects. 7 and 8.

2. Analog Front End Architecture & Specifications

An overview of the AFE is given in Fig. 1. Differential input signal from external strain gauge is amplified by a single-ended-output chopper-stabilized IA, splitted by a single-ended-to-balanced converter, and filtered by a balanced active MOSFET-C filter. An LDO regulates both the internal V_{dd} of 0.6 V and the strain gauge's bias voltage. An external 32.768 kHz tuning fork crystal, requiring two external pins, is used to generate a chopper clock for the IA. This clock is boosted by a two-stage charge pump to generate a tripled clock with swing of approximately 1.8 V. The charge pump also provides a stable 1.8 V voltage to bias the filter's MOSFET resistors.

Strain gauge connected in wheatstone bridge configuration, shown in Fig. 1, yields a linear relationship between its output voltage and its sensed strain given by

$$V_{in} = \frac{\Delta R}{R} \frac{R}{R + R_{bias}} V_{dd} \quad (1)$$

where $R/(R + R_{bias})V_{dd}$ is the strain gauge's bias voltage $V_{bias,sg}$ and the change of resistance ΔR is related to the sensed strain by

$$\Delta R = \epsilon GF R \quad (2)$$

where ϵ is the sensed strain and GF is the strain gauge's

gauge factor, that is pertaining to its sensitivity.

The differential output noise PSD of this configuration is simply $4kTR$. R_{bias} , which only contributes common-mode noise, influences input SNR since it sets the maximum signal's magnitude as shown in Eq. (1).

In this design, 1 k Ω strain gauge is used. With $V_{bias,sg}$ of 0.3 V, maximum strain of 30,000 μ , and GF of 2, it consumes 300 μ A of supply current, produces 0.18 mV of maximum output signal, and exhibits differential output noise voltage spectral density (VSD) of 4.07 nV/ $\sqrt{\text{Hz}}$. Even when biased at low voltage, the strain gauge's noise is not the limiting factor to the overall system's SNR.

Table 1 shows some of the typical strain gauge's parameters [8]. Mismatch in strain gauge's nominal resistance creates unavoidable DC offset at the IA's inputs. For example, choosing strain gauge with $\pm 0.15\%$ mismatch will yield 540 mV peak-to-peak output signal and 48 mV output offset for IA gain of 29.54 dB (30 V/V) which is marginally adequate to prevent output signal clipping. In this design, offset calibration is implemented by trimming the resistive voltage divider that biases the DDA's V_{-} terminal. The detailed implementation, similar to gain error calibration, is discussed briefly in the next section.

Table 1 Omega SGD series strain gauge parameters.

Parameter	Value
R Tolerance	$\pm 0.15\% - \pm 0.5\%$ depending on gauge spec
Gauge Factor	2.00 $\pm 5\%$
TC (Steel) (Ref=23°C)	11 ppm/°C
Operating Temp.	-75–200°C
Max. Strain	30,000 μ

Fig. 1 AFE's block diagram.

3. Active-Bootstrapped Chopper-Stabilized Instrumentation Amplifier

DDA [9] is an excellent choice to implement low voltage IA with reasonable power consumption. Compared to the three op-amp IA, the CMRR in a DDA-based IA does not depend on resistor matching. The current feedback IA [10], [11], although has excellent NEF, is not suitable for low V_{dd} operation.

The output voltage of a DDA-based IA, shown in Fig. 2, is given by

$$V_{out} = \frac{A_{ol}}{1 + A_{ol}\beta}(V_{in} + V_{os} + V_{bias}) + \frac{1}{2} \frac{1}{\beta} \frac{V_{in}}{CMRR_d} \quad (3)$$

where A_{ol} is the DDA's open loop gain, $\beta = R_{f2}/(R_{f1} + R_{f2})$ is the feedback factor, V_{in} is the strain gauge's output voltage, V_{os} is the combined DDA's and strain gauge's offset voltage, V_{bias} is the bias voltage applied to DDA's V_{-} terminal to set the DC output voltage at half V_{dd} , and $CMRR_d$ is the differential common-mode rejection ratio which quantifies rejection from the $\{(V_{++} - V_{+-}) + (V_{-+} - V_{--})\}/2$ signal.

A DDA has two sources of gain error, the finite open loop gain A_{ol} and the finite differential common-mode gain $CMRR_d$. While the error caused by finite A_{ol} is dominant when the chosen closed-loop gain $1/\beta$ is high, the error caused by finite $CMRR_d$ is constant regardless of the closed-loop gain. Finite $CMRR_d$ is mainly caused by g_m mismatch in the DDA's input transistors. This in turn is caused by the tail current source mismatch. As they are biased in weak inversion, the matching is poor and unavoidable in low V_{dd} operation.

Gain error can be digitally calibrated by implementing R_{f1} or R_{f2} using series resistor strings and switches. Monte Carlo simulations were done to measure the initial gain error of the IA (about 2%). The number of resistors and switches can be chosen to set the gain accuracy.

Accounting all the noise sources seen in Fig. 2, the IA's input-referred noise PSD is given by,

$$\begin{aligned} \frac{\overline{v_{ilAn}^2}}{\Delta f} &= \frac{\overline{v_{iDDAn}^2}}{\Delta f} + 4kTR_{f2}\beta + \frac{\overline{v_{biasn}^2}}{\Delta f} \\ &+ \frac{\overline{v_{ddn}^2}}{\Delta f} \left| \frac{1}{PSRR} + \frac{1}{2CMRR} \frac{R}{R + R_{bias}} \right|^2 \end{aligned} \quad (4)$$

where the terms on the right hand side of Eq. (4) are noise contributed by the DDA, feedback resistors, bias voltage,

Fig. 2 A DDA-based IA with non-idealities shown.

and supply rail respectively. The bias voltage can be easily obtained using a voltage divider from V_{dd} which is shown in the offset trim block in Fig. 1. The noise from this bias voltage appears as a common-mode noise at the outputs of the single-ended-to-balanced converter since the converter is biased by the same voltage divider ($V_{dd}/2$ in Fig. 1).

The active-bootstrapped technique can also be applied in a DDA to boost CMRR and to allow interfacing between input and output stage without using the folding structure. Shown in Fig. 3, it consists of two differential pairs M_{1a} , M_{1b} , M_{1c} , and M_{1d} biased by tail current sources M_{5a} and M_{5b} , active loads M_{2a} and M_{2b} biased by a gain-boosting OTA and an output-stage transistor M_3 biased by a pseudo class AB current source M_4 [12].

3.1 Closed-Loop Stability Analysis

Assuming high impedance tail current source, one can rearrange all the small-signal nodal equations of the circuit in Fig. 3 (feedback network not shown) to obtain the signal flow graph illustrated in Fig. 4. g_{m1} , g_{m2} , and g_{m3} are the transconductances of the input transistors, active loads, and output-stage transistor respectively. g_{mdm} and g_{mcm} are the OTA's differential-mode and common-mode transconductances. $R_1 = (r_{o1}/2) \parallel r_{o2}$ is the input-stage output resistance without active-bootstrap technique and $R_2 = r_{o3} \parallel r_{o4} \parallel (R_{f1} + R_{f2})$ is the output resistance of the output stage.

By applying the Mason's gain formula [13] to the signal flow graph shown in Fig. 4, one can see that the active-bootstrapped input stage is a three-stage amplifier. There are three feedforward paths from the inputs to the output: (i) M_{1b} common-source, (ii) M_{1b} common-source $\rightarrow$ OTA's

Fig. 3 Simplified schematic of the proposed DDA.

Fig. 4 Signal flow graph of the active-bootstrapped DDA.

inverting terminal $\rightarrow M_{2b}$ common-source, and (iii) $M_{1a,c}$ common-source $\rightarrow$ OTA's non-inverting terminal $\rightarrow M_{2b}$ common-source. Due to matching property, the positive and negative feedback loop gains, as indicated in Fig. 4, cancel each other. This leaves the three-stage feedforward gain paths intact.

By adding a common-source amplifier as an output stage, the rail-to-rail output swing capability is obtained. Since the IA is not designed for unity gain, Miller compensation is adequate in this design without any significant power drain.

The closed-loop transfer function of the active-bootstrapped DDA based IA is given by

$$A_{cl}(s) = \frac{A_{ol}}{1 + A_{ol}\beta} \frac{\left(1 + \frac{s}{z_1}\right) \left(1 + \frac{s}{z_2} + \frac{s^2}{z_2 z_3}\right)}{1 + \frac{s}{p_1} + \frac{s^2}{p_1 p_2} + \frac{s^3}{p_1 p_2 p_3} + \frac{s^4}{p_1 p_2 p_3 p_4}} \quad (5)$$

where the open loop gain A_{ol} is given by

$$A_{ol} = (g_{m1} R_1 g_{mdm} / g_{mcm}) (g_{m3} R_2) \quad (6)$$

and the input-stage output resistance R_1 is boosted by the OTA's CMRR g_{mdm} / g_{mcm} . In this design, the gain-boosting OTA is realized using pseudo-differential technique. Therefore, one can assume that OTA's common-mode gain is in the order of unity. In the case that OTA's CMRR is high, the input-stage output resistance is boosted by factor of $g_{mdm} R_{ota} g_{m2} R_1$.

The zeros are given by

$$z_1 = -\frac{g_{m3}}{C_c} \quad (7)$$

$$z_2 = \frac{g_{mdm}}{C_{gd2a}} \parallel -\frac{2g_{m2}}{C_{gd2a} + C_{gd2b}}; \quad z_2 z_3 = \frac{2g_{m2} g_{mdm}}{Y} \quad (8)$$

and the poles are given by

$$p_1 = \frac{(\beta g_{m1}) \parallel -g_{m3}}{C_c} \quad (9)$$

$$p_1 p_2 = \frac{\beta g_{m1}}{C_c} \left[\frac{g_{m3}}{X/C_c} \parallel -\frac{g_{m3}}{Y/C_c} \parallel \frac{g_{mdm} \parallel -g_{m2}}{C_{gd2a}} \right] \quad (10)$$

$$p_1 p_2 p_3 = \frac{\beta g_{m1}}{C_c} \left[\frac{g_{m2} g_{mdm}}{Z} \parallel \frac{g_{m3} (g_{mdm} \parallel -g_{m2})}{X C_{gd2a} / C_c} \parallel \frac{g_{m3} (g_{mdm} \parallel g_{m2})}{Y C_{gd2b} / C_c} \right] \quad (11)$$

$$p_1 p_2 p_3 p_4 = \frac{\beta g_{m1} g_{m2} g_{m3} g_{mdm}}{XZ} \quad (12)$$

where

$$X = C_L C_c + C_L C_1 + C_c C_1; \quad Y = (C_L + C_c) C_2 \quad (13)$$

$$Z = C_{ota} C_2 + C_{ota} C_{gd2a} + C_2 C_{gd2a} + C_2 C_{gd2b} \quad (14)$$

The following assumptions are used when obtaining the above expressions: (i) high single-stage amplifier gain (> 40 dB), (ii) small OTA's differential transconductance, and (iii) $C_{gd2a} \approx C_{gd2b}$ is small.

Fig. 5 Proposed pseudo-differential gain-boosting OTA.

Note that the underlined terms are pole-zero locations of a two-stage Miller compensated amplifier in closed-loop configuration. The modified pole-zero locations attributed by this technique will now be discussed.

Equation (10) indicates that RHP poles exist caused by the positive feedback loop. This effect can be minimized by ensuring the capacitive loading for the positive feedback loop is higher than that of negative feedback loop ($C_1 > C_2$).

Very crude approximation for p_2 and p_3 are: g_{m3}/C_L and $(g_{m2} g_{mdm} / g_{m3}) / (C_{ota} C_2 / C_c)$ respectively. This indicates potential peaking ($p_3 < p_2$) due to the small value of OTA's transconductance and the large size of C_{ota} (long channel device is used in M_2). Another design rule-of-thumb is to ensure $g_{mdm} \parallel -g_{m2}$ to be positive to reduce the potential presence of RHP pole.

3.2 Noise Analysis

The input-referred noise PSD of the DDA is given by

$$\frac{v_{iDDAn}^2}{\Delta f} = 4kT \frac{\gamma}{\alpha} \frac{1}{g_{m1}} \left(4 + 2 \frac{g_{m2}}{g_{m1}} \right) + \frac{v_{iOTAn}^2}{\Delta f} \frac{1}{g_{m1}^2 R_1^2} \left| \frac{\left(1 + \frac{s}{z_1}\right) \left(1 + \frac{s}{z_2}\right)}{1 + \frac{s}{p_1} + \frac{s^2}{p_1 p_2}} \right|^2 \quad (15)$$

with zeros and poles given by

$$z_1 = \frac{1}{R_1 (C_2 + C_{gd2a})}; \quad z_2 = \frac{g_{m2}}{C_{gd2b}} \quad (16)$$

$$p_1 = \frac{g_{mdm}}{C_{gd2a}} \parallel \frac{-2g_{m2}}{C_{gd2a} + C_{gd2b}}; \quad p_1 p_2 = \frac{2g_{m2} g_{mdm}}{Z} \quad (17)$$

where γ/α is a constant and is approximately 2/3 in long channel MOSFET.

For good $CMRR_d$ or gain error performance, both differential pairs are usually matched. This increases DDA's input-referred noise VSD by a factor of $\sqrt{2}$ compared to that of an op amp.

The gain-boosting OTA contributes little to the overall DDA's noise performance. It can be deduced from Fig. 5, OTA's input noise voltage is only amplified twice whereas the input signal has to go through three stages of amplification. By the same reasoning, the OTA's offset voltage can also be considered to be negligible.

3.3 Detailed Circuit Description

The complete schematic of the proposed DDA is shown in

Fig. 6 Complete schematic of the proposed active-bootstrapped chopper-stabilized DDA.

Fig. 6. The Dynamic Threshold MOS (DTMOS) [14], [15] devices are used as the input transistors M_{1a} , M_{1b} , M_{1c} , and M_{1d} for the DDA. The DTMOS is essentially a MOS transistor with shorted gate and bulk connection. As a result, the bulk transconductance (g_{mb}) directly adds to the gate transconductance (g_m), reducing noise PSD by approximately 20% ($g_{mb}/g_m \approx 0.2$).

To increase ICMR, the tail current sources M_{5a} and M_{5b} that can work in the triode region [5] are used in the design. As long as M_{7a} , M_{7b} , and M_{8a} remain in saturation, a constant current is forced to flow in M_{6a} and copied by M_{5a} to bias the input transistors. Transistors M_{7a} and M_{7b} replicate the input transistors and sense the common-mode signal. This common-mode signal is amplified by M_{6a} and fed back to M_{7a} through its non-inverting terminal. The resulting negative feedback suppresses the common-mode signal. The same also goes for M_{5b} , M_{6b} , M_{7c} , M_{7d} , and M_{8b} .

Small-signal analysis shows that the common-mode gain of an active-bootstrapped DDA using the feedback tail current source is given by

$$A_{cmDDA} = \frac{1}{2g_{mcm}R_{ota}} \left(\frac{1 - \frac{g_{m6}r_{o6}}{g_{m8}r_{o8}}}{g_{m2}r_{o6}} + \frac{1}{g_{m2}r_{o8}g_{m6}r_{o5}} \right) \quad (18)$$

The common-mode rejection is composed of factor $g_{m2}r_{o8}$ associated with “folded” tail current sources M_{8a} and M_{8b} and $g_{m6}r_{o5}$ associated with feedback’s loop gain. However, in this design the circuit is operated with M_{5a} , M_{5b} , M_{6a} , and M_{6b} in triode region and one can only get a modest common-mode rejection of around $g_{m2}r_{o8}$ neglecting mismatch (assume $g_{mcm}R_{ota}$ around unity since pseudo-differential topology is used). Combining this and Eq. (6), one gets CMRR of approximately $2g_{m1}R_1g_{mcm}R_{ota}g_{m2}r_{o8}$ in the ideal case.

The unique feature of the proposed IA is the adoption of pseudo-differential technique in the design of gain-

boosting OTA. This shows that the active-bootstrapped technique can also be used in $V_t + V_{dsat}$ supply operation. Besides boosting CMRR, this approach allows interfacing between the active-bootstrapped input stage and the PMOS common-source output-stage. One difficulty in using this approach is in the start-up phase of the amplifier since the bias current of pseudo-differential circuit depends on the input voltage. During start-up phase, the voltage at M_{2a} and M_{2b} ’s drain terminals are near V_{dd} because of higher parasitic capacitance from there to V_{dd} (C_{gs} of M_3) than that to ground. In that condition, the PMOS input transistors of the gain-boosting OTA M_{9a} and M_{9b} are turned off. No current will flow through M_{12a} and M_{12b} and the bias currents from M_{14a} and M_{14b} will bias the OTA’s active loads M_{13a} and M_{13b} . This in turn biases the main amplifier’s active loads M_{2a} and M_{2b} to discharge their parasitic drain capacitance. This large signal start-up loop is stable because of the positive sign of the OTA’s common-mode gain. Conventional OTA, however, is biased by tail current source which automatically biases the active load of the main amplifier. In that case, no start-up problem occurs.

To reduce noise contributed by the active loads M_{2a} and M_{2b} , they are operated in moderate-inversion using the current-driven bulk technique. Although strong-inversion operation is preferred for lower noise, M_{2a} and M_{2b} ’s headroom is fixed by $V_{dd} - V_{sg3}$. Therefore, their output resistance will drop and noise from the gain-boosting OTA starts to be noticeable when they are operated at strong-inversion (see Eq. (15)). The β insensitive bias circuit in [3] is not used in this design due to limited headroom. As an alternative, a new feedback-based bias circuit is proposed.

In the proposed CDB biasing circuit, a reference transistor M_{18} is biased to have the desired V_{gs} , 0.45 V for example. M_{19} is designed to have lower aspect ratio than M_{18} , which implies higher inversion level or lower g_m/I_d . To

Table 2 Comparison with the published IAs.

Parameter	[18]	[10]	[19]	[11]	[20]	[21]	[22]	[23]	This Work
Tech.	1.5 μm	0.5 μm	0.8 μm	0.5 μm	0.18 μm	0.13 μm	0.18 μm	0.18 μm	0.18 μm
A_{cl}	39.5 dB	20 dB	40 dB	48 dB	45 dB	-	46 dB	-	29.54 dB
-3 dB BW	7.2 kHz	40 kHz	100 Hz	28 kHz	150 Hz	-	-	-	18.8 kHz
CMRR	83 dB @ 5 kHz	127 dB @ 1 kHz	83 dB @ 50 Hz	120 dB @ 1 kHz	125 dB @ 50 Hz	105 dB @ 10 Hz	150 dB @ 10 Hz	131 dB @ 10 Hz	101 dB @ 50 Hz
PSRR	85 dB @ 5 kHz	80 dB @ 50 Hz	-	-	-	90 dB @ -	62 dB @ 10 Hz	84 dB @ 10 Hz	80 dB @ 50 Hz
$\frac{v_{iN}^2}{\Delta f}$ @ 1 kHz	21 $\frac{\text{nV}}{\sqrt{\text{Hz}}}$	57 $\frac{\text{nV}}{\sqrt{\text{Hz}}}$	100 $\frac{\text{nV}}{\sqrt{\text{Hz}}}$	55 $\frac{\text{nV}}{\sqrt{\text{Hz}}}$	-	50 $\frac{\text{nV}}{\sqrt{\text{Hz}}}$	-	54 $\frac{\text{nV}}{\sqrt{\text{Hz}}}$	53.4 $\frac{\text{nV}}{\sqrt{\text{Hz}}}$
Chop. Freq	-	4 kHz	16 kHz	2 kHz	-	250 kHz	-	-	33 kHz
V_{DD}	5 V	3 V	1.8 V	3 V	1 V	1.5 V	1.8 V	1.8 V	0.6 V
I_{DC}	16 μA	11.1 μA	1.11 μA	2.3 μA	165 μA	210 μA	2.22 μA	10.7 μA	14 μA
$V_{DD}I_{DC}$	80 μW	33.3 μW	2 μW	6.9 μW	165 μW	315 μW	4 μW	19.3 μW	9 μW
NEF	4.0	9.2	4.6	4.2	-	24	-	6.7	9.7

Fig. 7 DDA's open and closed loop transfer function.

match both transistors' V_{gs} , an amplifier formed by M_{20a} , M_{20b} , M_{21a} , and M_{21b} is used to control the bias transistor M_{22} . As a result, transistor with a higher inversion level can be designed using this technique.

To drive the relatively low 200 k Ω feedback resistors, a power efficient pseudo class AB output stage [12] is used. The cut-off operated transistor M_{15} implements a very large resistor to block the DC biasing whereas a coupling capacitor C_{bat} makes this configuration looks like a class AB amplifier during AC condition.

The second-stage is formed by a PMOS common-source amplifier. This peculiar arrangement limits ICMR if this amplifier is operated at high V_{dd} . However, this is not of a concern in a fixed low V_{dd} operation. The ICMR of the proposed topology is given by

$$\text{ICMR}_{\min} = V_{dd} - V_{sg3} + V_{dsat1} - V_{sg1} \quad (19)$$

$$\text{ICMR}_{\max} = V_{dd} - V_{dsat5} - V_{sg1} \quad (20)$$

$$\text{ICMR} = V_{sg3} - V_{dsat1} - V_{dsat5} \quad (21)$$

which indicates that ICMR is fixed regardless of V_{dd} .

The chopper-stabilization technique [16] can be used in conjunction with the active-bootstrapped technique to reduce offset and flicker noise of the DDA. Since the differential-to-single-ended conversion is implemented in the input-stage, the modulator placement in [17] is used. Chopper-stabilization is also applied to the gain-boosting OTA to remove its offset and flicker noise.

3.4 DDA Simulation Results

The simulated open-loop transfer function of the DDA is

Fig. 8 DDA's input-referred noise voltage spectral density. **Fig. 9** DDA's open loop gain and input transistors' transconductance vs. input common-mode voltage.

given in Fig. 7. The open-loop gain and GBW are 123 dB and 500 kHz respectively for 50 pF in parallel with 200 k Ω load. Since the DDA is dedicated to provide the gain function and it will not operate at 0 dB of gain, one can save power by biasing the second-stage just enough to drive the feedback resistors, which are constrained by the noise requirements. At a gain of 29.54 dB, the phase margin is 85°. Other DDA performance parameters are shown in Figs. 8–11. Table 2 shows that the DDA ultra-low voltage performances are comparable with the reported works.

To verify the agreement between theoretical analysis and simulation results, Spectre pole-zero analysis was performed for the DDA under closed-loop condition. The simulated pole-zero locations, ignoring the doublets, were compared with Eqs. (5)–(12) using parameters estimated from Spectre DC operating point simulation. Shown in Table 3,

Fig. 10 DDA's CMRR and PSRR frequency response.

Fig. 11 DDA's CMRR (50 Hz) 3 σ monte carlo simulations.

the theoretical analysis predicts the locations of poles and zeros with reasonable accuracy when considering the effects of gain-boosting OTA's internal poles and zeros, β frequency degradation caused by finite DDA's input capacitance, and complete quasi static capacitance modelling used by the simulator which includes the effects of C_{dg} .

In addition to the well known RHP zero caused by Miller compensation, this technique adds two complex zeros which is responsible for the peaking of the noise response in Fig. 8 at frequency around 400 kHz. The presence of the complex poles is harder to be seen since the complex poles and zeros damped each other in the closed-loop response, but nevertheless slight peaking is observed around 300 kHz in Fig. 8 followed by a notch caused by the complex zeros. Together, the theory predicts -270° of phase at high frequency after taking into account 1 RHP zero, 2 complex zeros, 2 complex poles, and 2 LHP poles which is true at frequency around the RHP zero (846.8 kHz which is at the highest frequency). The complete simulation, however, predicts more poles and zeros than that of the prediction of the theory. This is why the closed-loop frequency response goes beyond -270° of phase.

Transient response shown in Fig. 12 verifies that the design is stable. Note that the transient simulation was performed for the whole AFE and the IA is loaded by the filter in this case. The strain-gauge is modelled by resistors and some voltage controlled voltage sources to emulate the resistance changes (the input signal). The input signal glitches shown in Fig. 12 is caused by the input chopper modulator's finite non-overlapping clock and finite strain gauge's input resistances.

The noise responses of the DDA with and without chopper-stabilization simulated with PSS+PNOISE analyses are shown in Fig. 8. Chopper-stabilization reduces

Table 3 Predicted and simulated pole-zero locations.

Parameter	Predicted	Simulated
zero 1	$-115.0 + j 460.2 \text{ kHz}$	$-71.76 + j 393.3 \text{ kHz}$
zero 2	$-115.0 - j 460.2 \text{ kHz}$	$-71.76 - j 393.3 \text{ kHz}$
zero 3	728.1 kHz	846.8 kHz
zero 4	NA	-1.749 MHz
pole 1	-20.22 kHz	-17.77 kHz
pole 2	$-55.36 + j 315.2 \text{ kHz}$	$-33.32 + j 305.3 \text{ kHz}$
pole 3	$-55.36 - j 315.2 \text{ kHz}$	$-33.32 - j 305.3 \text{ kHz}$
pole 4	-187.9 kHz	-309.2 kHz
pole 5	NA	-1.208 MHz

Transconductances: $g_{m1} = 49.48 \mu\text{S}$, $g_{m2} = 63.43 \mu\text{S}$, $g_{m3} = 68.62 \mu\text{S}$, $g_{mdm} = 908.3 \text{ nS}$, and $\beta = 0.03333$.

Capacitances: $C_L = 50 \text{ pF}$, $C_c = 15 \text{ pF}$, $C_{ota} = 16 \text{ pF}$, $C_1 = 1.2 \text{ pF}$, $C_2 = 650 \text{ fF}$, and $C_{gd2a} = C_{gd2b} = 150 \text{ fF}$.

Fig. 12 IA's transient response.

flicker noise from $365 \text{ nV}/\sqrt{\text{Hz}}$ to $53.7 \text{ nV}/\sqrt{\text{Hz}}$ at 1 Hz at the cost of peaking at the chopper frequency of 32.768 kHz. Peaking predicted by Eq. (15) can also be seen in the noise response.

With $14 \mu\text{A}$ current consumption (without bias circuit) and integrated input noise voltage of 537.2 nVrms (0.5–100 Hz or 64 Hz noise bandwidth), the NEF is calculated to be 9.7. For a differential pair operated in weak inversion, its theoretical minimum NEF is 2.9 [18]. Since a DDA has four input transistors, its theoretical minimum NEF is 5.8. If the active load transistors have the same noise contribution with that of the input transistors, this NEF again degrades with $\sqrt{2}$ to 8.2. The gain-boosting OTA, output stage, and feedback resistors consume a total of $4 \mu\text{A}$. When compared with $10 \mu\text{A}$ input-stage current consumption, this additional current consumption degrades NEF by $\sqrt{1.4}$ to 9.7. This degradation of NEF is tolerable in view of low V_{dd} operation.

The DDA's open loop gain plotted against common-mode input voltage is shown in Fig. 9. The input transistors stay in saturation up to common-mode voltage of 0.2 V, which is more than sufficient in this application.

Frequency response of CMRR and PSRR is shown on Fig. 10. Note that the AC analysis overestimates low frequency CMRR based on assumption of perfect matching. In order to estimate the realistic CMRR performance metric, Monte Carlo simulations were conducted.

The 3 σ Monte Carlo simulation results for DC open-loop gain, CMRR, PSRR, gain error, and offset voltage without chopper are 114 dB, 101 dB at 50 Hz, 80 dB at 50 Hz, 2%, and 0.4 mV respectively. CMRR can be expected to get better with the use of chopper-stabilization

Fig. 13 Complete schematic of the proposed LDO.

technique.

4. Composite Cascode Low-Dropout Regulator

The complete schematic of the LDO is given in Fig. 13. The core LDO is composed by a pass transistor M_1 , feedback resistors R_{f1} and R_{f2} , and a pseudo-differential OTA formed by M_{2a} , M_{2b} , M_{3a} , M_{3b} , M_{4a} , and M_{4b} . Composite cascode devices M_{2a} , M_{2b} , M_{3a} , and M_{3b} are used as the OTA's input transistors to create a low impedance node for cascode compensation. In this design, both transistors M_{2a} and M_{3a} are operated in saturation region [24]. This requires M_{3a} to have larger aspect ratio than that of M_{2a} . For M_{2a} to have gain of 20, for example, M_{3a} should have 4 times the aspect ratio of M_{2a} neglecting body effect. At this operating condition, M_{2a} consumes only 60 mV of headroom. The same also goes for M_{2b} and M_{3b} .

Besides stability at no-load condition, cascode compensation has good PSR response [25]. Nevertheless, since the LDO output is referred to the reference voltage, the bandgap's supply noise can be dominant at low frequency.

To eliminate bandgap's PSR contribution, an RC LPF can be constructed using MOSFET M_{14} in cut-off region to implement a very high resistor [12]. Passive RC filtering is the proper choice to eliminate noise and to increase supply rejection of the bandgap in low power operation. However, the large time-constant required for the filtering implies slow start-up.

A new start-up circuit can be constructed whose function is to change M_{14} 's on-resistance during start-up. A key consideration for the design is not to let any parasitic capacitance connects the filter output capacitor C_h to the supply rail as this degrades PSR. This is implemented by common-source amplifier M_{17} loaded by diode connected transistor M_{18} which senses the filter's output voltage.

During start-up, the output voltage of M_{17} is high and the inverter M_{19} and M_{20} is low. This will turn on and turn off transistor M_{16} and M_{15} respectively. The gate terminal of M_{14} is effectively connected to V_{dd} , hence it is operated in triode region. During normal operation, M_{16} and M_{15} are off and on respectively. The gate terminal of M_{14} is effectively connected to the bandgap's output, hence it is operated in cut-off region.

In this design, the current-mode bandgap in [26] is used. Subthreshold-operated MOSFETs M_5 and M_6 are used to replace BJTs. Pseudo-differential OTA composed

Fig. 14 LDO's PSR response.

Table 4 Typical LDO's performance at 27°C.

Parameter	Value
Input Voltage	0.8–1.0 V
Output Voltage	0.6 V
Quiescent Current	5.58 μ A
Load Capacitor	100 pF
Noise at 1 Hz	74 μ V/ $\sqrt{\text{Hz}}$
Noise at 1 kHz	162 nV/ $\sqrt{\text{Hz}}$
TC	75 ppm/ $^{\circ}\text{C}$
Line Reg.	16 mV/V
Load Reg.	2 mV/mA
PSR @ 1 MHz	42 dB

by M_{8a} , M_{8b} , M_{9a} , and M_{9b} forms current mirrors with M_5 and M_6 . This arrangement [27] eliminates biasing circuitry for the OTA.

The LDO was designed to provide maximum current of 500 μ A, in which 300 μ A is supplied to the strain gauge. With the addition of 100 pF output capacitor, the LDO is stable at no-load condition with phase margin of 60°. The LDO achieves 42 dB of PSR at a frequency of 1 MHz. The PSR response, shown in Fig. 14 shows low-frequency pole caused by the filter. The LDO consumes quiescent current of 5.58 μ A, in which 3 μ A is consumed by the bandgap and filter's start-up circuit. Table 4 summarizes the overall LDO performance.

5. Balanced Active MOSFET-C Filter

A balanced MOSFET-C Tow Thomas Biquad, shown in Fig. 15, is used to implement a 2nd order LPF with 2 kHz of cut-off frequency. Active RC filter has the capability to process rail-to-rail input signal with good dynamic range, suitable for low V_{dd} application. Balanced topology [28] is used to cancel even-order of non-linearity and noise from both V_{dd} and V_{bias} . MOSFET resistors are used since a DC voltage is available from the charge-pump. With approxi-

Fig. 15 Balanced MOSFET-C Tow Thomas biquad.

Fig. 16 Fully differential amplifier.

Fig. 17 Proposed single-ended output amplifier.

mately 1.8 V gate bias and 540 mV input signal, this scheme will yield resistors linear enough for this application. Tuning is not implemented in this design since variations in filter's cut-off frequency will not affect SNR considerably.

As a building block for the filter, a pseudo-differential amplifier with common-mode feedforward (CMFF) [4] shown in Fig. 16 is used in this design. The amplifier uses composite cascode devices as the input-stage's active loads and output-stage common-source amplifiers to implement a two-stage cascode compensated amplifier. In contrast with the composite cascode used in the LDO, the bottom transistors M_{3a} , M_{3b} , M_{6a} , M_{6b} , M_{9a} , and M_{9b} are operated in triode region. This yields slight improvement in GBW [29] by factor of $1 + g_{ds3}/g_{m2}$. However, the location of complex poles and peaking's magnitude is lowered and increased by square root of the same factor respectively. This method reduces amplifier's output-stage current consumption with stability maintained. Additional capacitors can be added at the amplifier's outputs and gate terminals of M_{8a} , M_{9a} , M_{8b} , and M_{9b} to reduce peaking without any significant change in the biquad's transfer function.

To implement single-ended-to-balanced conversion, a unity gain inverting amplifier is used. The amplifier, shown in Fig. 17, implements a two-stage common-mode cancellation to eliminate biasing for the output-stage current source.

M_{3a} , M_{3b} , M_{4a} , and M_{4b} sense the common-mode signal. This signal is inverted by M_5 and M_6 and amplified by M_7 to cancel the common-mode signal amplified by M_8 . In contrast with its fully differential CMFF technique counterpart, this scheme does not require the CMFF circuitry to consume the same current as that of the input-stage for optimum cancellation. This technique can also be used to improve CMRR in an op amp with tail current source for non-inverting amplifier application.

Both amplifiers were designed for 0.3 V input common-mode voltage. To avoid overly large transistor associated with subthreshold operation, the proposed current-driven bulk bias circuit described in Sect. 3.3 is used. The amplifiers' bias current is chosen to minimize filter's output noise PSD after the filter's cut-off frequency. The fully-differential amplifier consumes $14.3 \mu\text{A}$ in which the input-stage consumes $6.2 \mu\text{A}$, the CMFF circuitry consumes $6.2 \mu\text{A}$, the output-stage consumes $0.67 \mu\text{A}$, and biasing consumes $0.1 \mu\text{A}$. The single-ended output amplifier consumes $13.4 \mu\text{A}$ in which the input-stage+CMFF circuitry consumes $7.1 \mu\text{A}$ and the output-stage consumes $6 \mu\text{A}$.

6. Clock Generator

A two-pin crystal oscillator in [2] generates 32.768 kHz chopper clock signal. This clock output is tripled by a two-stage charge pump in [30]. The charge pump also provides a stable DC output voltage to bias filter's MOSFET resistors. Since the charge pump only drives transistors' gate, its power consumption is negligible.

7. System Simulation Results and Discussions

The overall transfer function of the AFE, which is dominated by the filter, is shown in Fig. 18. The output noise VSDs with and without the chopper-stabilization of the IA are depicted in Fig. 19. The output noise VSDs of the AFE with chopper-stabilization are $3.917 \mu\text{V}/\sqrt{\text{Hz}}$ at 1 Hz, $3.229 \mu\text{V}/\sqrt{\text{Hz}}$ at 1 kHz and $146.7 \text{ nV}/\sqrt{\text{Hz}}$ at 10 kHz. The integrated output noise of the AFE from 1 Hz–1 MHz was simulated to be $171.7 \mu\text{V}$. With differential output signal of 1.08 V peak-to-peak (0.382 Vrms), this corresponds to 67 dB SNR or sensitivity of $13.4 \mu\text{Strain}$.

To verify the robustness of the design, Monte Carlo simulations were performed on the AFE. The average SNR, shown in Fig. 20, was found to be 65.6 dB. This slight deviation from the ideal condition can be attributed to gain error and mismatch which cause incomplete cancellation of V_{bias} 's and V_{dd} 's noise from the LDO. The calculation of SNR takes into account of the V_{dd} spread caused by the process variations in bandgap's output voltage. 3σ variation in V_{dd} ranges from 0.54 to 0.66 V. Unfortunately, Monte Carlo process model does not include capacitor's variation model. Nevertheless, even increase in filter's cut-off frequency by $\pm 50\%$ can be estimated to reduce SNR by only 1.76 dB.

The transient response of the AFE for a 2 kHz square-wave 18 mV peak-to-peak input signal is shown in Fig. 21.

Fig. 18 AFE's transfer function.

Fig. 19 AFE's output noise voltage spectral density.

Fig. 20 AFE's SNR 3 σ monte carlo simulations.

Fig. 21 AFE's transient response.

The THD for 18 mV 100 Hz sinusoidal input signal was simulated using transient analysis and found to be 0.837%.

Comparison with the published AFEs dedicated to strain-gauge monitoring in Table 5 shows that the proposed design achieves low power operation without sacrificing noise performance. Although this design does not feature an ADC or RF transmitter, the power consumption of the analog signal conditioning circuitry (IA and filter) is much less than the previously published designs.

Table 5 Comparison with the published AFEs dedicated to strain gauge monitoring.

Parameter	[31]	[32]	[33]	This Work
Tech.	2.0 μm	2.0 μm	0.7 μm	0.18 μm
SNR	100 dB	60 dB	-	65.6 dB
Bandwidth	20 Hz	200–600 Hz	2 kHz	2 kHz
Other Features	ADC Calibration Digital Filter	RF Transmitter	ADC	-
I_{DC}	3 mA	2.5 mA	382 μA	64 μA
V_{DD}	10 V	4 V	3.1 V	0.8 V
$V_{DD}I_{DC}$	30 mW	10 mW	1.184 mW	51.2 μW

8. Conclusion

This work presents a new low voltage AFE for strain-gauge sensory system. A new active-bootstrapped IA with pseudo-differential gain boosting OTA and CDB biasing technique is proposed to achieve high CMRR, low noise, and rail-to-rail output swing capability with 0.6 V supply voltage. A low-voltage LDO with the proposed filtering technique is useful to improve supply rejection and noise performance of the overall system. The design of a balanced active MOSFET-C filter alongside with pseudo-differential amplifier as its building block is presented for low voltage filtering applications. A single-ended-output amplifier with a new two-stage common-mode cancellation technique is used to implement single-ended-to-balanced conversion. The design techniques presented here are also applicable to the design of other types of low noise, low voltage sensory systems.

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