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Design and Analysis of Anchorless Shuttle Nano-electro-mechanical Non-volatile Memory for High Temperature Applications

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***Abstract*— This paper presents a novel nano-electro-mechanical (NEM) non-volatile memory (NVM) based on an anchorless structure for high operating temperature (>200°C). The proposed NEM NVM device has two stable mechanical states obtained by adhesion forces, and is actuated by electrostatic forces. This work further discusses the modeling of the NEM memory device and the scaling effects on the device performance. Finally, a memory cell consisting of the NEM memory device and two MOS transistors (1NEM-2T), and NEM NVM array structure are presented.**

Keywords- High temperature applications, Non volatile memories (NVMs), nano-electromechanical devices (NEMs)

I. INTRODUCTION

CONTINUOUS scaling in MOSFET channel lengths has led to a significant increase in CMOS static energy consumption due to the increase in the sub-threshold leakage current (I_{OFF}) [1]. This is a critical concern for both memory and logic devices, and becomes worse at higher temperatures. In general, scaling of memory cells such as SRAM, DRAM, or FLASH is limited by their tight requirements on static leakage and immunity to process variations and noise.

Emerging devices that can achieve zero standby leakage and low turn-on voltage have been proposed to alleviate these issues. However, any silicon-based *"CMOS-like"* devices such as tunnel-FET [1], impact-ionization MOSFET [2], and suspended-gate FET [3] also suffer from considerable I_{OFF}. To overcome this non-zero standby leakage issue, nano-electro-mechanical (NEM) devices with air gaps and resistive electro-mechanical contacts have been investigated for digital applications [5], [6] since they ideally have both zero I_{OFF} and abrupt switching. Similarly, non-volatile memories based on micro-electro-mechanical systems (MEMS) have been proposed for high temperature (HT) data storage [7]. MEMS memories can be categorized as either *storage-layer-based* devices, where the information is typically stored as a charge [8], and *storage-layer-free* devices, where non-volatility is obtained either by adhesion forces [7] or by a bistable mechanical design (zippering [9], buckling [10]).

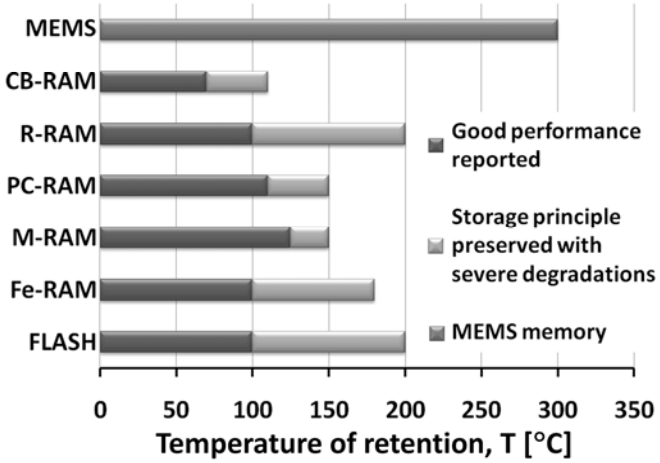

Figure 1. Maximum temperature of operation for various types of non-volatile memories. This review is based on recently published papers, constrains are more stringent for commercial memories [7]-[17].

Review of HT performances for various types of NVM is summarized in Fig. 1. The mainstream solution for NVM integration is FLASH technology [11], [12]. Emerging NVMs typically include resistive RAMs (R-RAM) [13], magnetic RAMs (M-RAM) [14], phase-change RAMs (PC-RAM) [15], conductive-bridge RAMs (CB-RAM) [16], and ferroelectric RAMs (Fe-RAM) [17]. Different physical mechanisms (FLASH: floating gate, M-RAM: free magnetic layer, Fe-RAM: ferroelectric polarization) are exploited to store non-volatile data, but all suffer from poor retention at HT.

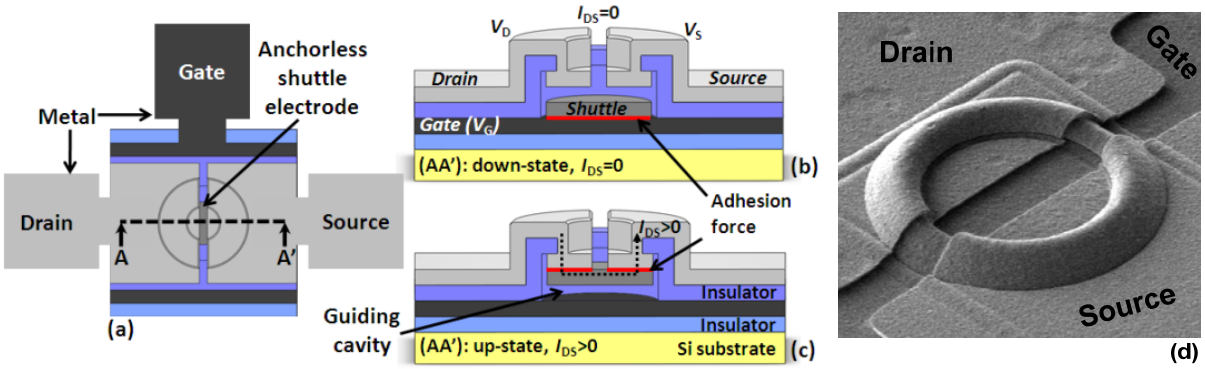

Figure 2. Proposed 3-terminal shuttle NEM memory device: (a) top-view layout, (b) AA' 3D cross section in the down-state, (c) AA' 3D cross section in the up-state. (d) Experimental circular test structure. Two metal electrodes (source and drain) are visible. A circular guiding pod is defined all around the circular shuttle to provide lateral guiding of the free shuttle.

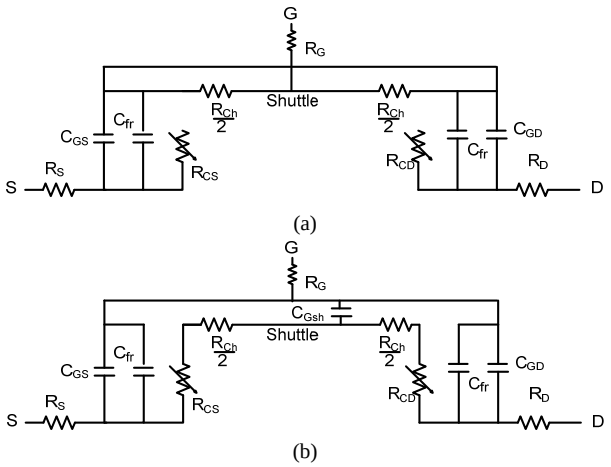

Figure 3. Electrical equivalent circuits: (a) down-state, (b) up-state.

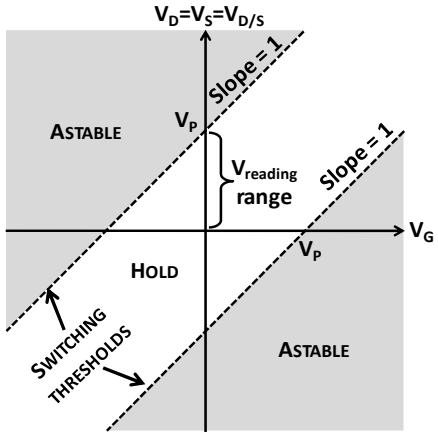

Figure 4. Stability and switching thresholds of the NVM device.

However, adhesion-based NEM memories can potentially offer seamless SET/RESET/READ/HOLD cycles over an extremely wide temperature range required in industrial, automotive, air and space, and defense electronics. The observation of metal-metal adhesion increase with temperature is reported in various studies focusing on electro-mechanical contacts [7]-[18], [19]. This effect can be explained by the metal softening at higher temperature. Therefore, the data retention capability of adhesion-based NEM memories is strengthened with temperature. This is an opposite trend compared to all storage-layer based NVMs.

However, all the previous adhesion-based NEM memories have employed structures with anchors, which are undesirable in device scalability. In this work, we present a novel anchorless shuttle NVM. Employing an anchorless design [20], the proposed NEM device is particularly advantageous for compactness. The remainder of the paper is organized as follows. Section II presents the new NVM structure and the operational details along with its static and dynamic features. Impacts of device scaling on the anchorless NEM NVM cell and array architectural details using the proposed NEM NVM device are explained in Section III. Finally, conclusions are offered in Section IV.

II. ANCHORLESS NEMS NVM

A. Structure and Operation

Fig. 2 presents the geometry of the proposed shuttle NEM NVM device with 3 terminals (D: Drain, S: Source, G: Gate), actuated by electrostatic forces [21]-[22]. A double air-gap geometry ensures that the free-flying shuttle electrode switches without stiction. The shuttle memory operation is based on the commuting of a floating (mechanical and electrical) electrode between the bottom fixed electrode (G) and the two anchored electrodes (D/S). Forces acting on the shuttle are (i) electrostatic force, (ii) adhesion force between the shuttle and fixed electrodes, (iii) damping force during transition, and (iv) gravity. Both damping force and gravity are neglected in this study. Switching occurs when the electrostatic force to the shuttle overcomes the adhesion forces. The down-state will occur by applying programming voltage (V_P) to the gate (G), and GND to the source (S) and drain (D), while the up-state is achieved by applying V_P to S and D, and GND to G. Fig. 3(a) and (b) show the electrical equivalent circuits of the two states in the proposed NEM NVM device respectively. Memory detection is through the large ON-resistance to OFF-resistance ratio between the drain and the source. This makes read operation simple and reliable.

TABLE I. OPERATING PRINCIPLE OF THE NEM NVM DEVICE

Operation	*Conditions*	*Remark*
Switching down	$V_D=V_S=0$ $V_G=V_P$	V_P: Pull-out voltage, $F_{electrostatic} > F_{adhesion}$
Switching up	$V_D=V_S=V_P$ $V_G=0$	Switching to both drain and source. Symmetric switching up/down (hysteresis)
Read	$V_D=V_R$, $V_S=0$ $V_G=0$	V_R: Read voltage ($V_R<<V_P$), Dow-state: $I_{DS}=0$, Up-state: $I_{DS}>0, I_{DS}\cong V_{DS}/2\cdot R_{ch}$
Hold	$V_D=V_S=V_G=0$	Non-volatility: adhesion increases with temperature

Memory reading is done by passing a reference current between the drain and the source (OPEN or SHORT). Reading is bidirectional to ease circuit design. The reading voltage (V_R) should be smaller than the programming voltage (V_P) to avoid undesired shuttle switching during read operation. Fig. 4 illustrates the stability and the switching threshold of the NEM NVM device. A hysteresis ideally centered at $V_D=V_S=V_G=0$ ensures that data are properly stored when the device is powered off. Details of the operating conditions are summarized in Table I.

The proposed anchorless design has advantages in terms of scalability and low variability compared to the previous anchor-based NEM NVMs. The absence of flexural (or torsional) beams makes the scalability of the proposed NEM structure ($9F^2$) comparable to CMOS devices. This is of key importance for achieving reasonable memory density.

B. Static and Dynamic Features of Shuttle and NEM NVM Device Modeling

In the static analysis of the shuttle electrode in vacuum, once the shuttle is lifted off, it *flies* until it eventually reaches the opposite electrode. The following discussion explains the shuttle transition from the drain/source side towards the gate. When a positive bias V_G is applied to the gate ($V_{D/S} = 0$), the shuttle is charged with $V_{D/S}$. If the applied voltage (V_G) is higher than the pull-out (switching) voltage (V_P), the shuttle is lifted off from the drain/source side by the electric field and carries a net charge ($Q_{shuttle}$) until it reaches the gate electrode. Once the shuttle lands on the gate, it is charged with an opposite charge ($-Q_{shuttle}$) and starts to rebound toward its initial position, which is not desirable for memory application. This effect is reported as *electrostatic pendulum* [23]. Therefore, the gate voltage needs to be turned off during the shuttle flight to prevent rebounding.

The following modeling is based on the charge distribution over the surface of metal electrodes, as shown in Fig. 5. The net charge on the shuttle splits between the top and bottom interface, and its redistribution depends on the applied voltages and the shuttle position ($0 < x < 2d_{gap}$). The narrow slit between source and drain is negligible in terms of area. From the charge conservation on the shuttle and the electrostatic law ($Q = C \cdot V$) of a capacitor (in this case, two air-gap capacitors), the charge equilibrium system is described by the following equations.

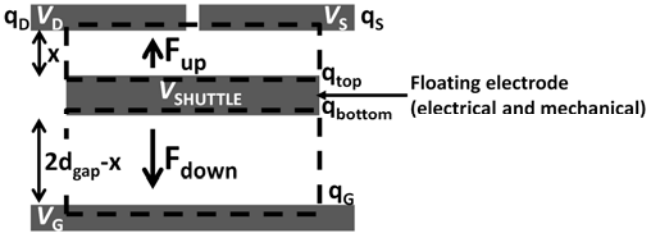

Figure 5. Double air gap capacitor divider with charge distribution. While switching, the shuttle electrode carries a fixed charge.

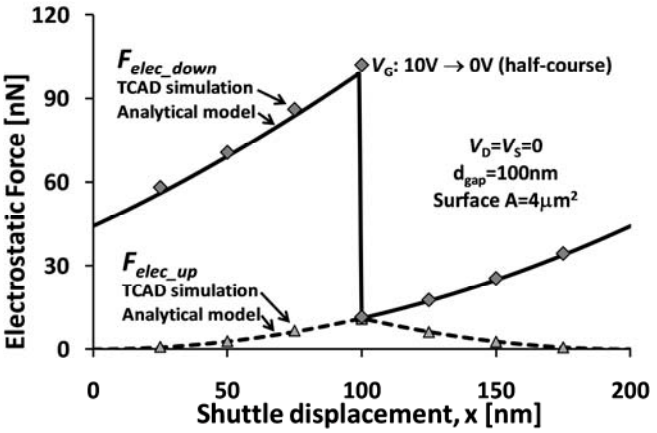

Figure 6. Analytical modeling of electrostatic forces F_{down} (shuttle → gate) and F_{up} (shuttle → drain/source) *vs.* shuttle displacement. V_G-pulse turn-off is applied after shuttle ½-course. Solid markers represent TCAD solutions (Coventorware simulations).

$$\begin{cases} q_D = q_S \\ q_D + q_S + q_{top} = 0 \\ q_{bottom} + q_G = 0 \\ q_{top} + q_{bottom} = Q_{shuttle} \\ q_G = -q_{bottom} = \dfrac{\varepsilon_0 \cdot A}{(2d_{gap} - x)} \cdot (V_G - V_{SHUTTLE}) \\ q_{top} = -q_D - q_S = \dfrac{\varepsilon_0 \cdot A}{x} \cdot (V_{SHUTTLE} - V_{D/S}) \end{cases} \quad (1)$$

The net charge on the shuttle ($Q_{shuttle}$) depends on its initial charging as written in (2).

$$Q_{shuttle} = Q = \frac{\varepsilon_0 \cdot A}{2 \cdot d_{gap}} \cdot V_G \quad (2)$$

As a result, two electrostatic forces, named F_{up} (towards D/S) and F_{down} (towards gate), build up during the switching, which is given in (3). One force (F_{up}) operates as a *break* while the other (F_{down}) as a *motor* for switching.

$$\begin{cases} F_{up} = \dfrac{q_{top}^2}{2 \cdot \varepsilon_0 \cdot A} = \dfrac{(q_D + q_S)^2}{2 \cdot \varepsilon_0 \cdot A} \\ F_{down} = \dfrac{q_{bottom}^2}{2 \cdot \varepsilon_0 \cdot A} = \dfrac{q_G^2}{2 \cdot \varepsilon_0 \cdot A} \end{cases} \quad (3)$$

Using (1)-(3), the evolution of the two electrostatic forces (F_{up} and F_{down}) as a function of the shuttle position (x) is extracted and plotted (see Fig. 6).

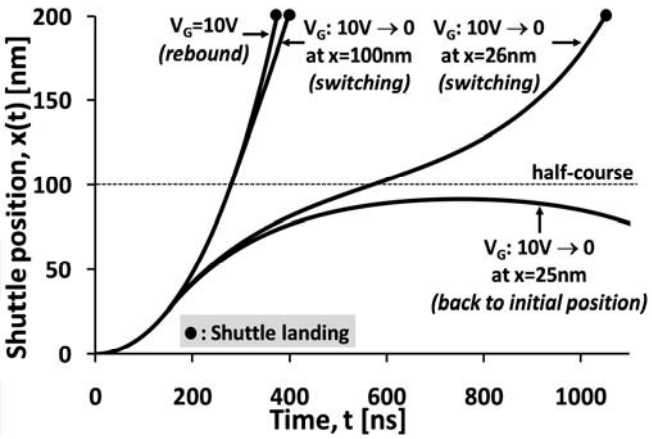

Figure 7. Position of the shuttle electrode as a function of time. Depending on the duration of the V_G pulse, three cases could happen: (i) the shuttle back to its initial position if pulse duration is too short, (ii) proper switching or (iii) shuttle electro-mechanical rebound if the pulse is too long.

Dynamic operation of the shuttle is solved from Newton's second law of motion. Utilizing the two forces applied to the shuttle (F_{up} and F_{down}), the resulting equation is given below.

$$m \cdot \frac{d^2x(t)}{dt^2} = \frac{q_{bottom}^2}{2 \cdot \varepsilon_0 \cdot A} - \frac{q_{top}^2}{2 \cdot \varepsilon_0 \cdot A} \quad (4)$$

where m is the shuttle mass. The shuttle position over time is demonstrated in Fig. 7. It indicates that a proper V_G pulse width range exists for a given V_G level. Too short programming pulse widths will retain the shuttle in the initial position while too long pulse widths will rebound the shuttle to the initial position. Therefore, a careful selection of the programming pulse width is necessary as illustrated by Fig. 7.

III. Anchorless NEM NVM Scaling and Memory Array Architecture

A. Impact of Scaling on the Performance of NEM NVM

Miniaturization is desirable for high device density. A pertinent question is how this continued scaling in dimensions and supply voltage influences the operating characteristics of the shuttle device and, indirectly, the critical design metrics such as switching voltage and power. Various scaling scenarios can be considered due to the aforementioned scaling parameters affecting one another.

Three different scaling models (*Full Scaling, General Scaling,* and *Fixed-Voltage Scaling*), similar to the MOS transistor [24], are reviewed in Table II. Assume that all device dimensions are scaled by the same factor S (with S > 1 for a reduction in size). Similarly, we assume all voltages, including supply voltage and switching voltages, are scaled by a same ratio, U. The relations governing the scaling behavior of the dependent variables are tabulated in the second column. In the *Full Scaling* (constant electrical field scaling) model, voltages and dimensions are scaled by the same factor S. The goal is to keep the electric field constant in the scaled device identical to those in the original device. The effects of *Full Scaling* on the NEM device and circuit parameters are summarized in the third column of Table II. In reality, *Full Scaling* is not followed as a feasible option. In order to keep new devices compatible to existing devices, voltages can not be scaled arbitrarily. To address this issue, Fixed-Voltage Scaling was introduced. The fifth column of Table II summarizes the impacts of Fixed-Voltage Scaling on the proposed NEM device and circuit parameters.

Scaling of CMOS technology reveals that a more generalized scaling (fourth column in Table II) is necessary as device dimensions and voltages are scaled independently. For example, if we assume 1/S = 0.7 for dimensions (30% scaling per technology generation) and 1/U = 0.85 for supply voltage (15% scaling per technology generation), the switching voltage (V_P) is scaled by the same 30% in all the three scenarios. Current density increases at a larger rate in *Fixed-Voltage Scaling* than the *Full Scaling* and *General Scaling* scenarios. Improvement in performance (reduction in delay and increase in ON current) and switching energy is observed in all the scaling scenarios. This shows the opportunity of the proposed NEM device with scaling for better memory design.

TABLE II. Scaling Scenarios for NEM NVM Devices

Parameter	***Relation***	***Full Scaling***	***General Scaling***	***Fixed-Voltage Scaling***
W, L, d_{gap}, $t_{shuttle}$,	Scaled parameters	1/S	1/S	1/S
V_{DD}	Supply voltage	1/S	1/U	1
Area	WL	$1/S^2$	$1/S^2$	$1/S^2$
V_P	$V_P = 4d_{gap}\cdot\sqrt{\frac{\Gamma\cdot\alpha}{d_{vdw}.\varepsilon_0}}$	1/S	1/S	1/S
I_{ON}	$\frac{V_{ds}}{R_{on}}$	1	S^3/U	S^3
Current Density	$\frac{I_{ON}}{W.L}$	S^2	S^5/U	S^5
C_{GS}	$\frac{\varepsilon_0\cdot A_S}{(2d_{gap}-x)}$	1/S	1/S	1/S
C_{fr}	$\frac{2\varepsilon_0\cdot W}{\pi}\cdot\ln\left(1+\frac{d_{gate}}{2d_{gap}}\right)$	$1/S^2$	$1/S^2$	$1/S^2$
C_g	Dominating C_{GS}	1/S	1/S	1/S
$t_{mechanical}$	$\sqrt{\frac{4\cdot d_{gap}}{a}}$	$1/S^{3/2}$	$1/S^{3/2}$	$1/S^{3/2}$
t_{int}	$\frac{C_g V_{DD}}{I_{ON}}$	$1/S^2$	$1/S^2\ U^2$	$1/S^2$
$t_{switching}$	Dominating $t_{mechanical}$	$1/S^{3/2}$	$1/S^{3/2}$	$1/S^{3/2}$
$P_{switching}$	$\alpha.C_g.V_{dd}^2.f_{switching}$	$1/S^{3/2}$	$S^{1/2}/\ U^2$	$S^{1/2}$
Power Density	$\frac{P_{switching}}{W.L}$	$S^{1/2}$	$S^{5/2}/\ U^2$	$S^{5/2}$
$E_{switching}$	$\alpha.C_g.V_{dd}^2$	$1/S^3$	$1/SU^2$	1/S

The scaling impact of the gap thickness (d_{gap}) on I_{DS} and the gate voltage (V_G) for programming is described in Fig. 8. It can be observed that an abrupt change in current occurs at a specific gate voltage (V_P). If V_G is smaller than V_P, the shuttle is in the up-state (initial state), shorting the source and drain electrodes. Once V_G becomes larger than V_P, the electrostatic

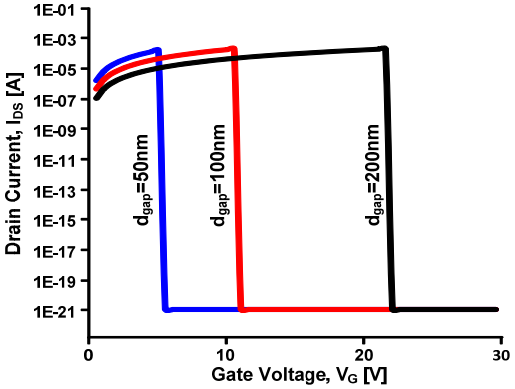

Figure 8. Plot of I_{DS} vs V_G of the shuttle based NEM memory cell for different actuation gap thickness (V_{DS} = 0.2V).

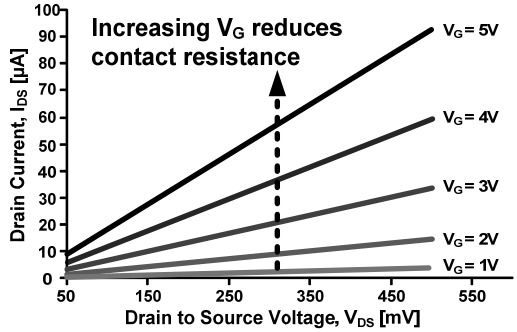

Figure 9. Plot of drain current (I_{DS}) of the shuttle based NEMs device as a function of V_{DS} for different V_G.

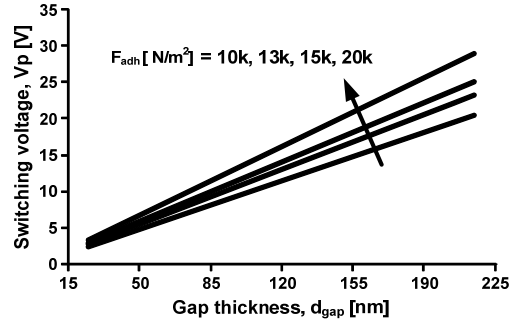

Figure 10. Plot of gate switching voltage as a function of gap thickness for different adhesive forces.

force overcomes the adhesive force and the shuttle moves down towards the down-state. Fig. 8 also shows that scaling of the gap thickness reduces the minimum switching voltage (V_P) required for switching the shuttle.

Fig. 9 shows the I-V characteristics of the proposed NEM NVM device. As expected, the drain current has a linear relationship to V_{DS} when the device in the up-state. Increasing V_G also increases the drain current due to the reduced contact resistance coming from the enlarged electrostatic force. Variations in the programming voltage (V_p) over different gap thicknesses and adhesive forces are also investigated and presented in Fig. 10. Smaller gap thickness is desired for lower V_p while electric field remains constant. Similarly, smaller adhesive force is beneficial to lower V_p. However, smaller adhesive force degrades the non-volatile capability.

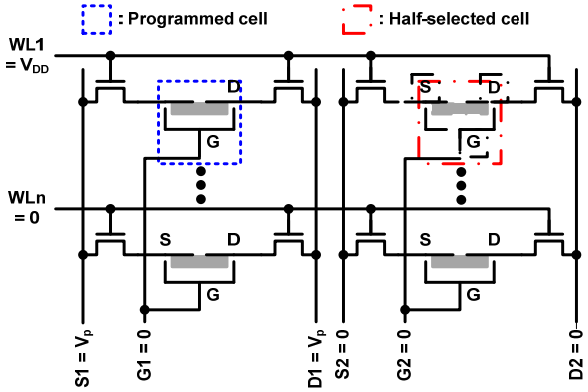

Figure 11. Proposed memory array structure using NEM memory device and two MOS transistors (1NEM-2T).

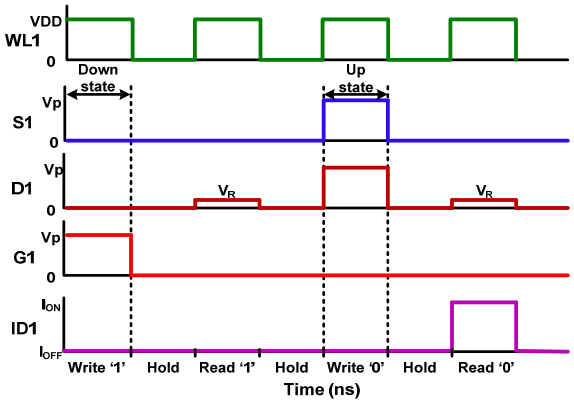

Figure 12. NEMs NVM cell read and write operations.

TABLE III. Operation of the Proposed NEMs NVM Array

Operation	*Conditions*	*Remark*
Writing 'down'	WL=V_{DD}, S1=D1=V_P, G1=0	$V_{DD} > V_p$
Writing 'up'	WL=V_{DD}, S1=D1= 0, G1=V_P	$V_{DD} > V_p$
Half-Select	WL=V_{DD}, S1=D1=G1= 0	No write operation
Unselected	WL=0, G1= 0 or V_p	Floating source (S) and drain (D) following voltage changes in 'G'

B. NEMs NVM Array Architecture and Integration

Fig. 11 shows the proposed memory array where each bit cell consists of two access NMOS transistors and one shuttle NEM NVM device. For writing, a proper terminal biasing condition has to be applied in the selected column. A word line is enabled for writing the data into the selected cell. The NEM devices in unselected columns will not be programmed by applying the same voltage to all three terminals. For reading, a small signal is applied to the selected source line (S) and is read from the selected drain line (D) to detect whether the shuttle is in the up-state or in the down-state. Fig. 12 illustrates the write/read operations of the implemented NEM memory array. Table III summarizes the bias conditions for the proposed NEM memory array during writing operation.

In order to avoid the operating voltage mismatch between the NMOS access transistors and the NEM devices, the NEM

dimension and the CMOS technology node has to be carefully selected. It is also suggested to use a SOI-CMOS technology for reliable operation at extremely high temperature (>200°C).

IV. Conclusion

A nano-electro-mechanical (NEM) NVM structure for data storage at high temperature (>200°C) is presented. The mechanical switching operation of the NEM achieves zero-leakage that is a topmost requirement in high temperature applications. The anchorless structure provides high scalability. The modeling, static and dynamic features, scaling effects, and array implementation details of the proposed NEM device are discussed comprehensively. Improvement in the NEM NVM performance with scaling highlights the scope of the anchorless shuttle-based NEM NVM for high density implementation compared to anchored NEM NVM structures.

Appendix

Symbol	***Quantity***	***Symbol***	***Quantity***
ε_0	dielectric constant of vacuum	R_{CS} or R_{CD}	contact resistance
ρ	shuttle metal density	C_{GS}	gate-source capacitance
A	shuttle surface	C_{GD}	gate-drain capacitance
L	shuttle length	C_{fr}	fringe capacitance between Gate and S/D
W	shuttle width	C_{gsh}	gate-shuttle capacitance
m	shuttle mass	C_g	total gate capacitance
d_{gap}	vacuum actuation gap	I_{ON}	on (shuttle in the up-state) Current density
$t_{shuttle}$	shuttle thickness	$t_{mechanical}$	mechanical delay
V_D	drain voltage	t_{int}	intrinsic delay
V_S	source voltage	$t_{switching}$	total switching delay
$V_{D/S}$	drain to source voltage	$P_{switching}$	switching power
V_G	gate voltage (pulsed-mode)	$E_{switching}$	switching energy
V_P	pull-out voltage	$Q_{shuttle}$	fixed shuttle charge
V_R	reading voltage	q_{top}	induced charge on shuttle top interface
R_G	gate resistance	q_{bottom}	induced charge on shuttle bottom interface
R_S	source resistance	q_D	induced drain charge
R_D	drain resistance	q_S	induced source charge
R_{Ch}	channel (shuttle) resistance	q_G	induced gate charge
R_{ON}	on-resistance (up-state)	F_{up}	electrostatic force shuttle → drain/source
R_{OFF}	off-resistance (down-state)	F_{down}	electrostatic force shuttle → gate

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