Integrated design of DC-DC power converters target for fast load transient applications

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**INTEGRATED DESIGN OF DC-DC POWER
CONVERTERS TARGET FOR
FAST LOAD TRANSIENT APPLICATIONS**

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A thesis submitted to the Nanyang Technological University in partial
fulfilment of the requirement for the degree of Doctor of Philosophy

2018

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I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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Abstract

Nowadays, highly integrated electronic products are becoming part and parcel of our daily life. With the technology improvement in Integrated Circuit (IC), more complicated functions can be incorporated into very large-scale systems, rendering the electronic products more powerful and entertaining. The increasing IC size and function blocks bring in new design challenges for its power management circuits, such as accuracy, efficiency, response speed, input and output voltage ranges, and driving capability. The State-of-the-art DC-DC regulators usually combine several control methods in order to fulfill all of the above-mentioned specifications. For instance, a dual mode DC-DC converter applies the Pulse-Width-Modulation (PWM) control method at heavy load condition and shifts to Pulse-Frequency-Modulation(PFM) control at light load condition. This hybrid dual mode operation can indeed improve the efficiency over a wide loading range. However, dual mode operation also implies more complicated circuits design and increased fabrication cost. Apart from it, uncontrolled switching frequency under PFM condition will cause unwanted Electron-Magnetic interference(EMI) issues and challenges of input filter design. Under PWM condition, a power-hungry error amplifier is generally required which will limit the transient response speed. Considering the existing drawbacks of conventional control methodologies and the future development of modern Power Management Units(PMU), several control methods were proposed in this thesis to improve the performances of switching-inductor based DC-DC converters targeting for different specifications.

In the beginning, a PWM DC-DC converter works in Discontinues-Conduction-Mode

(DCM) at light load condition was conducted in my research. With a novel Zero-Voltage-Detector (ZVD) implemented in this regulator, fast sensing and quick comparison were realized in order to avoid inverse conduction of inductor current. The time delay of ZVD sensing and comparing activities were only about 6ns, and a power conversion efficiency >85% was achieved over a loading range from 10mA to 250mA.

Subsequently, in order to be compatible with the development of modern DC-DC regulators, the conventional control methods based on linear control mechanism may not be the best options when dealing with frequently switched loadings. Take this limitation into concern, two designs of high-speed converters with hysteretic non-linear control mechanisms were proposed and conducted. Particularly, switching frequency locking properties were introduced into these two converters with a frequency locking range about several MHz. This hysteretic control method with frequency locking ability is called fixed switching frequency hysteretic control. The proposed designs were fabricated using 0.18 μ m CMOS process, and their switching frequencies were maintained at 10MHz with less than $\pm 1\%$ variations. The transient recovery time of Design I is about 2 μ s, and it is only about 0.3 μ s for Design II. A peak power efficiency of 91% was achieved over a loading range from 100mA to 600mA.

Compared to conventional hysteretic PFM controls, the proposed designs have a fixed switching frequency, so the electromagnetic interference (EMI) problems can be greatly reduced and the challenges on input filter design can be minimized. Furthermore, the proposed fixed frequency hysteretic non-linear control topologies can be further used for multi-phase interleaved DC-DC converters applications to provide large current drive capabilities.

In this thesis, the background information about DC-DC regulators was introduced, and then the motivations and objectives to conduct this research were inspired. Retrieving and analyzing existing technologies, the above mentioned three designs were fully discussed from conceptual ideas, followed by circuits implementations, and all the way to system simulations and measurements. Both advantages and disadvantages will be presented for further study.

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Chapter 1

Introduction

1.1 Background and Motivation

Switched inductor converters, have been with us for many years and can be found in almost all electronic devices. As compared to the linear regulators and the switched capacitor converters (charge pumps), they generally offer better efficiency, where the typical peak efficiency can hit more than 90%. In addition, the input and output voltage ranges are greatly extended because various structures for switching mode converters can be employed, including buck, boost, buck-boost, Cuk, and fly-back.

Pulse-Width-Modulation (PWM) is frequently utilized to control the switching mode converters [1.1], [1.2]. It has predictable Electromagnetic Interference (EMI) and provides good conversion efficiencies at medium to heavy load range. To achieve high power conversion efficiency over a wide load range, other modulation types, such as Pulse-Frequency-Modulation (PFM) and Pulse-Skipping-Modulation (PSM), are nor-

mally adopted to take over PWM at light load condition. Nowadays, electronic devices, especially portable devices, are generally required to have longer standby time (light load condition) as well as higher performance (heavy load condition). Therefore, to maintain a good power conversion efficiency over a wide load range, multiple control topologies are frequently combined together to fulfill this requirement. However, achieving better conversion efficiencies through hybrid operations generally implies more complicated circuit design and higher fabrication cost [1.3]. As a result, voltage regulators that operate in Discontinuous-Conduction-Mode (DCM) become as alternative options to provide good efficiency, simpler structure, and better loop stability.

Apart from good power conversion efficiency, modern power management units (PMU) should be robust when dealing with frequently switched loadings as more and more entertaining functions are integrated into a single chip. Therefore, traditional linear control method like PWM may not be the best option as its loop response speed is limited by the bulk compensation block. In order to enhance the transient response performance, advanced nonlinear control methodologies, including hysteretic control, constant on-time control, and V^2 control are extensively applied because they provide faster transient response and simpler structure. However, the hysteretic control and the constant on-time control lead to varied switching frequency, which may cause electromagnetic interference (EMI) issues and challenges of input filter design. Recently, A new type of nonlinear fixed-frequency hysteretic control methods catches designers' attention, and it is also called pseudo-PWM control[1.4]. As its name indicated, this type of control methods take the advantages of both PWM control and PFM control concurrently. When compared to conventional PWM, a hysteretic comparator is used to replace the error amplifier thus resulting in a faster loop response speed. Besides, the entire loop will have almost no

stability issues. When compared to conventional PFM, an extra frequency locking loop is added to lock the switching frequency to a referenced frequency value. EMI problems are much easier to be predicted and the challenges of input filter design are greatly reduced under the fixed switching frequency operation.

Furthermore, more and more challenging specifications including high power, high-frequency power conversion, large current driving ability, and low output voltage deviation in both steady-state and transient condition, are expected in modern microprocessor and communication systems. Multi-phase interleaved voltage regulators gradually become as a potential choice for providing a large load current and reduced output ripple noise [1.5]-[1.7]. Fixed-frequency hysteretic controlled DC-DC converter is a good option to be utilized as a unit cell for multi-phased interleaved applications as it maintains a fixed switching frequency as well as provides a fast transient response.

1.2 Objective and Work Scope

The main objective of my research is to design switch-inductor mode DC-DC converters targeting for fast transient dynamics, high efficiency, and high-frequency power conversion, and these converters are suitable for modern portable devices power management units (PMU) applications.

The detailed scope of work to achieve the objective can be specified as follows:

- A PWM DC-DC buck converter works in Discontinuous-Conduction-Mode (DCM) was implemented. Comparing with PFM operation at light load condition, it

achieved lesser EMI problems with predictable output ripple voltages, and realized a comparable power conversion efficiency. In addition, circuit architecture was much simpler and more stable when compared with hybrid mode control topologies. A novel Zero-Voltage-Detector(ZVD) with fast sensing and comparison abilities was proposed to avoid an inductor's inverse current conduction. In order to eliminate the voltage ringing phenomenon located at the switching node, a ringing suppression function block was utilized, and a dead-time detection logic was introduced to ensure the normal operation of the proposed converter.

- Due to the fast development of semiconductor technologies, modern electronic devices are highly integrated with an increase in high-performance function blocks but a decrease in silicon areas. Their power management units are specified to work at tens of megahertz, or even hundreds of megahertz in order to deal with ultra-fast loading dynamics as well as using much smaller off-chip filter components. In this project, a DC-DC buck converter with hysteretic fixed frequency nonlinear control was conducted. Its nonlinear control mechanism ensured it response fast enough for frequently switched load conditions, and made it possible to operate at a relatively high switching frequency to use smaller filter components. This control method combined the advantages of both conventional PWM control and PFM control. Fixed switching frequency led to predictable EMI issue and lesser challenges of input filter design. Hysteretic control method resulted in better transient response performance for fast loading dynamics. Besides, less switch conduction loss was achieved especially at heavy load condition as the power stage switching frequency maintained unchanged even if an increase in loading current. Furthermore, in this proposed DC-DC buck converter, a new method of phase frequency locking was

proposed such that its switching frequency was locked at 10MHz with frequency variation less than $\pm 1\%$.

- Another DC-DC buck converter design with fixed frequency hysteretic control was conducted as well. In this particular design, power stage switching frequency was maintained at 10MHz by proposed adaptively hysteretic window control. In addition, an auxiliary circuit was proposed to monitor the change of output voltage so the transient response performance was further enhanced. In the meantime, it also helped to regulate the output voltage.

1.3 Organization

This report is organized as follows:

Chapter 1 gives a brief introduction to switching mode DC-DC converters, especially two categories of modulations including PWM and PFM. Take both of them into concern, the motivation to conduct the following research work are introduced. Finally, the objective and scope of the research work are specified.

Chapter 2 reviews the fundamental topologies of the common switching mode DC-DC converters, and then moves on to the different modulation techniques associated with the analog controller. Critical parameters of a DC-DC regulator, such as input-output voltage relationship, output ripple voltage, power efficiency calculation, are discussed. In addition, closed loop small signal model is introduced and conventional compensation techniques are discussed as well.

Chapter 3 introduces a DCM DC-DC buck converter with a novel zero voltage detection topology. Compensation techniques are also discussed with respect to the DC-DC converter working in DCM.

Chapter 4 focuses on the fixed-frequency hysteretic buck converter in order to take both advantages of conventional PWM and PFM modulation. A novel frequency locking method is proposed and can tune the switching frequency from 8MHz to 10MHz. In addition, by locking the switching frequency to be 10MHz, a transient response improvement circuit is proposed, and it leads to a transient recovery time of less than $2\mu\text{s}$

Chapter 5 introduces another fixed-frequency hysteretic buck converter design. Concerning about the drawbacks of the buck converter in chapter 4, an auxiliary circuit is proposed together with the adaptive hysteretic window control to compensate for the transient response drawbacks in chapter 4. By doing so, a transient recovery time less than $0.4\mu\text{s}$ is achieved.

Chapter 6 summarizes all of the research works been done during the past four years, and also figures out what should be done for better improvement and more applications.

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Chapter 2

Literature Review

2.1 Nomenclature

Table 2.1: List of Expressions for Signals, Parameters, Components and Abbreviations

List of Signals and Parameters			
D	Duty Ratio	P_{sw}	Switching Loss
f_{sw}	Switching Frequency	Q	Capacitor Ripple Charge
$G_p(s)$	Power Stage Transfer function	T_{sw}	Periodic Time
$H(s)$	Compensator Transfer function	V_e	Error Amplifier Output Voltage
I	Load Current	V_{fb}	Feedback Voltage
i_C	Capacitor Charging Current	V_H	Hysteretic Window Upper Boundary
i_L	Inductor Current	V_{ref}	Reference Voltage
i_{pk}	Inductor Peak Current	V_{IN}	Input Supply Voltage
i_{ramp}	Compensation Ramp	V_L	Hysteretic Window Lower Boundary
Continued on next page			

Table 2.1 – continued from previous page

M	Conversion Ratio(DCM)	V_{osc}	Amplitude of Ramp Signal
P_{cond}	Conduction Loss	V_x	Switching Node Voltage
P_{FET}	PowerFET Conduction Loss	V_{OUT}	Output Voltage
P_{in}	Input Power	ΔI_L	Inductor Ripple Current
P_L	Inductor Conduction Loss	$< i_C >$	Average Capacitor Current
P_{load}	Output Power	Δv	Output Ripple Voltage
P_{loss}	Power Loss	$< v_L >$	Average Inductor Voltage
P_{static}	Static Loss	η	Conversion Efficiency
List of Components			
C	Output Filtering Capacitor	M_N	Power NFET
C_{IN}	Input Filtering Capacitor	M_P	Power PFET
L	Filtering Inductor	R	Load Resistor
r_C	Capacitor ESR	R_{cs}	Equivalent Current Sense Resistor
List of Abbreviations			
ADC	Analog to Digital Converter	MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
CCM	Continuous Conduction Mode	PFM	Pulse Frequency Modulation
DCM	Discontinuous Conduction Mode	PSM	Pulse Skip Modulation
DPWM	Digital Pulse Width Modulation	PWM	Pulse Width Modulation
EMI	Electro Magnetic Interference	ZCS	Zero Current Switching
ESR	Equivalent Series Resistor	ZVS	Zero Voltage Switching
ESL	Equivalent Series Inductance	MLCC	Multi Layer Ceramic Capacitor

2.2 DC-DC Converter Topologies in CCM

In this research, only second-order DC-DC converters will be considered due to its low component count. In the following sub-sections, a brief review of the various topologies and control methods will be conducted. For modern electronic devices with the integrated circuit, three major topologies for switching mode DC-DC converters are usually adopted, namely, buck, boost, and buck-boost structures.

2.2.1 Buck Converter

The generic DC-DC buck converter is shown in Fig. 2.1 Under PWM control, the buck converter operates in two phases and the output voltage (V_{OUT}) can be adjusted by controlling the duty ratio (D) of the switches. At steady-state operation, the average voltage across inductor L is zero, and thus the relationship between V_{IN} and V_{OUT} can be expressed as (2.1) below:

$$V_{OUT} = DV_{IN} \quad (2.1)$$

Figure 2.1: Schematic of a DC-DC Buck Converter.

2.2.2 Boost Converter

On contrary to the buck converter, the DC-DC boost converter, as shown in Fig. 2.2, regulates the V_{IN} and V_{OUT} such that V_{OUT} is always greater than V_{IN} . Under PWM control, the boost converter also operates in two phases to regulate V_{OUT} by adjusting D . The relationship between V_{IN} and V_{OUT} can be expressed as (2.2).

$$V_{OUT} = \frac{1}{1-D} V_{IN} \quad (2.2)$$

Figure 2.2: Schematic of a DC-DC Boost Converter.

2.2.3 Four Transistors Non-inverting Buck-Boost Converter(4TBB)

A common non-inverting buck-boost converter topology (4TBB) having the voltage relationship as expressed in (2.3), is as shown in Fig. 2.3, which has four switching transistors.

$$V_{OUT} = \frac{D}{1-D} V_{IN} \quad (2.3)$$

The 4TBB converter is a better choice over the buck or boost converter as it allows

Figure 2.3: Schematic of a 4TBB.

both bucking and boosting of voltage and current. In spite of being a more suitable topology, the 4TBB converter has the following disadvantages:

- (i) Four transistors are switched at every switching cycle, resulting in a low transistor utilization that achieves a maximum of 25% when D is 50%, and a high switching loss. Consequently, the 4TBB has a lower conversion efficiency than either the buck or boost converter.
- (ii) Similar to the inverting buck-boost converter, the 4TBB has a much higher average inductor current and inductor current ripple than either the buck or boost converter, further reducing the conversion efficiency of the 4TBB.
- (iii) The 4TBB has a higher component count due to two additional switches required.

2.3 Output Ripple Voltage

Apart from the input-to-output voltage ratio, another important specification for the switching mode DC-DC converter is the output voltage ripple Δv . Buck converter is chosen as an example to derive the output ripple voltage, and the rest topologies can be

done in a similar way. Fig. 2.4 shows the inductor current in the steady state. When power PMOS M_P is conducting, inductor current $i_L(t)$ keeps increasing, and this particular period is called the duty cycle period, which is represented by D . Once $i_L(t)$ reaches its peak value $i_L(DT_{sw})$, M_P will be cut off then M_N starts to conduct, and then the inductor current $i_L(t)$ keeps decreasing until the valley is reached. The average current indicated in Fig. 2.4 is the load current I , and all of the ripple current above I will flow to charge the output filter capacitor, and thus the magnitude of the output ripple voltage can be derived using the equations shown below.

Figure 2.4: Waveforms of Inductor Voltage and Current.

Figure 2.5: Waveforms of Load Capacitor Current and Voltage.

$$\Delta i_L = \frac{(V_{IN} - V_{OUT})}{2L} D T_{sw} \quad (2.4)$$

Substituting equation (2.1) into (2.4):

$$\Delta i_L = \frac{V_{OUT}}{2L} (1 - D) T_{sw} \quad (2.5)$$

Therefore, the total ripple charge Q can be estimated as a triangle's shadow area shown in Fig. 2.5,

$$Q = \frac{1}{2} \times \frac{T_{sw}}{2} \times \Delta i_L = \frac{(1 - D) V_{OUT}}{8L f_{sw}^2} \quad (2.6)$$

And the output ripple voltage is then derived as:

$$\Delta v = \frac{Q}{C} = \frac{(1 - D) V_{OUT}}{8LC f_{sw}^2} \quad (2.7)$$

Equation (2.7) clearly shows what are the parameters determining the value of output ripple voltage. For other topologies, the output voltage ripples according to [2.1] are listed in Table 2.2. Both ideal case and non-ideal case are included.

Table 2.2: Output Voltage Ripples of Buck, Boost and Buck-Boost Converters

	Ideal Case	Including Capacitor ESR
Buck	$\frac{V_{OUT}(1-D)}{8LC f_{sw}^2}$	$max : \frac{V_{OUT}(1-D)}{8L f_{sw}^2} + \frac{V_{OUT}(1-D) T_{sw} r_c}{L}$
Boost	$\frac{V_{OUT} D}{RC f_{sw}}$	$\frac{V_{OUT} D T_{sw}}{(R+r_c)C} + V_{OUT} \left[\frac{1}{(1-D)R} - \frac{D(1-D) T_{sw}}{2L} \right] r_c$
Buck-Boost	$\frac{V_{OUT} D}{RC f_{sw}}$	$\frac{V_{OUT} D T_{sw}}{(R+r_c)C} + V_{OUT} \left[\frac{1}{(1-D)R} - \frac{D(1-D) T_{sw}}{2L} \right] r_c$

2.4 DC-DC Converter Topologies in DCM

Switch mode DC-DC converters working in Discontinuous Conduction Mode (DCM) occurs because the inductor current ripple causes polarity of applied switch current to reverse, such that the current or voltage-unidirectional assumptions made in realizing the

switch are violated [2.1]. It commonly occurs in DC-DC converters when it is operating under light load conditions. Sometimes, DC-DC converters are purposely designed to operate in DCM at all load conditions. Comparing with Continuous Conduction Mode (CCM) operation, properties of converters change radically when DCM is entered: the voltage conversion ratio M becomes load-dependent, output impedance is increased, dynamics are altered, and control of output voltage may be lost when the load is removed.

2.4.1 CCM-DCM Mode Boundary

For a DC-DC converter in steady-state operation, the inductor current contains two parts, including a dc component I reflecting the output load condition and an ac component $i_L(t)$ reflecting the inductor ripple current. Recall the inductor ripple current as:

$$\Delta i_L = \frac{(V_{IN} - V_{OUT})}{2L} DT_{sw} \quad (2.8)$$

and the output load current can be calculated as:

$$I = \frac{V_{OUT}}{R} \quad (2.9)$$

Thus the minimum inductor current value in each cycle can be derived as:

$$i_L(t)_{min} = \frac{V_{OUT}}{R} - \frac{(V_{IN} - V_{OUT})}{2L} DT_{sw} \quad (2.10)$$

In other words, if $i_L(t)_{min} > 0$, the converter maintains in CCM operation, but if $i_L(t)_{min} < 0$, it will enter in DCM operation. By inserting buck converter expressions for I and Δi_L :

$$\frac{V_{OUT}}{R} - \frac{(V_{IN} - V_{OUT})}{2L} DT_{sw} < 0 \quad (2.11)$$

Rearrange equation(2.11) with $V_{OUT} = DV_{IN}$:

$$\frac{DV_{IN}}{R} < \frac{D\bar{D}T_{sw}V_{IN}}{2L} \quad (2.12)$$

Simplify:

$$\frac{2L}{RT_{sw}} < \bar{D} \quad (2.13)$$

This expression is of the form

$$K < K_{crit}(D) \quad for \ DCM \quad (2.14)$$

where $K = \frac{2L}{RT_{sw}}$ and $K_{crit}(D) = \bar{D}$. Solve K_{crit} equation for load resistance R :

$$R < R_{crit}(D) \quad for \ CCM \quad (2.15)$$

$$R > R_{crit}(D) \quad for \ DCM \quad (2.16)$$

where $R_{crit}(D) = \frac{2L}{\bar{D}T_{sw}}$. Table 2.3 summaries CCM-DCM mode boundaries for the buck, boost, and buck-boost converters.

Table 2.3: CCM-DCM Mode Boundaries for The Buck, Boost, and Buck-Boost Converters

Converter	$K_{crit}(D)$	$\max_{0 \leq D \leq 1} (K_{crit})$	$R_{crit}(D)$	$\min_{0 \leq D \leq 1} (R_{crit})$
Buck	$(1 - D)$	1	$\frac{2L}{(1-D)T_{sw}}$	$2 \frac{L}{T_{sw}}$
Boost	$D(1 - D)^2$	$\frac{4}{27}$	$\frac{2L}{D(1-D)^2T_{sw}}$	$\frac{27}{2} \frac{L}{T_{sw}}$
Buck-Boost	$(1 - D)^2$	1	$\frac{2L}{(1-D)^2T_{sw}}$	$2 \frac{L}{T_{sw}}$

2.4.2 Voltage Conversion Ratio M in DCM

The voltage conversion ratio M for a DC-DC converter working in DCM is different from its CCM counterpart. Techniques used to analyze M includes inductor volt-second balance and capacitor charge balance, which are represented by mathematic equation

(2.17) and (2.18), respectively.

$$\langle V_L \rangle = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_L(t) dt = 0 \quad (2.17)$$

$$\langle i_C \rangle = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_C(t) dt = 0 \quad (2.18)$$

Fig. 2.6 illustrates one period waveforms of inductor voltage and current in DCM

Figure 2.6: Waveforms of Inductor Voltage and Current in DCM.

operation. Under steady-state operation, the average voltage across the inductor should be zero. Thus the following equation can be built up according to volt-second balance:

$$\langle v_L(t) \rangle = D_1(V_{IN} - V_{OUT}) + D_2(-V_{OUT}) + D_3 0 = 0 \quad (2.19)$$

Solve for V_{OUT} :

$$V_{OUT} = V_{IN} \frac{D_1}{D_1 + D_2} \quad (2.20)$$

As for inductor current shown in Fig. 2.6, the average value of the inductor current $\langle i_L \rangle$ can be derived using the average value of an inductor current integration over one

switching cycle.

$$\langle i_L \rangle = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_L(t) dt \quad (2.21)$$

The value of the integration can be calculated using the triangle area:

$$\int_0^{T_{sw}} i_L(t) dt = \frac{1}{2} i_{pk} (D_1 + D_2) T_{sw} \quad (2.22)$$

The peak inductor current can be derived as:

$$i_{pk} = i_L(D_1 T_{sw}) = \frac{V_{IN} - V_{OUT}}{L} D_1 T_{sw} \quad (2.23)$$

Substituting equation (2.23) and (2.22) into (2.21), we will get:

$$\langle i_L \rangle = (V_{IN} - V_{OUT}) \frac{D_1 T_{sw}}{2L} (D_1 + D_2) \quad (2.24)$$

Then equate the average value $\langle i_L \rangle$ to dc load current:

$$\frac{V_{OUT}}{R} = (V_{IN} - V_{OUT}) \frac{D_1 T_{sw}}{2L} (D_1 + D_2) \quad (2.25)$$

Two equations (2.20) and (2.25) solve for two unknowns, thus the relationship between

V_{in} and V_{OUT} can be derived as:

$$V_{IN} = \frac{2}{1 + \sqrt{1 + \frac{4K}{D_1^2}}} V_{OUT} \quad (2.26)$$

Where $K = \frac{2L}{RT_{sw}}$ valid for $K < K_{crit}$. Table 2.4 summaries CCM-DCM characteristics for

the buck, boost, and buck-boost converters with $K = \frac{2L}{RT_{sw}}$, and DCM occurs for $K < K_{crit}$.

Table 2.4: Summary of CCM-DCM Characteristics for The Buck, Boost, and Buck-Boost Converters

Converter	$K_{crit}(D)$	DCM $M(D, K)$	DCM $D_2(D, K)$	CCM $M(D)$
Buck	$(1 - D)$	$\frac{2}{1 + \sqrt{1 + \frac{4K}{D^2}}}$	$\frac{K}{D} M(D, K)$	D
Boost	$D(1 - D)^2$	$\frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2}$	$\frac{K}{D} M(D, K)$	$\frac{1}{1 - D}$
Buck-Boost	$(1 - D)^2$	$-\frac{D}{\sqrt{K}}$	$\sqrt{K}$	$-\frac{D}{1 - D}$

2.5 Power Conversion Efficiency

DC-DC converters are designed to convert an unregulated input supply voltage into a regulated output voltage. Its efficiency is determined by the ratio of the output power delivered to the load (P_{load}) and the input power drawn from the power source (P_{in}). Its mathematic equation can be derived as:

$$\eta = \frac{P_{load}}{P_{in}} = \frac{P_{load}}{P_{load} + P_{loss}} \quad (2.27)$$

For a DC-DC converter design, the power loss caused by itself must be minimized so its efficiency will thus maximized. At system level of a DC-DC converter, two types of major power losses are defined, including static losses and dynamic losses [2.2], [2.3]. Static losses are unavoidable constant losses. An example of static loss is the quiescent current going into an internal circuitry such as band gap reference, operational amplifier and clock generator, etc. On the other hand, dynamic losses vary with line and load conditions. It can be further classified into two categories: conduction losses and switching losses.

Figure 2.7: Converter Power Losses Versus Load Current: (a) Fixed-Frequency Operation, (b) Variable Frequency Operation with Frequency Proportional to Load Current.

Conduction losses are load dependent and include losses caused by voltage drops across

power MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) and inductor ESR (Equivalent Series Resistor) of a converter. The conduction losses become higher when the load currents are higher. In contrast, a converter also has frequency dependent switching losses that include the MOSFETs' turn-on and turn-off losses, gate drive losses, and body diode conduction losses that occur in each switching cycle. As the name implies, these losses are proportional to the switching frequency. The relationships of these losses with respect to load are illustrated in Figure 2.7, and the detailed contents are listed in Table 2.5.

Table 2.5: Origins of Losses in A Conventional Fixed-Frequency Converter

Static	<i>Static Losses (P_{static})</i> Controller standby current MOSFET, diode, and capacitor leakage currents Cooling fan's power
Dynamic	<i>Conduction (Load-dependent) Losses (P_{cond})</i> MOSFET on resistance Diode forward voltage drop Inductor winding resistance Capacitor equivalent series resistance <i>Switching (Frequency-dependent) Losses (P_{sw})</i> MOSFET parasitic capacitance MOSFET body diode conduction Diode capacitance Diode stored minority charge Inductor and transformer core loss Snubber loss Gate driver losses i_D - v_{DS} overlap

Among all the power losses listed in Table 2.5, the three main causes of power

dissipation in a DC-DC converter are inductor conduction losses, MOSFET conduction losses, and MOSFET switching losses. The power supply's efficiency can be calculated through a quick and easy method without applying laboratory measurements.

2.5.1 Inductor Conduction Losses

Fig. 2.8 shows the current through the inductor in a typical DC-DC converter. The

Figure 2.8: Inductor Current.

inductor conduction loss in given by:

$$P_L = I_{RMS-L}^2 \times R_{DCR} \quad (2.28)$$

Where R_{DCR} is the DC-Resistance of the inductor. The rms inductor current is given by:

$$I_{RMS-L}^2 = I^2 + \frac{\Delta I_L^2}{12} \quad (2.29)$$

Where ΔI_L is the inductor ripple current. Typically ΔI_L is about 30% of the output current.

Therefore, the inductor current can be calculated to be:

$$I_{RMS-L} = I \times 1.00375 \quad (2.30)$$

Because the ripple current contributes only 0.375% of I_{RMS-L} , it can be neglected. The power dissipated in the inductor now can be calculated as:

$$P_L = I^2 \times R_{DCR} \quad (2.31)$$

2.5.2 MOSFET Conduction Losses

Fig. 2.9 shows the current flowing through the high-side MOSFET M_P of a buck converter. The power dissipated in the high-side MOSFET M_P is given by:

Figure 2.9: Buck Converter High-Side MOSFET Current.

$$P_{M_P} = I_{RMS-M_P}^2 \times R_{DSONP} \quad (2.32)$$

Where R_{DSONP} is the on-time drain-to-source resistance of the high-side MOSFET M_P .

Substituting for I_{RMS-M_P} :

$$P_{M_P} = \frac{V_{OUT}}{V_{IN}} \times \left(I^2 + \frac{\Delta I^2}{12} \right) \times R_{DSONP} \quad (2.33)$$

Fig. 2.10 shows the current flowing through the low-side MOSFET M_N of a buck converter. The power dissipated in the low-side MOSFET M_N is given by:

Figure 2.10: Buck Converter Low-Side MOSFET Current.

$$P_{M_N} = I_{RMS-M_N}^2 \times R_{DSONN} \quad (2.34)$$

Where $R_{DS\text{ONN}}$ is the on-time drain-to-source resistance of the high-side MOSFET M_N .

Substituting for I_{RMS-M_N} :

$$P_{M_N} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(I^2 + \frac{\Delta I^2}{12}\right) \times R_{DS\text{ONN}} \quad (2.35)$$

Thus the total power dissipated in both MOSFET is given by:

$$P_{FET} = P_{M_P} + P_{M_N} \quad (2.36)$$

Substituting for P_{M_P} and P_{M_N} :

$$P_{FET} = \left(I^2 + \frac{\Delta I^2}{12}\right) \times \left[\left(\frac{V_{OUT}}{V_{IN}}\right) \times (R_{DS\text{ONP}} - R_{DS\text{ONN}}) + R_{DS\text{ONN}}\right] \quad (2.37)$$

Where $\Delta I = \frac{(V_{IN}-V_{OUT})V_{OUT}}{L f_{sw} V_{IN}}$. As mentioned above, the inductor ripple current, ΔI , is less than 30% of the total output current for a typical buck power supply design. As a result, the contribution of $\frac{\Delta I^2}{12}$ to the total MOSFET conduction losses is negligible and can be dropped to get:

$$P_{FET} = I^2 \times \left[\left(\frac{V_{OUT}}{V_{IN}}\right) \times (R_{DS\text{ONP}} - R_{DS\text{ONN}}) + R_{DS\text{ONN}}\right] \quad (2.38)$$

Note that when $R_{DS\text{ONP}} = R_{DS\text{ONN}}$, the power dissipated in the MOSFETs is independent of the output voltage. Thus, the MOSFET conduction losses at any output voltage can be calculated. The other losses such as switching losses and inductor conduction losses are independent of output voltage and remain constant with changes in output voltage. Hence,

$$P_{loss} = P_L + P_{FET} + \text{OtherLosses} \quad (2.39)$$

The other losses include the MOSFET switching losses, quiescent current losses etc. If both the total power supply losses and power supply output power are known, the overall

efficiency at any output voltage can be calculated with.

$$\eta = \frac{P_{load}}{P_{load} + P_{loss}} \quad (2.40)$$

2.5.3 Power Conversion Efficiency Improvement

Categories of method can be adopted to improve the conversion efficiency:

- If high efficiency is required in a wide load range, then the hybrid-mode control is a good choice.
- To reduce the static losses of the internal control circuits, a common approach is to shut down all unnecessary blocks when the converter enters light load mode. For example, if a hybrid-mode converter utilizes PFM at light load condition, then the PWM clock and ramp generators can be disabled to save power.
- It should be noticed that, in most designs, static losses are less significant as compared to dynamic losses. In order to reduce dynamic losses, a dead time controller is usually used in a DC-DC converter to minimize the body diode conduction losses and avoid the shoot-through current of power switches [2.4]-[2.7].
- Another significant dynamic loss is caused by the power MOSFET, so the power transistor design is critical. The MOSFET current/voltage waveform is illustrated in Fig. 2.11. By increasing the transistor W/L ratio (i.e. increasing transistor size when the length L is fixed at minimum), the conduction loss is reduced as the transistor on-resistance is smaller. However, a larger transistor size means larger silicon area and higher parasitic capacitance, which will result in higher gate driving losses. Because of this conflict,

different layout methods are proposed for power transistors [2.8]-[2.13].

Figure 2.11: Illustration of Current/Voltage Transition Waveform During Power MOSFET Turning-Off.

- Furthermore, power transistor Dynamic Width Controlling (DWC, also called the power MOSFET segmentation technique) can be implemented to separate the whole transistor into many segments and turn on certain number of segments according to the load condition [2.14]-[2.19]. Thus at light load, the overall dynamic losses are reduced because the dominant gate driving loss is reduced and the conduction loss is insignificant due to the small current.

- There are also other methods that can be applied to further improve the conversion efficiency. For an instant, soft-switching reduces switching losses of the power components by achieving zero-current (ZCS) or zero-voltage switching (ZVS) [2.20-2.24]. A resonant gate driver can partially recover the gate charging energy and thus improve overall efficiency [2.25-2.29].

However, it should be noted that, although applying one of these methods normally improves the conversion efficiency, a converter includes all of these methods may lead to an extremely complicated controller and hence causes more power losses. Therefore, only one or two methods are usually adopted in the real application to reduce the most dominant power losses.

2.6 Control Methodologies

DC-DC converters are widely used in electronic devices. The most critical issue with the operation of a typical DC-DC converter is to generate a well-regulated supply voltage otherwise an unregulated supply voltage will cause the function circuit blocks to work improperly. In general, a DC-DC converter has an input which is an unregulated dc voltage, but its required outputs should be a fixed voltage irrespective of variations in load current or input voltage. Due to the development of power electronics with improved technology, requirements for more accurate and more reliable voltage regulation topologies are desired. This has led to need for more advanced and reliable design of the controller for DC-DC converters. In addition, different technique types of controller are usually required for DC-DC converter targeting for different specifications because it is hard for a single technique to fulfill the requirements of all DC-DC converters. Typically, controllers can be categorized into analog controllers and digital controllers accordingly, and they can further adopt either voltage mode or current mode topologies. The following part will give a brief introduction to the different modulation techniques.

2.6.1 Analog Control

Analog control is the conventional control method, and is still widely used today. It has a lower hardware requirement (i.e., smaller controller area) and continuous range of duty ratio. There are several popular analog modulators for switching mode DC-DC converters, such as Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM) and Pulse Skipping Modulation (PSM). They are discussed here based on a buck converter structure.

- **Voltage Mode Pulse Width Modulation (PWM)**

Although a number of control methods have been invented for high performance control systems, it is still very challenging to ensure these methods to be robust and reliable. Among all the controlling techniques, PWM is considered as the most reliable one according to the linear models [2.30],[2.31]. PWM control techniques are utilized in many applications[2.32]. With PWM controller, a fixed switching frequency of the DC-DC converter is achieved. The converter is controlled to get varieties of regulated output voltages aiming for different specifications by varying the duty ratio time rather than the switching period. Fig. 2.12 shows a voltage mode PWM controlled buck converter, and it can be further divided into trailing-edge modulation and leading-edge modulation. In the trailing-edge modulation, a duty cycle is initiated by the clock signal and terminated by the comparator signal; while in the leading-edge modulation, it is the opposite situation. PWM control method provides high power conversion efficiency at medium to heavy load conditions because the switching conduction loss will not increase under a fixed switching frequency condition.

Figure 2.12: A Voltage Mode PWM Buck DC-DC Converter: (a) Trailing-Edge Modulation and (b) Leading-Edge Modulation

- **Current Mode Pulse Width Modulation (PWM)**

Another advantage offered by PWM is that it can be applied not only in voltage mode, but also in current mode; while the current mode is preferable over the voltage mode because it offers dynamic simplification and also the inherent limitation. Fig. 2.13 shows the peak current mode structure and valley current mode structure. Similar to the trailing-edge and leading-edge modulations of the voltage mode structure, the duty cycle in peak current mode control is initiated by the clock signal and terminated by the comparator signal, and it is the opposite situation in valley current mode control. In terms of control, peak current mode control and valley current mode control are equivalent; but in terms of design, one may be easier than the other if current sensing is realized by senseFET technique. In peak current mode, current sensing is done at the main control switch, while in valley current mode, current sensing is done at the synchronous switch.

Figure 2.13: A Current Mode PWM Buck DC-DC Converter: (a) Peak Current Mode Control and (b) Valley Current Mode Control

If the duty ratio is larger than 50%, the current sensing circuit for the main switch will be easier to design as its settling time is longer, thus peak current mode is preferred. Due to the same reason, if the duty ratio is less than 50%, which means ON-period for the synchronous switch is larger than 50%, then valley current mode is preferred. It is very important to keep in mind that, a duty ratio larger than 50% in peak current mode (or, less than 50% in valley current mode) may cause subharmonic distortion, therefore a slope compensation ramp is usually required. Besides the peak and valley current mode controls, there are also the average current mode control and the charge control, which can be found in [2.33]. The PWM modulation is widely applied in switching mode DC-DC converters. Its fixed frequency ensures predictable Electro Magnetic Interference

(EMI) frequency, and also provides good line/load response. But at light load condition, when switching loss is dominant, PWM modulation encounters low-efficiency problem as it keeps on switching at the constant frequency. To solve this problem, PFM is normally used in light load condition, which will be discussed next.

- **Pulse Frequency Modulation (PFM)**

A DC-DC converter in PFM mode operates at a varying switching frequency, which results in its main disadvantage of EMI issue [2.34-2.38]. It is commonly used in light load condition to improve the power conversion efficiency. This is achieved by operating in Discontinuous Conduction Mode (DCM) to reduce the switching loss (i.e., use slow switching frequency), although PFM can also be designed for Continuous Conduction Mode (CCM) operation. It has several variations, such as single-pulse PFM, multi-pulse PFM, fixed ON-time PFM and fixed OFF-time PFM. However, all operate according to the basic principle of initiating switching cycles only as needed to maintain the output voltage.

Figure 2.14: Synchronous Buck Converter Working in PFM Mode with Fixed On-Time Control

Fig. 2.14 shows one of the conventional PFM controllers used in a synchronous buck

Figure 2.15: Inductor Waveforms for (a) DCM Single-Pulse PFM and (b) DCM Multi-Pulse PFM

converter [2.39] in DCM. When V_{OUT} drops below V_{ref} , the main switch will be turned on for fixed ON-time. The synchronous switch turns on after main switch off, and it will be turned off when the inductor current falls to zero.

Due to most of the applications are at light load conditions, PFM controlled converters usually operate in DCM, where the inductor current ramps down to zero at the end of each cycle. This single-pulse PFM mode is illustrated in Fig. 2.15(a) with fixed ON-time. The duration of zero inductor current is labeled as T_{D3} . When the load demand increases, the idle time decreases. When the load is increased enough so that the average load current demand is more than the current provided by the contiguous DCM pulses with no idle time, the converter automatically switches to multi-pulse operation. In multi-pulse operation, inductor current doesn't ramp down to zero after each switching cycle but ramps higher at the successive pulse until ramps down to zero after the second or the third pulse [2.40]. Normally, single-pulse PFM is preferred rather than multi-pulse PFM because the former one has smaller output voltage ripple. The conversion efficiency of PFM is limited at heavy load, since the switching frequency (i.e., switching loss) will be

increased dramatically [2.41].

- **Pulse Skipping Modulation (PSM)**

Power conversion efficiency can be greatly improved by using PFM instead of PWM at light load. However, as discussed previously, PFM has a variable switching frequency, thus it is difficult to design an input filter for the PFM controlled converter and EMI problems are caused. Another type of modulation, PSM, can be used to improve the EMI performance. PSM generates few charging pulses with fixed duty ratio followed by few skipping pulses (no switching) depending upon the status of the output voltage. Since the clock frequency of the PSM operation remains fixed (at least the switching can be predicted), it reduces the input EMI filter design difficulty. Over the past few years, several PSM control schemes have been reported [2.42-2.47]. One example for

Figure 2.16: Synchronous Buck Converter Working in PSM Mode

PSM control is illustrated in Figure 2.13 [2.48]. If the output voltage is lower than V_{ref} , the clock signal will serve as a fixed-frequency and fixed duty-ratio pulse. Thus the output voltage will be boosted up until it becomes larger than V_{ref} , then the converter will enter pulse-skipping mode with no switching. In general, PSM has a better conversion

efficiency at light to medium load as compared to PWM. But it is not suitable for wide-load-range application if simple PSM design with only fixed duty ratio is adopted. In application, by properly defining the duty ratio, PSM can be used as a transition from PWM to PFM [2.49-2.51]. This kind of hybrid control scheme achieves a wide-load-range efficiency at the expense of three individual controllers and a larger output voltage ripple in PSM mode.

- **Hysteretic Control**

Hysteretic control can be considered as a special PFM control, as it also has variable frequency. It is introduced separately here from PFM because the hysteretic converter is widely applied in CCM operation and its frequency normally does not depend on the output voltage. It is also referred to as nonlinear bang-bang control, and it can be further divided into current mode and voltage mode based on the feedback signal type. Fig

Figure 2.17: Synchronous Buck Converter Working in PFM Mode with Bang-Bang Control

2.17 in [2.52] shows a structure for voltage mode hysteretic control. It consists of two comparators and an S-R flip-flop. When V_{fb} goes higher than V_H , the output $\bar{Q}$ goes low to turn on the power PMOS and to turn off the power NMOS. Thus, the output

voltage is elevated up. If V_{ref} becomes lower than V_L , $\bar{Q}$ goes high to turn off the power PMOS and to turn on the power NMOS. V_{IN} is disconnected and the output voltage starts to drop. Accordingly, the magnitude of the output ripple is determined by the voltage difference (V_{dif}) of V_H over V_L . If the error amplifier is not inserted, the output ripple size will be slightly larger than V_{dif} if R_C is significantly large and the total time delay of the controller and the drivers is negligible. However, if the desired ripple is small, it is actually difficult to make V_H larger than V_L by an exact amount of V_{dif} . By inserting the error amplifier, the error signal is amplified, so V_{dif} can get larger for a given output ripple size. In addition, decreasing the voltage difference reduces the output ripple, but increases the switching frequency and hence affects the conversion efficiency.

2.6.2 Digital Control

Same as the IC design trend, digital controlled DC-DC converters enjoy growing popularity due to their immunity to analog component variations, possibility to implement complicated control algorithms, compatibility with digital systems, and faster design process [2.53-2.58]. However, a digital controller suffers from the resolution limitation of DPWM (Digital Pulse Width Modulation) and ADC (Analog to-Digital Converter). An example of the buck converter with a digital controller is shown in Fig. 2.18. It uses an ADC to convert the feedback voltage into digital format, and then compensates the loop and generates the duty pulse in digital domain. The digital compensator can either mimic the function of an analog compensator, or it can be programmed with more complex controls.

To achieve a highly accurate pulse width in a digital controller, usually two efforts can

Figure 2.18: Block Diagram of The Digital Voltage Mode Control

be made. First, if the DPWM design is based on a counter [2.59], [2.60], then increasing counter speed, i.e., clock frequency, can help to improve the DPWM resolution. This kind of design occupies small area, but for high switching frequency DC-DC converter (several MHz), the required clock frequency may go up to tens of GHz in order to achieve good DPWM resolution, which will cause large power consumption. Second, for those delay line based DPWM [2.61-2.63], the power consumption is low since switching activity is at the converter's switching frequency. However, they consume large chip area due to the huge number of delay units needed. A better choice may be the hybrid design combining a small delay line block with a mid-frequency counter. It balances the power consumption with the circuit area, but increases the design complexity.

At the same time, limitations in ADC design can affect the overall DC-DC converter performance. A lot of special ADCs are designed dedicatedly for DC-DC converter applications [2.64]. While fulfilling a basic resolution requirement, many designs employ digital controller instead of the analog controller to achieve smaller layout area with more sophisticated control. However, after sampling the output voltage by an ADC at the power converter's switching frequency, the controller cannot get any information about the voltage ripple, unless oversampling (at 20 100 times of switching frequency) is used.

As will be discussed in next chapter, the voltage ripple value can provide quite useful information in improving the power converter efficiency.

2.7 Stability Analysis

In this session, a buck converter with voltage-mode control and voltage-mode error amplifier is set as an example to explain the stability issues and the corresponding compensation techniques. This type of buck converter can be stabilized with a proportional-integral (PI) type of compensator. However, to have high performance, a more sophisticated compensation network is required, especially when MLCC (Multi Layer Ceramic Capacitor) capacitors are used. MLCC capacitors are widely used at the output of low voltage DC/DC converters because of their low equivalent series resistance (ESR) and low equivalent series inductance (ESL). Low ESL, which results in high resonance frequency, makes the MLCC capacitors desirable at high switching frequencies. Besides, low ESL and low ESR make the output voltage switching ripple smaller which is very desirable. On the other hand, stabilizing a DC/DC converter with MLCC output capacitors requires more attention as compared to stabilizing a converter with electrolytic output capacitors. Depending on the type/size of the components of output filter which are used and the design parameters (switching frequency, bandwidth, etc), different compensation networks might be required. In addition, to achieve the desired performance, the parameters of the compensation network must be adjusted properly. Fig. 2.19 shows a typical synchronous buck converter with voltage-mode control and voltage-mode error-amplifier. In Fig. 2.19, R_L is the inherent resistance of the output inductor and r_C is the equivalent series resistance (ESR) of the output capacitor.

Figure 2.19: Simplified Circuit Diagram of A Synchronous Buck Converter with A Voltage-Mode Error-Amplifier

ESL of the output capacitors is neglected to simplify the analysis. The circuit shown in Fig. 2.19 can be modeled with three blocks as presented in Fig. 2.20. The power stage $G_p(s)$ includes the power MOSFETs, the buffer drivers and the output inductor and capacitor. The model of the PWM generator is simply $\frac{1}{V_{osc}}$ [2.65], where $\frac{1}{V_{osc}}$ is the peak to peak amplitude of the ramp generator. The compensator block $H(s)$ represents the error-amplifier with the compensation network.

The transfer function of the power stage can be simplified as equation (2.41):

Figure 2.20: The Block Diagram Model of The Synchronous Buck Converter

$$G_p(s) = \frac{V_{OUT}}{D}(s) = \frac{R(C \cdot r_C \cdot s + 1)}{LC \cdot s^2(R + r_C) + s \cdot (L + R \cdot C \cdot r_C) + R} \cdot V_{IN} \quad (2.41)$$

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{LC}} \quad (2.42)$$

$$F_{ESR} = \frac{1}{2\pi \cdot r_C \cdot C} \quad (2.43)$$

Figure 2.21: The Bode Plot of The Power Stage of The Buck Converter

The transfer function of the power stage is a second order system with a double pole at the resonance frequency of the LC filter and a zero produced by the *ESR* of the output capacitor. The resonance frequency and the zero frequency associated with the *ESR* are given by (2.42) and (2.43). The approximate Bode plot of the power stage is sketched in Fig. 2.21. The double pole causes the gain to fall with a slope of -40dB/dec up to the zero frequency F_{ESR} which compensates one of the poles. The zero frequency is a characteristic parameter of the output capacitor and is dependant on the type of the capacitor used. This frequency can be as low as a few kHz for an electrolytic capacitor to as high as a few MHz for a ceramic capacitor.

With the feedback of the compensation network and the control loop, the desired loop

gain of the system can be defined by equation (2.44),

$$M(s) = \frac{1}{k} \cdot H(s) \cdot \frac{1}{V_{osc}} \cdot G_p(s) \quad (2.44)$$

The bode plots of power stage and desired loop gain are shown in Fig. 2.22, where F_0 is the zero crossover frequency defined as the frequency when loop gain equals unity. It is also called the bandwidth of the loop. In general, F_0 can be set to 1/10 to 1/5 of the

Figure 2.22: Bode Plot of The Power Stage, Desired Loop Gain, and Loop Phase

switching frequency. The speed of the system response to load transients is determined by F_0 . In other words, the higher the crossover frequency, the faster the load transient response would be. However, the crossover frequency should be low enough to allow attenuation of switching noise. At F_0 , the slope of the loop gain should be about -20dB with the phase margin to be 45° to ensure the overall stability.

2.7.1 Type II Compensator

Type II compensation is frequently used for applications when the frequency of ESR zero (F_{ESR}) caused by output capacitor is smaller than the closed loop bandwidth (F_0) as described below:

$$F_{LC} < F_{ESR} < F_0 < \frac{F_{sw}}{2} \quad (2.45)$$

This condition is usually met when the output capacitor is of electrolytic type. The F_{ESR} for this type of capacitor is in the range of a few kHz[2.66]. The schematic of the type II compensator is depicted in Fig. 2.23. The transfer function of type II compensator can be derived as:

Figure 2.23: Type II Compensator

$$H(s) = \frac{V_e}{V_{OUT}} = -\frac{1 + R_{C1}C_{C1}s}{sR_{f1}(C_{C1} + C_{C2})\left(\frac{R_{C1}C_{C1}C_{C2}}{C_{C1} + C_{C2}}s + 1\right)} \quad (2.46)$$

The capacitor C_{C2} is chosen so $C_{C2} \ll C_{C1}$, therefore:

$$H(s) \approx -\frac{1 + R_{C1}C_{C1}s}{sR_{f1}C_{C1}(R_{C1}C_{C2}s + 1)} \quad (2.47)$$

As shown in equation (2.47), the compensator has a pole at the origin, and another pole and one zero as given below:

$$F_{Z1} = \frac{1}{2\pi R_{C1}C_{C1}} \quad (2.48)$$

$$F_{P2} = \frac{1}{2\pi R_{C1}C_{C2}} \quad (2.49)$$

The approximate bode-plot of the power stage, the Type II compensator, and the desired loop gain has been drawn in Fig. 2.24. Each pole makes the phase of the loop drop by 90° and each zero makes the phase rise by 90° . The phase change of a zero/pole starts

Figure 2.24: Bode Plot of The Buck Converter Power Stage, Desired Loop Gain, and Type II Compensator

at about 1 decade below the frequency of the zero/pole and ends about 1 decade above it. Since the compensator has a pole at the origin, the zero (F_{Z1}) of the compensator should be placed at a frequency lower than the double poles of the LC filter to make

sure the phase of the loop does not drop close to 0° around F_{LC} . The second pole of the compensator should be placed higher than the cross-over frequency so that its phase drop does not decrease the phase margin of the loop. On the other hand, it should be placed lower than the switching frequency, so that enough attenuation at the switching ripple is obtained.

2.7.2 Type III Compensator

For a general solution for unconditional stability for any type of output capacitors, and a wide range of ESR values, local feedback should be implemented with a type III compensation network. Specially, when $F_0 < F_{ESR}$ type II compensator is not useful and type III compensator must be used. The typically type III compensation network which is used for a voltage-mode PWM converter is shown in Fig. 2.25.

Figure 2.25: Type III Compensator

The transfer function of type III compensator is given by:

$$H(s) = \frac{V_e}{V_{OUT}} = - \frac{(1 + R_{C1}C_{C1}s)[1 + C_{f3}(R_{f1} + R_{f3})s]}{sR_{f1}(C_{C1} + C_{C2})\left(\frac{R_{C1}C_{C1}C_{C2}}{C_{C1} + C_{C2}}s + 1\right)(1 + R_{f3}C_{f3}s)} \quad (2.50)$$

In general, $C_{C2} \ll C_{C1}$. Therefore:

$$H(s) \approx -\frac{(1 + R_{C1}C_{C1}s)[1 + C_{f3}(R_{f1} + R_{f3})s]}{sR_{f1}C_{C1}(R_{C1}C_{C2}s + 1)(1 + R_{f3}C_{f3}s)} \quad (2.51)$$

The compensator has two zeros and three poles as given below:

$$F_{Z1} = \frac{1}{2\pi R_{C1}C_{C1}} \quad (2.52)$$

$$F_{Z2} = \frac{1}{2\pi C_{f3}(R_{f1} + R_{f3})} \quad (2.53)$$

$$F_{P1} = 0 \quad (2.54)$$

$$F_{P2} = \frac{1}{2\pi R_{f3}C_{f3}} \quad (2.55)$$

$$F_{P3} = \frac{1}{2\pi R_{C1}C_{C2}} \quad (2.56)$$

According to different locations of F_{ESR} , type III compensator is further divided to type III-A compensator and type III-B compensator.

- **Type III-A Compensator**

If the zero caused by the ESR is below half of the switching frequency, that is if (2.57) is valid. Type III-A compensation method is used, and the approximate bode-plot of the power stage for the type III-A compensator and the desired loop gain has been drawn in Fig. 2.26.

$$F_{LC} < F_0 < F_{ESR} < \frac{F_{sw}}{2} \quad (2.57)$$

The first zero of the compensator (F_{Z1}) compensates the phase drop of the pole located at the origin. The second zero (F_{Z2}) is to compensate for one of the poles of the LC filter so that at F_0 the slope of the bode plot of the loop is about -20dB/dec. The second pole of the compensator (F_{P2}) and the zero of the ESR of the capacitor (F_{ESR}) cancel each other

and the third pole (F_{P3}) is to provide more attenuation for frequencies above $\frac{F_{SW}}{2}$.

Figure 2.26: Bode Plot of The Buck Converter Power Stage, Desired Loop Gain, and Type III-A Compensator

• Type III-B Compensator

If the zero caused by the ESR is above half of the switching frequency, that is if (2.58) is valid, Type III-B compensation method is used.

$$F_{LC} < F_0 < \frac{F_{SW}}{2} < F_{ESR} \quad (2.58)$$

F_{Z2} and F_{P2} pair are considered as a lead-compensator and are located so that the maximum phase lead of this pair results at crossover frequency (F_0). The following formulas can be used to locate F_{Z2} and F_{P2} in order to get a maximum phase lead of θ at crossover frequency [2.67]:

$$F_{Z2} = F_0 \sqrt{\frac{1 - \sin\theta}{1 + \sin\theta}} \quad (2.59)$$

$$F_{P2} = F_0 \sqrt{\frac{1 + \sin\theta}{1 - \sin\theta}} \quad (2.60)$$

The approximate bode-plot of the power stage, the desired loop gain and the type III-B compensator has been drawn in Fig. 2.27. Sometimes, the value of F_{P2} calculated by (2.60) falls above F_{P3} . The order of the poles is not important, however, the important fact is that there are always two compensator poles above F_{P2} as shown in Fig. 2.27. F_{Z1} compensates the phase lag of the pole which is at origin. F_{Z2} and F_{P2} form a lead compensator and provide their maximum leading phase at crossover frequency and F_{P3} provides further attenuation for frequencies above $\frac{F_{SW}}{2}$.

Figure 2.27: Bode Plot of The Buck Converter Power Stage, Desired Loop Gain, and Type III-B Compensator

Table 2.6 summarizes the varieties locations of the zero frequency caused by different output capacitors, and their corresponding compensation types.

Table 2.6: The Compensation Type and Location of Zero Crossover Frequency

Compensator Type	Relative location of the crossover and power-stage frequencies	Output capacitor
Type II (PI)	$F_{LC} < F_{ESR} < F_0 < \frac{F_{SW}}{2}$	Electrolytic, POS-Cap, SP-Cap
Type III-A (PID)	$F_{LC} < F_0 < F_{ESR} < \frac{F_{SW}}{2}$	POS-Cap, SP-Cap
Type III-B (PID)	$F_{LC} < F_0 < \frac{F_{SW}}{2} < F_{ESR}$	Ceramic

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Chapter 3

Proposed PWM DC-DC Buck

Converter in Discontinuous

Conduction Mode (DCM)

In the previous chapter, different modulation types for switching mode DC-DC converters were briefly introduced (e.g., Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM) and Pulse Skip Modulation (PSM)). Both advantages and disadvantages of them were also compared and discussed. As well known, their efficiency varies with load condition, and each of them normally provides good efficiency only within a limited load range. Therefore, most of the traditional DC-DC converters combine several modulators, and use piecewise control to cater for large load variation. The requirement of multiple modulators normally increases the design complexity and chip area.

For modern portable devices, a long standby time and excellent functional perfor-

mance are two of the most important specifications expected by customers. Therefore, maintaining a good power conversion efficiency over a wide loading range has become the most crucial part of modern power management units (PMU) design. Switch-inductor based buck converters are frequently used because of their high power conversion efficiency and large current drive capability. For area saving purposes, state-of-the-art buck converters operate at switching frequencies in the range of megahertz, or even hundreds of megahertz, to enable the use of smaller-value off-chip output filters [3.1], [3.2], and even on-chip inductors [3.3]. However, the higher the switching frequency, the more power loss is caused by gate driving and switching conduction activities. Particularly, the overall power conversion efficiency is heavily degraded in the light load condition. Although Pulse-Frequency-Modulation (PFM) has been used to improve the light-load power efficiency by scaling down the switching frequency [3.4], its varied switching frequency brings about Electro-Magnetic-Interference (EMI) issues and input filter design challenges.

Considering the above mentioned pros & cons, several control methods were proposed in my works to improve the performances of switching inductor mode DC-DC converters targeting for different applications. Instead of using complicated multi-mode operation, in this chapter, a Pulse-Width-Modulation (PWM) buck converter working in DCM is implemented as an alternative approach to improve the power conversion efficiency, particularly for light load conditions. A novel zero-voltage detector (ZVD) is added as shown in Fig. 3.1 to avoid the occurrence of a reverse inductor current, thus enabling a small value inductor to be used even if the switching frequency is low. Furthermore, switching node voltage ringing was eliminated with corresponding control technology. Compare to the DC-DC regulator with multiple modulators, the circuit implementations

of proposed design were much simpler and the control loop was much easier to be stabilized. However, only simulated results for this particular design is presented due to fabrication delay.

Figure 3.1: Structure of Proposed PWM Buck Converter in DCM.

3.1 Nomenclature

Table 3.1: List of Expressions for Signals, Parameters, Components and Abbreviations

List of Signals and Parameters			
Clock	Clock Signal	T_{sw}	Periodic Time
D	Duty Ratio	V_{ramp}	Ramp Signal
f_{sw}	Switching Frequency	V_{ref}	Reference Voltage
f_{ref}	Reference Frequency	V_{in}	Input Supply Voltage
I_{load}	Load Current	V_x	Switching Node Voltage
i_L	Inductor Current	V_{out}	Output Voltage

Continued on next page

Table 3.1 – continued from previous page

List of Components			
C	Output Filtering Capacitor	M_P	Power PFET
L	Filtering Inductor	R	Load Resistor
M_N	Power NFET	R_f	Feedback Resistor
List of Abbreviations			
CCM	Continuous Conduction Mode	PSM	Pulse Skip Modulation
DCM	Discontinuous Conduction Mode	PWM	Pulse Width Modulation
DTD	Dead Time Detection	PMU	Power Management Unit
EMI	Electro Magnetic Interference Modulation	SC	Switched Capacitor
ESR	Equivalent Series Resistor	PSM	Pulse Skip Modulation
OTA	Operational Transconductance Amplifier	VRM	Voltage Regulation Module
PFM	Pulse Frequency Modulation	ZVD	Zero Voltage Detector

3.2 Conventional Zero Voltage Detection Topologies

For DC-DC regulator working in DCM, one of the most crucial issues is the design of zero-voltage detection for switching node V_x . The required zero-voltage detection circuit needs to sense the voltage information at V_x and make the corresponding reaction as fast as possible to avoid inductor reverse conduction. However, its accuracy and response speed are directly affected by its comparison speed. Recently reported comparators used for zero voltage detection activities can be divided into two categories: continuous time comparators [3.5] and discontinuous time comparators [3.6], [3.7]. The continuous time comparator needs extra time, equivalent to hundreds of nanoseconds to turn on in each switching cycle.

As shown in Fig 3.2, a common-gate topology is used for the continuous time

Figure 3.2: Structure of A Common-Gate Input Continuous-Time Comparator.

comparator in [3.5]. When the power PFET M_P is turned on, V_x is approximately equal to V_{in} , and thus the comparator remains in OFF state. Once the power NFET M_N is turned on, switching node voltage V_x becomes to negative initially, then the comparator changes to ON state, and starts to monitor voltage condition at V_x . However, changing from OFF state to ON state can cause a time delay in hundreds of nanosecond particularly for this type comparator structure, and such time delay leads to significant power conduction loss due to long conduction time of the body diode of M_N .

The discontinuous time comparators in [3.6] and [3.7] use the switched-capacitor (SC) based structures as shown in Fig. 3.3 to ensure the comparators remains on during the whole switching cycle. By doing so, the time delay caused by ON/OFF state change is reduced effectively. However, the SC comparator in [3.6] requires a clock signal,

which is 100 times faster than the switching frequency, to generate ϕ_1 and ϕ_2 , and such clock generator is generally power hungry. The implementation of the zero voltage detection circuit in [3.7] is complicated. In addition, both of the two discontinuous time comparators need more than two phases to control, and any mismatch in each of the capacitor pair will reduce the accuracy of the comparator.

Figure 3.3: A Fully Differential SC comparator for Zero-Voltage Detection

3.3 Principle of Proposed Zero Voltage Detector

The proposed zero-voltage detector (ZVD) contains two parts as illustrated in Fig. 3.4. When power transistor M_N in Fig. 3.1 is conducting, the voltage variation at V_x is small, generally in the range of mV, due to the small turn-on resistance of M_N . A pre-amplifier is used at the first stage to provide enough gain and thus reduce the effect of the input offset voltage. Its output node V_{pre} is connected to a self-biased comparator at the second stage to provide a fast comparison.

Table 3.2 lists the operation states of the proposed ZVD. During ϕ_1 with conditions $G_p = 0$ and $G_n = 0$, M_N is turned off. In both the pre-amplification stage and the comparison stage, the input nodes are connected to ground, and the ZVD is maintained

Figure 3.4: Structure of Proposed Zero Voltage Detector.

Table 3.2: Operation of Proposed ZVD

G_p	G_n	ϕ_1	ϕ_2	V_x	V_{zvd}	M_n
0	0	✓	×	+	Don't care	OFF
1	1	×	✓	-	1	ON
1	1	×	✓	+	0	OFF

in the “ON” state although no comparison is made. As the logic value of V_{zvd} does not affect the operation of the converter, it is marked as “don’t care”. Voltage information at node V_{pre} is stored into a capacitor C . During ϕ_2 with conditions $G_p = 1$ and $G_n = 1$, M_N is conducting with the current flowing from the ground to the switching node V_x . The voltage at V_x is less than zero initially, and becomes larger than zero once the inductor current reaches zero and starts to conduct inversely. The whole process that takes place in ϕ_2 is pre-amplified at the first stage, and the amplified voltage at V_{pre} is consistently compared with the voltage information stored into the capacitor during ϕ_1 . As a result, a logic transition from “1” to “0” that implies a successful zero voltage detection is produced at node V_{zvd} . This logic transition will then be used to turn off M_N to avoid unnecessary inverse inductor conduction.

Recall Fig. 3.1 for overall stability analysis. A simplified small signal DCM PWM switch model [3.8] is shown in Fig 3.5. Thus the duty-cycle-to-output transfer function

for the buck power stage operating in DCM can be derived as equation (3.1).

$$\frac{\Delta V_{out}}{\Delta d} = \frac{jRr}{(r+R)(1 + \frac{rRC+L}{r+R}s + \frac{RLC}{r+R}s^2)} \quad (3.1)$$

where,

$$\left\{ \begin{array}{l} j = \frac{2(1-M)V_{in}}{DMR_e}; \\ r = M^2 R_e = R(1-M); \\ D = M \sqrt{\frac{K}{1-M}}; \\ M = \frac{V_{out}}{V_{in}}; \\ K = \frac{2L}{RT_{sw}}; \\ R_e = \frac{2L}{D^2 T_{sw}}; \end{array} \right. \quad (3.2)$$

Figure 3.5: Small Signal DCM PWM Switch Model.

As $\frac{rRC+L}{r+R} \gg \frac{RLC}{r+R}$, and $rRC \gg L$, a low-frequency pole and a high-frequency pole will formed with the high frequency pole generally been ignored. Then equation (3.1) can be further simplified to equation (3.3).

$$\frac{\Delta V_{out}}{\Delta d} = \frac{jRr}{(r+R)(1 + \frac{rRC}{r+R}s)} \quad (3.3)$$

Equation (3.3) means that the switching stage of DCM operation only contributes a single pole to the loop instead of a pair of complex poles created by that of CCM operation.

In general, type III compensation technique is applied for CCM operation as it creates two low-frequency zeros to compensate the complex poles produced at power stage, thus an output capacitor with a small equivalent series resistor (ESR) can be used. Besides, the loop bandwidth will be boosted up leading to a fast transient response. Theoretically speaking, a single pole system under DCM operation is unconditional stable with nearly 90° phase margin. However, relatively narrow bandwidth and 90° phase margin may cause a slow transient response. Hence, type II compensation is utilized as illustrated in Fig.3.1 at the beginning of this chapter. The transfer function can be derived as equation (3.4).

$$\left\{ \begin{array}{l} H(s) = \frac{1 + R_{C1}C_{C1}s}{sR_{f1}C_{C1}(1 + R_{C1}C_{C2}s)}; \\ F_{z1} = \frac{1}{2\pi R_{C1}C_{C1}}; \\ F_{p2} = \frac{1}{2\pi R_{C1}C_{C2}}; \end{array} \right. \quad (3.4)$$

One pole is created at the origin, and a low frequency zero F_{z1} can compensate the pole at origin and the pole introduced by power stage to maintain a phase margin of about 60° . A high-frequency pole F_{p2} is also created to suppress the ESR zero at the output stage. By choosing $R_{C1} = 250k\Omega$, $C_{C1} = 30pf$ and $C_{C2} = 3pf$, the loop frequency response is plotted in Fig. 3.6 with a 68° phase margin. The crossover frequency is about 80 kHz, which is about tenth of switching frequency, 700 kHz.

Figure 3.6: Loop Frequency Response.

3.4 Circuits Implementations and Design Considerations

3.4.1 Zero-Voltage Detector

For transistor level design considerations, two simple common-source amplifier stages are cascaded as shown in Fig. 3.7(a) to provide enough gain for pre-amplification. Then, a voltage source follower is used to provide a low impedance node located at V_{pre} so a high-frequency pole is created without reducing the response speed. Besides, a replica circuit is added to copy the voltage information at node V_{pre} in order to provide a stable common mode input voltage at the second comparison stage.

The second comparison stage involves a self-biased comparator as shown in Fig. 3.7(b). Its comparison speed will not be limited by the biasing conditions. In between these two stages, only one capacitor is utilized to store voltage information during ϕ_1 , thus no capacitor matching issues are of concern. In comparison to the previously reported discontinuous time comparator with a power hungry clock signal, ϕ_1 and ϕ_2 in this design

are generated from the output of the dead-time controller with a frequency that is equal to the switching frequency. Fig. 3.8 shows the waveforms of ϕ_1 and ϕ_2 . There is no overlap in conduction time for the switches conducting in ϕ_1 and those conducting in ϕ_2 . As a result, the short-circuit leakage current, which will affect the voltage information stored in the capacitor, is avoided.

(a)

(b)

Figure 3.7: Transistor Level Implementation of (a) Pre-amplifier Stage, (b) Comparison Stage.

Figure 3.8: Waveforms of Clock Signals.

3.4.2 Dead Time Controller

The transistor level implementation of the dead time controller, which is also used in the proposed design to generate the clock signal (ϕ_1 and ϕ_2), is shown as Fig. 3.9. The lengths of dead time are determined by the inverter chain time delay as marked in blue for logic “1” to “0” transition and in red for logic “0” to “1” transition. In this case, a dead time about 3 gates drive time delay, which is roughly 600ps, is generated with each inverter providing 200ps time delay. The dead time control can be optimized by adding extra adaptive control techniques, but it will increase the design complicities.

3.4.3 Dead Time Detector

When the inductor current decreases to zero, both M_p and M_n are turned off. The remaining energy stored at node V_x has no path to be discharged. Therefore, the voltage ringing phenomenon is frequently observed because of the parasitic LC tank located at node V_x . In general, an auxiliary transistor M_{EMI} working as a ringing suppression circuit as shown in Fig. 3.1 is connected across inductor L, and M_{EMI} will be turned on to

Figure 3.9: Schematic of The Dead Time Controller.

provide a low resistive path across inductor L . This extra low resistive path is used for energy discharge when both M_p and M_n are turned off. However, as the waveforms in Fig. 3.10(a) illustrate, both M_p and M_n are turned off not only in region III, but also in the dead-time region. The operation of the converter will be interrupted if the ringing suppression block is activated in the dead-time region. In order to differentiate between the dead-time region and region III, a dead-time detection (DTD) block with logic gates shown in Fig. 3.10(b) is implemented. The DTD circuit not only depends on the current states of M_p and M_n through monitoring G_p and G_n signals but also relies on the previous

logic level at node Y. As the state diagram of Fig. 3.10(a) shows, although the states of G_p and G_n are the same for both the dead-time region (where the inductor current is maximum) and region III (where the inductor current is zero), the previous state logic level at node Y is “0” for the dead-time region and logic “1” for the region III. By adding the previous state “Y” as an extra condition, these two regions are separated along with the two previous regions (region I and region II, respectively).

Figure 3.10: (a) Waveforms of The Dead Time Detector, (b) Logic Gates of The Dead Time Detector.

3.4.4 High Gain Error Amplifier

A high gain and high g_m operational transconductance amplifier (OTA) structure are used in this design. The g_m of the OTA can be increased by K-fold by setting the current mirror ratio to 1:K. To achieve a high dc gain for realizing optimal regulation, a wide swing cascade technique is applied. M_{n9} to M_{n12} are also used as current sources to extract the current from the input stage. Therefore, the extracted current is not mirrored to the output stage, thereby minimizing the static current. Because the output impedance is inversely proportional to the square root of the drain current, M_{n9} to M_{n12} can improve efficiency as well as increase the compensator's dc gain.

Figure 3.11: High Gain and High g_m OTA for Error Amplifier Design.

3.5 Results and Discussions

The proposed buck converter operates at a switching frequency of about 700 kHz, and provides a regulated output voltage of 2.4V with a maximum load current about 250mA. Fig. 3.12 and Fig. 3.13 provides the inductor current profile with load currents at 10mA, 50mA, 100mA and 200mA respectively. When the inductor current reaches zero, the proposed ZVD takes only about 6ns to react and turn off M_n , and leads the power stage into the idle state. Besides, the voltage ringing at the switching node V_x is completely eliminated by the ringing suppression circuits.

(a)

(b)

Figure 3.12: Inductor Current Profile at (a) $I_{load} = 10\text{mA}$, and (b) $I_{load} = 50\text{mA}$.

(a)

(b)

Figure 3.13: Inductor Current Profile at (a) $I_{load} = 100\text{mA}$, and (b) $I_{load} = 200\text{mA}$.

In Fig. 3.14, the transient response times are $12\mu\text{s}$ for both the 200mA step-up load and 200mA step-down load, and the output ripple voltage is about 20mV in steady state operation. Fig. 3.15 shows the power conversion efficiency for different load conditions with a 3.3V supply voltage, and a peak efficiency of about 94.2% is achieved at $I_{load} = 130\text{mA}$.

Table 3.3 summaries all of the performance parameters, and it should be noticed that only 33pf capacitors in total are used for compensation. The total size of the capacitor used for compensation is much less than that of the CCM buck regulator with conventional type III compensation in [3.9], which is 110pf . Fig. 3.16 shows the chip layout of the

Figure 3.14: Transient Response of a 200mA Load Step.

Figure 3.15: Power Conversion Efficiency at $V_{in} = 3.3V$.

proposed buck converter with a silicon area of $1mm \times 0.9mm$.

Table 3.3: Comparison with Prior Work

	This work	[3.9]JSSC'2010
Input Voltage	3.3V	3V
Output Voltage	2.4V	0.8-2.4V
Load Current	10-250mA	600mA
Switching Frequency	700kHz	1MHz
Inductor L	1 μ H	4.7 μ H
Capacitor C	10 μ F	4.7 μ F
Total Compensation Capacitor and Resistors	$R_{C1} = 250k\Omega$, $C_{C1} = 30pf$, $C_{C2} = 3pf$	$R_C = 120k\Omega$, $C_C = 110pf$
Peak Efficiency	94.2%	97%
Technology	0.18 μ m	0.35 μ m

Figure 3.16: Layout of The Chip.

3.6 Summary

A novel zero voltage detector introducing a single capacitor to store comparison information and its two-phase switches controlled by the dead time logics have been analyzed and discussed. Fast sensing ability and high resolution of the proposed detector ensure the optimized operation of the power transistors, and thus improve the overall power conversion efficiency of the DCM buck regulator by minimizing the reverse inductor current conduction, especially at light load condition. Besides, loop frequency response of the proposed DCM buck regulator has also been discussed. Type II compensation technique is applied based on the concerns of loop transient response speed and the total capacitor size of the compensation network. In a battery-operated portable device, the proposed DCM buck regulator will greatly increase the power efficiencies, and result in a longer run time.

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Chapter 4

A Fixed Frequency Hysteretic

Controlled Buck Converter-Design I

For the above mentioned DC-DC converter operates in discontinuous conduction mode, the circuit level implementation is simplified when compared to its hybrid mode counterpart. A reasonable conversion efficiency is achieved as well. However, the main drawback of it is a bulk compensation network is still used. More important, the loop control technique is mainly based on linear control theory which will limit the loop response speed. Modern portable devices are highly integrated with a number of functional blocks as expected by customers. Thus, as more and more multi-functional system-on-chip applications are integrated into these portable devices, their power management units (PWU) should provide a well-regulated supply voltage despite large and frequently varied loading current [4.1]. As a result, a more reliable and more robust voltage regulator system that dealing with various loading conditions and more complicated dynamics is urgently needed. However, the performance of traditional voltage regulators are

generally constrained by control loop's stability issue. When taking the loop stability into concern, conventional linear control technology like PWM generally has a limited bandwidth of 10-20% of the voltage regulator's switching frequency [4.2], which implies a big challenge to design a DC-DC converter with fast transient response. However, if the transient responses of the voltage regulators are slow when dealing with frequently changed loading current, a long settling time will reduce the system reliability [4.3] or will result in degraded Signal-to-Noise Ratio (SNR) performance of noise-sensitive circuits [4.4],[4.5]. Thus, traditional linear control methodology may not be the best option. Therefore, the nonlinear hysteretic controlled DC-DC converter has become as a promising alternative solution to be used in fast-transient-response power supplies for microprocessors and digital signal processor because of its simple and reliable structure. Besides, excellent dynamic characteristics make it possible to use the smaller size and the lower cost output filtering components [4.6].

In this chapter, a DC-DC buck converter with fixed switching frequency hysteretic control is proposed. This control method combines the advantages of both conventional PWM control and PFM control techniques. Compared to conventional PFM control, fixed switching frequency results in predictable Electro-Magnetic Interference (EMI) issue, more stable output ripple voltages, and lesser input filter design challenges. Meanwhile, a hysteretic comparator taking over the bulk error amplifier appearing in conventional PWM control technology leads to better transient response and fewer stability considerations. Furthermore, good conversion efficiency will be achieved over a wide loading range as the switching frequency will not increase with an increase in loading current.

4.1 Nomenclature

Table 4.1: List of Expressions for Signals, Parameters, Components and Abbreviations

List of Signals and Parameters			
CLK_{ref}	Reference Clock	V_{band}	Hysteretic Window
D	Duty Ratio	V_{fb}	Feedback Voltage
f_{sw}	Switching Frequency	V_H	Hysteretic Window Upper Boundary
f_{ref}	Reference Frequency	V_{ref}	Reference Voltage
I	Load Current	V_{in}	Input Supply Voltage
I_{sync}	Adjustable Current	V_L	Hysteretic Window Lower Boundary
i_L	Inductor Current	V_x	Switching Node Voltage
t_{tran}	Transient Recovery Time	V_{out}	Output Voltage
T_{sw}	Periodic Time		
List of Components			
C	Output Filtering Capacitor	M_N	Power NFET
C_{fb}	Feedback Capacitor	M_P	Power PFET
L	Filtering Inductor	R	Load Resistor
r_C	Capacitor ESR	R_{fb}	Feedback Resistor
r_L	Inductor ESR		
List of Abbreviations			
CCM	Continuous Conduction Mode	PFD	Phase Frequency Detector
CP	Charge Pump	PLL	Phase Lock Loop
CMHC	Current-Mode Hysteretic Control	PWM	Pulse Width Modulation
EMI	Electro Magnetic Interference Modulation	VCO	Voltage Controlled Oscillator
ESR	Equivalent Series Resistor	VLS	Voltage Level Shifter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor	VMHC	Voltage-Mode Hysteretic Control
PFM	Pulse Frequency Modulation	VRM	Voltage Regulation Module
SNR	Signal to Noise Ratio	PMU	Power Management Unit

4.2 Conventional Fixed Frequency Hysteretic Control

In a hysteretic controlled converter, transient recovery time is no longer limited by its switching frequency. Instead, it's determined by the input and output voltage as well as the LC filter. Fig. 4.1 shows a simplified waveform to estimate the transient recovery time. The transient recovery time caused by an up step load can be roughly estimated as:

Figure 4.1: Waveforms of Output Voltage Transient Response.

$$\Delta V_{out} = \left(\frac{V_{in} - V_{out}}{L} \right) t_{tran(up)} \quad (4.1)$$

Where ΔV_{out} should be inversely proportional to load capacitor C . Hence,

$$\Delta V_{out} = \frac{m}{C} \quad (4.2)$$

Where m is a coefficient related to load step. Then combining above two equations,

$$t_{tran(up)} \approx \frac{mL}{C(V_{in} - V_{out})} \quad (4.3)$$

The transient recovery time caused by a down step load can be derived in a similar way,

$$t_{tran(down)} \approx \frac{mL}{CV_{out}} \quad (4.4)$$

Equation (4.3) and (4.4) demonstrate all of the parameters related to the transient recovery time. Instead of responding to load transient after a few switching cycles as PWM control does, the hysteretic controlled regulator can achieve nearly instantaneous response [4.7-4.9]. Nevertheless, hysteretic nonlinear control method indeed provides certain benefits like faster transient speed and more stable structure, but its variable switching frequency brings in potential Electro-Magnetic Interference (EMI) failure for noise-sensitive systems (e.g., RF transceiver) and phase interleaving problems for high current capability multi-phase designs (e.g., Voltage Regulation Module (VRM) for microprocessor) [4.10].

Fig. 4.2 shows two typical hysteretic control structures: the voltage-mode hysteretic control (VMHC) and current-mode hysteretic control (CMHC), where the inductor current information is excluded from or included in the feedback signals, respectively. In both cases, a hysteretic comparator with a hysteretic window V_{band} is used. The switching frequencies for these two structures depend on the output filter characteristics, input and output voltage, hysteresis window, and internal delays. In addition, the simplified expression of switching frequencies under continuous conduction mode (CCM) can be derived as below:

$$f_{sw(VMHC)} \approx \frac{V_{out}(V_{in} - V_{out})r_c}{LV_{in}V_{band}} \quad (4.5)$$

$$f_{sw(CMHC)} \approx \frac{V_{out}(V_{in} - V_{out})}{R_{fb}C_{fb}V_{in}V_{band}} \quad (4.6)$$

As equation (4.5) and equation (4.6) indicated, reducing the hysteretic window will increase the switching frequency, and vice-versa. However, if the switching frequency becomes higher and higher, frequency variation will become more significant because of additional parameters like internal circuit delay, input supply voltage noise and output voltage noise. Especially for VMHC, the Equivalent Series Resistance (ESR) of the

(a)

(b)

(c)

Figure 4.2: Typical hysteretic buck converters: (a) with VMHC structure, (b) with CMHC structure, and (c) CCM operation waveform of the feedback signal oscillating within the hysteretic window under VMHC with significant R_c or under CMHC.

output capacitor plays an important part in determining the switching frequency. Thus, connecting a number of ceramic capacitors in parallel will lower down the ESR and make the switching frequency becomes very low.

As a result, a new type of control methodology called fixed frequency hysteretic control becomes more attractive. As the name indicated, it combines both characteristics of linear control method (PWM) and nonlinear control method (PFM). Unlike the conventional linear PWM control, a hysteretic comparator is used to replace the slow

error amplifier for the purpose of fast transient response and better loop stability. In the meantime, comparing to conventional nonlinear PFM control with varied switching frequency and large output ripple noise, the switching frequency in the fixed frequency hysteretic control will be locked to a reference clock frequency which can be externally provided or generated from the internal circuit. Hence, such a fixed frequency hysteretic control method is also called pseudo-PWM control [4.11]. Some previous works have been reviewed and they can be categorized into 4 groups according to their frequency locking methods as shown below.

- *Frequency locking by adjusting the on/off duty period in the fixed-on-time or fixed-off-time control schemes [4.12-4.14].*

Figure 4.3: Fixed Frequency Hysteretic Buck Converter with Adaptive-On/Off-Time

Fig. 4.3 shows a voltage-mode constant ON-time or constant OFF-time hysteretic DC-DC converters. A frequency control loop, consisting of a phase frequency detector (PFD) and a charge pump (CP) with a low-pass filter (LPF), is added to lock the switching frequency to reference clock by adjusting the ON/OFF duty period. Voltage mode hysteretic converter generally requires a relatively large r_C value, otherwise the

comparator need to be very sensitive to detect the output ripple voltage, and such a comparator consumes a lot of power.

- Advantage: simple structure of frequency controller.
- Disadvantage: trade-off between voltage regulation and frequency locking range.
- *Frequency locking by adding in an adjustable delay [4.12], [4.15].*

Figure 4.4: Fixed Frequency Hysteretic Buck Converter with Adjustable Delay

Fig. 4.4 shows current-mode hysteretic DC-DC converter. An RC tank is in parallel with inductor to monitor its current and then the current information is compared with the hysteretic window. The digital output at the output of the comparator will first compare with a clock reference through a phase frequency detector (PFD), a charge pump (CP), and a low pass filter (LPF). The voltage value of V_c will adjust the delay time, and finally the switching frequency to turn on or turn off the power MOSFETs will be locked to the reference clock frequency.

- Advantage: simple structure of frequency controller.
 - Disadvantage: tradeoff between voltage regulation and frequency locking range.
- *Frequency locking by adjusting hysteretic window [4.16-4.19].*

Figure 4.5: (a) Fixed Frequency Hysteretic Buck Converter with Adjustable Hysteretic Window, (b) Hysteretic Comparator with Adjustable Window.

Fig. 4.5(a) utilizes an adjustable hysteretic window to lock the switching frequency to the reference one. In general, the adjustable hysteretic window together with the comparator can be implemented as shown in Fig. 4.5(b). A variable resistor R_4 , which is normally a transistor working in the triode region, is used to adjust the hysteretic window and then the switching frequency will be locked to the reference clock frequency. However, a transistor works in the triode region can only provide a very narrow range of resistance, hence the frequency tuning range will also be limited. Moreover, the voltage regulation loop will lead to a more complicated circuit design as more function blocks are introduced and more stability issues needed to be concerned.

- Advantage: implementation through discrete components is possible.

- Disadvantage: complicated controller (large silicon area and power consumption), bad voltage regulation, narrow frequency locking range.
- *Frequency locking by injecting periodic synchronization signal at V_{ref} [4.20], [4.21].*

Figure 4.6: Fixed Frequency Hysteretic Buck Converter with A Periodic Synchronization Signal

The reference clock is initially modulated into a periodic signal and injected into V_{ref} as a synchronization signal. The synchronization signal can be either a current or a voltage, e.g., the periodic I_{sync} in Fig. 4.6. It adds a ripple into V_{ref} , which will appear on the hysteretic window as well, so that feedback signal V_{fb} will follow the envelope of the periodic ripple, leading to $f_{sw} = f_{ref}$.

- Advantage: simplest structure of frequency controller.
- Disadvantage: very narrow frequency locking range, frequency control is not precise, unstable operation when the frequency is out of range.

In all reported works, the output voltage regulation is affected by the frequency controller, unless a dedicated voltage regulation is utilized [4.18], [4.19]. But then the compensation network in the voltage loop requires an additional operational amplifier

or trans-conductance amplifier, and will increase design difficulty and slow down the transient response.

Based on the above considerations, this work investigates a new fixed-frequency current-mode hysteretic control. More specifically in this work, a fixed switching frequency control method by adjusting the hysteretic window through an adjustable current source is proposed. Besides, a transient detection circuit is proposed to improve transient response performance particularly for this type of current mode hysteretic control method as well as output voltage regulation.

4.3 Principle of Proposed Fixed Frequency Hysteretic Controlled Buck Converter

As Fig. 4.7 illustrated, a series connected RC filter is in parallel with the inductor to imitates its current information, and which will be reflected by voltage, V_{fb} . The feedback signal V_{fb} has a DC level voltage equal to buck converter output (if ignoring voltage drop across inductor ESR, r_L), and an AC ripple reflecting the inductor current cycle-to-cycle variation. V_{fb} is compared with the hysteretic window which is pre-defined by the positive feedback across a normal comparator. Subsequently, the duty ratio signal D will be generated at the output of the comparator, and it will be further used to control the ON/OFF states of power transistors. In the meantime, frequency information of the duty ratio signal D will be fed back to compare with a reference frequency (CLK_{ref}) through a phase frequency detector (PFD). It is then followed by a charge pump (CP), and a low pass filter (LPF) to generate voltage V_c , which is used to adjust the hysteretic

window and lock the switching frequency to the reference clock (CLK_{ref}).

Figure 4.7: Structure of Proposed Fixed Hysteretic Controlled Buck Converter.

Fig. 4.8 shows how the hysteretic window is adjusted in detail. Two adjustable current sources controlled by duty ratio signal D are connected to the positive input node of the hysteretic comparator. When V_{fb} reaches the lower boundary of the hysteretic window, V_L , the duty ratio signal D changes to logic high, which is equal to the supply voltage V_{DD} . Then it is used to turn on power PMOS through a dead-time controller and an inverter buffer chain. Meanwhile, V_{DD} will be shifted to a voltage level equals to two times of V_{ref} by a voltage level shifter (VLS), and the threshold voltage of the hysteretic comparator will shift to the upper boundary of the hysteretic window, V_H , simultaneously. Hence, V_H can be derived from Fig. 4.8(b):

$$\frac{2V_{ref} - V_H}{R_2} = \frac{V_H - V_{ref}}{R_1} + I_{sync} \quad (4.7)$$

After rearrangement,

$$V_H = \frac{2R_1 + R_2}{R_1 + R_2} V_{ref} - \frac{R_1 R_2}{R_1 + R_2} I_{sync} \quad (4.8)$$

Figure 4.8: (a) Proposed hysteresis comparator with an adjustable current source, (b) $D=1$, generating upper boundary V_H of the hysteretic window, (c) $D=0$, generating lower boundary V_L of the hysteretic window.

Similarly, when V_{fb} reaches the upper boundary of the hysteretic window, V_H , the duty ratio signal D will change to logic low. Power NMOS is turned on and the VLS is disabled. As a result, the threshold voltage of the hysteretic comparator will shift back to the lower boundary of the hysteretic window, V_L . Hence, V_L can be derived from Fig. 4.8(c):

$$\frac{V_{ref} - V_L}{R_1} + I_{sync} = \frac{V_L}{R_2} \quad (4.9)$$

Thus,

$$V_L = \frac{R_2}{R_1 + R_2} V_{ref} + \frac{R_1 R_2}{R_1 + R_2} I_{sync} \quad (4.10)$$

Combining equation (4.8) and (4.10), we can calculate the band of hysteretic window as:

$$V_{band} = V_H - V_L = \frac{2R_1}{R_1 + R_2} V_{ref} - 2 \frac{R_1 R_2}{R_1 + R_2} I_{sync} \quad (4.11)$$

Equation (4.11) shows that changing I_{sync} will then tune the hysteretic window. As a result, varieties of switching frequencies can be achieved with such hysteretic window tuning mechanism. In addition, Fig. 4.9 provides a more intuitive way to understand how

Figure 4.9: Hysteretic Window Tuning Mechanism.

the hysteretic window is tuned. In steady-state operation, the average value of V_{fb} shown in Fig. 4.9 will be located at the middle of the hysteretic band.

Figure 4.10: Inductor Current Sensing by A RC Filter.

Fig. 4.10 shows the feedback circuit, which is also an inductor current sensor. Ideally, it can be derived from Fig.4.10 that the average value of the switching node voltage V_x is equal to the average value of the output voltage V_{out} . However, by considering the r_L of

the inductor, there is a DC voltage drop between them. As the r_L induced voltage error reduces linearly with the load current, an inductor with small r_L is necessary and then the voltage error can be ignored since the comparator offset induced voltage error will dominate at the loading current range specified in the proposed design [4.22]. In addition, the average value of V_x is two times the average value of V_{fb} . Thus, the average value of V_{out} is derived as:

$$V_{out} = 2(V_L + \frac{1}{2}V_{band}) \quad (4.12)$$

Then substituting equation (4.10) and (4.11) into equation (4.12), we can get:

$$V_{out} = 2V_{ref} \quad (4.13)$$

Equation (4.13) is valid as the difference between the converter real output voltage and the nominal output voltage is negligible, and the delay existing in the control loop is ignored as well as the voltage across the inductor ESR is negligible. Seen from equation (4.13), the output voltage will be determined by reference voltage only. Hence, adjusting the current I_{sync} for frequency tuning will not affect the output voltage regulation.

As mentioned previously, the feedback voltage V_{fb} will be compared with the hysteretic window in order to get the duty ratio information. Thus the amplitude of V_{fb} should equal to the hysteretic window V_{band} .

$$\Delta V_{fb} = V_{band} \quad (4.14)$$

Seen from Fig. 4.10, if the turn on resistance of the power PMOS is small, V_x approximately equals to the input supply voltage V_{in} . Besides, the average value of V_{fb} equals

to one half of the output voltage V_{out} as mentioned above. Thus, ΔV_{fb} can be roughly calculated as:

$$\Delta V_{fb} = \frac{\left(\frac{V_{in} - \frac{1}{2}V_{out}}{R_{fb}} - \frac{\frac{1}{2}V_{out}}{R_{fb}} \right) \times D \times T_{sw}}{C_{fb}} \quad (4.15)$$

with the assumption that ΔV_{fb} or the hysteretic window V_{band} is much smaller than V_{in} .

Then equation (4.15) can be simplified as:

$$\Delta V_{fb} = \left(\frac{V_{in} - V_{out}}{R_{fb}} \right) \frac{V_{out} T_{sw}}{V_{in} C_{fb}} \quad (4.16)$$

Combining equation (4.11), (4.13), (4.14) and (4.16), the switching frequency can be derived as follow:

$$\frac{1}{f_{sw}} = \frac{2\pi V_{in} R_{fb} C_{fb} R_1}{(V_{in} - V_{out})(R_1 + R_2)} \left(1 - \frac{2R_2 I_{sync}}{V_{out}} \right) \quad (4.17)$$

Equation (4.17) demonstrates that the switching frequency will be affected by the supply input voltage and the output voltage as well as all of the relevant passive devices. Hence, by implementing an adjustable current source, I_{sync} , the switching frequency can be accurately tuned within a certain frequency range. Besides, the value of I_{sync} is determined by the difference between free-running switching frequency and reference clock frequency. Larger the frequency difference, more current of I_{sync} is generated, and vice versa.

Recall Fig. 4.7 for stability consideration, there are 3 loops existing in the proposed buck converter. Loop 1 containing an R_{fb} - R_{fb} - C_{fb} filter then followed by a hysteretic comparator is the main control loop. The feedback voltage V_{fb} is oscillating within the hysteretic window which is generated by the hysteretic comparator to ensure the power stage works properly.

Figure 4.11: Small Signal Model of The Proposed Frequency/Phase Locking Loop.

Loop 2 is a frequency/phase locking loop which is used to lock the switching frequency to an external reference clock. Fig. 4.11 shows a small signal model of the second order frequency/phase locking loop implemented in the proposed design. The combination of PFD, CP, and LPF can be modeled as $\frac{I_B}{2\pi} (R_{c1} + \frac{1}{C_{c1}s})$, where I_B is the current of the CP. R_{c1} and C_{c1} are the passive devices of the LPF. In addition, a small parallel capacitor C_{c2} is introduced to produce a high-frequency pole to reduce the variation at V_c . By choosing the value of C_{c2} to be about one-tenth of C_{c1} , the closed-loop time and frequency responses remain relatively unchanged, and hence it can be ignored to simplify stability analysis. The VCO comprises the proposed window control circuit (I_{sync} & hysteretic comparator) and its small signal model of I_{sync} plus hysteretic comparator can be represented by $\frac{k}{s}$ as they imply the integration of V_c , which is called excess phase as well. k is a simplified coefficient related to I_{sync} and the comparator. Then the open loop transfer function is equal to:

$$\frac{\phi_D}{\phi_{CLK_{ref}}}(s)|_{open-loop} = \frac{I_B k (1 + R_{c1} C_{c1} s)}{2\pi C_{c1} s^2} \quad (4.18)$$

Two low-frequency poles cause 180° phase drop at low frequency, and one zero is

introduced to compensate for it. Then the close loop transfer function is equal to:

$$\frac{\phi_D}{\phi_{CLK_{ref}}}(s)|_{close-loop} = \frac{\frac{I_B k}{2\pi C_{c1}}(R_{c1}C_{c1}s + 1)}{s^2 + \frac{I_B}{2\pi}R_{c1}s + \frac{I_B}{2\pi C_{c1}}k} \quad (4.19)$$

Fig. 4.12 shows the bode plot of the PLL. By choosing proper values of R_{c1} , C_{c1} , and C_{c2} , the loop GBW is set at 50kHz with a phase margin of 63° . Hence, it can ensure the stability of the PLL.

Figure 4.12: Bode Plot of PLL.

Loop 3 is a positive feedback loop with a capacitive feedback path formed by C_{fb} and C . Although the positive feedback loop is existed, the feedback factor is derived as equation (4.20):

$$\beta = \frac{C_{fb}}{C_{fb} + C} \quad (4.20)$$

As the size of C_{fb} is much smaller than that of C . Thus, the overall positive loop gain will be much smaller than one so the overall stability will not be affected.

4.4 Circuits Implementations and Design Considerations

4.4.1 Frequency and Phase Locking Loop Design

Figure 4.13: Frequency and Phase Locking Loop.

Seen from equation (4.17) shown above, it is clear that the switching frequency will vary a lot corresponding to different input supply voltages and output voltages as well as devices' process variations. In order to get a more stable operating switching frequency, an extra parameter that can be manually controlled, for instance, I_{sync} in this case, needs to be used. As Fig. 4.13 illustrated, with the variation of V_{in} , V_{out} and the passive devices, a free running switching frequency is estimated initially with the duty ratio signal represented by D . Then, D is connected to the input of a phase/frequency detector (PFD) and then compared with a reference clock CLK_{ref} , which is the desired working frequency. The amount of phase/frequency difference between CLK_{ref} and D

will be reflected by digital signals “UP” and “DN” at the output of the PFD. Both “UP” and “DN” will be used to control the switches of a charge pump and the pulse width of them implies the charge pump charging or discharging time, respectively. At the output

Figure 4.14: Simulated Waveforms of The Phase Frequency Detector in Lock Condition.

of the charge pump, the pulse width information will be accumulated on a low pass filter resulting in a voltage level indicated by V_c . At last, V_c is converted into I_{sync} through a voltage-to-current converter, and I_{sync} is further used to adjust the hysteretic window of the comparator and finally lock the switching frequency f_{sw} to CLK_{ref} . Under lock condition, no frequency/phase difference between CLK_{ref} and D . Therefore, the pulse width of “UP” and “DN” will become zero, leading the charge pump to be closed and V_c as well as I_{sync} to remain unchanged. However, real circuits will generate certain time delay or system noise because of the parasitic components located at the signal path. This is the reason why “UP” and “DN” in Fig. 4.14 have a portion of overlapping pulses even in locking condition. Fortunately, the width of overlapping areas for “UP” and “DN” are

almost equal because they suffer from the same time delay. So the net charge caused by real circuits delay will be cancelled if the charging current and the discharging current of the charge pump are equal. As a result, a charge pump circuit with good charging current and discharging current matching property is required, especially when the switching frequency is higher, signal process delay becomes more serious.

• **Phase/Frequency Detector Design**

Figure 4.15: (a) Conceptual Operation of PFD, (b) Implementation of PFD, (c) Implementation of D Flip-Flop.

In Fig. 4.15(a), CLK_{ref} leads the duty signal D . Digital signal “UP” continues to produce pulses whose width is proportional to $\phi_{CLK_{ref}} - \phi_D$, while digital signal “DN” remains at zero. By symmetry, if CLK_{ref} lags D or has a lower frequency than B , then

“DN” produces corresponding pulses and “UP” remains quiet. As a result, the dc contents of “UP” and “DN” provide information about $\phi_{CLK_{ref}} - \phi_D$ or $\omega_{CLK_{ref}} - \omega_D$.

Fig. 4.15(b) shows a simple implementation consisting of two edge-triggered D flip-flops with their “D” input tied to a logical ONE. The input of interest, CLK_{ref} and D , serve as the clocks of the flip-flops. If “UP”=“DN”=0 and CLK_{ref} goes high, “UP” rises. If this event is followed by a rising transition on D , “DN” goes high and the AND gate resets both flip-flops. In other words, “UP” and “DN” are simultaneously high for a short time but the difference between their average values still represents the input phase or frequency difference correctly. Each flip-flop can be implemented as shown in Fig. 4.15(c), where two RS latches are cross-coupled. Latch 1 and Latch 2 respond to the rising edges of CLK and Reset, respectively.

• Proposed Charge Pump Design

Based on the above-mentioned considerations, a charge pump with wide swing current mirror structure shown in Fig. 4.16(b) is proposed to provide a better-charging current and discharging current matching property. Besides, as the conceptual idea of the charge pump illustrated in Fig. 4.16(a), the position of the two switches and the two current sources are switched. By doing so, the switching noise at node V_C is greatly reduced so a more flatten voltage signal V_C can be realized. If “UP” and “DN” are logic high, charge pump will be turned on to charge or discharge node V_C , respectively. On the contrary, if “UP” and “DN” are logic low or in lock condition, it will be turned off by connecting the gate of PMOS to supply voltage and the gate of NMOS to ground, respectively.

• Proposed Isync Generator

As mentioned in Fig.4.8 previously, both upper boundary and lower boundary of

Figure 4.16: Schematic of (a) Conceptual Idea of Proposed CP, (b) Transistor Level Implementation of Proposed CP.

the hysteretic window will be adjusted concurrently to achieve a wide frequency tuning range. Hence, it requires the adjustable current source I_{sync} has both of current driving and current sinking capabilities. As a result, the duty ratio signal D is added into the adjustable current source generator as shown in Fig. 4.17 to determine the current source or current sink option. When the duty ratio signal D is logic high, I_{sync} is sank to the ground to adjust the upper boundary V_H as indicated in Fig. 4.8(b); and when it is logic low, I_{sync} is source from the power supply to adjust the lower boundary V_L as indicated in Fig. 4.8(c).

Figure 4.17: Schematic of Proposed Isync Generator.

4.4.2 Transient Detection Circuitry

As mentioned at the beginning of this chapter, a voltage mode hysteretic controlled DC-DC converter provides an almost instantaneous transient response because the output voltage is directly fed back to the control loop with a non-linear control mechanism. Current mode hysteretic control proposed in this work is also based on nonlinear control mechanism and it provides a fast transient response as well. However, as a result of lacking direct voltage regulation at V_{out} , the feedback loop of the proposed current mode hysteretic control cannot respond as quick as that of conventional voltage mode hysteretic control does. As a capacitor C_{fb} is connected between V_{out} and V_{fb} , even if a sudden overshoot or undershoot caused by loading variation appears, the feedback loop cannot react immediately because the voltage stored in capacitor C_{fb} will compensate for such variation [4.23]. Hence, the power stage will still works in steady state for certain time

Figure 4.18: Schematic of Proposed Transient Detection Circuit.

before reacting, and thus results in a degraded transient response performance. In this work, a g_m -RC filter structure is added to enhance the transient response performance. Meanwhile, the g_m -RC filter also improves V_{out} regulation. As Fig. 4.18 illustrated, the output voltage changes dynamically to provide different supply voltages for different applications, so conventional operational transconductance amplifier (OTA) topologies cannot ensure a well defined g_m over a wide input range. However, a varied g_m cannot always guarantee enough gain for the proposed transient detection circuit and thus may

affect the transient response performance. Therefore, a g_m -RC filter structure with g_m proportional to a constant value is proposed. A super source follower structure is implemented at the input stage to force constant biasing current and thus maintain a well-defined g_m . In the small signal model, the g_m can be derived as equation (4.21).

$$g_m = \frac{2K(\frac{v_A - v_B}{R_{gm}})}{v_{in+} - v_{in-}} \quad (4.21)$$

The output resistance seen from node V_A can be derived as:

$$r_o = r_{B1} \parallel r_{o4} \parallel \left(\frac{r_{o2} + r_{B2}}{[1 + (g_{m2} + g_{mb2})r_{o2}](1 + g_{m4}r_{B2})} \right) \quad (4.22)$$

By assuming ideal current source and $(g_{m2} + g_{mb2})r_{o2} \gg 1$.

$$r_o \approx \frac{1}{g_{m2} + g_{mb2}} \left(\frac{1}{g_{m4}r_{o2}} \right) \quad (4.23)$$

equation (4.23) implies the negative feedback through transistor M4 reduces the output resistance by a factor of $g_{m4}r_{o2}$ when comparing with a simple source follower. Therefore, such low output resistance seen from node V_A is suitable to drive a small resistive load R_{gm} , and this property is similar at node V_B as well. In addition, the voltage gain of the super source follower is derived as equation (4.24) and (4.25) by assuming ideal current source.

$$\frac{v_A}{v_{in+}} = \frac{g_{m2}r_{o2}}{1 + (g_{m2} + g_{mb2})r_{o2} + \frac{1}{g_{m4}r_{o4}}} \quad (4.24)$$

$$\frac{v_B}{v_{in-}} = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{1}{g_{m3}r_{o3}}} \quad (4.25)$$

As $g_{m3}r_{o3} \gg 1$ and $g_{m4}r_{o4} \gg 1$, equation (4.24) and (4.25) show that the derivation of the gain from unity is similar to that of a simple source follower. Hence by simplicity, the voltage gain can be approximately calculated as one. Therefore, equation (4.21) can be simplified as:

$$g_m = \frac{2K}{R_{gm}} \quad (4.26)$$

where K is a constant multiplier and R_{gm} is a passive resistor.

During steady state operation, V_{out} is equal to two times of V_{ref} and the g_m -RC filter is biased at certain DC operating point with a small I_{gm} to regulate V_{out} . Thus, the feedback voltage V_{fb} contains almost the inductor current sensing information V_{fb1} . Once an overshoot or undershoot appears at the output node, such variation will be directly fed back to V_{fb} through the proposed g_m -RC filter with a gain derived as equation (4.27).

$$\frac{\Delta V_{fb2}}{\Delta V_{out}} = \frac{KR_{fb}}{R_{gm}(1 + s\frac{1}{2}R_{fb}C_{fb})} \quad (4.27)$$

Overall, by superposition,

$$\Delta V_{fb} = \Delta V_{fb1} + \frac{K\Delta V_{out}R_{fb}}{R_{gm}(1 + s\frac{1}{2}R_{fb}C_{fb})} \quad (4.28)$$

As equation (4.28) indicated, an overshoot or undershoot appears at V_{out} will now lead V_{fb} changes immediately through the g_m -RC filter path. Then the inductor current will be saturated or be idled. As a result, a faster transient response is achieved. In addition, the process variation will be cancelled if R_{fb} and R_{gm} are well matched. Fig. 4.19 shows the overall transistor level implementation of the proposed phase/frequency lock loop including a phase-frequency detector (PFD), a proposed charge pump (CP), and a dual

side adjustable current generator (I_{sync}), and the proposed transient detection circuit built up by a super source follower.

Figure 4.19: Transistor Level Implementation of Proposed Adjustable Current Source and Transient Detection Circuit.

4.5 Results and Discussions

The proposed fixed-frequency hysteretic controlled buck converter was fabricated in 180nm CMOS technology, and experimental results were analyzed and discussed to compare with the prior works. As illustrated in Fig. 4.20, Fig 4.21, and Fig. 4.22, the

(a)

(b)

Figure 4.20: The Switching Frequency Is Locked at: (a) 8MHz and $I_{load}=200mA$, (b) 8MHz and $I_{load}=400mA$.

(a)

(b)

Figure 4.21: The Switching Frequency Is Locked at: (a) 9MHz and $I_{load}=200mA$, (b) 9MHz and $I_{load}=400mA$.

frequency locking capability was tested at 3.3V to 2.4V voltage conversion condition. Besides, the loading currents were set at 200mA and 400mA accordingly for illustration purpose. An external reference clock was manually adjusted, and then how the switching frequencies track the reference clock were recorded. As the measured waveform shows, the switching frequencies which were indicated by the duty ratio signal D were locked to

be 8.04MHz, 9.06Mhz, and 10.06MHz when the reference clock was adjusted to 8MHz, 9MHz, and 10MHz, respectively. Frequency variations less than 1% were realized. The frequency variations were caused mainly because of the real circuit delay through phase/frequency locking loop and testing equipment. The frequency locking test revealed

(a)

(b)

Figure 4.22: The Switching Frequency Is Locked at: (a) 10MHz and $I_{load}=200\text{mA}$, (b) 10MHz and $I_{load}=400\text{mA}$.

that the proposed fixed frequency hysteretic control method indeed helped to predict the

switching frequencies, and the switching frequencies could be controlled by a reference clock within a particular frequency range. Unlike the conventional hysteretic controlled DC-DC converter with an unpredictable switching frequency, the proposed design will help to reduce Electro-Magnetic Interference (EMI) issues and challenges on input filter design.

In addition, frequency locking tests were applied to different input supply voltages and varied loading conditions. Fig. 4.23 summarizes how the switching frequencies

Figure 4.23: Measured Switching Frequency at Different Input Voltage.

varies at different input supply voltage with the reference clock chosen to be 10MHz. Within a typical Li-ion battery working range, the proposed design always locked the switching frequencies to be around 10MHz with a variation of less than $\pm 1\%$. Fig. 4.24 summarizes how the switching frequencies vary at different loading conditions, and the reference clock was chosen to be 10MHz as well. It can be seen that the switching

Figure 4.24: Measured Switching Frequency at Different Loading Current.

frequencies were locked at around 10MHz over a wide loading range. A portion of frequency variation exists because of the system noise or the measuring accuracy.

As for transient response test, Fig. 4.25(a) and Fig. 4.25(b) show the output voltage and the inductor current information at a 500mA up-step loading and a 500mA down-step loading, respectively. The undershoot and overshoot are measured to be 200mV and 180mV with the size of the power stage LC filter chosen to be 500nH and 470nF, respectively. With the help of the proposed transient detection circuit, the transient recovery time of the up-step loading and down-step loading achieve to be 2us and 1.8us, respectively. Fig. 4.26 plots the measured power-conversion efficiency for different I_{load} under different switching frequency (8MHz,9MHz,10MHz). A peak efficiency of around 90% is achieved at the loading about 150mA. When the loading current exceeds 400mA, the overall efficiency drops sharply because of the increasing conduction loss at

(a)

(b)

Figure 4.25: Measured Load Transient Response for A Loading Change From (a) 100mA to 600mA, and (b) 600mA to 100mA.

heavy load condition. Moreover, the die area is around 0.9mm x 0.9mm with the chip micrograph shown in Fig. 4.27.

Table 4.2 summarizes the performance of the proposed fixed frequency hysteretic controlled buck converter. Five prior designs are chosen for comparison and discussion purpose with three designs having a switching frequency of 1 MHz [4.11], [4.24], [4.25], and two designs having a switching frequency of several tens of MHz [4.26], [4.27]. Comparing with those designs having a switching frequency of 1MHz, the proposed

design uses the smaller size of inductor and capacitor benefiting from higher switching frequency. In addition, the smaller value of inductor and capacitor is also compatible with the development trend of modern DC-DC converters for highly integrated devices. Although some existing DC-DC converters with a switching frequency of hundreds of MHz have already fully integrated power stage LC filter into a single chip, the overall efficiency is relatively low as the switching conduction loss increases sharply under such high switching frequency. Besides, the transient recovery time is shorter in the proposed design than the other three designs benefitting from higher switching frequency and the proposed transient detection circuitry. The peak efficiency of the proposed design is around 90% because of more switching conduction loss. When comparing with those designs having a switching frequency of tens of MHz, the power conversion efficiency is better, and a comparable transient recovery time is achieved as indicated by the ratio of Recovery Time divided by Load Current Step. In fact, the transient recovery time of the proposed design largely depends on the gain of the proposed transient detection circuitry.

Figure 4.26: Measured Efficiency versus Loading Current for Different Switching Frequency.

Figure 4.27: Die Photo of The Proposed Buck Converter.

Table 4.2: Performance Comparison with Prior Designs

	[4.24]VLSIC'12	[4.11]TVLSI'12	[4.25]TPEL'16	[4.28]TPEL'18	[4.26]JSSC'15	[4.27]JSSC'09	This Work
Fsw stabling technology	Adapt. Ind. Curr Sensing	Adapt.Hyst. Window	AOT & Load Curr Correct	COT & PWT	T-PID PWM	Hysteretic	Adapt.Hyst. Window
Technology(μm)	0.13	0.35	0.18	0.028	0.065	0.5	0.18
Chip Size(mm^2)	2.13	4.18	1.095	2.5	1	3.3	0.81
Inductor(μH)	5	4.7	N.A.	1	0.09	0.11-0.22	0.5
Capacitor(μF)	10	4.7	N.A.	4.7	0.47	0.19	0.47
Fsw(MHz)	1	1	1	2.5	30-70	25-70	8-10
Vin(V)	2.5	2.4-4.2	2.7-3.6	3.3	1.8	4-5	3-4.2
Vout(V)	0.7-1.8	1.8	1-1.2	1.05	0.6-1.5	0.86-3.93	2.4
Max. Load(mA)	900	500	1100	1700	800	1000	600
Load Step(mA)	600	200	700	1400	400	300	500
Offset(mV)	N.A.	N.A.	N.A.	4	N.A.	N.A.	18
Trecovery(μs) Up/Step	10/10	4/5	5/5	4/5	1.6/2	0.8/0.8	2/1.8
Undershoot/ Overshoot(mV)	61/72	40/40	N.A.	75/90	140/200	350/350	200/180
Peak Efficiency(%)	93	95	88.2	94	87	83	90
FOM1	3	4	N.A.	2.96	0.16	0.87	3.69
FOM2	N.A.	N.A.	N.A.	7.39	N.A.	N.A.	2.05

$$FOM_1 = \frac{L * I_{load} * 100}{C_{OUT} * F_{SW} * T_R}; FOM_2 = \frac{L * I_{load} * 1000}{C_{OUT} * F_{SW} * T_R * V_{offset}}$$

4.6 Summary

A fixed frequency hysteretic controlled DC-DC buck converter is discussed and implemented in this paper. Circuit designs like charge pump, adjustable current source have been presented in this paper. Besides, a transient detection circuit with a predictable g_m is proposed for this particular current mode hysteretic controlled buck converter as well. The design has been fabricated using 180nm CMOS technology. With the help of the transient detection circuit, the measured transient recover time is 2us and 1.8us for a 500mA up-step loading and a 500mA down-step loading, respectively. The switching frequency can be accurately locked from 8MHz to 10MHz with a frequency variation within $\pm 1\%$. This type of hysteretic controlled DC-DC converter with switching frequency predicted by a reference clock is suitable to work as a unit cell for multi-phase interleaved DC-DC converter applications in order to provide large current drive capability.

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Chapter 5

A Fixed Frequency Hysteretic

Controlled Buck Converter-Design II

In modern portable devices, the rapid development of processor technology has posed enormous challenges for the design of power management units (PMU). Frequent load switching requires the converters to have fast load transient responses with recovery times in the order of μs , and therefore switching frequencies within the MHz range [5.1]. Advanced control methods of DC-DC converters are extensively applied because of their fast response and simple architecture. Among existing advanced control methods, hysteretic control approaches [5.2]–[5.5] demonstrate the fastest loading dynamics. However, with regard to switching frequency, the conventional hysteretic control techniques result in varied switching frequencies, which may cause Electro-Magnetic-Interference(EMI) issues and challenges in input filter design. As a result, a new type of control methodology called fixed-frequency hysteretic control becomes more attractive.

In chapter 4, some previous works related to fixed-frequency hysteretic control methods were reviewed. According to their frequency locking method, they were categorized into 4 groups as shown below:

- Frequency locking by adjusting the on/off duty period in the fixed-on-time or fixed-off-time control schemes.
- Frequency locking by adding in an adjustable delay.
- Frequency locking by adjusting the hysteretic window.
- Frequency locking by injecting a periodic synchronization signal.

A new current-mode fixed-frequency hysteretic control method with transient response improvement circuit was proposed as well to deal with frequently switched loadings. As proven by the experimental results, the switching frequency of the proposed design can be accurately controlled within 8MHz to 10MHz, and a transient recovery time less than $2\mu s$ was achieved. Nevertheless, the transient response time was limited by the gain of the transient response improvement circuit, and it could be further optimized by adding other control techniques. A phase-locked loop (PLL) is generally applied as an additional control loop to maintain the switching frequency at the desired value through negative feedback correction. Several approaches that involve the use of PLLs to realize a fix switching frequency are reported in [5.2], [5.4], [5.6], and [5.7]. In [5.2] and [5.4], PLLs were used to control adaptive delay circuits according to the output voltages and load conditions. In [5.6] and [5.7], PLLs were used to adjust a hysteretic window according to a switching frequency referenced from an external clock; this control method is called the adaptive window control.

This chapter presents a fixed-frequency hysteretic buck converter designed and fabricated using 0.18- μm CMOS process. With a phase-locked loop (PLL) based adaptive window control, the proposed buck converter can achieve a fixed switching frequency, and this frequency can be tuned within a certain range through a reference clock frequency. Concurrently, a novel auxiliary circuit is proposed to monitor the converter's output loading dynamics to reduce the converter's transient recovery time. It will also help to regulate the output voltage at the steady-state operation as well. With the supply voltage ranging from 3V to 4.2V, and an output voltage of 1.8V, the simulated switching frequency is maintained at 10MHz because of the PLL control. The transient response time is only 0.3 μs and 0.4 μs for step-up load and step-down load, respectively. However, only simulated results for this particular design is presented due to fabrication delay.

5.1 Nomenclature

Table 5.1: List of Expressions for Signals, Parameters, Components and Abbreviations

List of Signals and Parameters			
CLK_{ref}	Reference Clock	V_{band}	Hysteretic Window
D	Duty Ratio	V_{fb}	Feedback Voltage
f_{sw}	Switching Frequency	V_H (V_{HH})	Hysteretic Window Upper Boundary
f_{ref}	Reference Frequency	V_{ref}	Reference Voltage
I	Load Current	V_{in}	Input Supply Voltage
I_{sync}	Adjustable Current	V_L (V_{LL})	Hysteretic Window Lower Boundary
i_L	Inductor Current	V_x	Switching Node Voltage
t_{tran}	Transient Recovery Time	V_{out}	Output Voltage
T_{sw}	Periodic Time		
Continued on next page			

Table 5.1 – continued from previous page

List of Components			
C	Output Filtering Capacitor	M_N	Power NFET
C_{fb}	Feedback Capacitor	M_P	Power PFET
L	Filtering Inductor	R	Load Resistor
R_C	Capacitor ESR	R_{fb}	Feedback Resistor
R_L	Inductor ESR		
List of Abbreviations			
CCM	Continuous Conduction Mode	PFD	Phase Frequency Detector
CP	Charge Pump	PLL	Phase Lock Loop
CMHC	Current-Mode Hysteretic Control	PWM	Pulse Width Modulation
EMI	Electro Magnetic Interference Modulation	VCO	Voltage Controlled Oscillator
ESR	Equivalent Series Resistor	VLS	Voltage Level Shifter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor	VMHC	Voltage-Mode Hysteretic Control
PFM	Pulse Frequency Modulation	VRM	Voltage Regulation Module
SNR	Signal to Noise Ratio	PMU	Power Management Unit

5.2 Principle of Proposed Fixed Frequency Hysteretic Controlled Buck Converter

This work proposes a fixed frequency hysteretic buck converter. A novel adaptive window control circuit is designed to obtain a fixed switching frequency as this method involves lesser control complexity than the adaptive delay controller. Therefore, in the proposed study, a PLL was used to control the hysteretic window to achieve a fixed switching frequency through a relatively simple approach. The PLL adopts the conventional architecture, which includes a phase frequency detector (PFD), a charge

pump (CP), and a low pass filter (LPF). Its output is used to control both the upper and lower boundaries of the adaptive window. Based on the proposed window control circuit, an auxiliary circuit is added to provide instantaneous hysteretic window shifting as well as a change to the slope of the feedback voltage to further enhance the transient response performance.

Figure 5.1: Structure of Proposed Fixed-Frequency Hysteretic Buck Converter.

Fig. 5.1 shows the system diagram of the proposed fixed-frequency hysteretic buck converter. The quasi- V^2 structure enables sensing the inductor current information through a feed-forward RC network without using an output capacitor with high equivalent series resistor (ESR). The sensed feedback signal V_{fb} can be estimated as the equation shown below:

$$\begin{cases} V_{fb}(t) \approx V_{fb}(0) + \frac{(V_x - V_{out})}{R_{fb}C_{fb}}t, & 0 \leq t \leq DT_{sw} \\ V_{fb}(t) \approx V_{fb}(DT_{sw}) + \frac{(V_x - V_{out})}{R_{fb}C_{fb}}(t - DT_{sw}), & DT_{sw} \leq t \leq T_{sw} \end{cases} \quad (5.1)$$

Equation (5.1) indicates that V_{fb} is in phase with the inductor current; however, this

signal has a dc offset as the output voltage. The output voltage can be regulated by controlling the sensed feedback signal in a fixed hysteretic window.

Fig. 5.2 illustrate the operating waveform of the proposed converter. When V_{fb} is charged to the upper boundary of the hysteretic window V_H , the duty ratio signal D changes to logic high, which is equal to the supply voltage. Then it is used to turn off the high side power MOS switch (M_P) and turn on the low-side power MOS switch (M_N) through a dead-time controller (DTD), and then the feedback voltage V_{fb} is discharged to the lower boundary of the hysteretic window V_L . Similarly, when V_{fb} is discharged to the lower boundary (V_L), the duty ratio signal D changes to logic zero, which is equal to the ground voltage. Then M_P is turned on and M_N is turned off at this time in order to charge V_{fb} to the upper boundary V_H again. In steady state operation, the sensed feedback voltage V_{fb} will oscillate in the hysteretic window with a dc offset equal to the output voltage V_{out} .

Apart from utilizing the duty ration signal D to control the power MOS switches, it is also used to represent the switching frequency and is locked to a reference clock frequency (CLK_{ref}) through a phase/frequency locking loop (PLL). When the DC-DC regulator turns on initially, the free-running switching frequency f_{sw} is determined by a series of parameters including the input supply voltage V_{in} , the output voltage V_{out} , the values of the feedback R_{fb} - C_{fb} network, and the size of the hysteretic window V_{band} . The simplified equation to evaluate f_{sw} can be derived as equation (5.2)

$$f_{sw} \approx \frac{V_{out}}{R_{fb}C_{fb}V_{band}} \left(1 - \frac{V_{out}}{V_{in}}\right) \quad (5.2)$$

The duty ratio signal D is fed back to compare with the reference frequency (CLKref)

Figure 5.2: Operating Waveforms of The Proposed DC-DC Buck Converter.

through a phase frequency detector (PFD). It is then followed by a charge pump (CP), and a low pass filter (LPF) to generate the window control voltage V_{ctrl} . Then the size of hysteretic window V_{band} is adjusted by V_{ctrl} adaptively. According to the switching frequency of the proposed converter expressed in (5.2), at a higher input voltage V_{in} with a constant output voltage V_{out} , the control voltage V_{ctrl} should increase the size of the hysteretic window V_{band} to maintain a constant frequency. Similarly, at a lower input voltage V_{in} with a constant output voltage V_{out} , the control voltage V_{ctrl} should decrease the size of the hysteretic window V_{band} to maintain a constant frequency. This adaptive adjustment can be understood in a more intuitive way in Fig. 5.2. When the input voltage changes to a relatively high value and the hysteretic window remains constant, the switching period decreases; this is because the charging slope of the inductor current rises and the discharging slope remains constant. Therefore, the hysteretic window should

be larger to lengthen the charging time to ensure that the same switching frequency is achieved. Similarly, the hysteretic window should be smaller when the input voltage decreases. In a nutshell, the PLL can accurately lock the switching frequency to the desired reference frequency CLK_{ref} under different input voltage conditions by adjusting the hysteretic window.

Figure 5.3: Schematic of The Transient Detection Circuit in Chapter 4.

As for transient response performance enhancement, the transient detection circuit proposed in chapter 4 is recalled to discuss at first. As shown in Fig. 5.3, a g_m -RC filter structure with g_m proportional to a constant value is proposed to provide a fast loading transient detection. A super source follower structure is implemented at the input stage to force constant biasing current and thus maintain a well-defined g_m . In the small signal model, the g_m can be derived as equation (5.3).

$$g_m = \frac{2K \left(\frac{V_A - V_B}{R_{gm}} \right)}{V_{in+} - V_{in-}} \quad (5.3)$$

As derived in chapter 4, the equivalent transconductance g_m can be simplified as below:

$$g_m = \frac{2K}{R_{gm}} \quad (5.4)$$

where K is a constant multiplier and R_{gm} is a passive resistor.

During steady-state operation, the g_m -RC filter is biased at certain DC operating point with a small I_{gm} to regulate V_{out} . Thus, the feedback voltage V_{fb} contains almost the inductor current sensing information V_{fb1} . Once an overshoot or undershoot appears at the output node, such variation will be directly fed back to V_{fb} through the proposed g_m -RC filter with a gain derived as equation (5.5).

$$\frac{\Delta V_{fb2}}{\Delta V_{out}} = \frac{KR_{fb}}{R_{gm}(1 + s\frac{1}{2}R_{fb}C_{fb})} \quad (5.5)$$

Overall, by superposition,

$$\Delta V_{fb} = \Delta V_{fb1} + \frac{K\Delta V_{out}R_{fb}}{R_{gm}(1 + s\frac{1}{2}R_{fb}C_{fb})} \quad (5.6)$$

As equation (5.6) indicated, an overshoot or undershoot appears at V_{out} will now lead V_{fb} changes through the g_m -RC filter path. Then the inductor current will be saturated or be idled, and thus a faster transient response is achieved. However, the gain and the bandwidth of the g_m -RC filter are constrained by the values of the feedback R_{fb} - C_{fb} networks. As the values of R_{fb} and C_{fb} are the two major parameters used to determine the switching frequency f_{sw} , so their values to be chosen are very limited. Hence the gain and the bandwidth may not be optimized although a PLL is used for switching frequency tuning within a certain frequency range. As a result, the transient response performance may not be optimized and needs to be further improved by adding in other techniques. Therefore, an auxiliary circuit is proposed to compensate for the drawbacks of the transient detection circuit proposed in chapter 4.

The working mechanism of the auxiliary circuit can be explained by the waveforms shown in Fig. 5.4. When an up-step loading is taken place at the output stage, an undershoot sensed at V_{out} will decrease the slope of the feedback voltage V_{fb} from k_1 and k_2 to k_3 and k_4 , respectively. By doing so, the charging time of the high-side power MOS M_P is increased, and the discharging time of the low-side power MOS M_N is decreased. Similarly, when a down-step loading is taken place at the output stage, an overshoot sensed at V_{out} will increase the slope from k_2 and k_1 to k_6 and k_5 , respectively. By doing so, the charging time of the high side power MOS M_P is decreased, and the discharging time of the low side power MOS M_N is increased. This is what the transient detection circuit in chapter 4 actually does and how it leads to a short transient recovery time. Equation (5.7), (5.8), and (5.9) demonstrate the mathematic derivations of these slopes.

$$\begin{cases} k_1 = \frac{\frac{V_{in}-V_{out}}{R_{fb}}}{C_{fb}}; \\ k_2 = \frac{\frac{-V_{out}}{R_{fb}}}{C_{fb}}; \end{cases} \quad (5.7)$$

$$\begin{cases} k_3 = \frac{\frac{V_{in}-V_{out}}{R_{fb}} - I_{gm}}{C_{fb}}; \\ k_4 = \frac{\frac{-V_{out}}{R_{fb}} - I_{gm}}{C_{fb}}; \end{cases} \quad (5.8)$$

$$\begin{cases} k_5 = \frac{\frac{V_{in}-V_{out}}{R_{fb}} + I_{gm}}{C_{fb}}; \\ k_6 = \frac{\frac{-V_{out}}{R_{fb}} + I_{gm}}{C_{fb}}; \end{cases} \quad (5.9)$$

In the proposed design as shown in Fig. 5.4, the proposed auxiliary circuit will also shift the hysteretic window upper boundary from V_H to V_{HH} once an up-step loading is detected, and it will also shift the hysteretic window lower boundary from V_L to V_{LL} once a down-step loading is detected. With the help of hysteretic window boundary shifting, the charging time of the high-side power MOS M_P is further increased for an up-step loading, and the discharging time of the low-side power MOS M_N is further increased for a down-step loading as well. As a result, the transient recovery times realized are even shorter than those in chapter 4. At last, both the undershoot voltage and the overshoot voltage decline, and the converter enters in steady-state operation with the hysteretic window shift from V_{HH} back to V_H and from V_{LL} to V_L , respectively.

5.3.1 Adaptive Hysteretic Window with Auxiliary Circuit.

Figure 5.5: Schematic of The Proposed Adaptive Window with Auxiliary Circuit.

Fig. 5.5 illustrates the transistor level implementations of the proposed adaptive window control circuit and the auxiliary circuit. The OTA structure with a supper follower input pair proposed in chapter 4 is utilized here again as the proposed auxiliary circuit. Based on this OTA, two extra auxiliary current branches are added under the control of switches S_p and S_n . In steady-state operation, V_{out} is equal to V_{ref} , a small I_{gm} is injected into the control loop for better output voltage regulation. Both switches S_p and S_n are in OFF state, and they will turn on only during transient state to provide the pre-mentioned instantaneous hysteretic window shift (V_H to V_{HH} and V_L to V_{LL}), and more detail will be presented later together with the transient detection logic. Furthermore in steady-state operation, the power stage switching frequency is in a “lock” condition with referred to a reference frequency CLK_{ref} , and thus the control voltage V_{ctrl} remains unchanged. Then the hysteretic window can be determined as:

$$V_{band} = \frac{(V_{ctrl} - V_{GS})(R_1 + R_2)}{R_{ctrl}} \quad (5.10)$$

Assuming that $V_{band} \ll V_{in}$, and the turn on resistances of power transistors are negligible, the power stage switching frequency can be simplified from equation (5.2) as:

$$f_{sw} = \frac{R_{ctrl}(V_{in} - V_{out})V_{out}}{(V_{ctrl} - V_{GS})(R_1 + R_2)R_{fb}C_{fb}V_{in}} \quad (5.11)$$

As equation (5.11) indicated, the switching frequency f_{sw} are determined by input supply voltage, output voltage, R_{fb} - C_{fb} feedback network, and other components used in the design. By introducing in an extra parameter V_{ctrl} , by which reflects the phase and the frequency difference between f_{sw} and CLK_{ref} , the hysteretic window is controlled by it adaptively, so does the switching frequency.

5.3.2 Transient Detection Logic

Figure 5.6: Schematic of The Proposed Transient Detection Logics.

In the transient state operation, the proposed logic gates of the transient detection circuit shown in Fig. 5.6 determines whether the switches (S_p or S_n) are turned on or off

accordingly. For a step-up load, an undershoot at V_{out} will be detected with the condition $p=0$. S_p in Fig. 5.5 will turn on, causing an extra path of current to be generated from the supply and absorbed at the output node of the buffer. An instantaneous shifting of V_H to V_{HH} is achieved. Simultaneously, a larger I_{gm} is drawn from node V_{fb} such that the slope of V_{fb} shown in Fig. 5.4 will decrease from k_1 to k_3 and k_2 to k_4 , respectively. The power stage inductor will be fully charged because of the shift in the upper boundary and decrease in the slope. Therefore, a shorter undershoot recovery time will be achieved. Similarly for a step-down load, an overshoot at V_{out} will be detected with the condition $n=1$. S_n will turn on, and an extra path of current will be drawn to the ground from the output node of the buffer. An instantaneous shifting of V_L to V_{LL} will be achieved, and a larger I_{gm} is injected into node V_{fb} such that the slope of V_{fb} will increase from k_1 to k_5 and k_2 to k_6 , respectively. The power stage inductor will be fully discharged because of the shift in the lower boundary and increase in the slope. Therefore, a shorter overshoot recovery time will be achieved as well.

5.3.3 Phase/Frequency Lock Loop Design

As for the phase/frequency lock loop design, circuit transistor level implementations have been discussed in chapter 4 with a second order low pass filter to ensure the frequency lock loop stability. The only difference in this chapter is the charge pump circuit design. As the phase/frequency detector (PFD) explains in chapter 4, the pulse width of the digital signal “UP” and “DN” determine the charging time and the discharging time of the charge pump, respectively. As shown in Fig. 5.7, the digital signals “UP” and “ $\overline{UP}$ ” are connected to a differential input pair of PMOS, and the digital signals “DN”

and “ $\overline{DN}$ ” are connected to a differential input pair of NMOS. When the switching frequency f_{sw} is larger than or the phase of it is leading that of the desired reference frequency CLK_{ref} , “ UP ” is logic “1” and “ DN ” is logic “0”. Thus a current I_B will flow through M_{P1} , M_{P2} , M_{P3} , M_{N9} , M_{N7} , M_{P5} , and M_{P6} to charge the node V_{ctrl} . Then the voltage level of V_{ctrl} will increase leading to a larger hysteretic window. As both the increasing slope and the decreasing slope of the feedback voltage V_{fb} are unchanged, a smaller switching frequency or a lagging phase compared to CLK_{ref} will be achieved. The whole process will continue iteratively through the phase lock loop (PLL) until the

Figure 5.7: Schematic of The Proposed Charge Pump Circuit.

switching frequency f_{sw} is locked to the desired frequency CLK_{ref} . Similarly, when the switching frequency f_{sw} is smaller than or the phase of it is lagging that of the desired reference frequency CLK_{ref} , “ UP ” is logic “0” and “ DN ” is logic “1”. Thus a current I_B will flow through M_{N1} , M_{N2} , M_{N4} , M_{P9} , M_{P7} , M_{N5} , and M_{N6} to discharge the node V_{ctrl} . Then the voltage level of V_{ctrl} will decrease leading to a smaller hysteretic window. A larger switching frequency or a leading phase compared to CLK_{ref} will be achieved. The switching frequency will also be locked to the CLK_{ref} through the PLL iteratively. In

addition, almost a rail-to-rail voltage swing can be realized at the output node, V_{ctrl} , of the proposed charge pump, thus a wide frequency tuning range can be achieved.

5.4 Results and Discussion

The proposed fixed-frequency hysteretic buck converter is fabricated in $0.18\mu\text{m}$ C-MOS process and operates at a switching frequency locked at 10MHz. The calculated frequency variation is less than $\pm 1\%$. In Fig. 5.8(a), when the load current switches

Figure 5.8: (a) Upper Boundary V_H Shift to V_{HH} by A 400mA Up-Step Loading, and (b) Lower Boundary V_L Shift to V_{LL} by A 400mA Down-Step Loading.

Figure 5.9: Transient Response Without(w/o) and With(w/) The Proposed Auxiliary Circuit.

from 100mA to 500mA, the power stage inductor current is fully charged because the undershoot of output voltage causes the upper boundary V_H shifting to V_{HH} simultaneously. Similar in Fig. 5.8(b), when the load current switches from 500mA to 100mA, the power stage inductor current is fully discharged because the output voltage overshoot cause the lower boundary V_L shifting to V_{LL} simultaneously. The switching frequency f_{sw} , which is indicated by duty ratio signal D , is interrupted initially, and takes about $5\mu s$ to reach the “lock” condition again.

Fig. 5.9 shows the transient response performance with and without the proposed auxiliary circuit, and the magnified views of the graph are shown in Fig. 5.10 and Fig. 5.11. When the transient detection circuit and auxiliary circuit are disabled, the transient recovery time is at about $2\mu s$ for both the step-up load and step-down load. The undershoot and overshoot are about 200mV. When they are enabled(ENB), the transient recovery time is at about $0.3\mu s$ and $0.4\mu s$ for the step-up load and step-down load, respectively. The undershoot and overshoot are reduced to about 60mV. Based on the comparison, Fig. 5.9 clearly clarifies that the proposed auxiliary circuit helps to reduce the transient recovery time.

Fig. 5.12 summarizes the power conversion efficiency with the input supply voltages chosen to be 3V, 3.3V, and 3.9V, respectively. With a loading range from 30mA to 600mA, a peak efficiency of about 91% is achieved at 200mA with an input supply voltage of 3V. At light load condition, the power conversion loss is dominated by gate drive loss; at heavy load condition, the power conversion loss is dominated by transistor conduction loss. Fig. 5.13 shows the chip layout of the buck converter with an area of $1.3\text{mm} \times 1.2\text{mm}$. Table 5.2 provides the performance comparison with the state-of-the-art works, especially the design mentioned in chapter 4.

Figure 5.10: Magnified Graph of Fig 5.9 (a) Up-Step Loading Without(w/o) The Proposed Auxiliary Circuit, and (b) Down-Step Loading Without(w/o) The Proposed Auxiliary Circuit.

Figure 5.11: Magnified Graph of Fig 5.9 (a) Up-Step Loading With(w/) The Proposed Auxiliary Circuit, and (b) Down-Step Loading With(w/) The Proposed Auxiliary Circuit.

Figure 5.12: Power Conversion Efficiency.

Table 5.2: Performance Comparison with Prior Designs

	[4.28]TPEL'18	Design I	This Work(simulated)
Fsw stabling technology	COT & PWT	Adapt.Hyst. Window	Adapt.Hyst. Window
Technology(μm)	0.028	0.18	0.18
Chip Size(mm^2)	2.5	0.81	1.56
Inductor(μH)	1	0.5	0.5
Capacitor(μF)	4.7	0.47	0.47
Fsw(MHz)	2.5	8-10	6.5-11.5
Vin(V)	3.3	3-4.2	3-4.2
Vout(V)	1.05	2.4	1.8
Max. Load(mA)	1700	600	600
Load Step(mA)	1400	500	500
Offset(mV)	4	18	14
Tran-recovery(μs) Up/Step	4/5	2/1.8	0.3/0.4
Undershoot/ Overshoot(mV)	75/90	200/180	60/60
Peak Efficiency(%)	94	90	91
$FOM_1 = \frac{L \cdot \Delta I_{load} \cdot 100}{C_{OUT} \cdot F_{SW} \cdot T_R}$	2.96	3.69	27.3
$FOM_2 = \frac{L \cdot \Delta I_{load} \cdot 1000}{C_{OUT} \cdot F_{SW} \cdot T_R \cdot V_{offset}}$	7.39	2.05	19.5

Figure 5.13: Chip Layout.

5.5 Summary

A fixed-frequency hysteretic buck converter with novel adaptive hysteretic window control and transient response enhancement circuits was proposed and discussed. A PLL was utilized to maintain the power stage switching frequency at 10MHz. With the above-mentioned topologies, the transient recovery times were improved from $2\mu\text{s}$ to $0.3\mu\text{s}$. With the same output filter components, the undershoot and overshoot were reduced from 200mV to about 60mV, which would benefit low voltage applications. Furthermore, the fixed switching frequency with a $\pm 1\%$ variation error can be easily adopted in multi-phase DC-DC converter applications to achieve phase interleaving.

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Chapter 6

Conclusions and Future Works

In this chapter, an overall conclusion of all the designs proposed in this research project is drawn. Besides, a brief discussion for the future direction of this research project is also presented.

6.1 Conclusions

This research project was conducted mainly focusing on improving the performance of the integrated switching-inductor mode DC-DC converter that targets for different applications, especially for modern portable devices. The background information about conventional converter structures and their corresponding control methods were reviewed. Besides, compensation techniques were also discussed for system stability concern. By analyzing the advantages and disadvantages among all the conventional control methods, new control methods are proposed.

In the beginning, a PWM DC-DC converter works in Discontinuous-Conduction-Mode (DCM) was successfully conducted. The system structure is much simpler than that of DC-DC converter with hybrid mode control. A zero-voltage detector (ZVD) is typically used for DCM operation to avoid inductor current reverse conduction. Two major categories of comparators used for zero-voltage detection, including an operational-transconductance-amplifier (OTA) structure based continuous-time comparator and a switch-capacitor (SC) structure based discontinuous-time comparator, were discussed. Concerning of their drawbacks, a novel ZVD with a pre-amplification stage was proposed in this buck converter. When compared to the conventional continuous-time comparator, faster voltage sensing and comparing activities were realized; when compared to the conventional discontinuous-time comparator, a lesser power hungry clock signal was generated and devices matching issues were avoided. With the proposed ZVD, the time delay of sensing and comparing activities was only about 6ns, and a power conversion efficiency >85% was achieved over a loading range from 10mA to 250mA.

Subsequently, in order to be compatible with the development of modern DC-DC regulators, a high-speed DC-DC buck converter with hysteretic non-linear control method was proposed and implemented because the conventional control methods that based on linear control mechanism might not be the best options when dealing with frequently switched loadings. The major drawback of the conventional hysteretic control methods was its varied switching frequency. As a result, switching frequency locking property was introduced in the proposed design. By utilizing a phase lock loop (PLL) to control an adjustable current source, the switching frequency was locked to the desired reference value. The proposed adjustable current source controlled by the PLL changed the hysteretic window adaptively and thus realized a frequency locking range about several

MHz. This hysteretic control method with frequency locking ability was called fixed-switching frequency hysteretic control. In addition, a transient detection circuit was proposed particularly for this design to improve the transient response performance as well as the output voltage regulation. The proposed design was fabricated using $0.18\mu\text{m}$ CMOS process, and its switching frequency was maintained at 10MHz with less than $\pm 1\%$ variations. The transient recovery time was about $2\mu\text{s}$. A peak power efficiency about 91% was achieved over a loading range from 100mA to 600mA.

Last but not least, although the fixed-frequency hysteretic control method proposed in chapter 4 achieved a fast transient response by a transient detection circuit, its transient response performance was still limited by the gain and the bandwidth of the proposed transient detection circuit. In one hand, the gain and the bandwidth were constrained by the values of the feedback R_{fb} - C_{fb} networks. In another hand, the values of R_{fb} and C_{fb} were the two major parameters used to determine the switching frequency f_{sw} , so their values to be chosen were very limited. Hence the gain and the bandwidth might not be optimized although a PLL was used for switching frequency tuning within a certain frequency range. In consequence, the transient response performance might not be optimized and needed to be further improved by adding in other techniques. Concerning of the trade-offs, another fixed-frequency hysteretic controlled buck converter design with adaptive hysteretic window control was proposed in chapter 5, and an auxiliary circuit was proposed to compensate the drawbacks of the transient detection circuit as presented in chapter 4. The transient recovery times were further shorten to less than $0.4\mu\text{s}$.

6.2 Future Works

The proposed fixed-frequency hysteretic controlled buck converter in chapter 4 have been proved on silicon, so this part of the project has been fully completed. However, due to the long cycle time associated with IC design, the PWM DCM DC-DC buck converter proposed in chapter 3 and the second design of the fixed-frequency hysteretic controlled buck converter are yet to be completed, allowing future works to be proposed as follows:

In chapter 3, simulation results demonstrate that the proposed zero-voltage detector (ZVD) cause a sensing and comparison delay only about 6ns, and a peak efficiency of 94.2% was achieved. The proposed design has been sent for taping out in $0.18\mu\text{m}$ CMOS technology, and the layout graph is shown in Fig. 3.16. Silicon measurements need to be done in the future once it is ready for testing.

In chapter 5, the simulation results shown in Fig. 5.9, Fig. 5.10, and Fig. 5.11 have clarified that the transient response performance has been greatly improved by the proposed auxiliary transient detection circuit. Besides, switching frequency locking capability was also achieved with adaptive hysteretic window control method. Similarly, the proposed design has been sent for taping out in $0.18\mu\text{m}$ CMOS technology, and the layout graph is shown in Fig. 5.13. Silicon measurements need to be done in the future once it is ready for testing.

As for fixed-frequency hysteretic controlled DC-DC regulators proposed in this research project, the most potential use is to work as a unit cell of multiphase-interleaved DC-DC Converters, which is one of the developing trends about DC-DC converters.

Hysteretic control methods ensure excellent dynamic performance, and fixed switching frequency makes the multiphase interleaving operation become possible. When compared with its single-phase DC-DC converter counterpart, the multiphase-interleaved DC-DC converter applications brought in many advantages including larger current drive capability, smaller output ripple voltage at the same switching frequency, and the redundancy property for loading range tuning. However, new challenges are also brought in by multiphase-interleaved applications. The most crucial one among them is the current sharing issue for each phase [6.1]. Some previous works with different current sharing methods were retrieved [6.2]-[6.6]. So the future direction of this research project could be utilizing the proposed fixed-frequency hysteretic control topologies for multiphase-interleaved DC-DC regulator applications, and better current sharing method can be investigated at the same time.

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