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2018

Chew, P. S., Ma, K., Kong, Z. H., & Yeo, K. S. (2018). Miniaturized wideband coupler for 60-GHz band in 65-nm CMOS technology. *IEEE Microwave and Wireless Components Letters*, 28(12), 1089-1091. doi:10.1109/LMWC.2018.2875351

<https://hdl.handle.net/10356/102639>

<https://doi.org/10.1109/LMWC.2018.2875351>

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Miniaturized Wideband Coupler for 60GHz Band in 65nm CMOS Technology

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Abstract— A compact and wideband coupler for the 60GHz frequency band applications using 65nm CMOS technology is presented. By meandering the coupled-line, a miniaturized coupler can be obtained. The proposed coupler achieves a measured insertion loss between the input port and through port (S21) of 6.3dB and between the input port and the coupled port (S31) of 5.6dB at 60GHz. The measured amplitude imbalance and phase difference are 0.75dB and 92° respectively at 60GHz. Overall, the proposed coupler can achieve a measured amplitude imbalance of <1dB phase imbalance of <4°, return loss and isolation better than 13dB and 20dB respectively from 50 – 67GHz. In addition, the proposed coupler occupies a core area of only 156um x 157um (0.024mm²).

Index Terms—Coupler, 60GHz, Millimeter-wave.

I. INTRODUCTION

BROADBAND hybrid couplers are one of the most fundamental passive components in microwave circuits. They are used to combine/divide signals with phase difference of 90° and are widely used in power amplifiers, phase shifters [1] and six-port receivers [2]. Typically, there are two major forms of configuration namely branch-line configuration [3] and the coupled-line configuration [4], each with their own pros and cons. The branch-line configuration is simple but relatively large in size due to the usage of four $\lambda/4$ transmission lines, whereas for the coupled-line configuration, it requires multi-layer realization which is not available in some of the CMOS technologies.

The growing demand for high data rate applications in the millimeter-wave as well as the availability of 7-9GHz unlicensed 60GHz band [5] has created significant interest in developing low-cost 60GHz wireless communications systems. In addition to the high data rate, the radio systems need to be compact as well to be attractive to consumers. Numerous designs of the coupler in the literature [6-8] are based on the branch-line configuration. However, the enormous size of the branch-line couplers is limited by the four quarter-wavelength

Fig. 1 Configuration of coupled-line coupler

transmission lines. Therefore, it is important to reduce the size of the couplers to increase the level of system integration as well as reduce the fabrication cost. Several techniques such as meander elevated coplanar waveguide (ECPW) [6], loaded elevated-center coplanar waveguide (EC-CPW) [7] and slow wave CPW [8] can reduce the area for the branch-line couplers to 0.08mm², 0.102mm² and 0.083mm² respectively were reported.

In this letter, we present a very compact hybrid coupler using the coupled-line configuration [4] which can be operated throughout a very wide range of frequencies from 50 to 67GHz. The proposed coupler can achieve a measured amplitude imbalance of <1dB, phase imbalance of <4°, return loss and isolation of better than 13dB and 20dB respectively from 50 – 67GHz. By meandering the coupled-line, the proposed coupler is achieved with a compact core area of only 0.024mm² (156umx157um).

II. DESIGN OF COUPLER

In this letter, we present an inductively-coupled circuit based on the coupled-line configuration. By equating the transmission line and lumped component models in Fig. 1a and 1b respectively, the values for L_s , M , C_g and C_m can be derived [9]. The size can be optimized by making C_g and C_m to be part of the parasitic capacitance of the coupler.

Manuscript received January 31, 2018, accepted September 22, 2018.

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Fig. 2 The proposed coupler

In [10], by introducing a transformer coupling coefficient, k

$$L_s = \frac{Z_o}{\omega_o} \frac{\alpha}{k\sqrt{1-\alpha^2}} \quad (1)$$

where Z_o is the characteristic impedance, ω_o is the design frequency and the coupling factor, α is 0.707. From (1), the inductance can be reduced with a higher k and smaller inductance means that the area of the inductor will be reduced. The transformer coupling coefficient, k is chosen to be 0.73 to have a compromise between the amplitude and phase imbalance. To further reduce the area of the proposed coupler, the coupler is formed by stacking two metal layers.

The proposed coupler was implemented in 65nm CMOS technology that consists of nine metal layers. The two metal layers, OI and EA with 3.3 μ m and 0.9 μ m thickness respectively are used for the design of the proposed coupler due to the high conductivity compared to other metal layers shown in Fig.2a. The gap between the two metal layers is 0.6 μ m. In Fig.2b and 2c, the secondary and primary coils are constructed with both OI and EA metals, each with half a turn, such that the structure is symmetrical. The structure need to be symmetrical such that when the input is excited at either Port 1 (Input/Isolated) or Port 4 (Isolated/Input), the proposed coupler will perform its intended function as shown in the S-parameter matrix below [3]

$$[S]_{90^\circ} = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \quad (2)$$

The primary and secondary are meandered to make the whole design very compact. ANSYS High Frequency Structure Simulator (HFSS) V.15 is used to design the proposed coupler.

Fig. 3 Simulated and measured transmission (S_{21} and S_{31})

Fig. 4 Simulated and measured return losses and isolation

Fig. 5 Simulated and measured phase difference and amplitude imbalance

III. MEASUREMENT RESULTS

The measurement is performed on-chip using Agilent N5247 PNA-X network analyzer and Cascade Elite 300 probe station. The measured data of the proposed design are shown in Fig.3 – Fig. 5. In Fig.3, the measured insertion loss between the input port and through port (S21) is 6.3dB and between the input port and the coupled port (S31) is 5.6dB at 60GHz. From Fig.3, it can be seen that there is 1.5-2dB difference between the simulated and the measured results. Part of the loss is due to the interconnects, which contribute to 0.7dB loss as simulated in HFSS, to the pad required for measurement purpose. The remaining loss is due to the dummies created during the fabrication as the inductor mark was not drawn in the layout to prevent the dummies creation. The measured isolation and return loss are better than 20dB and 13dB respectively from 50 to 67GHz as depicted in Fig.4. The measured amplitude imbalance and phase difference are 0.75dB and 92° respectively at 60GHz. Fig.5 shows that the measured phase difference ranges from 89° to 94° from 30 to 67GHz and measured amplitude imbalance is less than 1dB from 51 to 67GHz. Fig.6 depicts the micrograph of the proposed coupler. The proposed coupler occupies a compact core area of 0.024mm² (156umx157um). Table I compares this work with other CMOS hybrid coupler operating at the 60GHz band. From the table, it can be seen that the proposed design can achieve a large bandwidth and compact size as compared with the state of art designs. The return loss, isolation, amplitude and phase imbalance are comparable with, if not better than the designs in the literature.

IV. CONCLUSION

In this letter, a miniature 60GHz wideband coupler fabricated in a 65nm CMOS process is presented. The proposed coupler has achieved an amplitude imbalance of <1dB, phase imbalance of <4°, return loss and isolation better than 13dB and 20dB respectively from 50 – 67GHz with a compact area of 0.024mm². The measurement results have validated its usage for wireless applications at 60GHz with high data rate.

ACKNOWLEDGMENT

The authors would like thanks to GlobalFoundries team for their helps in the fabrication and Mr. Li Chen Yang for his help in measurement.

REFERENCES

- [1] Y. Yu, P. G. M. Baltus, and A. H. M. v. Roermund, "Integrated 60GHz RF Beamforming in CMOS," (Springer Science+Business Media B.V., New York, 2011).
- [2] F. M. Ghannouchi and A. Mohammadi, "The Six-Port Technique With Microwave and Wireless Applications," (ARTECH HOUSE, Norwood, MA, 2009).
- [3] D. M. Pozar, "Microwave Engineering," (John Wiley & Sons, Inc., New York 2011, Fourth Edition).
- [4] R. K. Mongia, I. J. Bahl, P. Bhartia, and J. Hong, "RF and Microwave Coupled-Line Circuits," (ARTECH HOUSE, Norwood, MA, 2007, 2nd Edition).

TABLE I: SUMMARY OF 60GHz COUPLERS IN CMOS TECHNOLOGY

Ref.	[11]*	[12]	[13]*	This Work
Technology	65nm CMOS	90nm CMOS	130nm CMOS	65nm CMOS
Frequency (GHz)	58 - 67	50 - 67	54 - 66	50 - 67
IL (dB)	4 @60GHz	4 @60GHz	4.1 @60GHz	5.2 - 6.5
Δ Amp (dB)	<0.5	<0.3	<2	<1
Δ Phase (°)	<0.5	<3	<1	<4
RL (dB)	>27	-	>13	>13
Isolation (dB)	>20	-	>10	>20
Area (mm ²)	0.034	0.038	0.015	0.024

* - EM simulation results

Fig. 6 Micrograph of the proposed coupler

- [5] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: prospects and future directions," *IEEE Communications Magazine*, vol. 40, pp. 140-147, 2002.
- [6] K. Hettak, R. E. Amaya, and G. A. Morin, "A novel compact three-dimensional CMOS branch-line coupler using the meandering ECPW, TFMS, and buried micro coaxial technologies at 60 GHz," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, 2010, pp. 1576-1579.
- [7] I. Haroun, J. Wight, C. Plett, and A. Fathy, "Experimental characterization of EC-CPW transmission lines and passive components for 60-GHz CMOS radios," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, 2010, pp. 1-1.
- [8] C. Y. Kuo, A. Y. K. Chen, C. M. Lee, and C. H. Luo, "Miniature 60 GHz slow-wave CPW branch-line coupler using 90 nm digital CMOS process," *Electronics Letters*, vol. 47, pp. 924-925, 2011.
- [9] J. Hogerheiden, M. Ciminera, and G. Jue, "Improved planar spiral transformer theory applied to a miniature lumped element quadrature hybrid," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, pp. 543-545, 1997.
- [10] T. Y. Chin, J. C. Wu, S. F. Chang, and C. C. Chang, "Compact S-/Ka-Band CMOS Quadrature Hybrids With High Phase Balance Based on Multilayer Transformer Over-Coupling Technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, pp. 708-715, 2009.
- [11] C. Deyun, S. Yang, Y. Hao, and R. Junyan, "Design of Ultra-Low-Power 60-GHz Direct-Conversion Receivers in 65-nm CMOS," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, pp. 3360-3372, 2013.
- [12] T. Nakatani, T. Shima, and J. Sato, "Small and low-loss quadrature hybrid and T/R local signal selection switch for 60 GHz direct conversion transceivers," in *2013 IEEE 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2013, pp. 3-5.
- [13] T. W. Li and H. Wang, "A Millimeter-Wave Fully Integrated Passive Reflection-Type Phase Shifter With Transformer-Based Multi-Resonance Loads for 360° Phase Shifting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, pp. 1406-1419, 2018.