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A 0.058 mm² 13 Gb/s inductorless analog equalizer with low frequency equalization compensating 15 dB channel loss

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This letter presents an inductorless 13 Gb/s analog equalizer with an additional low frequency equalization (LFEQ) to counter the low frequency channel losses. An active feedback topology for the proposed equalizer together with negative capacitance circuit is used to extend the bandwidth to compensate a 15 dB channel loss at Nyquist. The LFEQ improves the measured data jitter of the conventional equalizer from 0.41 UI to 0.12 UI, for a pseudorandom binary sequence (PRBS) of 2³¹-1. The proposed prototype was implemented in 65 nm CMOS, occupying active area of merely 0.058 mm². It exhibits a power efficiency of 1.07 mW/Gb/s under a supply voltage of 1.2 V and a BER < 10⁻¹².

Introduction: Due to the demand for wide bandwidth at data rate of tens of Gb/s, inductive peaking [1] for the analog equalizers is commonly used in the wireline receivers. However, the passive inductors result in large area, thus making the overall solution not suitable for compact on-chip wireline solutions. Conventional linear equalizers [2-5] also tend to overlook the low frequency losses from the cable, owing to smooth slope of the low frequency losses compared to the sharp slope of high frequency losses. However, as the eye measurement extends over several UI, the long-term inter-symbol interferences (ISIs) caused by the low frequency losses result in increased data jitter.

The proposed analog equalizer implements an intermediate to high frequency equalization, while providing an additional LFEQ to counter the long-term ISIs. Bandwidth improvement in the absence of inductive peaking is achieved by an active feedback [6] topology as well as through capacitance reduction at the output, via a negative capacitance (NC) circuit [7]. The fixed LFEQ in the active feedback creates a zero-pole pair at low frequencies and thus, counters the low frequency channel losses resulting in an improved transient performance over long measurement samples.

Analog Equalizer Cell: The proposed equalizing cell (Fig.1) consists of a continuous time linear equalizer (CTLE), a fixed LFEQ and a NC circuit. The CTLE comprises of a transconductance stage which is source degenerated with a resistor (R_{s1}) and a varactor (C_s), which are tuned by two voltage controls, V_{c,R} and V_{c,Cs} respectively. The second stage of the equalizing cell uses an active feedback for bandwidth extension in the absence of inductive loading as well as provides a fixed equalization in the lower and wider frequency range with minimal peaking.

Fig. 1. Schematic of the proposed equalizing cell

The variable RC-degeneration in the first stage (Fig. 1) provides the dc gain and high frequency peaking, without an inductive load. The variable gain boosting is realized by varying the resistive degeneration. As V_{c,R} increases, the source node of M₁ gets increasingly degenerated with a reduced R_{s1}, leading to an overall increase in the dc gain. The zero and the poles of the CTLE are given in (1). ω_{z1} is decided by the degeneration elements, R_{s1} and C_s. C_s primarily decides the location of ω_{p1} , for a given bias current of the differential stage. R_{L1} and the effective load capacitance, C_{L1} as seen by the CTLE output, decide ω_{p2} .

$$\omega_{z1} \approx \frac{1}{R_{s1}C_s} \quad \omega_{p1} \approx \frac{g_{m1}}{C_s} \quad \omega_{p2} \approx \frac{1}{R_{L1}C_{L1}} \quad (1)$$

For the proposed 13 Gb/s equalizer with variable digital filter, the zero-pole pair of the CTLE has to be restricted around the frequency range of 1 to 6.5 GHz, to target the intermediate and high frequency losses in the cable. This brings in the necessity of additionally equalizing the low frequency losses.

The LFEQ is based on an active feedback topology. Unlike the resistive feedback techniques, the unilateral feedback in the active feedback prevents trade-off between feedback strength and open-loop gain. The second stage (Fig. 1) introduces a fixed LFEQ targeting the gentle slope of the low frequency loss of the channel and provides a zero-pole pair at lower frequencies, with a wider bandwidth. The zero for the second stage is decided by R_f-C_f pair, as shown by (2). $\omega_{z1-fb} - \omega_{p1-fb}$ pair are placed together by designing the feedback gain accordingly as shown in (3), where C_{L2} is the total parasitic capacitance at the output node (V_{op}). While the high frequency equalization requires that the zero and pole of the CTLE to be restricted to frequencies in the range of 1 to 6.5 GHz, the low frequency equalizing stage is designed to have a zero around 250 MHz. Additionally, it can be noted that, the feedback topology, which is implemented as a differential pair (M₄) lowers the feedback factor at higher frequencies, thus improving the gain-bandwidth product. The zero and the poles of the LFEQ are given as

$$\omega_{z1-fb} \approx \frac{1}{R_f C_f} \quad \omega_{p2-fb} \approx \frac{1}{R_{L2} C_{L2}} \quad (2)$$

$$\omega_{p1-fb} \approx \frac{1}{R_f C_f} \left(1 + \frac{g_{m2} R_{L2} g_{m3} R_{L3} g_{m4} R_{L1}}{1 + 0.5 g_{m3} R_{S3}} \right) \quad (3)$$

The NC circuit is used to further improve the bandwidth by effective capacitance reduction at the output of the second stage in the equalizing cell. It can be modelled as a combination of negative capacitance and negative resistance. The stability of this positive feedback loop is guaranteed by ensuring that the bias currents are smaller compared to the second stage bias current.

Fig. 2. Measured channel loss (a) and simulated frequency responses in the presence of channel (b) of the conventional equalizer and the proposed equalizer with LFEQ.

Top-level architecture: An inductorless analog equalizer is designed by cascading two proposed equalizing cells in Fig. 1. A limiting amplifier follows two cascaded stages of the equalizing cell, to vary the signal swing at the overall equalizer output, towards impedance matching. The limiting amplifier does not worsen the data jitter performance at the equalizer output. Different tuning voltages used in the equalizing filter help in independent tuning of the dc gain and the high frequency peaking.

Considering the measured channel loss (Fig. 2a), which shows a loss of ~15 dB at 6.5 GHz, the equalized frequency response is shown in Fig. 2b. The LFEQ stage in each of the equalizing cell provides a gain of ~2.8 dB. The improvement in the simulated frequency response of the overall equalizer, for the lower frequencies starting at ~250 MHz in the presence of the channel with LFEQ is demonstrated in Fig. 2b.

The frequency responses of the overall linear equalizer were simulated to verify the tunability of V_{c,R} (Fig. 3a) and V_{c,Cs} (Fig. 3b). When V_{c,Cs} = 1.0 V, the overall gain variation is up to 15 dB. The zeros shift towards higher frequency as V_{c,Cs} decreases under the fixed V_{c,R}. For the time-domain response, the effect of LFEQ is seen as an improved jitter performance. The parasitic annotated simulations of the overall equalizer show that the peak-to-peak data jitter improved from 25 ps of that of a conventional equalizer to 6.5 ps with the proposed equalizer.

Fig. 3. Simulated frequency response of the proposed analog equalizer
a With $V_{c,R}$
b With $V_{c,Cs}$

Measurement Results: The proposed prototype was fabricated in 65 nm CMOS with a compact active area of 0.058 mm², as shown in the die photograph with zoomed-in layout (Fig. 4). The measurement setup for the prototype consists of the probe station, the serial J-BERT (N4903B) and oscilloscope (Agilent 86100A).

Fig. 4. Die photo with zoomed-in layout

The eye diagrams at the output of the conventional CTLE without LFEQ (Fig. 5a) and at the output of the proposed equalizer with LFEQ (Fig. 5b) at 13 Gb/s are shown for a 2³¹-1 PRBS input pattern, with >1.3k input samples. The pk-to-pk data jitter shows a marked improvement from 32 ps (0.41 UI) in the conventional CTLE to 9.34 ps (0.12 UI) in the proposed equalizer with an eye height of 185 mVpp. The design achieves a measured horizontal eye opening of 0.66 UI at BER < 10⁻¹². The total active power consumption is 14 mW under a supply voltage of 1.2 V, resulting in a figure of merit (FOM) of 0.071 pJ/bit/dB. Table 1 summarizes the die performance and the comparison with the prior art.

Fig. 5. Measured 13 Gb/s eye diagrams
a Conventional CTLE without LFEQ
b Proposed equalizer with LFEQ

	[1]	[4]	[5]	This Work
Data rate (Gb/s)	10	10	8.5-13	13
Technology (CMOS)	130 nm	45 nm	28 nm	65 nm
Supply (V)	1.2	1.1	1.0	1.2
Channel loss @ Nyquist (dB)	12	15	35	15
Inductor load	Yes	No	No	No
Area(mm ²)	0.35	-	0.22	0.058
Horizontal Eye* (UI) / BER	0.36 / -	0.68 / -	0.62 / 10 ⁻¹²	0.66 / 10 ⁻¹²
Power Efficiency (mW/Gb/s)	0.41	1.43	3.8	1.07
FOM (pJ/bit/dB)	0.034	0.095	0.108	0.071

*Measured from the eye diagram

Conclusion: This letter has reported an inductorless analog equalizer with the LFEQ. Fabricated in 65 nm CMOS, the prototype exhibits a FOM of 0.071 pJ/bit/dB at 13 Gb/s and an ultra-compact active area of 0.058 mm². The proposed equalizer reduces the equalized data jitter from 0.41 UI to 0.12 UI for 15 dB channel loss against a conventional linear equalizer.

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