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An Asynchronous Sub-Two-Step Quantizer for Continuous-Time Sigma-Delta Modulators

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***Abstract*—This paper presents an asynchronous sub-two-step circuit architecture to reduce the complexity and power consumption of internal analog-to-digital converter (quantizer) for Continuous-Time Sigma-Delta Modulator (CTSDM). By using the proposed new circuit topology, only 1/3 of comparators for a 5-bit quantizer design are needed when compared with the conventional flash based counterpart. The proposed quantizer has been implemented and fabricated in a UMC 65-nm CMOS process. The measured results have shown that the quantizer consumes 0.59 mW at an operating frequency of 250 MS/s in a 1.2 V supply and achieves 28.82 dB SNDR (4.5 ENOB) from the output spectrum.**

I. INTRODUCTION

Continuous-Time Sigma-Delta Modulator (CTSDM) is popular in wireless applications since it offers high bandwidth data conversion with low power consumption [1-3]. To achieve a high resolution for a wideband signal, increasing the filter's order or the sampling clock frequency (i.e., a high oversampling ratio (OSR)) is not preferred because these approaches require more demanding circuit requirements, which lead to higher power consumption [4].

Alternatively, a multibit quantizer could be adopted to allow more aggressive noise shaping, thus increasing the effective resolution [2]. As shown in Fig. 1, the single-loop multibit CTSDM structure contains a loop filter, a multibit quantizer and a multibit DAC. The conventional implementation of the quantizer is a flash ADC due to its fast response. However, each extra bit calls for doubling the number of comparators in a flash based quantizer [3, 5-7] leading to large area as well as power consumption [1, 2]. Therefore, several quantizer structures like tracking ADC [1], successive approximation ADC [2, 8], asynchronous sequential binary search ADC [4] have been adopted into quantizer designs.

However, these alternatives have their own limitations. For tracking ADC [1] design, the signal slope must be smaller than its internal feedback signal slope which thereby limits the SDM input frequency at certain over-sampling ratio (OSR). Besides, the noise transfer function gain must be smaller than 2 dB to ensure a time domain signal with fluctuation less than 1 LSB. This sacrifices some noise shaping response, thus reducing the merit of multibit quantization [1, 4]. For synchronous SAR ADC [2] design, due to its time interleave property, both high speed internal sampling clock and sample-and-hold (*S/H*) circuits are required to finish the quantization in specified period of time. The asynchronous SAR ADC [8] design eliminates the high

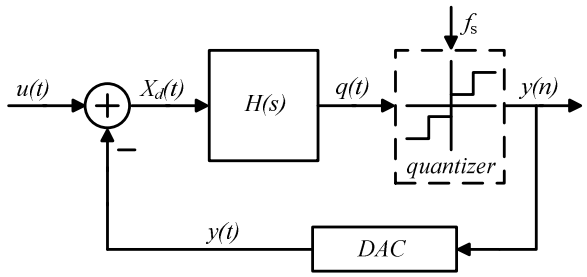

Fig. 1. Structure of continuous-time sigma-delta modulator.

frequency DLL, but the internal capacitor array consumes large silicon area and power, especially under high frequency switching. This limits its sampling frequencies. For the asynchronous sequential binary search ADC [4] design, it has a very low power consumption with only n comparators being switched on for an n-bit design. However, same as SAR ADC [2, 8], it gives the quantization outputs bit-by-bit. This requires a long time to finish the whole process, limiting the sampling frequency or the OSR of SDM. Meanwhile, a large quantizer delay, which contributes to the excess loop delay (ELD) of the SDM, may cause instability of the system [5].

In view of that, a low-power sub-two-step quantizer for CTSDM applications is proposed. It utilizes a reference switching scheme with reduced number of comparators such that the area and power consumptions are reduced significantly. Meanwhile, one step timing plus one step internal asynchronous control time interval is adopted to avoid high frequency clock generation and reduce the quantization time. Owing to the new structure with small latency in conjunction with its internal high-speed comparators, the quantization time can be made approximately 1.5 times as that of the flash quantizer.

II. QUANTIZER STRUCTURE

The proposed quantizer structure and its control signal waveforms are depicted in Fig. 2(a) and Fig. 2(b), respectively. The quantizer comprises a clock generator, a passive S/H circuit, two stages of comparator bank, a range detection circuit, a reference switching block and a resistor ladder. The resistor ladder is equally partitioned into 8 ranges with 4 reference values in each range. The 1st stage contains 7 dynamic comparators whereas the 2nd stage contains 3 static comparators. Due to its simple reference switching structure, the proposed sub-two-step quantizer eliminates the residue subtractor and the feedback DAC

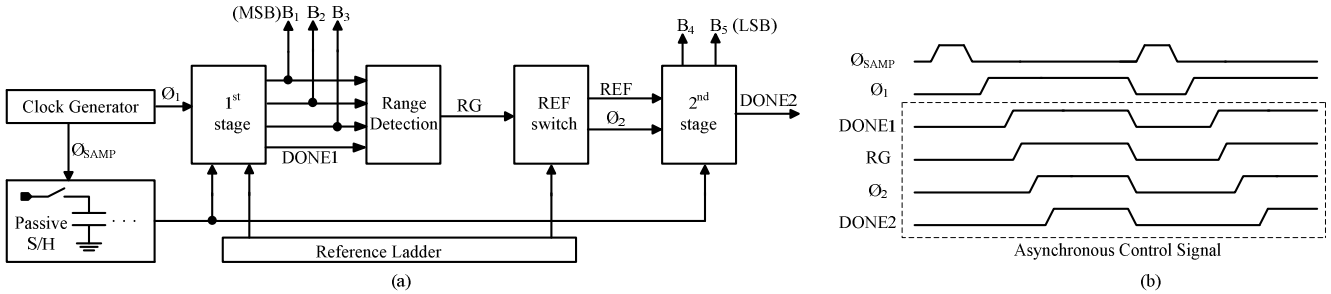

Fig. 2. (a) Structure of proposed quantizer (b) Clock generation and asynchronous control signal diagram.

which are used in the conventional two-step synchronous ADC. Moreover, it utilizes the dynamic and static comparators for the respective 1st and 2nd step conversion with an asynchronous control for the 2nd step conversion. As such, a good optimization of accuracy, speed, and power consumption can be achieved.

As shown in Fig. 2(b), the working principle and the signal flow of the quantizer are explained in the following. After the S/H circuit samples the input signal, the generated clock $Ø_1$ is asserted to turn on the 1st stage comparators. The 1st stage outputs are then passed to the range detection block when all the comparators have finished its comparison (DONE1 changes to high). The logic inside the ranges detection block gives the range of the input signal quickly and changes the reference voltages for the 2nd stage accordingly. After a small delay to permit the reference voltages of the 2nd stage comparators settle down, the 2nd stage control signal is then turned on ($Ø_2$ changes to high) to give the last two bits of the quantization outputs. Another done signal (DONE2) for the 2nd stage is also generated to indicate that the quantizer has already completed the quantization process.

Through the new scheme, the number of comparators is reduced to 10 for a 5-bit quantizer design. This leads a good compromise between conversion time and power consumption. It is important to note that both the area and power consumption are reduced approximately by 2/3 in context of the 5-bit flash based quantizer counterpart as a reference. The quantizer's conversion time is much smaller than that of the sequential designs [2, 4].

III. Circuit Implementation

The following sections describe the circuits being implemented in the 5-bit quantizer.

A. Dynamic Comparator

To avoid a large capacitive loading for the resistor ladder, a four-input comparator structure is used. The 1st stage employs a four-input sense amplifier based dynamic comparator [9] as shown in Fig. 3. The comparator displays low power consumption as well as high speed characteristic.

When CLK is asserted, the four input transistors are turned on and discharge (A, B) and (C, D) at different rate which gives a small voltage difference between them. The regenerative latch amplifies the difference and gives a full swing output at VOP and VON. Before the comparator is used, the offset of the comparator is calibrated using a binary weighted capacitor array (CAL CAPs in Fig. 3). At calibration mode, VP and VN are shorted to VRP and VRN respectively. The capacitor array is steered to one direction at the initial calibration stage to deliberately generate a large initial offset. During calibration, a digital counter changes the direction of the switch until the output polarity changes. In this design, a 6 bit counter is adopted such that it could calibrate a large offset voltage range with a small calibration LSB size. As such, the accuracy of the comparator operation is guaranteed.

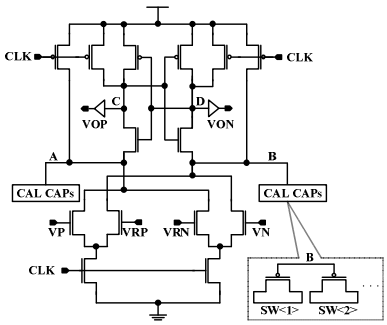

Fig. 3. Dynamic Comparator implemented in 1st stage.

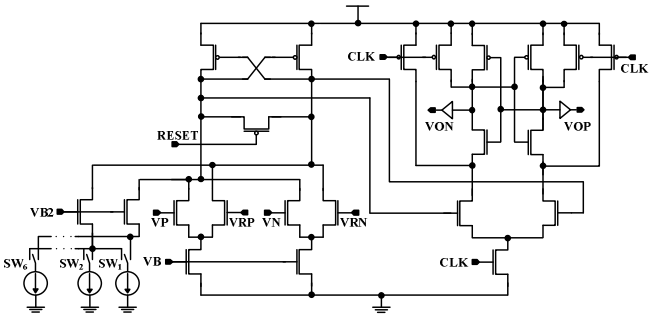

Fig. 4. Static comparator implemented in 2nd stage.

B. Static Comparator

Since the reference voltage of the 2nd stage comparators are switching along with the input signal change. A comparator with offset insensitive to input and reference voltages is used. The comparator shown in Fig. 4 exhibits less offset variation than that of the dynamic comparator implemented in 1st stage since the bias current is fixed. It contains a high gain preamplifier and a two-input sense amplifier based latch. When the RESET signal changes to high, the pre-amplifier amplifies the difference between the input and reference voltage and gives a large input

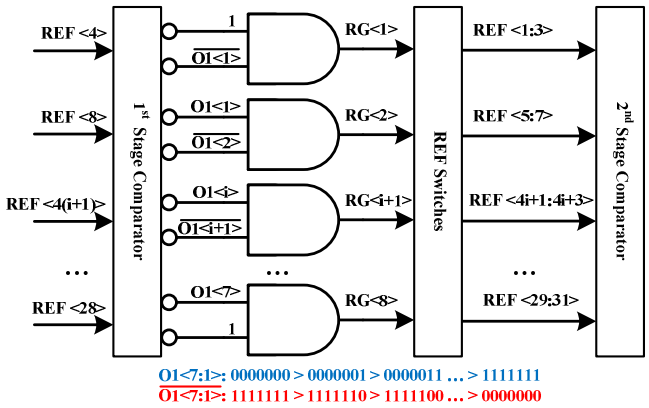

Fig. 5 Range detection and reference switching mechanism.

voltage difference for the 2nd stage. After a short delay (around 200ps), the 2nd stage is turned on. It generates a full swing digital output code within a short period of time. Same to the dynamic comparator, the offset of the static comparator is also calibrated by using a binary weighted current source array [10]. The calibration process is the same as that of the dynamic comparator in 1st stage.

C. Range Detection and Reference Switching Matrix

Since the outputs of the 1st stage comparators are in thermal code format, the range detection circuit consists of eight two-input AND gates only. Based on the range signal output, the reference switching matrix will connects the respective reference voltage to the 2nd stage comparator's input. The control mechanism can be explained using Fig. 5. Due to the oversampling and the multibit quantization features in the CTSDM, the input to the quantizer changes slowly (normally smaller than 1 LSB for one cycle). Thus the range and reference signals switch slowly as well. Added with the simple circuit implementation, the power consumption of the range detection and the reference switching matrix is small.

D. Passive S/H Circuit

To ensure that the two comparator banks having the same input voltage whilst not limiting the slew rate of the input signal as in [4], a distributed passive S/H circuit is implemented for each comparator. This method also reduces the effect of the kick back noise since all the comparators are not sharing the input voltages. Because the offset of each comparator has been calibrated by the offset calibration circuit, small input transistors can be used for the comparator which allows a small sampling capacitor. This will also reduce the driving requirement of the integrator (or summation circuit) inside CTSDM [11], thus reducing the power consumption of the modulator ultimately.

IV. Measurement Results

The proposed 5-bit quantizer has been fabricated in a UMC 65-nm CMOS process with a 1.2 V supply. The measurement results have validated that the proposed quantizer can operate with 4.5 bit at 250 MS/s whilst consuming 0.59 mW of power.

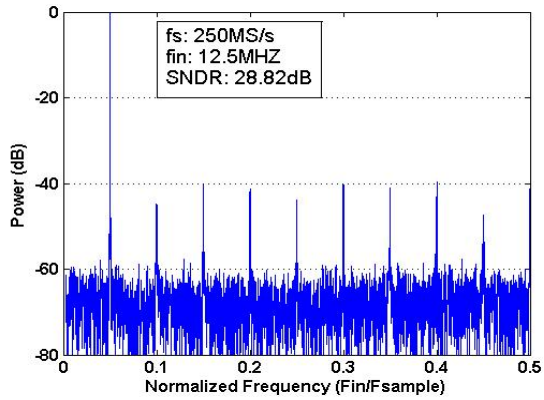

Fig. 6. FFT spectrum with 12.5MHz input (OSR = 10).

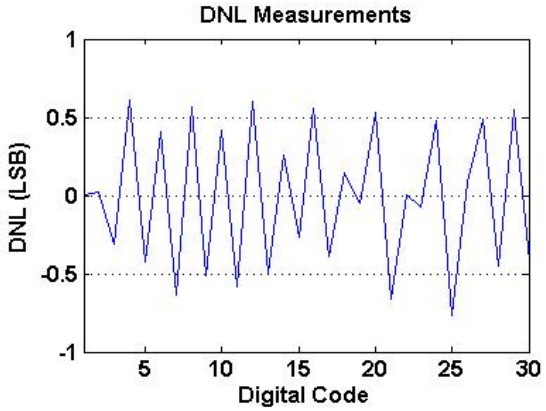

Fig. 7. DNL plot of the proposed quantizer.

The analog part, digital part and resistor ladder dissipate 0.26 mW, 0.21 mW, and 0.12 mW respectively. Excluding the input sampling time, the conversion process consumes less than 1.5 ns which is only 37.5% of the clock period. Fig. 6 shows the FFT plot at 12.5 MHz input frequency (OSR = 10). It gives a SNDR of 28.82 dB (4.5 ENOB). The DNL and INL of the quantizer are measured as 0.8 LSB and 0.6 LSB and shown in Fig. 7 and Fig. 8, respectively. The performance figures are not of major concern because the nonlinearity of quantizer is divided by the gain of preceding integrators [11]. As such, the DNL and INL requirements become relaxed in this 5-bit qunatizer design.

The microphotograph of the proposed quantizer is shown in Fig. 9. The active area (enclosed by dash line) of the core quantizer is 0.052 mm^2, which excludes the output buffer for tapping the internal signals for testing purpose. Table I summarizes the performance of the proposed work with respect to the reported designs. It is given that the parameter R defines the number of equivalent steps with respect to the flash based quantizer which serves as the benchmark. For larger value of R, the power consumption and delay of the quantizer will be large on the basis of identical sampling frequency. It is vice versa for small R value. FoM_1 is the conventional Figure-of-Merit whereas FoM_2 includes the factor R that takes into account of

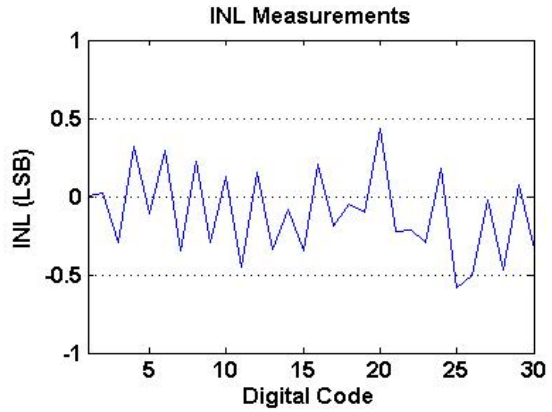

Fig. 8. INL plot of the proposed quantizer.

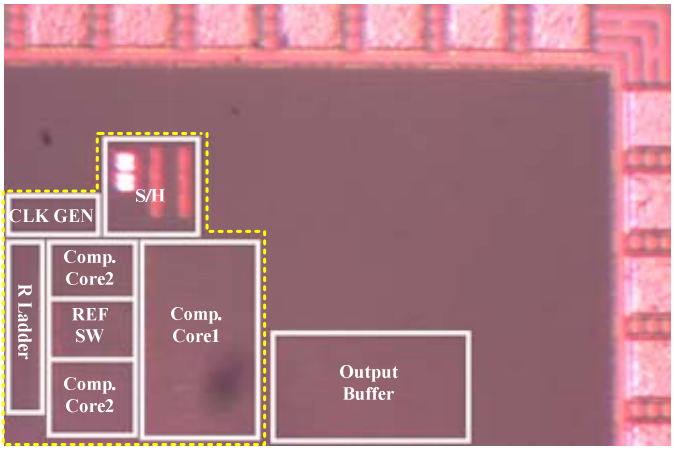

Fig. 9. Microphotograph of the proposed quantizer.

the quantization delay. The formulae of the FOMs are given as follows:

$$FoM_1 = Power/ (f_s * 2^{\wedge ENOB})$$

$$FoM_2 = Power*R/ (f_s * 2^{\wedge ENOB})$$

As can be seen from the table, the proposed work gives better or comparable performance metrics when compared with the state-of-the-art quantizer designs, suggesting the energy efficiency of the proposed quantizer suitable for high-speed low OSR CTSDM.

V. Conclusion

A 5-bit 250 MS/s asynchronous sub-two-step quantizer has been proposed and implemented in 65-nm CMOS process. It reduces the number of comparators to 1/3 of the conventional flash based counterpart. To get an optimized power efficiency and accuracy, a combination of dynamic and static comparators together with respective calibration circuit is realized in this structure. The measurement results have demonstrated that the energy efficiency of the proposed quantizer. It is useful for high-speed low OSR CTSDM design.

TABLE I PERFORMANCE SUMMARY

Parameter	[1]	[2]	[4]	[7]	[8]	This work
Structure	Tracking	Syn. SAR	Asyn. Seq	Flash	Asyn. SAR	**Asyn.S2S**
Process	0.13µm	0.13µm	90nm	90nm	40nm	**65nm**
ENOB(bit)	4*	5*	4*	4*	6*	**4.5**
f_s (MHz)	104	184.32	60	500	65	**250**
Step (R)	1†	6	~5	1	1.5	**1.52**
Power (mW)	0.4	1.3	N.A	3	0.36	**0.59**
FoM_1 (fJ/conv.)	240.4	220.4	N.A	375	86.5	**104.3**
FoM_2 (fJ/conv.)	240.4	1322.4	N.A	375	129.8	**158.5**

*assume that the reported quantizer has achieved full ENOB
†assume that the input signal has been tracked by the quantizer

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