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2013

Cai, D., Shang, Y., Yu, H., & Ren, J. (2013). Design of ultra-low-power 60-GHz direct-conversion receivers in 65-nm CMOS. *IEEE Transactions on Microwave Theory and Techniques*, 61(9), 3360-3372.

<https://hdl.handle.net/10356/103285>

<https://doi.org/10.1109/TMTT.2013.2268738>

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Design of Ultra-Low-Power 60-GHz Direct-Conversion Receivers in 65-nm CMOS

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Abstract—This paper has explored an ultra-low-power design of two 60-GHz direct-conversion receivers in a 65-nm CMOS process for single-channel and multi-channel applications under the IEEE 802.15.3c standard, respectively. One subthreshold biasing 0.4-V transconductance mixer is designed with a compact quadrature hybrid coupler ($160\ \mu\text{m} \times 210\ \mu\text{m}$ with measured 3-dB intrinsic loss) in receivers to achieve low power (8 mW for single channel and 12.4 mW for multi-channel) and high gain (55 dB for single channel and 62-dB for multi-channel). One three-stage low-noise amplifier employs high- Q passive matchings. A double-layer-stacked inductor is utilized for matching in the single-channel receiver and a high-impedance transmission line is utilized for matching in the multi-channel receiver, respectively. In addition, one new modified Cherry–Hooper amplifier is applied for the variable-gain amplifier design to achieve high gain-bandwidth product and high power efficiency. The single-channel receiver is implemented with 0.34-mm^2 chip area. It is measured with a power consumption of 8 mW, a minimum single-sideband noise figure (NF) of 4.9 dB, a 3-dB bandwidth of 3.5 GHz, and a maximum conversion gain of 55 dB. The multi-channel receiver is implemented with 0.56-mm^2 chip area. It is measured with a power consumption of 12.4 mW, a 3-dB bandwidth of 8 GHz (59.5~67.5 GHz), and a maximum conversion gain of 62 dB. The measurement results show that the two demonstrated 60-GHz direct-conversion receivers can achieve high gain and low NF with ultra-low power in 65-nm CMOS.

Index Terms—CMOS 65 nm, direct-conversion receiver, quadrature hybrid coupler, 60 GHz, ultra-low power.

I. INTRODUCTION

THE 7-GHz unlicensed band at 60 GHz has resulted in active research in CMOS integrated circuits (ICs) for high data-rate wireless communication systems. In 60-GHz transceiver designs [1]–[12], the receiver front-end is a critical block that amplifies a small RF signal from the antenna and converts it down to baseband under a specified signal-to-noise ratio. In order to achieve high-order modulation with efficient bandwidth utilization with desired communication range, the receiver must satisfy design specifications of high gain, high linearity, and

low noise figure (NF), which introduces significant expense in terms of power overhead [4]. Furthermore, due to the high path loss at 60 GHz, the phased-array beam-forming techniques with multiple transmitters and receivers [8] can further increase the power consumption with the multiplication number in the receiver array such that it is of great importance to design each receiver with low power in such a phase-arrayed system.

There are commonly two architectures for the 60-GHz receiver. One is direct conversion and the other is heterodyne. Compared to the heterodyne receiver, the direct-conversion receiver has a lower power requirement due to simpler structure with less building blocks. As such, direct-conversion receivers have been explored in 60 GHz [2], [3], [5], [6], [13], [14], which includes key building blocks such as the low-noise amplifier (LNA), mixer, variable-gain amplifier (VGA), and baseband. Moreover, many studies [2], [3], [6], [13], [14] assume one branch direct-conversion receiver. In [1] and [4], two in-phase/quadrature (I/Q) branches are deployed in a 60-GHz transceiver with quadrature phase-shift keying (QPSK) modulation for higher spectrum efficiency at the cost of more power. For simplicity of demonstration, one branch direct-conversion receiver is considered in this paper, which can be easily extended for two I/Q branches.

The primary interest here is thereby to investigate the tradeoff between power consumption and performance, such as gain and NF, during the design of direct-conversion receiver. In order to reduce the total power consumption and achieve a high gain with low NF at 60 GHz, building blocks in the receiver, including the LNA, mixer, and VGA, need to be designed for low power. Low-power design techniques, such as the use of high- Q and compact passive devices and transistors operated at the subthreshold region, have to be explored for the direct-conversion receiver design at 60 GHz. A low-power one-branch 60-GHz receiver in 65-nm CMOS was reported in [14]. Due to 2-D passive g_m -enhancement, it can achieve a high gain without sacrificing extra power in the LNA. However, the LNA in [14] cannot cover a wide bandwidth in 60 GHz and the following Gilbert mixer contributes high power to the whole receiver. A 60-GHz mixer with quadrature hybrid coupler was presented in [15] to achieve low power with the subthreshold biasing. However, the quadrature hybrid consumes a large area with additional expense for the full-chip integration.

Two ultra-low power, yet low NF and high-gain direct-conversion receivers are demonstrated in this paper at 60 GHz in 65-nm CMOS. One single-channel receiver that covers one band in (59.4 ~ 61.56 GHz) according to the IEEE 802.15.3c standard [16] can achieve low power and also low NF. The other multi-channel receiver is designed to cover three bands in (59.4 ~

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802.15.3c standard [16], which can achieve low power and also high gain. ($160 \mu\text{m} \times 210 \mu\text{m}$ with measured 3-dB intrinsic loss). The transistors in the mixer are biased at subthreshold region to achieve low power and high gain. One three-stage LNA is employed with high- Q passives for matching. A double-layer-stacked inductor is utilized for matching in the single-channel receiver and a high-impedance transmission line (T-line) is utilized for matching in the multi-channel receiver, respectively. Furthermore, one VGA is designed for two cases with one new modified Cherry-Hooper amplifier, which can achieve high gain-bandwidth product and high power efficiency. Both receivers are demonstrated in 65-nm CMOS with measurements. The single-channel receiver consumes 8 mW and occupies a core area of 0.34 mm^2 . The measurement results show that it achieves the minimum single-sideband (SSB) NF of 4.9 dB, the 3-dB bandwidth of 3.5 GHz, and the maximum conversion gain of 55 dB. The multi-channel receiver consumes 12.4 mW and occupies a core area of 0.56 mm^2 . The measurement results show that it achieves the 3-dB bandwidth of 8 GHz (59.5~67.5 GHz), and the maximum conversion gain of 62 dB.

This paper is organized as follows. Section II introduces the overview for architecture and design considerations of the ultra-low-power 60-GHz CMOS direct-conversion receiver. Section III presents details of low-power designs for the LNA, mixer, and VGA with analysis. The implementation and measurement results are shown and discussed in Section III. Conclusions are drawn in Section IV.

II. 60-GHz DIRECT-CONVERSION RECEIVER

The direct-conversion transceiver architecture is commonly deployed for the transceiver design for portable devices with advantages such as high selectivity, simple structure, and low implementation cost. In this section, ultra-low-power design perspectives for 60-GHz direct-conversion architecture are discussed.

A. Channelization of 60-GHz High-Data-Rate Communication

According to the IEEE 802.15.3c standard [16], there are four 2.16-GHz bands commonly allocated for the 60-GHz high-data-rate communication system, as depicted in Fig. 1. In spite of the difference for permitted channels in different countries, two common global channels (2 and 3) are available during the early standardization of 60-GHz systems. The center frequencies of channels 2 and 3 are located at 60.48 and 62.64 GHz, respectively. The frequency range of channel 2 is from 59.4 to 61.56 GHz, and the frequency range of channel 3 is from 61.56 to 63.72 GHz. The front-end designs such as the LNA and power amplifier (PA) are required to cover all four bands in the 60-GHz wireless communication system. Generally, one device with wider bandwidth consumes more energy. The power consumption of a 60-GHz wireless communication system covering the multi-channel would consume much higher power than that of the single-channel counterpart. For application of portable devices with battery power limitation, it requires a more energy-efficient solution to only operate at one channel or single

Fig. 1. Channelization of 60-GHz high-data-rate wireless communication system under IEEE 802.15.3c standard.

channel. As such, the 60-GHz receivers in this paper will address both single- and multi-channel receiver designs based on the IEEE 802.15.3c standard mentioned above. For example, the single-channel receiver in this paper is designed with 3-dB bandwidth from 59.4 to 61.56 GHz (channel 2); and the multi-channel receiver in this paper is designed with 3-dB bandwidth from 59.4 to 65.88 GHz (channels 2–4).

B. Architecture and Design Considerations

Compared to the heterodyne receiver, the direct-conversion receiver has no additional frequency planning for resolving the image problem. This can result in simplified integration with lower power consumption. However, the direct-conversion receiver needs to address the issues of dc offset, I/Q mismatch, and LO leakage. Note that the design of ultra-low power 60-GHz receiver needs to consider the power consumption of the phase-locked loop (PLL) [17], which includes a voltage-controlled oscillator (VCO) [18], [19], divider, charge pump, etc. An ultra-low power 60-GHz PLL has been demonstrated in [20] for the direct-conversion receiver. This is beyond the scope of this paper and will be addressed in our future work. In addition, for a phase-arrayed transceiver architecture, it can include many receivers with a much larger power budget than one PLL.

A high-gain and ultra-low power 60-GHz direct-conversion receiver architecture is demonstrated in this paper, as shown in Fig. 2. It consists of a three-stage common source (CS) LNA, a transconductance mixer with an on-chip compact quadrature hybrid coupler, and a four-stage VGA. To achieve low power, but also high gain, compact and high- Q on-chip passive devices are extensively utilized to boost the gain and to match the interface between different blocks as follows. Similar to [1]–[3], a single-ended LNA is selected in our design instead of the differential one. The differential LNA may result in better NF, but it may also double the power consumption. Once the designed single-ended LNA can achieve a low NF for 60-GHz application, it is selected for the low-power consideration. Here the common source with inductive-degeneration topology is deployed to achieve simultaneous noise and power matching at the first stage. In single-channel operation, inductor-based

Fig. 2. Architecture of 60-GHz direct conversion receiver.

matching is utilized, while T-line based matching is utilized in multi-channel operation. For the single-channel LNA, a high- Q inductor can reduce the area and the loss of the matching network. For the multi-channel LNA, the T-line based approach can achieve wider bandwidth.

Moreover, one new transconductance mixer is proposed in this paper for high gain and low power. Compared to the commonly used Gilbert-cell mixer [21] with transistors biased at the saturation region, the transconductance mixer with transistors biased at the subthreshold region can significantly reduce the power consumption while maintaining the required conversion gain. The transconductance mixer requires a quadrature hybrid coupler to convert the single-ended RF input to a differential IF output with a single-ended LO signal. Generally, the quadrature hybrid coupler is realized by T-line sections with lengths in $\lambda/4$ at the center frequency, which consumes large area. To reduce the area, this paper introduces a compact transformer-based quadrature hybrid coupler, which can be modeled by a coupled T-line structure. Compared to the $\lambda/4$ T-line, our design has smaller phase mismatch over wideband and all four ports can be matched to Z_0 simultaneously with good isolation between LO and RF ports. Moreover, the input matching in the mixer is designed between the quadrature hybrid and nMOS transistors to avoid the gain reduction and the feed-through from LO to RF.

In addition, a new modified Cherry-Hooper amplifier is applied during the VGA design, working as the core amplifier stage to achieve high gain-bandwidth product. Compared to the VGA in [22], the proposed control in our design has much better power efficiency. Since it can be directly connected to a power detector for automatic gain control, the power consumption of additional control circuits can be further reduced. Note that dc-offset cancellation and source-follower feedback are also applied for gain and bandwidth enhancement, respectively.

Note that a source-follower buffer is designed to drive off-chip 50- Ω terminations without the need for output matching.

The system performance can be estimated by the following equations. The total gain of the receiver (G_{tot}) is given by

$$G_{\text{tot}} = G_{\text{lna}} G_{\text{mix}} G_{\text{vga}} \quad (1)$$

where G_{lna} , G_{mix} , and G_{vga} denote the gain of the LNA, mixer, and VGA, respectively. Each component design with a high gain results in a high gain for the whole receiver. However, the matching between the LNA, mixer, and VGA needs to be designed carefully. For example, the output impedance of the LNA has to be designed to 50 Ω to match the input hybrid coupler of mixer. The output signals of the mixer need to be ac coupled to the input of VGA or the first stage of the VGA cannot work normally.

Moreover, the total NF of the receiver (NF_{tot}) is calculated as

$$\text{NF}_{\text{tot}} = 1 + (\text{NF}_{\text{lna}} - 1) + \frac{\text{NF}_{\text{mix}} - 1}{G_{\text{lna}}} + \frac{\text{NF}_{\text{vga}} - 1}{G_{\text{lna}} G_{\text{mix}}} \quad (2)$$

where NF_{lna} , NF_{mix} , and NF_{vga} denote the NF of the LNA, mixer, and VGA, respectively. Equation (2) indicates that the noise contributed by each stage decreases as the gain of preceding the stage increases, implying that the LNA in a receiver is the most critical for the NF. To minimize the NF, CS topology [23] is utilized in the LNA. Furthermore, both source degeneration and optimum current density are applied in the LNA to reduce the NF.

III. DESIGN OF LOW-POWER CIRCUIT BLOCKS

In this section, the circuit design of low power with high performance for the 60-GHz direct-conversion receiver is discussed. The building blocks such as LNA, mixer, and VGA are illustrated in detail one by one starting with the LNA.

Fig. 3. Study of 65-nm CMOS technologies for simultaneous noise and power matching with source degeneration in CS amplification topology.

A. Low-Power LNA

As shown in (2), the overall NF of the direct-conversion receiver is mainly determined by the LNA. The key challenge for LNA design is to reduce the power consumption without affecting the LNA performance such as NF and gain. One can achieve this requirement by exploring the design of both active and passive devices as follows.

1) *Three-Stage LNA*: In a 65-nm CMOS process at 60 GHz, CS topology can achieve the lowest NF and highest gain [24], [25]. The NF of one CS stage consisting of a parallel resistor R_p with respect to a source resistance R_s is given by

$$\text{NF} = 1 + \frac{R_s}{R_p}. \quad (3)$$

The NF can be minimized by maximizing R_p . However, the maximum power transfer is achieved when R_s is equal to R_p . Thus, it is difficult for the CS stage to achieve simultaneous noise and power matching. Inductive degeneration can be used to address this issue, where an inductor is inserted between the source terminal of the nMOS transistor and ground. Fig. 3 illustrates the simulated optimum reflection coefficient for the minimum NF and the input S_{11} for different combinations of number of fingers (individual finger width of $1 \mu\text{m}$) with respect to the degeneration inductor and 65-nm nMOS transistor in the CS. One can observe that simultaneous noise and power matching can be achieved by searching the matched sizes of the transistor and degeneration inductor. The optimized values are shown in Figs. 5 and 6.

Moreover, in order to minimize the power consumption, one needs to reduce the size of the transistor. Usually the current density of transistors is fixed first to design an LNA with the optimum gain and NF [26]. Note that the dc current of an LNA is proportional to the transistor size. As depicted in Fig. 4(a) and (b), the $\text{NF}_{\min}$ and the available gain are almost independent of transistor size when the degeneration inductor is very small. This reveals the possibility to design a low-noise and high-gain LNA with small-size nMOS transistors ($10 \mu\text{m}$)

Fig. 4. Design exploration of CS topology with inductive degeneration in 65-nm CMOS process for: (a) $\text{NF}_{\min}$ and (b) available power gain when $S_{11} = \Gamma_{\text{opt}}^*$.

Fig. 5. Schematic of single-channel LNA design with high- Q dual-layer inductor matching.

such that the power consumption can be reduced. In addition, when the degeneration inductor value is increased, both $\text{NF}_{\min}$ and the available gain will drop at the same time. As such, inductive degeneration is suitable to be applied for the first stages that are noise sensitive, but is not suitable for the later stages that are gain demanding.

For the single-channel case, the schematic of the single-ended three-stage LNA is shown in Fig. 5(a). CS with inductive-degeneration topology is used for M1 to have a lower NF in the first stage, and CS without degeneration is used for M2 and M3 to have higher gain. The current consumption can be reduced by the transistor size reduction [23]. The transistor size is chosen to be $10 \mu\text{m}$ in the single-channel case. As only one band is targeted, the power consumption is extremely small.

For the multi-channel case, a single-ended three-stage LNA design is shown in Fig. 6. The structure is similar to the single-channel LNA design, except for the matching network. What is the most important point here is that the NF in Fig. 6 is larger than the single-channel LNA design above due to the extend of the bandwidth. In this multi-channel case, $30 \mu\text{m}$ is found to be an optimum nMOS transistor size when considering the tradeoff between the bandwidth and power in LNA design.

Fig. 6. Schematic of multi-channel LNA design with high- Q T-line matching.

2) *Single-Channel LNA With Matching by High- Q Dual-Layer Inductor*: For the 60-GHz single-channel LNA design, an inductor is deployed in the matching network. A high- Q inductor design is needed to reduce the area and the loss of the matching network. In order to improve the Q factor of the matching network, the design of dual-layer inductor is deployed. As shown in Fig. 5(b), the aluminum layer (AL) is stacked on the top-most copper layer (M6) for the design of matching inductor.

As verified by the EM simulation (ADS Momentum) with results shown in Fig. 5(c), the Q factor of the dual-layer inductor (15.5) is almost 50% higher than the one (10.5) of the single-layer inductor on M6 at 60 GHz when using the standard 65-nm CMOS process. The high- Q inductors are applied in the input/output stage and interstage matching. For the input and output matching, 210- and 150-pH inductors are applied, respectively. For the first and second stage matching, a 150-pH inductor is designed. For the second and third stage matching, a 140-pH inductor is employed.

The post-layout simulation results further show that the proposed LNA with inductor matching has 12-dB gain and 4.2-dB NF, and the measured power consumption is 5.4 mW. The bandwidth of the LNA is 3.5 GHz to cover one single channel from 59.4 ~ 61.56 GHz.

3) *Multi-Channel LNA With Matching by High-Impedance T-Line*: To achieve multi-channel amplification and NF reduction, a single-ended three-stage LNA design is further designed with the use of a high-impedance T-line (170 Ω) matching network [27], [28] as follows.

The well-known nodal quality factor Q_n can be used to describe the bandwidth of the LNA, which is expressed as

$$Q_n = \frac{2|\Gamma_i|}{1 - \Gamma_r^2 - \Gamma_i^2} \quad (4)$$

where Γ_i and Γ_r are the real and imaginary parts of the input reflection coefficient, respectively. A lower Q_n results in a larger bandwidth. As shown in Fig. 3 (red line in online version), when the Q_n value is decreased by increasing finger numbers of transistors, the bandwidth of the LNA is increased. In this case, a

small inductor value is needed in the matching network, which can be achieved by the use of the T-line.

Compared to the inductor-based matching network in the single-channel case above, the T-line-based approach has lower loss within wideband. As such, one can achieve high gain and wideband LNA by a T-line-based matching network. Moreover, it is of great importance to ensure the wideband inner stage stability, which is achieved by connecting a 2- Ω resistor to the decap in the drain bias network.

The post-layout simulation results show that the designed LNA has 15-dB gain and 9-mW power consumption. The bandwidth is extended to 30 GHz to cover all four bands from 57.24 ~ 65.88 GHz. However, the power consumption is increased by 3.6 mW at the same time because more bands are covered.

B. Transconductance Mixer With Compact Quadrature Hybrid Coupler

As the second important building block of the direct-conversion receiver, the design of the down-conversion mixer affects the receiver performance, such as conversion gain, NF, and power consumption. Conventionally, a Gilbert-cell mixer is used at 60 GHz for its compact size and low-cost implementation. As all transistors operate in the saturation region, and also a large LO-voltage swing required for the Gilbert mixer to enable an effective mixing, there is an excessive power dissipation in the mixer. For example, each Gilbert-cell mixer consumes relatively large power of around 18 mW at 60 GHz [21]. On the contrary, the transconductance mixer [29] has much smaller power consumption with maintained high conversion gain. The signal mixing behavior of a single-gate mixer is contributed by the nonlinear transistor biased at the subthreshold region with a large gain, but a low power. As such, the transconductance mixer is more suitable for low-power design at 60 GHz, and hence, is adapted in this paper for both single- and multi-channel cases.

However, one disadvantage of the transconductance mixer is the requirement of the quadrature hybrid coupler. Generally, quadrature hybrid couplers are realized by T-line sections with

Fig. 7. Layout of the compact quadrature hybrid coupler in transconductance mixer.

Fig. 8. Coupled T-line model of quadrature hybrid coupler.

lengths of $\lambda/4$ at the center frequency. As such, they are very difficult to implement on-chip due to the relatively large area [15], [30], [31].

1) *Compact Low-Loss Quadrature Hybrid Coupler*: The chip size of the quadrature hybrid coupler can be significantly reduced by using lumped elements instead of a $\lambda/4$ T-line. However, the output phase balance will be seriously degraded by the parasitic effects and losses in the CMOS process. The inductively and capacitively coupled hybrids are found having negative and positive phase errors, respectively [32]. The combination of the inductive coupling coefficient of the transformer and capacitive coupling across the transformer winding can significantly reduce the output phase error in CMOS components [33]. Based on this observation, a transformer-based quadrature hybrid coupler is introduced in this paper to mix the LO and RF signals feeding the nMOS transistor. A compact quadrature hybrid coupler is realized with the area of $160 \mu\text{m} \times 210 \mu\text{m}$, as shown in Fig. 7. It can reduce the chip area with nine times reduction than the meander-line coupler used in [15].

As shown in Fig. 8, the quadrature hybrid coupler can be modeled by a coupled T-line structure. When excited at port 1, the output voltage V_3 and V_4 can be expressed as

$$\begin{aligned} V_3 &= V \frac{jC \tan \theta}{\sqrt{1 - C^2} + j \tan \theta} \\ V_4 &= V \frac{\sqrt{1 - C^2}}{\sqrt{1 - C^2} \cos \theta + j \sin \theta} \end{aligned} \quad (5)$$

where C is the coupling factor shown as follows:

$$C = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}}. \quad (6)$$

Comparing V_4 and V_3 , one can reach

$$\frac{V_4}{V_3} = \frac{\sqrt{1 - C^2}}{jC \sin \theta}. \quad (7)$$

Fig. 9. (a) S -parameter of quadrature hybrid coupler. (b) Magnitude and phase mismatch between Port 2 and Port 3 of quadrature hybrid coupler.

Equation (7) shows that the coupler always has 90° phase difference between ports 3 and 4, independent of the coupling factor (C) and coupler length (θ). As such, it has smaller phase mismatch over a wideband frequency region when compared to the $\lambda/4$ T-line. As such, all four ports can be matched to Z_0 simultaneously with good isolation achieved between LO and RF ports.

In addition, assuming the magnitude of V_3 is equal to V_4 , one can reach

$$C = \frac{1}{\sqrt{1 + \sin^2 \theta}}. \quad (8)$$

As such, in order to have a small coupler length (θ) for compact design, the coupling factor (C) is designed as large as possible to achieve the magnitude matching.

The electromagnetic (EM) simulation results (ADS Momentum) of the proposed quadrature hybrid coupler are given in Fig. 9(a). It is shown that all ports of the coupler are matched to $50\text{-}\Omega$ impedance, and the RF/LO isolation is more than 20 dB from 20 to 100 GHz. As Fig. 9(b) shows, the magnitude and phase mismatch between Port 2 and Port 3 are less than 0.5 dB and 0.5° in the frequency range of interest ($58 \sim 67$ GHz), respectively. After applying the transconductance mixer with the proposed compact quadrature-hybrid coupler, both the chip area and power consumption of the mixer are largely reduced. Compared to the use of the meander-line coupler ($490 \mu\text{m} \times 600 \mu\text{m}$) [15], nine times area reduction is achieved in this paper with the reduced mismatch of magnitude and phase.

2) *Transconductance Mixer*: As shown in Fig. 2, the transconductance mixer that incorporates the RF and LO signal on-chip combining is selected for the 60-GHz direct-conversion receiver in this paper. For the active mixing design, a single nMOS transistor biased in the strongly nonlinear region at subthreshold is used to improve conversion gain with reduced power. In addition, LO-to-IF feed-through is high due to the unbalanced operation of the LO. Thus, to improve LO-to-IF isolation, the $\lambda/4$ T-line LO short is employed at the drain of the nMOS transistor to terminate the LO. To save chip area, a resistive load, optimized for conversion gain and linearity, is used instead of the RF choke [15].

Note that the drain current of the single-gate mixer can be expressed as

Fig. 10. (a) Fourier coefficient a_0 of the transconductance (g_m) versus V_{GS} and figure width of nMOS transistor. (b) Fourier coefficient a_1 of the transconductance (g_m) versus gate-source voltage (V_{GS}) and amplitude of 60-GHz LO signal (V_{LO}).

$$I_d(t) = g_m(t)V_{RF}(t)$$

$$g_m(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega_{LO}t) \quad (9)$$

where a_n , $n = (0, 1, 2, \dots)$ are the Fourier coefficients of g_m with respect to ω_{LO} . It can be shown that a_0 and a_1 represent the fundamental transconductance and the first-order mixing product of $(\omega_{RF} - \omega_{LO})$, respectively.

The simulated Fourier coefficients a_0 and a_1 based on a 65-nm nMOS transistor are illustrated in Fig. 10(a) and (b). For the fundamental transconductance, the value of a_0 is increased with V_{GS} and transistor size, but for the first-order mixing product, the value of a_1 reaches its maximum well below the threshold voltage. This effect enables a low-power, yet high conversion-gain mixer designed in the 65-nm CMOS process at 60 GHz.

Moreover, the principle of the frequency mixing by the transconductance mixer is shown as follows. The output voltage of the mixer can be expressed as

$$V_{IFN}(t) = a_1 \cos(\omega_{LO}t) V_{RF} \cos\left(\omega_{RF}t + \frac{\pi}{2}\right) R_L$$

$$V_{IFP}(t) = a_1 \cos\left(\omega_{LO}t + \frac{\pi}{2}\right) V_{RF} \cos(\omega_{RF}t) R_L. \quad (10)$$

Since we only need to consider the first-order mixing product, (10) can then be rewritten as

$$V_{IFN}(t) = \frac{1}{2} a_1 V_{RF} \sin(\omega_{LO}t - \omega_{RF}t) R_L$$

$$V_{IFP}(t) = -\frac{1}{2} a_1 V_{RF} \sin(\omega_{LO}t - \omega_{RF}t) R_L \quad (11)$$

where R_L is the resistance of the resistive load.

As such, by using this structure, the single-ended input RF can be converted into differential IF output with a single-ended LO. The conversion gain is also related to the LO input power, and an optimized value can be chosen to achieve the highest conversion gain. From (11), the conversion gain is determined by a_1 , which depends on V_{GS} and transistor size shown in

Fig. 10. Thus, 0.4-V bias voltage is chosen and $16 \mu\text{m}$ is found to be an optimum nMOS transistor size in the mixer.

3) *Input Matching*: After the design of the quadrature hybrid coupler and transconductance mixer, there is an important issue of the matching network from the hybrid output to the input of the transistor. The four ports of the quadrature hybrid coupler are matched to 50Ω , while the input impedance of transistors is not 50Ω . The feed-through from the LO to RF will become serious without a matching network, and the conversion gain will also be reduced. Thus, it is important to design a matching network between the two.

As shown in Fig. 2, an inductor matching network instead of a T-line is explored in this paper for area saving. The series capacitance and the inductance are 100 fF and 300 pH, respectively. The parallel inductance is 100 pH. They can be implemented easily on chip. The inductors are implemented by a top layer metal and the capacitors are designed with metal-to-metal layers to reduce loss. The quadrature hybrid coupler and the matching network are both passive devices and can be simulated together in Agilent Technologies' Advanced Design System (ADS). With the use of the matching network, the feed-through can be reduced dramatically.

The S -parameters of the passive devices in the mixer are extracted using ADS and then imported into Cadence for co-simulation. In addition, parasitics of the active devices are extracted by PEX in Cadence. The post-layout simulation of the whole mixer is then done in a Cadence environment together with the S -parameters extracted from ADS. The simulation results show 6-dB conversion gain, 11-dB NF, and 22-dB LO-to-RF isolation with only 0.5-mW power consumption.

C. VGA With Modified Cherry-Hooper Amplifier

A wideband VGA is required in a 60-GHz wireless communication system for the wide range of gain control. The VGA design entails a challenging tradeoff among gain, bandwidth, tuning range, power, etc. Many of the published CMOS VGAs operate below 1 GHz with high power [22], [34], [35]. To increase the bandwidth, an on-chip peaking inductor has been utilized in the VGA design, but it consumes a large chip area [36]. In this work, we explore the design of a the Cherry-Hooper amplifier, which was first introduced in [37] with the following advantages. Firstly, it can provide high gain-bandwidth product without the extra supply voltage. Secondly, there is no additional chip area needed for inductively peaked gain stages by active or passive inductors. As such, the Cherry-Hooper amplifier is one choice for both power-efficient and chip-area-efficient VGA design for 60-GHz direct-conversion receiver.

In this paper, a modified Cherry-Hooper amplifier with gain control is proposed in the design of the main amplifier stage. A source-follower feedback and an additional feedback resistor for gain enhancement are also introduced. Furthermore, active feedback and inversely scaling techniques are employed as well to increase bandwidth instead of using the on-chip peaking inductor.

The developed VGA with amplifier gain-cells and dc-offset cancelling networks [38] is depicted in Fig. 11, and is deployed for both single- and multi-channel cases. Since a one-stage gain-

Fig. 11. Schematic of Cherry-Hooper amplifier-based low-power VGA design.

cell can only provide about 10-dB gain, a multi-stage gain-cell is needed. The developed VGA consists of four-stage gain-cells, a dc-offset cancellation circuit, and an output buffer. The four-stage gain-cells can afford sufficient voltage gain to increase the sensitivity. Moreover, the dc-offset cancellation circuit exhibits a negative feedback by the low-pass filter to eliminate the dc-offset voltage from device mismatch at 65 nm. A source-follower buffer is designed to drive off-chip 50- Ω termination without the need of output matching. Furthermore, low- V_t transistors are employed in all the CMOS transistors to relax the voltage headroom in the VGA.

Note that the gain-cell of the VGA shown in Fig. 11 is controlled by the external applied voltage VC over a wide-range of control or tuning. When the drain-source resistances of M7 and M9 are changed by VC , the gain of the VGA can be adjusted accordingly. For example, when VC is increased, the gain will be decreased with lower drain-source resistance of M7 and M9. The highest gain can be achieved when VC is equal to 0; and the lowest gain can be achieved when VC is equal to 1.2 V. However, when VC is equal to 0, the drain-source resistances of M7 and M9 will become very high, which makes the dc current close to 0. Thus, the gain-cell cannot work normally. To avoid such a problem, parallel resistors R_1 and R_3 are added to limit the highest resistance. When VC is equal to 0, the total parallel resistance is mainly determined by R_1 (R_3). When VC is equal to 1.2 V, the total parallel resistance is mainly determined by M7 (M9).

The simplified small-signal half circuit of the gain-cell [39] is shown in Fig. 12 along with the most significant parasitic elements. The small-signal gain of the gain-cell is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1} (R_3 \parallel R_{f9} + R_5) \left(R_1 \parallel R_{f7} + \frac{1}{g_{m11}} \right)}{2 \left(\frac{1}{g_{m5}} + R_5 \right)} \quad (12)$$

Fig. 12. Simplified small-signal half circuit of the gain-cell.

Fig. 13. Die photograph of transformer-based quadrature hybrid coupler.

where R_{f7} and R_{f9} are the drain-source resistances of M7 and M9, respectively. From (12), one can observe that a wide gain-tuning range can be easily achieved by changing R_{f7} and R_{f9} .

In addition, the bandwidth extension without extra chip area can be achieved by the following two techniques [38]. Firstly, inverse scaling of the input nMOS size for each gain-cell [40] reduces the load capacitance C_L of the next gain-cell stage, which further increases the overall bandwidth of the VGA under a lower power consumption. Secondly, the second feedback amplifier between VGA3 and VGA4 acts like an active negative feedback, which results in a higher gain bandwidth [41].

The post-layout simulation results show that the proposed VGA has the highest gain of 38- and 50-dB tuning range with 2.1-GHz bandwidth, while 50-dB gain-tuning range is achieved via adjusting VC from 0.7 to 1.2 V with 2-mW power consumption. Due to the limitation of R_{f7} and R_{f9} , the gain variation when adjusting VC from 0 to 0.7 V is small.

IV. SILICON IMPLEMENTATION AND MEASUREMENT RESULTS

A. Quadrature Hybrid Coupler

As shown in Fig. 13, the proposed quadrature hybrid coupler for the transconductance mixer is implemented in the standard

Fig. 14. Measured and simulated phase difference between ports 3 and 4 of the quadrature hybrid coupler.

Fig. 15. Isolation between ports 1 and 2 and magnitude at ports 3 and 4 of the quadrature hybrid coupler.

65-nm CMOS process to validate the phase and magnitude balance. The S -parameters were measured on a Cascade Microtech Elite-300 probe station and an Agilent PNA-X (N5247A) network analyzer with frequency sweeping up to 67 GHz.

The de-embedded measurement results of the proposed quadrature hybrid coupler are shown in Figs. 14 and 15, as well as the EM simulation results (ADS Momentum). The size is $160\ \mu\text{m} \times 210\ \mu\text{m}$, which is nine times smaller than the meander-line coupler ($490\ \mu\text{m} \times 600\ \mu\text{m}$) in [15]. One can also observe that all ports can be matched to $50\ \Omega$. The RF and LO isolation is more than 20 dB. The magnitude and phase mismatch between Port 3 and Port 4 are less than 1 dB and 2° over the whole 60-GHz band. Note that good impedance matching is ensured for four ports, of which the return-loss measurement results are greater than 16 dB.

B. Single-Channel Receiver

The single-channel (channel 2) 60-GHz direct-conversion receiver is fabricated in the UMC standard 65-nm CMOS process. It occupies 0.34-mm^2 chip area, of which a die photograph is shown in Fig. 16.

In order to connect external dc-control signals and high-frequency RF signals concurrently, the receiver chip is wire-bonded to an open cavity package and soldered to a

Fig. 16. Die photograph of single-channel 60-GHz direct-conversion receiver.

Fig. 17. Measurement setup of receivers.

printed circuit board (PCB). As shown in the measurement setup in Fig. 17, all analog control pins are connected to the digital-to-analog converters (DACs) on the PCB, which is externally controlled from a serial IO interface through an 8051 microcontroller. The RF, LO, and IF ports are connected through the CASCADE Microtech Elite-300 probe station. The Agilent PNA-X network analyzer N5247A is used for the conversion gain, NF, and S -parameter measurement. Note that cold-source method is utilized in the NF analysis.

The receiver operates with 1-V power supply with merely 8-mW power consumption excluding a testing buffer. The LNA, mixer, and VGA consume 5.5-, 0.5-, and 2-mW power according to the measurement, respectively. The receiver conversion gain, NF, and input S_{11} are measured when the LO power at the quadrature hybrid coupler input is set to $-3\ \text{dBm}$, and the measurement and simulation results are shown in Fig. 18. It is observed that the measured gain is around 3 dB lower than the simulation results, and the measured NF and S_{11} are quite close to the simulation results. The maximum gain of 55 dB in the measurement is located at 59.5, and 3.5-GHz bandwidth is obtained from 58.5 to 62 GHz. The minimum SSB NF of 4.9 dB is observed at 60.5 GHz and the NF is in the range of $5 \sim 7\ \text{dB}$ at $59 \sim 64\ \text{GHz}$. The maximum input

Fig. 18. Measured and simulated results: conversion gain, NF, and input S11 of single-channel direct conversion receiver.

Fig. 19. Measured results: (a) attenuation (dB) versus voltage of VGA gain control (VC) and (b) normalized conversion gain versus P_{out} .

Fig. 20. Die photograph of multi-channel 60-GHz direct-conversion receiver.

S11 of -8 dB implies good power matching at the receiver input. Furthermore, Fig. 19(a) depicts the attenuation control of the output signal power operation with VC voltage at different IF frequencies. The attenuation of the VGA increases almost linearly with VC in the operation range of $0.7 \sim 1.2$ V. A flat frequency response is monitored, as less than 3-dB variation of the attenuation level is monitored over different frequencies when VC is smaller than 1 V. In addition, the normalized conversion gain versus the output power (P_{out}) at different frequencies are shown in Fig. 19(b). The gain shown in Fig. 19(b) is normalized to the small-signal gain. The 1-dB gain compression point is clearly shown to be in the range of $-12.6 \sim -8.8$ dBm.

Fig. 21. Measured and simulated results: conversion gain, NF, and input S11 of multi-channel direct conversion receiver.

Fig. 22. Measured results: (a) attenuation (dB) versus voltage of VGA gain control (VC) and (b) IF bandwidth in IEEE 802.15.3c channels 2–4.

Fig. 23. Channel 3 measurement results: input/output P1 dB and NF of the multi-channel 60-GHz direct-conversion receiver.

C. Multi-Channel Receiver

The multi-channel (channels 2–4) direct-conversion receiver is fabricated in a GF standard 65-nm CMOS process. The die micrograph of the receiver is shown in Fig. 20 with a die area of 0.56 mm^2 (excluding pads), as well as the testing structure of the proposed transformer based quadrature hybrid coupler. Note that the same structures of the mixer and VGA are used in the two receivers. However, the experiment results of the two blocks will be slightly different. Furthermore, different from the single-channel receiver, the LNA in the multi-channel receiver is designed with the T-line matching network to broaden the bandwidth. In this multi-channel case, the receiver operates

TABLE I
STATE-OF-THE-ART 60-GHz CMOS RECEIVER PERFORMANCE COMPARISON

Parameters	Gain (dB)	NF (dB)	BW (GHz)	Power (mW)	Supply (V)	LO	CMOS Process	Area (mm ²)
[2]	55	6.1	4	24	1	Ext	65 nm	1.6
[3]	14.7	5.6	10	84	1	Ext	65 nm	0.12
[6]	18	9	9.8	50	1.8	Ext	130 nm	1.2
[14]	60	3.9	1	20	1	Ext	65 nm	0.2
[13]	-9.5	7	6.2	21.9	1.2	Int	130 nm	2
This work (Single-channel)	55	4.9	3.5	8	1	Ext	65 nm	0.34
This work (Multi-channel)	62	7.9	8	12.4	1	Ext	65 nm	0.56

with 1-V power supply with merely 12.4-mW power consumption excluding the testing buffer. The LNA, mixer, and VGA consume 9-, 0.5-, and 2.9-mW power according to the measurement, respectively.

The receiver conversion gain, NF, and input S_{11} are measured when the LO power at the quadrature hybrid coupler input is set to 0 dBm, and the measurement and simulation results are shown in Fig. 21. It is observed that the measured gain is around 3 ~ 6 dB lower than the simulation results in the 60-GHz band, and both the measured NF and S_{11} are slightly higher than the simulation results. The measured maximum gain of 62 dB located at 63- and 8-GHz bandwidth is obtained from 59.5 to 67.5 GHz. The minimum SSB NF of 7.9 dB is observed at 63 GHz and the NF is mostly in the range of 8 ~ 10 dB at 57 ~ 66 GHz. The NF of the multi-channel receiver is around 4 dB worse than the single-channel receiver, mainly due to the mismatch at the input of LNA stage, which is due to the deviation of transistor gate capacitance in the fabrication. The input matching of the receiver is shown in Fig. 21, which is below -4 dB for the entire 60-GHz band.

Furthermore, Fig. 22(a) depicts the attenuation control of the output signal power operation with VC voltage at different IF frequencies. One can observe that the receiver has a wide-gain tuning range of about 55 dB, which allows the system to operate in a wide dynamic range for input signals. The IF bandwidths of IEEE 802.15.3c channels 2-4 are shown in Fig. 22(b), and the 3-dB IF bandwidth is larger than the 1.08-GHz requirement from IEEE 802.15.3c, half of 2.16 GHz from direct conversion.

Large-signal performance of the multi-channel receiver at the center band and also its corresponding NF are shown in Fig. 23. At the minimum attenuation level, the output P1 dB is determined by the VGA, of which the measurement results are very close for both multi- and single-channel receivers due to the similar VGA design. As the attenuation level is increased, the nonlinearity inside the mixer and LNA becomes dominant so the output P1 dB drops as the VC is increased. On the other hand, the noise contribution from the VGA becomes larger so the NF is increased with VC . Moreover, due to the growing attenuation, the input P1 dB increases with VC , which can be used to obtain a wide dynamic range.

D. Performance Comparison

The proposed 60-GHz CMOS single- and multi-channel receivers are compared to several recently published one-branch 60-GHz direct-conversion receivers in Table I. For an effective and fair comparison, only the maximum gain and the minimum NF are listed, and the receiver power is shown excluding the

signal generation circuit (LO) and output buffer. Note that LO signals are mainly from external sources, except [13], which is from internal sources. The lowest power consumption of 8 mW is demonstrated by the proposed single-channel receiver with high gain (55 dB), low NF (4.9 dB), and sufficient wide bandwidth (3.5 GHz) for channel 2 operation. The highest power efficiency is demonstrated with the proposed multi-channel receiver, which shows the highest gain (62 dB), very low power consumption (12.4 mW), and wide bandwidth (8 GHz) for channels 2-4 in IEEE 802.15.3c 60-GHz standard. One can observe that the overall 8- and 12.4-mW power of the two proposed receivers are 3 ~ 6 times lower than all the rest of the receiver designs at 60 GHz. Moreover, compared to the previous studies in [2], [6], and [13], the proposed receivers show the highest conversion gain within the smallest chip area.

V. CONCLUSION

Two ultra-low power direct-conversion receivers with high gain and low NF have been presented in this paper for a 60-GHz wireless communication system in 65-nm CMOS. The power consumption of the proposed receiver is significantly reduced from low-power designs of each component such as LNAs, mixers, and VGAs. High- Q passive devices of dual-layer inductor matching and T-line matching are deployed in the design of single- and multi-channel LNAs, respectively. A compact quadrature hybrid coupler is utilized in the low-power design of the transconductance mixer. In addition, a modified Cherry-Hooper amplifier is used in the VGA for improved power efficiency and high gain as well.

There are four channels under the IEEE 802.15.3c standard for the 60-GHz wireless communication system. The first single-channel 60-GHz direct-conversion receiver with channel 2 is implemented with a 0.34-mm² chip area. The measured results show 8-mW power, the minimum SSB NF of 4.9 dB, and the maximum power conversion gain of 55 dB. The second multi-channel 60-GHz direct-conversion receiver with channels 2-4 is implemented with a 0.56-mm² chip area. It is measured with the power consumption of 12.4 mW, a 3-dB bandwidth of 8 GHz (59.5 ~ 67.5 GHz), and a maximum power conversion gain of 62 dB. Both of the proposed receivers have demonstrated ultra-low-power consumption around 10 mW, as anticipated, which enables a tremendous power reduction in the 60-GHz high-data-rate wireless communication system.

ACKNOWLEDGMENT

The authors appreciate the support from MediaTek for UMC 65-nm CMOS tape-out of the single-channel receiver, the sup-

port from Global Foundries for GF 65-nm CMOS tape-out of the multi-channel receiver, and the measurement support by W.-M. Lim, VIRTUS IC Design Center of Excellence, Nanyang Technological University, Singapore.

REFERENCES

- [1] K. Okada, N. Li, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, S. Ito, W. Chaivipas, R. Minami, T. Yamaguchi, Y. Takeuchi, H. Yamagishi, M. Noda, and A. Matsuzawa, "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE802.15.3c," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011.
- [2] B. Afshar, Y. Wang, and A. Niknejad, "A robust 24 mW 60 GHz receiver in 90 nm standard CMOS," in *IEEE Int. Solid-State Circuits Conf.*, 2008, pp. 182–183.
- [3] A. Tomkins, R. Aroca, T. Yamamoto, S. Nicolson, Y. Doi, and S. Voinigescu, "A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2085–2099, Aug. 2009.
- [4] C. Marcu, D. Chowdhury, C. Thakkar, J.-D. Park, L.-K. Kong, M. Tabesh, Y. Wang, B. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, E. Alon, and A. Niknejad, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3434–3447, Dec. 2009.
- [5] F. Vecchi, S. Bozzola, E. Temporiti, D. Guermandi, M. Pozzoni, M. Repossi, M. Cusmai, U. Decanis, A. Mazzanti, and F. Svelto, "A wideband receiver for multi-Gbit/s communications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 551–561, Mar. 2011.
- [6] C.-C. Chen, Y.-S. Lin, J.-H. Lee, and J.-F. Chang, "A 60 GHz CMOS receiver front-end with integrated 180° out-of-phase Wilkinson power divider," in *IEEE RFIC Symp.*, 2010, pp. 373–376.
- [7] A. Siligaris, O. Richard, B. Martineau, C. Mounet, F. Chaix, R. Ferragut, C. Dehos, J. Lanteri, L. Dussopt, S. Yamamoto, R. Pilard, P. Busson, A. Cathelin, D. Belot, and P. Vincent, "A 65-nm CMOS fully integrated transceiver module for 60-GHz wireless HD applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3005–3017, Dec. 2011.
- [8] S. Emami, R. Wiser, E. Ali, M. Forbes, M. Gordon, X. Guan, S. Lo, P. McElwee, J. Parker, J. Tani, J. Gilbert, and C. Doan, "A 60 GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in *IEEE Int. Solid-State Circuits Conf.*, 2011, pp. 164–166.
- [9] M. Uzunkol, W. Shin, and G. Rebeiz, "Design and analysis of a low-power 3–6-Gb/s 55-GHz OOK receiver with high-temperature performance," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3263–3271, Oct. 2012.
- [10] H.-C. Kuo, H.-L. Yue, Y.-W. Ou, C.-C. Lin, and H.-R. Chuang, "A 60-GHz CMOS sub-harmonic RF receiver with integrated on-chip artificial-magnetic-conductor Yagi antenna and balun bandpass filter for very-short-range gigabit communications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1681–1691, Apr. 2013.
- [11] W. Fei, H. Yu, Y. Shang, and K. S. Yeo, "A 2-D distributed power combining by metamaterial-based zero-phase-shifter for 60 GHz power amplifier in 65 nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 505–516, Jan. 2013.
- [12] **[Au. Must provide inclusive page numbers.]** W. Fei, H. Yu, W. M. Lim, and J. Ren, "A 53-to-73 GHz power amplifier with 74.5 mW/mm² output power density by 2-D differential power combining in 65 nm CMOS," in *IEEE RFIC Symp.*, 2013, pp. ???–???
- [13] J. J. Lee, D. Y. Jung, K. C. Eun, I. Y. Oh, and C. S. Park, "A low power CMOS single-chip receiver and system-on-package for 60 GHz mobile applications," in *IEEE RFIT Conf.*, 2009, pp. 24–27.
- [14] N.-Y. Wang, H. Wu, J.-C. Liu, J. Lu, H.-H. Hsieh, P.-Y. Wu, C. Jou, and M.-C. Chang, "A 60 dB gain and 4 dB noise figure CMOS V-band receiver based on two-dimensional passive *Gm*-enhancement," in *IEEE RFIC Symp.*, 2011, pp. 1–4.
- [15] R. Amaya and C. Verver, "A 60 GHz CMOS balanced downconversion mixer with a layout efficient 90° hybrid coupler," in *IEEE Custom Integr. Circuits Conf.*, 2009, pp. 235–238.
- [16] *IEEE Standard for Information Technology—Telecommunications and Information Exchange between Systems—Local and Metropolitan Area Networks—Specific Requirements. Part 15.3: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for High Rate Wireless Personal Area Networks (WPANs) Amendment 2: Millimeter-Wave-Based Alternative Physical Layer Extension*, IEEE Standard 802.15.3c-2009, Dec. 2009, (amendment to IEEE Standard 802.15.3-2003), pp. c1–187.
- [17] D. Cai, H. Fu, J. Ren, W. Li, N. Li, H. Yu, and K. S. Yeo, "A dividerless PLL with low power and low reference spur by aperture-phase detector and phase-to-analog converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 1, pp. 37–50, Jan. 2013.
- [18] Y. Shang, H. Yu, D. Cai, J. Ren, and K. S. Yeo, "Design of high-*Q* millimeter-wave oscillator by differential transmission line loaded with metamaterial resonator in 65 nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1892–1902, May 2013.
- [19] W. Fei, H. Yu, Y. Shang, D. Cai, and J. Ren, "A 96 GHz oscillator by high-*Q* differential transmission line loaded with complementary split ring resonator in 65 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 3, pp. 127–131, May 2013.
- [20] M. Tabesh, J. Chen, C. Marcu, L. Kong, S. Kang, A. Niknejad, and E. Alon, "A 65 nm CMOS 4-element sub-34 mW/element 60 GHz phased-array transceiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3018–3032, Dec. 2011.
- [21] T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi, and I. Seto, "A 60-GHz CMOS receiver front-end with frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 1030–1037, Apr. 2008.
- [22] M. Elmala, B. Carlton, R. Bishop, and K. Soumyanath, "A 1.4 V, 13.5 mW, 10/100 MHz 6th order elliptic filter/VGA with DC-offset correction in 90 nm CMOS [WLAN applications]," in *IEEE RFIC Symp.*, 2005, pp. 189–192.
- [23] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A bidirectional TX/RX four-element phased array at 60 GHz with RF-IF conversion block in 90-nm CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 5, pp. 1438–1446, May 2010.
- [24] A. M. Niknejad and H. Hashemi, *mm-Wave Silicon Technology 60 GHz and Beyond*. Berlin, Germany: Springer, 2008.
- [25] **[Au. Must provide inclusive page numbers.]** Y. Shang, H. Fu, H. Yu, and J. Ren, "A –78 dBm sensitivity 96 GHz super-regenerative receiver with quench-controlled metamaterial oscillator in 65 nm CMOS," in *IEEE RFIC Symp.*, 2013, pp. ???–???
- [26] T. Yao, M. Gordon, K. Tang, K. Yau, M.-T. Yang, P. Schvan, and S. Voinigescu, "Algorithmic design of CMOS LNAs and PAs for 60-GHz Radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.
- [27] F. Schnieder, R. Doerner, and W. Heinrich, "High-impedance coplanar waveguides with low attenuation," *IEEE Microw. Guided Wave Lett.*, vol. 6, no. 3, pp. 117–119, Mar. 1996.
- [28] Y. Shang, W. Fei, and H. Yu, "A fractional-order RLGC model for terahertz transmission line," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2013.
- [29] Y. Jin, J. Long, and M. Spirito, "A 7 dB NF 60 GHz-band millimeter-wave transconductance mixer," in *IEEE RFIC Symp.*, 2011, pp. 1–4.
- [30] H. Tanaka, Y. Sasaki, T. Hashimoto, Y. Yagi, and Y. Ishikawa, "Miniaturized 90 degree hybrid coupler using high dielectric substrate for QPSK modulator," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 1996, vol. 2, pp. 793–796.
- [31] Z. Liu and R. M. I. Weikle, "A compact quadrature coupler based on coupled artificial transmission lines," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 12, pp. 889–891, Dec. 2005.
- [32] D. Ozis, J. Paramesh, and D. Allstot, "Integrated quadrature couplers and their application in image-reject receivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1464–1476, May 2009.
- [33] T.-Y. Chin, J.-C. Wu, S.-F. Chang, and C.-C. Chang, "Compact *S*/*Ka*-band CMOS quadrature hybrids with high phase balance based on multilayer transformer over-coupling technique," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 3, pp. 708–715, Mar. 2009.
- [34] H. D. Lee, K. A. Lee, and S. Hong, "A wideband CMOS variable gain amplifier with an exponential gain control," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 6, pp. 1363–1373, Jun. 2007.
- [35] O. Jeon, R. Fox, and B. Myers, "Analog AGC circuitry for a CMOS WLAN receiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2291–2300, Oct. 2006.

- [36] C.-H. Wu, C.-H. Lee, W.-S. Chen, and S.-I. Liu, "CMOS wideband amplifiers using multiple inductive-series peaking technique," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 548–552, Feb. 2005.
- [37] E. Cherry and D. Hooper, "The design of wideband transistor feedback amplifiers," *Proc. IEEE*, vol. 110, no. 2, pp. 375–389, Feb. 1963.
- [38] Y. Wang, B. Afshar, L. Ye, V. Gaudet, and A. Niknejad, "Design of a low power, inductorless wideband variable-gain amplifier for high-speed receiver systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 696–707, Apr. 2012.
- [39] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York, NY, USA: Wiley, 2001.
- [40] E. Sackinger and W. Fischer, "A 3-GHz 32-dB CMOS limiting amplifier for SONET OC-48 receivers," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1884–1888, Dec. 2000.
- [41] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18- μ m CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2138–2146, Dec. 2003.

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