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2014

<https://hdl.handle.net/10356/103533>

<https://doi.org/10.1049/iet-pel.2013.0353>

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Subproportion Control of Double-Input Buck Converter for a Fuel-Cell/Battery Hybrid Power Supply System

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Abstract—In renewable energy hybrid systems (REHSs), the utilization of a multiple-input converter (MIC), instead of several parallel-connected single-input converters topology, has the advantages of integrating circuit structure, reducing cost, and simplifying controller design. To transit from one operating mode to another seamlessly and smoothly is one of the critical issues, about which the energy management for REHSs should concern. Normally, the mode transition (MT) in controller design of the REHS usually requires for the auxiliary circuits and components, which runs opposite to the MIC's intrinsic advantages and may cause potential problems on system's reliability and stability. In this paper, the proposed subproportion control (SPC) approach is able to combine two operating modes (single-source-powered mode and dual-source-powered mode) into a single control algorithm module without any hardware-assistance. The concept of subproportion (SP) is an additional control variable served as a certain proportion of the voltage-controlling duty cycle d_v . The product of the SP and d_v composes the current-controlling duty cycle for the first power source, in which way, not only the current of the source can be regulated, but also a seamless and smooth MT can be implemented automatically and spontaneously. The small-signal modeling for the three most-commonly-used topologies in the MIC family showed the SPC's universal applicability. The SPC was employed on a 1kW double-input-buck-converter-based fuel cells/battery REHS prototype and succeeded in regulating two system's control objectives and an auto-MT function.

Index Terms—subproportion control, renewable energy hybrid system, DC-DC power conversion, mode transition, multiport circuits

Nomenclature

Abbreviation

MIC(s)	multiple-input converter(s)
REHS(s)	renewable energy hybrid system(s)
FC(s)	fuel cell(s)
MPP	maximum power point
EM	energy management
MT	mode transition
DIC(s)	double-input converter(s)
SSP	single-source-powered
DSP	dual-source-powered
DIbC(s)	double-input buck converter(s)
OVR	output voltage regulation

ICR	input current regulation
MTSS	modified-time-sharing switching
DOF	degree of freedom
SPC	subproportion control
ICA	input-capacitor-added
FCS(s)	fuel cell system(s)
ESD(s)	energy storage device(s)
DIBBC(s)	double-input buck-boost converter(s)
DISC(s)	double-input SEPIC converter(s)
IC(s)	input-capacitor(s)
MEP	maximum efficiency point
SP	subproportion
PWM	pulsating-width modulation
ESR(s)	equivalent series resistor(s)
EP	equilibrium point
TF(s)	transfer function(s)
PID	proportion-integration-differentiation
COF	cross-over frequency
PM	phase margin
BNFCS(s)	Ballard Nexa fuel cell system(s)

1 Introduction

In the recent decade, multiple-input converters (MICs) are attracting more and more attentions in the areas of power electronics and renewable energy techniques, because of their irreplaceable advantages such as comparative higher efficiency, less component count, lower cost and simpler control method comparing with those conventional hybrid-used converter structures. Thus, recently MICs are widely concerned and utilized in field of renewable energy hybrid systems (REHSs). Renewable energies, or called alternative power sources, such as wind, solar, fuel cells (FCs), etc. possess some specialized characteristics on their electrical properties. For instance, photovoltaic cells have a maximum power point (MPP) which varies with different external circumstances; fuel cells in high power level have an apparent time-delay features on responding to sudden changes of load demand[1]. Therefore, the power regulation of these sources in a REHS appears of great significance to the entire system's reliability, economy, and efficiency. Meanwhile, energy management (EM) strategy is definitely required for an MIC to appropriately distribute its input sources to the load demand, which will be various according to the various characteristics of the renewable energy sources. When considering the EM strategy, the REHS should keep holding its primary capability on output voltage regulation (OVR) as well [2]. To transit from one operating mode to another seamlessly and smoothly is one of the critical issues that the EM strategy for REHSs should concern.

In almost all of the literatures, mode transition (MT) is realized by importing auxiliary circuits and components, which definitely runs opposite to the MIC's intrinsic advantages and may cause potential problems on system's reliability and stability. Normally, there are two modes in a double-input converter (DIC) system's operation: single-source-powered (SSP) mode and

dual-source-powered (DSP) mode; the EM strategy includes: a) OVR and b) input power distribution over the two power sources. One-cycle control for double-input buck converter (DIbC) proposed in [2] imported a multiplexer and a Schmitt trigger to meet the MT requirement, unavoidably introducing more complexity to its circuit and controller. In [3], two closed-loop PI controllers were supposed to take charge of the two control objectives. Additional circuit including a diode, a resistor, and an adder was employed for MT. When it operated at SSP mode, the primary output of the OVR regulator was added to the input of the input-current-regulation (ICR) controller via the diode, consisting dual-loop control for OVR. Although it achieved acceptable MT function, the superfluous dual-loop control at SSP mode would increase the complexity of the regulator design and consume excessive power dissipation. The literature [4] proposed a novel modified-time-sharing switching (MTSS) strategy that relieved switching pulses generation over each operating period. With this technique, the MIC can be reduced to an equivalent-single-input converter for analysis and its OVR can be realized with a single PI controller. The experimental results showed its MT performance is spontaneous and effective. Unfortunately, this MTSS strategy possessed only one degree of freedom (DOF), implying only one control object was able to be regulated while the other DOF was abandoned. Power distribution among input sources was related to the sharing factor β_i and limited to coarse regulation through changing hardware connection of the logical gating circuit. Without exception, the published control methodologies, considering EM strategy and MT function, employed auxiliary circuits and components that were definitely against the MIC's simplicity, integrity, and efficiency. The purpose of this paper, therefore, aims to bring out a novel MT-functioned control approach that contains simple and legible composition without any hardware assistance or sacrificing any DOF. With the purpose of that, subproportion control (SPC) is thus put forward.

The SPC's application objective in this paper is chosen as an input-capacitor-added (ICA) double-input buck converter (DIbC) that is equipped to a 1kW-fuel-cell-system (FCS)/battery REHS, for the following three considerations: a) the buck-type MIC is one of the mostly commonly used topologies in research and application areas [2, 3, 5-11]. Its mathematical modeling, operating analysis, and closed-loop control system design are of great typicality and reference value; b) the time-delayed feature and the soft-electrical-characteristic that exist in a FCS are mostly liable to unfold the significance of a MIC-based REHS [1]. The REHS is able to hybridize the FCS and an energy storage device (ESD) for stabilizing the FC's operating condition hence prolonging the FC's life-span [12, 13]. It should be noted that the proposed SPC is not limited to this ICA DIbC topology but can be applicable to other types of MIC, because all the topologies in the MIC family abide by the homologous operating principle with respect to the same applied TSS-based switching functions. Double-input buck-boost converter (DIbBC) and double-input SEPIC converter (DISC) are deemed as the most-commonly-used MIC topologies in practical applications besides DIbC. In this paper, their SPC-based small-signal modeling results will also be provided in Section III for proving the SPC's universal applicability and convenience of readers' further research and application. The ICA DIbC topology presented in Fig. 1 is hereby utilized for the SPC research and verification. More detailed stories about this topology's relevant equations and operating principles are available in [8].

In this paper, the FCS (V_{s1}) is considered as the master device that provides the base-loaded part of the load demand, while the lithium battery bank (V_{s2}) is served as the slave device that compensates the intermittent or fluctuating rest part of the load demand. There are four control targets that the FCS/battery REHS should simultaneously obtain: a) OVR for the DIbC; b) to limit the FC's input current when the system is operating at SSP mode; c) to control the FC's input current at its maximum efficiency point (MEP) when the system is operating at DSP mode; d) to realize smooth and seamless MT between SSP and DSP modes. The control objectives in the ICA DIbC, therefore, result in ICR of the averaged input current of the FCS (I_{s1}) and OVR of the converter's output voltage (v_o).

Fig. 1. Utilized ICA DIbC topology for the FCS/battery REHS.

The concept of “subproportion (SP)” is served as a control output from one of the two PI controllers and introduced for limiting I_{s1} to a presetting value at DSP mode. Moreover, when the load requirement is lower than that the FCS can provide, the SPC is able to automatically shut off the axillary slave power source V_{s2} without modifying any controller’s parameter or hardware structure. The upcoming contents are organized as follows. Section II will propose the concept and the theory about the SPC and describe its operating principles and regulating rules. In Section III, the closed-loop feedback control system design for the utilized ICA DIbC equipped with the SPC approach will be put forward, based on its small-signal modeling analysis and Bode diagram. After that, in Section IV, a series of simulations and prototype-based experiments will be carried out for verification and discussion. Finally, Section V will give the concluding remarks.

2 Subproportion Control Approach

As is mentioned in Section I, for high reliability and economic efficiency of a FC-sourced REHS, the FC’s input current is expected to be maintained at an expected value, such as its MEP or MPP [14]. It becomes one of the control targets that the SPC has to reach. It is clear that the DOF of the ICA DIbC is 2, i.e., two parameters from the converter can be selected as the control variables. Hereby, they must be the two switching signals, i.e., duty cycles d_1 and d_2 , which are applied on SW_1 and SW_2 , respectively. Therefore, the purpose of the SPC falls on the following two aspects: a) to stabilize the DIbC’s output voltage; b) to regulate input power distribution between V_{s1} and V_{s2} . Assumed V_{s1} and V_{s2} are invariable, controlling the input current of any one of them means controlling its input power. So the two control objectives are set as: v_o and I_{s1} (or I_{s2}). In one-control-objective-case of the control design for MICs [7, 9, 10, 15], v_o is controlled via a duty cycle signal d_v which is decided by the two actual duty cycles d_1 and d_2 :

$$d_v = d_1 + d_2. \quad (1)$$

From (1), one can see that d_v must be larger than d_1 . However, in the process of two-control-objectives-case, when another objective besides v_o is required regulation, this constraint cannot be guaranteed by simply generating d_1 from another regulator without considering the interaction from d_v . In other words, d_1 is probably larger than d_v due to the irrelevance between the two regulators. If it happens, d_2 will be negative, causing V_{s2} out of service. So v_o and I_{s1} cannot be simultaneously regulated via d_1 only and the entire system operation will lose control at any time. In order to avoid negative value of d_2 , controllers are often designed to

enforce d_1 to control I_{s1} meanwhile d_2 to control v_o . However, the by-effect is its MT function could not be implemented unless other auxiliary methods are imposed on the system.

The SPC is brought out for optimizing controller's structure and simplifying MT realization. The core of the SPC is the definition of a new variable p_1 which is used to represent the proportion of d_1 out of d_v . By this means, d_1 will always be <1 . If another dependent variable p_2 , which equals to $(1 - p_1)$, is defined, we can establish the following relations:

$$\begin{cases} d_1 = p_1 d_v, \\ d_2 = p_2 d_v = (1 - p_1) d_v. \end{cases} \quad (2)$$

In (2), the variable p_1 connects the two control variables v_o and I_{s1} , making them relevant to each other and ensuring $d_v > d_1$. If p_1 is able to be adjusted by another regulator besides the v_o -controlling one, then p_2 will be under control as well. Fig. 3 shows the detailed schematic block diagram of the proposed SPC approach applied in the ICA DIbC REHS. V_{ref} and I_{ref} denote the reference output voltage and the reference current of the FCS, respectively. Re #1 and Re #2 denote the two regulators, respectively. Ge #1 and Ge #2 denote the two pulsating-width modulation (PWM) generators, respectively. SP #1 and SP #2 denote the SPs of d_1 out of d_v and d_2 out of d_v , respectively.

The brief on the SPC's regulation process is hereby given: when v_o falls below V_{ref} in the steady-state operation, the increasing error will make output of Re #1 rise, which means d_v will become larger to prolong switch-on period. Then v_o will be restored to V_{ref} . Meanwhile, the rise of d_v will increase d_1 through p_1 and decrease d_2 through p_2 , which indicates a rise potential of I_{s1} . Therefore, the error between I_{ref} and I_{s1} will become negative and the output of Re #2 will be reduced, thus I_{s1} will go back to I_{ref} . It is worth noting that the rise of I_{s1} will reduce the voltage of V_{s1} if a practical power source, instead of ideal voltage source, is taken. But this influence is barely sensitive to the control behavior of Re #1 since the variation of I_{s1} is constrained within a limited range by Re #2. A likewise process applies when v_o increases above V_{ref} . The control stream about this process is illustrated in Fig. 2.

The most important contribution of the SPC is: if the power demand is lower than $V_{s1}I_{ref}$ (at SSP mode), p_1 will automatically rise up to 1 since the error between I_{ref} and I_{s1} is always positive, which means $d_1 = d_v$ and $d_2 = 0$. Therefore, the FCS is served as the master power supply to the REHS and v_o is regulated though d_1 only. The SPC composition is simple and legible, supporting the system running at both SSP and DSP modes without any additional hardware assistance, meanwhile the two DOF are retained. The upcoming section reveals the design process of the SPC's parameters and proves the SPC's capability in two-control-variable-case in addition to its auto-MT function.

3 Small-Signal Modeling and Controller Design

3.1 Dynamic Equations for Averaged Model

For sake of systematic analysis and controller's parameters design, the averaged dynamic equations of the DIbC and its small-signal model are necessary to be built. Based on the analysis result obtained in Section II, and in terms of an averaged model in a whole operation cycle, a general DIbC topology is able to replace the proposed ICA DIbC one. An equivalent circuit with equivalent series resistors (ESRs) for L and C (R_L and R_C) is used here as Fig. 4a shows, expecting for a more practical model and a more precise tuning to its controller. V_{s1} and V_{s2} are assumed as the ideal voltage sources. The open-loop dynamic equations for the averaged model were calculated in the form of the matrix as follows:

Fig. 3. Schematic block diagram of REHS with SP control approach.

Fig. 2. Stream of the SPC's control actions.

Fig. 4. Equivalent circuit of (a) ICA DIBC, (b) DIBC, and (c) DISC topologies.

$$\begin{bmatrix} \frac{dv_c}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{C} \left[R_o i_L / (R_o + R_c) - v_c / (R_o + R_c) \right] \\ \frac{1}{L} \left[- \left(R_L + \frac{R_o R_c}{R_o + R_c} \right) i_L - \frac{R_o v_c}{R_o + R_c} + d_v V_e \right] \end{bmatrix}, \quad (3)$$

where $V_e = V_{s2} + p_1 (V_{s1} - V_{s2})$. The equilibrium point (EP) of the model expressed in (3) is

$$\begin{bmatrix} V_c \\ I_L \end{bmatrix} = \begin{bmatrix} R_o d_v V_e / (R_o + R_c) \\ d_v V_e / (R_o + R_c) \end{bmatrix}. \quad (4)$$

3.2 Small-Signal Modeling

Taking Laplace transform for (3) and considering $v_o(s) = (1 + R_c Cs)v_c(s)$ and $i_{s1}(s) = d_1 i_L(s) = p_1 d_v i_L(s)$, we obtain:

$$\begin{cases} v_o(s) = (R_o R_c Cs + R_o) d_v V_e / \Delta_1, \\ i_{s1}(s) = [(R_o + R_c)Cs + 1] p_1 d_v^2 V_e / \Delta_1, \end{cases} \quad (5)$$

where $\Delta_1 = (R_o + R_c)LCs^2 + [R_L(R_o + R_c)C + R_o R_c C + L]s + R_o + R_L$. Small variations $\hat{i}_{s1}$, $\hat{v}_o$, $\hat{d}_v$, and $\hat{p}_1$ with respect to their nominal values I_{s1} , V_o , d_v , and p_1 are introduced here. Dividing by the disturbances of the two control variations leads to its control-to-output TF:

$$\begin{bmatrix} \hat{v}_o(s) \\ \hat{i}_{s1}(s) \end{bmatrix} = \begin{bmatrix} G_{v1}(s) & G_{v2}(s) \\ G_{c1}(s) & G_{c2}(s) \end{bmatrix} \begin{bmatrix} \hat{d}_v(s) \\ \hat{p}_1(s) \end{bmatrix} \quad (6)$$

where $G_{v1}(s) = R_o V_e (1 + R_c Cs) / \Delta_2$, $G_{v2}(s) = R_o d_v (V_{s1} - V_{s2}) (1 + R_c Cs) / \Delta_2$, $G_{c1}(s) = p_1 d_v V_e [(R_o + R_c)Cs + 1] / \Delta_2$, and $G_{c2}(s) = p_1 d_v^2 (V_{s1} - V_{s2}) [(R_o + R_c)Cs + 1] / \Delta_2$.

As is previously said that the SPC approach is applicable for all of the TSS-based MIC topologies, without losing any generality, the control-to-output TF for DIbBC, considering the ESRs of L and C , was deduced as well, based on the equivalent circuits given in Fig. 4(b). Its operating principle was specified in [16]. DIbBC has the identical matrix form to (6) while the entries $G_{v1}(s)$, $G_{v2}(s)$, $G_{c1}(s)$, and $G_{c2}(s)$ are:

$$\begin{cases} G_{c1}(s) = [V_e (R_o + R_c)^2 Cs + V_e (R_o + R_c) + 2R_o R_c + R_o V_c - (1 - d_v) R_o^2 I_L] p_1 d_v / \Delta_3, \\ G_{c2}(s) = [d_v (V_{s1} - V_{s2}) (R_o + R_c)^2 Cs + d_v (V_{s1} - V_{s2}) (R_o + R_c)] p_1 d_v / \Delta_3, \\ G_{v1}(s) = [R_o (1 - d_v) G_{c1}(s) + R_o I_L p_1 d_v] / [p_1 d_v (R_o + R_c)Cs + p_1 d_v], \\ G_{v2}(s) = G_{c2}(s) / [p_1 d_v (R_o + R_c)Cs + p_1 d_v], \\ \Delta_3 = (R_o + R_c)^2 LCs^2 + \left\{ (R_o + R_c)L + [R_L (R_o^2 + R_c^2) + 2R_L R_o R_c + (R_o + R_c)(1 - d_v)^2 R_o R_c] C \right\} s \\ \quad + R_L R_o + R_L R_c + (1 - d_v)^2 R_o R_c. \end{cases} \quad (7)$$

DISC has a relatively complicated and implicit form for its control-to-output TF and is difficult to obtain its symbolic expression; thus we present the DISC's small-signal model in its state-space form, based on the circuits given in Fig. 4(c). Readers can refer to [17] for its state-space averaging model and operating principle. As is shown in the figure, the DISC has 6 state variables:

$\mathbf{X} = [\hat{i}_{L1} \quad \hat{i}_{L2} \quad \hat{i}_L \quad \hat{v}_{c1} \quad \hat{v}_{c2} \quad \hat{v}_c]^T$. If its control inputs $\mathbf{u} = [\hat{d}_v \quad \hat{p}_1]^T$ and outputs $\mathbf{y} = [\hat{v}_o \quad \hat{i}_{s1}]$, we can transform the original state-space averaging model into the following one:

$$\begin{cases} \mathbf{X} = \mathbf{A}\mathbf{X} + \mathbf{B}\mathbf{u}, \\ \mathbf{y} = \mathbf{C}\mathbf{X} + \mathbf{D}\mathbf{u}. \end{cases} \quad (8)$$

$$\text{where } \mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & -1/L_1 & 0 & -1/L_1 \\ 0 & 0 & 0 & 0 & -1/L_2 & -1/L_2 \\ 0 & 0 & 0 & \frac{p_1 d_v}{L} & \frac{(1-p_1)d_v}{L} & \frac{d_v-1}{L} \\ \frac{1-p_1 d_v}{C_1} & \frac{-p_1 d_v}{C_1} & \frac{-p_1 d_v}{C_1} & 0 & 0 & 0 \\ \frac{p_1-1}{C_2} & \frac{1-(1-p_1)d_v}{C_2} & \frac{p_1-1}{C_2} & 0 & 0 & 0 \\ \frac{1-d_v}{C} & \frac{1-d_v}{C} & \frac{1-d_v}{C} & 0 & 0 & \frac{-1}{R_o C} \end{bmatrix},$$

$$\mathbf{B} = \begin{bmatrix} \frac{V_o + p_1 V_{s1} + (1-p_1)V_{s2}}{L_1} & \frac{(V_{s1} - V_{s2})d_v}{L_1} \\ \frac{V_o - p_1 V_{s1} + (1+p_1)V_{s2}}{L_2} & \frac{(V_{s2} - V_{s1})d_v}{L_2} \\ \frac{V_o + p_1 V_{s1} + (1-p_1)V_{s2}}{L} & \frac{(V_{s1} - V_{s2})d_v}{L} \\ \frac{-p_1(I_L + I_{L1} + I_{L2})}{C_1} & \frac{-(I_L + I_{L1} + I_{L2})d_v}{C_1} \\ \frac{-(1-p_1)(I_L + I_{L1} + I_{L2})}{C_2} & \frac{(I_L + I_{L1} + I_{L2})d_v}{C_2} \\ \frac{-(I_L + I_{L1} + I_{L2})}{C} & 0 \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \text{ and } \mathbf{D} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

By applying (8) with specific parameters in practice, one can solve the control-to-output TF through $\mathbf{G}(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}$, where $\mathbf{I}$ is the identity matrix. Mapping to (6), $G_{v1} = \mathbf{G}_{11}$, $G_{v2} = \mathbf{G}_{12}$, $G_{c1} = \mathbf{G}_{21}$, and $G_{c2} = \mathbf{G}_{22}$. Since DIBC, DIBBC, and DISC have the identical small-signal modeling form and can realize OVR and ICR by d_v and p_1 , they must share the analogous design process for their closed-loop feedback controllers, which we will discuss as follows.

3.3 Closed-Loop Control Design

Fig. 5 illustrates the small-signal closed-loop control system, which integrates with the open-loop model from (6), regulators, filters, PWM generators, voltage samplers, and voltage dividers. Hereby, $G_{vr}(s)$, $G_{cr}(s)$, $G_{filter}(s)$, $G_{vf}(s)$, $G_{cf}(s)$, and $G_{PWM}(s)$ represent the TFs of the voltage regulator, the current regulator, the filter, the feedback amplification of the sampled output voltage, the feedback gain of the sampled current, and the PWM generators, respectively. Other types of topology in the MIC family are sharing the identical control schematic to Fig. 5.

The V_{ref} -to- v_o loop gain TF of v_o is

$$T_v(s) = G_A(s) \cdot [G_{v2}(s) - G_{v2}(s)G_B(s)G_{c1}(s)] \quad (9)$$

Fig. 5. Closed-loop control system block diagram with SPC.

where $G_A(s) = G_{PWM}(s)G_{vr}(s)G_{filter}(s)G_{vf}(s)$ and $G_B(s) = \frac{G_{PWM}(s)G_{cr}(s)G_{filter}(s)G_{cf}(s)}{1 + G_{PWM}(s)G_{cr}(s)G_{filter}(s)G_{cf}(s)G_{c2}(s)}$.

Similarly, the I_{ref} -to- i_{s1} loop gain TF of i_{s1} is

$$T_c(s) = G_c(s) \cdot [G_{c2}(s) - G_{c1}(s)G_D(s)G_{v2}(s)] \quad (10)$$

where $G_C(s) = G_{PWM}(s)G_{cr}(s)G_{filter}(s)G_{cf}(s)$ and $G_D(s) = \frac{G_{PWM}(s)G_{vr}(s)G_{filter}(s)G_{vf}(s)}{1 + G_{PWM}(s)G_{vr}(s)G_{filter}(s)G_{vf}(s)G_{v1}(s)}$.

Proportion-integration-differentiation (PID) controller with filter is utilized here to act as the regulators and the filters for the two control variables. The PID's TFs have the following forms:

$$\begin{cases} G_{vr}(s) = k_{pv} + k_{iv} / s + k_{dv} \cdot s \cdot N_{fv} / (s + N_{fv}) \\ G_{cr}(s) = k_{pc} + k_{ic} / s + k_{dc} \cdot s \cdot N_{fc} / (s + N_{fc}) \end{cases} \quad (11)$$

where N_{fv} and N_{fc} is the filter coefficients.

According to the parameter values of the components used in the tested prototype, the parameters of the PID controllers are determined by tuning each control-loop independently. Equation (2) clearly showed that d_1 is decided by d_v and p_1 , indicating the value of d_1 can be figured out by tuning the value of p_1 only when the value of d_v is determined. If d_v is in the process of determination and changing, p_1 is following d_v to change as well. Therefore, d_v must be considered as the master control signals while p_1 is the slave one. The cross-over frequency (COF) of $T_v(s)$ should be designed lower than that of the current loop. Both of them should be far lower than the switching frequency (100 kHz). Both loops should have a phase margin (PM) higher than 45°. Bode diagrams of the corresponding loop gains at the required EP ($V_c = 30$ V, $I_L = 12.5$ A, $I_{s1} = 5$ A, $I_{s2} = 4.75$ A) are plotted by using the components in the developed prototype as Table I listed.

Bode diagrams of T_v and T_c before and after PID control are given in Fig. 6. One can see both loops have no PM or COF before

Fig. 6. Bode diagrams of the (a) current loop gain and (b) voltage loop gain before and after compensation.

TABLE II
PARAMETERS OF SOURCES, COMPONENTS, AND CONTROLLERS AT EP

Parameter	Value	Parameter	Value
V_{s1}	37 V	V_{s2}	40 V
d_v	0.78	p_1	20/39
f	100 kHz	L	4.225×10^{-5} H
C	1×10^{-3} F	R_o	2.4 Ω
R_L	8.6×10^{-2} Ω	R_c	1.82×10^{-1} Ω
G_{vf}	2.5×10^{-3}	G_{cf}	0.1
G_{PWM}	1/3		

compensation. PID controller can help them enhance PM by inserting zeros. The current loop gain should be designed firstly. With the parameters of $G_{cr}(s)$ as $k_{pc} = 59.77$, $k_{ic} = 751662$, $k_{dc} = 0.0002234$, and $N_{fc} = 267487$, the COF and PM of $T_c(s)$ are 17.9 kHz and 57.2° , respectively. The voltage loop gain is then designed with the parameters of $G_{vr}(s)$ as $k_{pv} = 986.4$, $k_{iv} = 303589415$, $k_{dv} = 0.0001228$, and $N_{fv} = 304934$. It can be observed from the Bode diagrams that the COF and PM of $T_v(s)$ are 206 Hz and 119° . Finally, the Bode diagrams of $T_c(s)$ with compensation of both $G_{vr}(s)$ and $G_{cr}(s)$ are drawn for verification. From the result shown in Fig. 6, one can see that Bode diagrams of $T_c(s)$ with $G_{cr}(s)$ only and those with both regulators almost overlap with each other, which means the existence of $G_{vr}(s)$ merely affects $T_c(s)$. So far, the closed-loop SPC design is done.

4 Case Study

For better understanding and verification of the SPC theory, the short-term and the long-term simulation and experimental studies for the ICA DIbC circuit with the parameters listed in Table II are respectively carried out. The short-term test results help us study the SPC's regulating performance and robustness to the sudden resistive load transient, especially for observing the MT process between SSP and DSP modes. The long-term test results provided more information about the durability and stability of the SPC approach in the relatively-higher-power-level long-time operation.

For convenience and simplicity of modeling the utilized FCS, the ohmic polarization section in the V-I curve of the FCS can be simply represented by a resistor. According to the AC impedance experimental data in [18], the average single cell resistance of a Ballard FCS is approximately 8 m Ω at current of 10 A and at 70 °C. Here the current of the FCS is limited at 5 A and the operating temperature is regulated around 55-60 °C, thus the average single cell resistance is bound to be higher than 8 m Ω and might as well be set to 20 m Ω . As a result, for the 47-cell Ballard Nexa FCS (BNFCS) applied in this paper, a 42V-voltage-source series connected with a 1 Ω -resistor is proper to serve as the FCS model in the simulation. It is easily to calculate that $V_{s1} = 37$ V when $I_{s1} = 5$ A. V_{s2} was 40V-voltage source. V_{ref} and I_{ref} were set to 30 V and 5 A, respectively (assume 5 A, i.e., 185 W, is the FCS's MEP). The other parameters of the components used in the PLECS model can be found in Table II.

4.1 Simulation Stage: Short-Term Test and Discussion

As for the short-term test, the model was given a series of load step changes with 0.03s-intervals around the EP. In the first 0.03s-interval, load demand was set to 12 Ω ($P_o = 75$ W) to test OVR capability at the SSP mode; In the second 0.03s-interval, the load step-changed to 3.3 Ω ($P_o = 273$ W) to test the SPC's regulating performance on both the OVR and the ICR at the DSP mode and the MT process from the SSP mode to the DSP mode; in the last 0.03s-interval, load demand was pulled up to 16 Ω ($P_o = 56$ W) to observe the MT process from the DSP mode to the SSP mode.

The dynamic curves of I_{s1} , I_{s2} and v_o are given in Fig. 7. Simulation results for (a) the waveforms of I_{s1} , I_{s2} , and v_o , and (b) the dynamics of d_v , p_1 , d_1 , and d_2 against the short-term 0.03s-interval-load-step-changing test.(a), and its corresponding duty cycles dynamics of d_v , p_1 , d_1 , and d_2 are presented in Fig. 7. Simulation results for (a) the waveforms of I_{s1} , I_{s2} , and v_o , and (b) the dynamics of d_v , p_1 , d_1 , and d_2 against the short-term 0.03s-interval-load-step-changing test.(b). One can see I_{s1} maintained around 2 A while v_o kept at 30 V within the first 0.03s-interval, which well-matched the theoretical calculating results (2.027 A and 30 V). During this period, p_1 was rising to 1, making Re#1-generated d_v directly control v_o via the master power source V_{s1} ($d_v = d_1$) without taking power from V_{s2} ($d_2 = 0$). After 0.03 s, d_1 and d_2 were both in operation. The SSP-DSP-MT process completed almost instantly, and was smooth and seamless. d_v was still responsible for controlling v_o . According to the real-time value of d_v , p_1 was modifying timely to adapt the change of d_v for the purpose of maintaining I_{s1} at I_{ref} . I_{s1} was limited at I_{ref} (5 A) with ripples less than 10%, and I_{s2} was following and compensating the load demand changes with rise time less than 3 ms up to approximate 2.1 A (the theoretical EP: $I_{s1} = 5$ A, $I_{s2} = 2.157$). v_o was controlled at 30 V with ripples less than 1%. There is a ± 1 V-oscillation at the MT point lasting for 1 ms, responding to the SP control action. The corresponding d_v and p_1 are close to 0.8 and 0.7, respectively, in comparison with the theoretical value 0.791 and 0.695. At the end of the second 0.03s-interval, the load was pulled down to 56 W and the SPC automatically transit the DSP mode to the SSP mode within 5 ms. The value of I_{s1} dropped back to 1.42 A to supply the load alone due to p_1 went up to 1 immediately. The calculating value of I_{s1} at this 0.03-interval is 1.52 A.

The short-term load-step-changing test validated the SPC control theory and closed-loop design, revealed the relevance between control variables and their objectives, and proved the effectiveness of the auto-MT ability inherited in the SPC approach.

4.2 Simulation Stage: Long-Term Test and Discussion

17 step load changes ranging from 1.5 to 10 Ω (90 to 600 W) with 0.5s-intervals were connected to the SPC-regulated ICA DIbC model. The 18 load resistances were set to 10 $\Omega \rightarrow 7.5 \Omega \rightarrow 4 \Omega \rightarrow 3 \Omega \rightarrow 2 \Omega \rightarrow 3.5 \Omega \rightarrow 2.5 \Omega \rightarrow 4 \Omega \rightarrow 1.6 \Omega \rightarrow 3.5 \Omega \rightarrow 2 \Omega \rightarrow 3 \Omega \rightarrow 1.5 \Omega \rightarrow 3.5 \Omega \rightarrow 7.5 \Omega \rightarrow 8.5 \Omega \rightarrow 9 \Omega \rightarrow 10 \Omega$. Fig. 8 presents the simulation results. The voltage v_o was regulated at 30 V and I_{s1} at I_{ref} (5 A) at the DSP mode (2-8 s); at the SSP mode (0-1 s and 8-9 s), the FCS, supplied the load alone. The 30V-OVR

Fig. 7. Simulation results for (a) the waveforms of I_{s1} , I_{s2} , and v_o , and (b) the dynamics of dv , p_1 , d_1 , and d_2 against the short-term 0.03s-interval-load-step-changing test.

Fig. 8. Simulation results for the (a) current and (b) voltage waveforms of the FCS, the battery, and the output of the ICA DIBC model against the long-term 0.5s-interval-load-step-changing test.

hold and 5A-ICR was automatically disabled. The test results obey the operating principle of the SPC approach, and inspected its long-term operating performance, stability, and durability. Furthermore, the SPC is proven to be able to immediately respond to load variations at the same mode. At the SSP mode, the master power source individually answered for the load demand; at the DSP mode, the ICR took effect and the FCS's averaged input current was limited to 5 A and always powered the base-load only. The

fluctuating load demand was compensated by the battery in time.

4.3 Experimental Stage

A 1kW-prototype of FCS/battery ICA DIbC REHS was developed for experimental verification. The BNFCs were served as V_{s1} and a Phylion 10-cell 10Ah lithium battery was chosen as V_{s2} . Environmental temperature was 25 °C. 99.99% pure hydrogen gas was supplied to the BNFCs with 200 kPa pressure. Fig. 9 demonstrates its experimental installation. The PCB board integrated with the ICA DIbC circuit, interface circuit and an embedded Texas Instruments DSP (TMS320F2808) controller as a self-contained synthetic system. The DSP controller was responsible for implementing operation, supervision, and control of the whole system through the developed programs. The details of sources and components index applied were listed in Table II. Identical to simulation stage tests, V_{ref} and I_{ref} were set to 30 V and 5 A, respectively (assume 5 A is the MEP of the BNFCs here). V_{s1} , I_{s1} , V_{s2} , I_{s2} , v_o , and i_o were monitored and recorded by oscilloscope (Tektronix DPO 4034) with 1 MHz scan frequency. The same step-load-changing test as we did at the simulation stage was carried out. Fig. 10 presents the short-term experimental results and Fig. 11 presents the long-term ones.

As for the short-term test, the same configuration on the circuit and the controller as that in simulation test was set up, leading to the current and voltage waveforms screenshot in Fig. 10, corresponding to the simulation results in Fig. 7. The simulation and experimental results agreed with each other well. Details about magnitudes, responding times, ripples, and oscillation are specified and marked in the figure.

As for the long-term test, the experimental results in Fig. 11 agree with the simulation ones except for the inevitable current ripples ($\pm 10\%$) that were due to the switching signal interference and the input-capacitors' filtering performance. Fig. 11(b) shows the obvious rise time in FC-voltage dynamic that was not reflected on the corresponding waveform in Fig. 8(b). This time-delayed characteristic in the FCS should be manifested through the specific model [1], which is out of the research scope of this paper.

5 Conclusion

In most cases, the actions of adding auxiliary circuits and devices to a MIC-based REHS for its EM and MT run definitely opposite to simplicity, integrity, economy, and efficiency that the MIC topology would bring in. These shortcomings have been wiped out by employing the proposed SPC, where a new variable p_1 is put forward to represent the proportion of d_1 out of d_v . This legible-configured modification is completely based the control algorithm itself, and is verified to be able to realize rapid, smooth, and seamless auto-MT between SSP and DSP modes on both simulation and experimental stages. More importantly, the MT controlled by SPC occurs spontaneously without requiring any hardware assistance or manual intervention; meanwhile, the SPC preserves full DOF of the system. The beauty of the SPC is its easy-understood-and-simple-implemented feature plus its nature and smooth auto-MT function. Designers would never concern the system's reliability and stability when the system is changing modes frequently between SSP mode and DSP mode, as long as the SPC's parameters have been designed once for both the modes' requirements. Furthermore, the success of applying the SPC on the 1kW-ICA-DIbC-based FCS/battery REHS prototype for v_o -regulation and I_{s1} -limitation proves the SPC's regulation capability in two-control-objectives-case. The derived TFs for the SPC-controlled closed-loop control system provide those published related techniques with an applicable platform to achieve TF-decoupling, advanced control, system-level EM strategies, etc. In future work, this SPC technique is expected for a wider application range in MIC-based REHSs, that is, to extend it to multivariable cases (more than two), as well as for bidirectional MIC topologies.

TABLE II

INDEX OF SOURCES AND COMPONENTS FOR THE REHS PROTOTYPE

Sources/ Components	Value
BNFCS	26-42 V (v_{s1}), 0-46 A (i_{s1}), 47 cells
Battery	37-41 V (v_{s2}), 0-20 A (i_{s2}), 10 cells
D	MBR60H100CTG (60 A, 100 V)
C_1 , C_2 , and C	ECOS2AA102CA (1×10^{-3} F, R_C : 1.82×10^{-1} Ω)
$MOSFET_1$ & $MOSFET_2$	IRFP4468PBF (290 A, 100 V)
D_{buf1} , D_{buf2}	S5B (5 A, 200 V)
C_{buf1} , C_{buf2}	1×10^{-5} F
R_{buf1} , R_{buf2}	1.5 Ω

Fig. 9. Photograph of experimental installation.

Fig. 10. Experimental results for the waveforms of (a) I_{s1} , I_{s2} , and (b) v_o against the short-term 0.03s-interval-load-step-changing test.

Fig. 11. Experimental results for the (a) current and (b) voltage waveforms of the FCS, the battery, and the output of the ICA DIBC model against the long-term 0.5s-interval-load-step-changing test.

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