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A Highly Efficient Fully Integrated GaN Power Amplifier for 5-GHz WLAN 802.11ac Application

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Abstract—In this letter, a novel compact on-chip output matching network to achieve harmonic impedance matching is proposed. With the proposed matching network, a highly efficient GaN MMIC power amplifier (PA) is designed for 5 GHz WLAN 802.11ac application. The implemented PA achieves a maximum power-added efficiency (PAE) of 49.5%-61.3% over the frequency band from 4.9 to 5.9 GHz, with a saturated output power (Psat) of 34.6-36.1 dBm. When tested with 802.11ac VHT80 MCS9 (80MHz, 256-QAM) signal with 11.3 dB peak-to-average power ratio (PAPR), the PA achieves an average output power of 23.7-26.3 dBm, with PAE of 24.9%-30.9%, while meeting the standard EVM specification of -32 dB.

Index Terms—Monolithic microwave circuit (MMIC), high efficiency, GaN power amplifier.

I. INTRODUCTION

RECENTLY, the accelerating growth of smartphones and mobile devices is propelling wireless communication to evolve towards higher data rate and lower latency. As new generation of WLAN standards, 802.11ac system utilizes a wider bandwidth and more complex modulation scheme, and can provide up to 866 Mbps data rate per transmit/receive path. However, wider bandwidth and more complex modulation scheme result in large PAPR, posing stringent requirements of linearity and efficiency on power amplifier design.

To achieve high efficiency, several switched mode Class-E or Class-E/F PAs have been proposed [1], [2]. However, the maximum operation frequency ($f_{max,E}$) of Class-E is inherently limited by output capacitance of device and output power [2]. Beyond $f_{max,E}$, idealized optimum conditions for appropriate waveform shaping cannot be satisfied anymore, and consequently, the performance of Class-E PA will deteriorate to a large extent. Therefore, Class-E topology is not

an appropriate choice for PA design with watt-level output power to target high efficiency above 5 GHz.

To achieve the highest possible efficiency, harmonic impedance matching technique is widely used [3]-[7]. In practice, this technique is usually realized by using transmission lines to achieve low loss as well as broadband performance. However, when the operation frequency is low, the size of transmission lines will be large, thus this technique is not well suitable for integrated PA constrained by die size. We therefore seek to find an on-chip output harmonic matching network with compact size and low loss over the 802.11ac band from 4.9 to 5.9 GHz.

In this letter, a novel compact output harmonic matching network is proposed. During the design, the second harmonic impedance is firstly targeted, and then the fundamental impedance is matched. A highly efficient GaN MMIC PA using the proposed matching network is designed for 802.11ac access points, which delivers a saturated output power of 34.6-36.1 dBm with PAE of 49.5%-61.3%.

II. HARMONIC OUTPUT MATCHING NETWORK DESIGN

Based on the required saturated output power level of 35 dBm, the transistor size is set at 800 μm /0.25 μm , and this GaN device can deliver maximum output power of 36.6 dBm under a drain voltage of 28 V.

A. Fundamental and Harmonic Impedance Analysis

For a practical PA design, the second and third harmonic impedances are generally considered to extract high efficiency. To demonstrate the impact of second and third harmonic impedance on efficiency, load-pull simulation has been performed at 5.4 GHz and the results are depicted in Fig.1(a). As observed, the second harmonic impedance has more significant impact on efficiency than the third harmonic impedance, and the PAE may deteriorate by as much as 10% without careful consideration of the second harmonic matching. Therefore, only the second harmonic impedance is taken into consideration for output matching in the design. Fig.1(b) shows the desired fundamental and second harmonic impedances for frequency range from 4.9 to 5.9 GHz. With these desired impedances, PA can achieve over 85% drain efficiency at approximately 36.3 dBm output power. It can be observed the required second harmonic load should be reactive

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Fig. 1. (a) Second and third harmonic load-pull at 5.4 GHz
(b) Load-pull simulation results for fundamental and second harmonic

Fig. 2. Schematic of proposed PA

Fig.3. Load impedance of output matching network at: (a) second harmonic (b) fundamental

impedance [2], [5].

B. Harmonic Matching Network Design

A new on-chip matching network consisting of one open-circuit stub, one capacitor and two inductors is proposed, as depicted in Fig.2. The design procedure of output matching network is presented as follows.

To begin with, considering that the objective of matching network is to provide an inductive impedance for the second harmonic, using an inductor is the simplest way to achieve so. With this concept, one open-circuit stub TL_1 with electrical length θ of $\lambda/8$ at 5.4 GHz and one series inductor L_1 are used in the matching network, as shown in Fig.3(a). At the second harmonic frequency, the TL_1 provides a perfect ground and the inductor L_1 provides the required inductance. The load impedance Z_L is,

$$Z_L = j\omega L_1 \quad (1)$$

The value of L_1 is set at 1.55 nH based on the optimum second harmonic impedance at the center frequency of 10.8 GHz,

Secondly, after targeting an inductive second harmonic impedance, we step to add more components in the matching network to realize fundamental impedance matching. With the consideration of low loss and compact size, the number and size of components to be integrated should be as less as possible. Hence, only two more components, capacitor C_1 and inductor L_2 , are added to the matching network, as shown in Fig.3(b). In this case, the load impedance at the fundamental frequency can be expressed as

$$Z_L = j\omega L_1 + \text{Re}(Z_A) + j\text{Im}(Z_A) \quad (2)$$

Fig. 4. Simulated load impedances, second harmonic load-pull for -2% and third harmonic load-pull for -0.5% PAE contour

where,

$$\text{Re}(Z_A) = \frac{Y'^2 \omega^2 R L_2^2}{R^2 + \left(\frac{1}{\omega C_1} - Y' \omega L_2\right)^2} \quad (3)$$

$$\text{Im}(Z_A) = \frac{Y'(\omega R^2 L_2 + \frac{L_2}{\omega C_1} - Y' \frac{\omega L_2^2}{C_1})}{R^2 + \left(\frac{1}{\omega C_1} - Y' \omega L_2\right)^2} \quad (4)$$

$$Y' = \frac{1}{1 - \frac{\omega L_2 \tan(\theta)}{Z_0}} = \frac{1}{1 - \frac{\omega L_2}{Z_0}} \quad (5)$$

, where Z_0 and θ are the characteristic impedance and electrical length of the transmission line TL_1 at fundamental frequency. Setting Z_0 at 50 ohm, L_2 and C_1 are derived as 1.1 nH and 2.25 pF.

The simulated load impedance from 4 to 19 GHz is plotted in Fig.4. Compared with the desired impedance plotted in Fig.1(b), the fundamental impedance matches well across the whole band. However, for the second harmonic, the desired impedance moves counter-clockwise with increasing frequency on Smith chart, while the load impedance of the proposed matching network moves clockwise. During the design procedure, the second harmonic load impedance is targeted to match the desired value at the center frequency of 10.8 GHz. Although the complete second harmonic matching cannot be achieved, the simulated load impedances for the second harmonic over the whole band (9.8 to 11.8 GHz) is located within -2% PAE contour. As to the third harmonic, the simulated load impedance is located within -0.5% PAE contour.

III. IMPLEMENTATION AND MEASUREMENT

The PA was fabricated in a 0.25 μm GaN on SiC technology and wire bonded to PCB implemented using RO4350 substrate with 20 mil thickness. Fig.5 depicts the photograph of fabricated die with dimension of $2.2 \times 1.1 \text{ mm}^2$ and PCB. Both the stabilization circuit consisting of R_0 , R_1 and L_3 [8], and high-pass input matching circuit consisting of L_0 and C_0 are integrated on-chip. No external components including RF choke and DC blocking capacitor, are utilized in this PA, thus facilitating full integration of the PA.

A gate voltage of -3 V and a drain voltage of 28 V were chosen for deep Class-AB bias condition, giving a quiescent

Fig. 5. Photo of GaN die and testing board

Fig. 6. Measured S-parameters

Fig. 7. Measured CW performance (a) Psat and maximum PAE versus frequency (b) Gain and PAE versus output power at different frequencies

Fig. 8. (a) Measured average output power and PAE with 802.11ac signals (b) Output spectrum for VHT80, MCS9 signal with -32 dB EVM at 5.21 GHz

current of 14 mA. Small signal S-parameters were measured to validate basic amplification function and input/output matching. The measured S-parameters are shown in Fig. 6, indicating the PA has a small signal gain larger than 9.8 dB from 4.9 GHz to 5.9 GHz. The PA was tested with continuous wave (CW), and the measured saturated output power and maximum PAE are reported in Fig. 7(a). The measured saturated output power and maximum PAE are between 34.6-36.1 dBm and 49.5-61.3% over the 802.11ac band, respectively. The measured power gain and PAE versus output power at 4.9, 5.4 and 5.9 GHz are shown in Fig. 7(b).

To evaluate how the proposed PA performs practically for standard 802.11ac application, the PA was tested using HT20 MCS7 (20 MHz, 64-QAM) and VHT80 MCS9 (80 MHz, 256-QAM) signals without digital pre-distortion (DPD). When satisfying the standard specification of EVM < -32 dB for VHT80 MCS9, PA delivers average output power of

TABLE I
PERFORMANCE COMPARISON BETWEEN THE PROPOSED PA AND OTHER GAN PAs

Ref.	This work	[3]	[7]	[9]	[10]
Freq(GHz)	4.9-5.9	4.8-6.2	5-6	5.2-6.8	5.2-6.2
Psat(dBm)	35-36.2	33	47.7	46	42.1-43
PAE(%)	49.5-61.3	31-51	40-43	51.5-56.5	37-41
Size(mm ²)	2.2×1.1	N.A.	3.2×5.3	12.54	4.5×3.5

23.7-26.3 dBm and achieves PAE of 24.9-30.9%, as shown in Fig. 8(a). Meanwhile, when satisfying the specification of EVM < -28 dB for VHT20 MCS7, average output power and efficiency are between 26.8-29 dBm and 32.9-36.9%, respectively. In addition, the measured output spectrum for VHT80, MCS9 at 5.21 GHz is depicted in Fig. 8(b). Finally, the PA's performance is summarized and compared with other published GaN PAs [9], [10], reported in Table. I.

IV. CONCLUSION

This work introduces a novel broadband harmonic output matching network and discusses the design methodology explicitly. A highly efficient GaN MMIC power amplifier is designed using the proposed matching network. The mechanism of harmonic impedance matching to achieve high efficiency was verified by the measurement results. Besides of high efficiency, the PA exhibits high linearity when tested with standard WLAN modulation signals.

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