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DESIGN AND ANALYSIS OF A 2.4 GHZ VCO WITH FORWARD NOISE REDUCTION THROUGH HYBRID TYPE AUTOMATIC AMPLITUDE CONTROL LOOP

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This paper presents a Voltage-Controlled Oscillator (VCO) with Automatic Amplitude Control (AAC) loop. The proposed AAC VCO employs a hybrid type AAC loop and targets the Industrial, Scientific and Medical (ISM) band applications. The proposed AAC loop can also prevent the AAC from generating extra noise to the VCO and avoid stability problem which is common for conventional AAC loop. Detail transient analysis of this AAC VCO is derived. Based on this analysis, design steps applicable for such type of AAC loop is obtained. Measurement result shows the peak amplitude variation over the operation range of 2.25 GHz to 2.54 GHz is less than 9mV (without the AAC loop, amplitude variation can be as large as 40 mV, or 22.2% for 180mV amplitude). Power consumption of the proposed AAC VCO is 4.5 mW while the power consumed by the loop is 0.8 mW and phase noise is -105 dBc/Hz at 100 kHz offset frequency. Worst case settling time is less than 10.5 μ s.

Keywords: VCO; hybrid type automatic amplitude control loop; transient analysis; design steps.

1. Introduction

Embedding an AAC loop into the VCO of a frequency synthesizer offers several advantages. Firstly, AAC VCO can help to improve the performance of the frequency divider. As shown in Ref. 1, locking range of the injection locking frequency divider is proportional to the power injected. Ref. 2 and 3 also reported for TSPC and ETSPC divider, there is an optimum input DC level and AC amplitude, which comes from VCO's output. With the AAC loop, VCO can provide optimum input amplitude for the divider. This helps the frequency divider to achieve better performance. As introduced in Ref. 4, this property is important for wide band PLL. Secondly, an optimum value of

excess loop gain for VCO can be achieved with AAC loop. This means reliable startup can be achieved. Thirdly, with the AAC loop, the VCO can achieve optimized performance in terms of power consumption and phase noise simultaneously during steady state.

Currently, reported AAC architectures can be divided into two major types. The first one is the digital type, which requires large area and high power consumption. Circuits such as current source arrays, clock signal generator and counter also greatly increases circuit complexity. In addition, the clock signal in the digital approach may introduce extra noise into the VCO's output.⁵ Although the analog approach is relatively simple, it may have stability problem as well as phase noise degradation introduced by the AAC loop.⁵⁻⁸

To overcome the disadvantages of the two AAC types mentioned above while keeping their advantages, a hybrid type of AAC VCO is proposed in this paper. Similar to the conventional AAC structures, the VCO's output is converted to a DC signal. This DC signal varies proportionally according to the variation of the VCO's output amplitude. Conventional analog AAC structures employ an error amplifier to sense the difference between the DC signal and a reference voltage. Output of the error amplifier will then control the bias current to adjust the VCO's output amplitude. As a result, the loop is always closed as long as the VCO is on. This introduces stability problem and cause extra noise feeds into the VCO's output. To overcome this problem, the proposed hybrid AAC structure uses a pair of comparators to compare to digitalize the comparison results between the DC signal and a pair of reference voltages. By doing so, the AAC loop is closed only when VCO's output amplitude is not of the desired level. This means some blocks of the proposed AAC is off in steady state. As a result, total power consumption is reduced. In addition, the proposed hybrid AAC structure uses the comparison results to control a charge pump to adjust the biasing current of the VCO continuously. Hence circuits such as the current source arrays, clock signal generator and counter that are essential for conventional digital AAC structures to adjust the biasing current of the VCO discretely can be avoided. This reduces the circuit complexity and the extra noise introduced by these circuits.

The proposed design is discussed in the following sections. The main blocks and the operation of the AAC loop are introduced in Section 2. Impact of the AAC loop on the VCO's phase noise performance is shown in Section 3. Section 4 analyzed the performance of the Peak Detector (PD). Transient analysis of the AAC loop and the design steps are presented in Section 5. Measurement results of the proposed circuit are shown in Section 6 followed by the conclusion in Section 7.

2. Block Diagram of the Proposed AAC VCO

The schematic of the proposed AAC VCO is shown in Fig. 1. It consists of four main blocks: VCO, PD, Comparator and Charge-pump (CP) with load. The control circuit is formed by the last three blocks. The operation of the AAC circuit is explained as follows.

Firstly, the PD generates a DC signal that indicates the VCO's amplitude level for comparison. Relationship between VCO's amplitude level and this DC signal can be defined by the gain of the Peak Detector, K_{PD} as:

$$K_{PD} = \Delta V_{PD} / \Delta V_{VCO} \quad (1)$$

where V_{PD} is the output voltage of the PD and V_{VCO} is VCO's output amplitude. Two comparators compare V_{PD} with two externally set reference voltages (V_{REF1} and V_{REF2} where $V_{REF1} < V_{REF2}$). A voltage range for the V_{PD} is defined by these two reference voltages. This voltage range $V_{PDRange}$ is converted from the desired range of V_{VCO} (this desired range will be referred to as $V_{VCORange}$ in the following part). Suppose the lower limit of this range is V_{VCO1} and the higher limit is V_{VCO2} , then the following relationship can be obtained:

$$V_{REF1} = V_{PDoffset} + K_{PD} \cdot V_{VCO1}$$

and

$$V_{REF2} = V_{PDoffset} + K_{PD} \cdot V_{VCO2} \quad (2)$$

Fig. 1: Block Diagram of the proposed AAC VCO

The outputs of the two comparators are then used to control the state of CP. Since the output of a comparator can be treated as a state, the CP works as a finite state machine. With proper logic setting, the CP only turns on when the PD's output is not in the desired region (which indicates that the VCO's output amplitude is not in desired region). The DC output of the load C_{CP} is controlled through the CP. This DC output voltage controls the current source of the VCO and will be called " V_{ADJ} " below. V_{ADJ} is connected to M_3 which acts as a secondary current source to provide additional bias current besides R_1 , which is the main current source for the VCO.

In the proposed design, AAC loop is closed only when the PD's output is beyond the desired range $V_{PDRange}$. This means under steady state, AAC loop will not induce

instability. However, this range should be carefully set to balance between the accuracy amplitude locking while preventing self-oscillation.

In the analysis below only the charging case is considered for simplicity (for discharging case, the analysis is almost the same except the sign of current is opposite). Suppose the CP provides constant current I_{CP} when it is on and the V_{ADJ} signal is linearly proportional to I_{CP} , given by:

$$\Delta V_{ADJ} = \frac{1}{C_{CP}} \cdot I_{CP} \cdot t \quad (3)$$

where C_{CP} is the total load capacitance of CP and t is the time of charging.

The relationship between V_{VCO} and the biasing current of the VCO I_B is given in Ref.6 as:

$$V_{VCO} = \frac{4}{\pi} \cdot R_{tank} \cdot I_B \quad (4)$$

where R_{tank} is the tank resistance of VCO.

Suppose the transconductance of M_3 is gm and $\Delta I_B = \Delta V_{ADJ} \cdot gm$. By rearranging Eq. (4), relationship between V_{ADJ} and V_{VCO} can be expressed as:

$$\Delta V_{VCO} = \frac{4}{\pi} \cdot \Delta V_{ADJ} \cdot gm \cdot R_{tank} \quad (5)$$

Substituting Eq. (3) into (5), ΔV_{VCO} can be obtained:

$$\Delta V_{VCO} = \frac{4}{\pi} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot gm \cdot R_{tank} \cdot t \quad (6)$$

The term $I_{CP} \cdot R_{tank} \cdot gm / C_{CP}$ of Eq. (6) determines the rate of change for V_{VCO} . It will be referred to as CR below.

Furthermore, ΔV_{PD} can be expressed as:

$$\Delta V_{PD} = \frac{4}{\pi} \cdot \Delta V_{ADJ} \cdot gm \cdot R_{tank} \cdot K_{PD} = \frac{4}{\pi} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot gm \cdot R_{tank} \cdot t \cdot K_{PD} \quad (7)$$

The role of the CP in the proposed AAC is examined here. In an ideal case, the time delay between the output of the PD start to response and the VCO output's amplitude changes is 0. The procedure of the AAC to achieve locking state can be divided into 3 steps Step I: V_{VCO} reaches the desired level $V_{VCOrange}$, Step II: V_{PD} reaches the region $V_{PDrange}$ and Step III: the CP shuts down and the V_{ADJ} signal keeps its value. In an ideal case, these 3 steps happen simultaneously. In reality Step I and II cannot happen simultaneously since the load capacitor of the PD, C_I , requires a certain time to charge up. Consequently Step III cannot happen simultaneously with Step I either. This means V_{ADJ} will continue to change for a short time and causes the V_{VCO} to keep on changing. If V_{VCO} changes too drastically, it may leave $V_{VCOrange}$ and this may leads to self-oscillation. To

prevent this, the value of C_I and CR should be properly selected. In addition, the value of $V_{PDrange}$ which determines the amplitude locking accuracy cannot be arbitrarily small. This will be further discussed in Section 5. Analysis of K_{PD} and the C_I will be given in Section 4 and the detail analysis on the effect of C_I 's charge up time will be shown in Section 5.

The output of the comparator is expressed in binary form (0 or 1) and it controls the state of CP. When CP is turned on, the magnitude of output current is constant and the direction is determined by the comparison result of V_{PD} with V_{REF1} and V_{REF2} but not the exact value of V_{PD} . So the proposed AAC loop can be treated as a finite state machine. The overall open-loop transfer function can be expressed as:

$$\Delta V_{VCO} = \frac{4}{\pi} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot gm \cdot R_{tank} \cdot t \cdot [(\bar{A} \cap \bar{B}) - (A \cap B)] \quad (8)$$

where A is the logic value of $V_{PD} \geq V_{REF1}$ and B is the logic value of $V_{PD} \geq V_{REF2}$

Since Eq. (8) is state dependent, it cannot be transferred from time domain to frequency domain. In addition, the loop is close only when V_{VCO} is out of the desired range $V_{VCOrange}$ and in this case $\Delta V_{VCO} \neq 0$. Thus although the proposed AAC VCO is similar to the Charge-Pump Phase Lock Loop (CPLL), the close loop frequency domain analysis used for CPLL is not applicable to this AAC loop. Transient analysis will be applied instead.

3. Impact of AAC on VCO's Phase Noise

The focus of this section is on the noise contribution of the AAC components to the VCO's phase noise. Phase noise performance is a major concern for VCO design. It is important to minimize the extra noise introduced by the AAC circuit. In the proposed design, the AAC loop is open when V_{VCO} is within $V_{VCOrange}$, which means noise from both the PD and the comparators do not feed forward, as shown in Fig. 2.

Fig. 2: Direction of the AAC loop noise propagation

To verify this, circuit shown in Fig. 3 is set up for simulation, which the AAC loop is broken at V_{ADJ} . For fair comparison, CP & LPF is connected to a dummy VCO block and the secondary current source of the VCO is connected to an ideal DC source. Voltage of this DC source is the same as the V_{ADJ} in Fig. 2. Compare the simulation results of Fig. 3 with Fig. 2, the oscillation frequency varies by 0.01%, which is negligible. Total noise power increment is 0.3%. The equivalent phase noise difference at 1 MHz offset frequency is 0.03 dB, which is also negligible.

Fig. 3: Circuit set-up with no forward noise propagation

However, since the PD is directly connected to the VCO's output and is always on, the noise generated from the PD feeds back into VCO's output is inevitable, as shown in both Fig. 2 and Fig. 3. This feedback noise consists of both low frequency and high frequency components. Frequency of the later component is at the 2nd harmonic of the VCO's output. With the help of Fig. 4, noise voltage at one of the VCO's output terminal from the PD's output will be:

$$V_{output_noise} = V_{noise} \cdot \frac{C_{gs} \cdot C_{VCO} + C_{gs} \cdot C_{coupling}}{C_{gs} \cdot C_{VCO} + C_{gs} \cdot C_{coupling} + C_{VCO} \cdot C_{coupling}} \quad (9)$$

where V_{noise} is the noise voltage at V_{PD} , $C_{gs1/2}$ is the parasitic gate-source capacitance of M_1 and M_2 , $C_{coupling}$ comes from the coupling AC capacitor inserted between VCO and PD, while C_{VCO} is the capacitance looking into the VCO from its output terminal. The non-linear effect of the varactor and the transistors at the VCO's output upconverts the low frequency component into phase noise^{9,10} while transistors down converts high frequency component. So both the components contribute to VCO's phase noise.

Fig. 4: Simplified schematic showing the noise propagation from PD to VCO

Compared to $C_{coupling}$ and C_{VCO} , C_{gs} is usually much smaller, so the ratio $V_{output_noise}/V_{noise}$ is small and this noise contribution is not so significant. Simulation result shows total noise contribution from the PD to phase noise is about 10%, or equivalent to 0.4 dBc/Hz total phase noise degeneration. However, if the current source of the PD is replaced with a resistor, low frequency component of the noise feedback can be significantly reduced since resistor introduces no flicker noise.

For the VCO designed, without the amplitude locking loop, its amplitude variation can be as large as 40mV (since the amplitude is 180mV, this is equal to 22%) over the whole frequency tuning range. This is significant especially if the VCO is connected to an injection locking frequency divider. According to Adler's locking range figure of merit¹¹, the locking range of an injection locking frequency divider is proportional to the amplitude injected. Simulation shows this amplitude variation would introduce around 15% locking range variation.

4. Peak Detector Design

Besides the amplitude, VCO's output contains other two variables: DC level and frequency. To achieve accurate peak detecting, PD's output should be independent or insensitive to these two variables. Fig. 5 shows the simplified topology of the PD used. An AC coupling structure is added to the input of the PD to shift the input signal's DC level so the DC level of the PD's input is constant. Analysis below will show the PD structure used is insensitive to frequency.

Initially the amplitude of the input signal of the PD is 0 and V_{PD} stabilizes at V_{PD1} . When the amplitude changed abruptly to V_{VCO} , V_{PD} will deviates from V_{PD1} . To simplify the analysis, following assumptions are made: (4-1) The PD is properly biased so that each transistor is on for half cycle of the input signal; (4-2) There is no overlap between the on periods of the two transistors; (4-3) V_{PD} changes only at the end of each input signal cycle and its value is $V_{PD}(n)$ on the n th cycle after the amplitude of the input signal changes. Total charge injected into the capacitor during the $n+1$ th input cycle can be expressed as:

$$Q = 2 \cdot gm_{PD} \cdot \int_0^{1/2f} [V_{VCO} \cdot \sin 2\pi ft - V_{PD}(n) + V_{PD1}] dt \quad (10)$$

where gm_{PD} is the transconductance of each transistor and f is the frequency of the input signal. Changes of V_{PD} at the end of the n th cycle is:

$$V_{PD}(n+1) - V_{PD}(n) = \frac{Q}{C_1} = \frac{2}{C_1} \cdot gm_{PD} \cdot \int_0^{1/2f} [V_{VCO} \cdot \sin 2\pi ft - V_{PD}(n) + V_{PD1}] dt \quad (11)$$

which can be simplified as:

$$V_{PD}(n+1) - V_{PD}(n) = \frac{gm_{PD}}{C_1 \cdot f} \cdot [V_{PD1} - V_{PD}(n) + \frac{2}{\pi} V_{VCO}] \quad (12)$$

Fig. 5: Simplified topology of the proposed Peak Detector

With the initial condition $V_{PD}(0) = V_{PD1}$, $V_{PD}(n)$ can be solved as:

$$V_{PD}(n) = -\frac{2}{\pi} \cdot \left(1 - \frac{gm_{PD}}{C_1 \cdot f}\right)^n \cdot V_{VCO} + \frac{2}{\pi} \cdot V_{VCO} + V_{PD1} \quad (13)$$

The voltage increment of V_{PD} at the end of n th cycle is:

$$\Delta V_{PD-1step}(n) = V_{PD}(n) - V_{PD1} = -\frac{2}{\pi} \cdot \left(1 - \frac{gm_{PD}}{C_1 \cdot f}\right)^n \cdot V_{VCO} + \frac{2}{\pi} \cdot V_{VCO} \quad (14)$$

It is clear that $V_{PD}(n)$ converges only when the absolute value of $1 - gm_{PD}/(C_1 \cdot f)$ is less than 1. Under this condition, it converges at $V_{PD}(n) = 2 \cdot V_{VCO}/\pi + V_{PD1}$. So the gain of the PD can be calculated as:

$$K_{PD} = \frac{V_{PD}(n) - V_{PD1}}{V_{VCO}} = \frac{2}{\pi} \quad (15)$$

which is independent of the frequency and transconductance.

To achieve fast settling, the absolute value of $1 - gm_{PD}/(C_I \cdot f)$ should be close to 0, which means $gm_{PD}/(C_I \cdot f)$ should be set close to 1.

However, the analysis above is based on the ideal model. In practice, assumption (4-1) is not valid and the current source is non-ideal with a resistance R .

To overcome these two limitations, K_{PD} can be re-derived. When V_{PD} finally stabilized at V_{PD2} , (10) needs to be modified as:

$$\begin{aligned} Q &= 2 \cdot gm_{PD} \cdot \int_{\alpha 1}^{\alpha 2} [V_{VCO} \cdot \sin 2\pi ft - V_{PD}(n) + V_{PD1}] dt \\ &= 2 \cdot gm_{PD} \cdot k \cdot \int_0^{1/2f} [V_{VCO} \cdot \sin 2\pi ft - V_{PD}(n) + V_{PD1}] dt \end{aligned} \quad (16)$$

where $\alpha 1$ and $\alpha 2$ indicate the conduction angle and k is a constant which determined by $\alpha 1$ and $\alpha 2$.

When V_{PD} finally stabilized at V_{PD2} , total charge to be injected into C_I during one input cycle is 0. On the other hand, in order to maintain voltage increment of V_{PD} , total charge to be injected into the current source is $(V_{PD2} - V_{PD1})/(R \cdot f)$ during one input cycle. So Eq. (16) can be rewritten as:

$$\begin{aligned} \left(\frac{V_{PD2} - V_{PD1}}{R} \right) \cdot \frac{1}{f} &= \frac{V_{PD}(n) - V_{PD1}}{V_{VCO}} \\ &= 2 \cdot gm_{PD} \cdot k \cdot \int_0^{1/2f} [V_{VCO} \cdot \sin 2\pi ft - V_{PD}(n) + V_{PD1}] dt \end{aligned} \quad (17)$$

Solving this equation, K_{PD} can be expressed as

$$K_{PD} = \frac{V_{PD}(n) - V_{PD1}}{V_{VCO}} = \frac{2 \cdot gm_{PD}}{\pi \cdot (gm_{PD} + \frac{1}{k \cdot R})} \quad (18)$$

Eq. (18) shows that if gm_{PD} is large enough or insensitive to frequency, K_{PD} is independent of input signal's frequency. It is not necessary to pursue larger gm_{PD} since it leads to larger power consumption. For quick estimation, K_{PD} in Eq. (15) will be used below. Fig. 6 shows the calculated value of K_{PD} based on Eq. (15) matches the simulation result.

Fig. 6: Calculated and simulation result of K_{PD}

5. Transient Analysis of the AAC Loop

The following initial conditions and assumptions are made for transient analysis:

- (5-1) The amplitude of the VCO's output is well below the desired range defined as $V_{VCO_{range}}$ initially. This means V_{PD} is also below the lower boundary of $V_{PD_{range}}$ (which is V_{REF1}) and the CP is turned on to increase V_{ADJ} .
- (5-2) V_{ADJ} increment for each cycle of VCO's output is constant when the CP is on. Thus the change of V_{VCO} during each cycle of VCO's output is also constant.
- (5-3) The settling time for amplitude adjustment is long enough, e.g. several micro seconds, compare with period of VCO's output (0.42ns for 2.4GHz), so increment of amplitude can be treated as discrete.
- (5-4) VCO's amplitude only changes at the end of each VCO's output cycle.

Refer to Eq. (6), suppose for each cycle, V_{VCO} increases by $V_{step} = 4 \cdot I_{CP} \cdot g_m \cdot R_{tank} / (\pi \cdot f \cdot C_{CP})$, then at the end of the p -th cycle, the total amplitude increment should be $p \cdot V_{step}$. Ideally at the end of the p -th cycle V_{PD} should increase by $2 \cdot p \cdot V_{step} / \pi$ based on Eq. (15). However, due to the delay between Step I and II introduced in Section 2, the actual response of V_{PD} is more complicated.

The actual PD's output at the end of the p -th cycle can be treated as the superposition of the response of p cycles. As shown in Fig. 7, for the step occurs at i -th cycle, at p -th cycle its response has lasted for $(p-i)$ cycles. Refer to Eq. (14), this means the power n in this equation should be $p-i$. Since the change of V_{VCO} is the superposition of each independent V_{step} at different cycles, the overall response of V_{PD} should be the sum of the response of each V_{step} . Substitute $V_{VCO} = V_{step}$ into Eq. (14), the change of V_{PD} output can be given as:

$$\begin{aligned}
V_{PDtransient} &= \sum_{m=0}^p \Delta V_{PD-1step}(m) \\
&= \sum_{m=0}^p \left[-\frac{2}{\pi} \cdot \left(1 - \frac{gm_{PD}}{C_1 \cdot f}\right)^m \cdot V_{step} + \frac{2}{\pi} \cdot V_{step} \right] \\
&= \frac{2}{\pi} \cdot p \cdot V_{step} - \frac{2}{\pi} \cdot \left[1 - \left(1 - \frac{gm_{PD}}{C_1 \cdot f}\right)^{p+1}\right] \cdot \frac{C_1 \cdot f}{gm_{PD}} \cdot V_{step}
\end{aligned} \tag{19}$$

Fig. 7: Individual steps (left column) and their response (right column)

The difference between Eq. (19) and that of the ideal case, which should be $2 \cdot p \cdot V_{step} / \pi$ is $2 \cdot C_1 \cdot f \cdot [1 - (1 - gm_{PD} / (C_1 \cdot f))^{p+1}] / (gm_{PD} \cdot \pi)$. Refer to assumption (5-3), p is usually in the order of 10k so this voltage difference due to the delay (will be mentioned as V_{delay} below) can be simplified as $2 \cdot C_1 \cdot f / (\pi \cdot gm_{PD}) \cdot V_{step}$. Due to this voltage difference, when V_{VCO} reaches V_{VCO1} , PD's output V_{PD} is still below $V_{PDrange}$ by this V_{delay} . In that case, V_{VCO} will continue to increase even it is already inside $V_{VCOrange}$ until V_{PD} reaches V_{REF1} . Let the final value of V_{VCO} exceeding V_{VCO1} to be V_{extra} . Theoretically, V_{PD} should increase by $2 \cdot V_{extra} / \pi$ after it reaches the lower boundary of $V_{PDrange}$, as shown in Fig. 8. If voltage difference between V_{REF1} and V_{REF2} is smaller than $2 \cdot V_{extra} / \pi$, V_{PD} will increase to higher

than the upper boundary of $V_{PDrange}$ and this would start another amplitude locking process. This may cause the AAC loop to self-oscillate. So the value of V_{extra} should be properly designed to prevent this.

Fig. 8: (a) Change of V_{VCO} (b) and V_{PD}

As mentioned above, when n is large enough, V_{delay} can be simplified as $2 \cdot C_1 f / (\pi \cdot g m_{PD}) \cdot V_{step}$. V_{PD} needs $|C_1 f / g m_{PD}|$ cycles to make up for this V_{delay} . So V_{extra} can be calculated as $|C_1 f / g m_{PD}| \cdot V_{step}$, which means the minimum voltage difference between V_{REF1} and V_{REF2} should be at least $2 \cdot |C_1 f / g m_{PD}| \cdot V_{step} / \pi$.

The proposed AAC VCO is simulated to verify the analysis above. Figure 9 shows the transient waveform of I_{CP} , V_{ADJ} and V_{PD} . In the simulation, V_{REF1} is set to 0.75 V. As shown in the figure, when V_{PD} reaches 0.75 V, I_{CP} drops to 0 and V_{ADJ} stops increasing. However V_{PD} continue to increase exponentially even after I_{CP} drops to 0, as predicted in Eq.(19). The simulation waveform matches the analysis above well.

Fig. 9: Transient response of I_{CP} , V_{ADJ} and V_{PD}

To realize accurate amplitude control, the voltage difference between V_{REF1} and V_{REF2} should be small. This means to minimize $C_1 f / g m_{PD}$. Analysis in Section IV shows $C_1 f / g m_{PD}$ should be smaller but very close to 1, so theoretically the minimal voltage difference between V_{REF1} and V_{REF2} should be $2 \cdot V_{step} / \pi$.

In analysis above, only the charging case is considered. As mentioned previously, the analysis for discharging case is similar except that the sign of the current I_{CP} is opposite. So for discharging case, the final value of V_{VCO} is lower than V_{VCO2} . It is worth to note that V_{extra} can be calculated as $|C_1 f / g m_{PD}| \cdot V_{step}$ thus it is proportional to V_{step} . Since V_{step} is proportional to I_{CP} , V_{extra} is proportional to I_{CP} . If the charging and discharging current

provided by the CP has the same magnitude, the voltage difference between the final value of V_{VCO} and V_{VCO2} is also V_{extra} . If the magnitude of the discharging current is lower, the corresponding V_{extra} is smaller than that of the charging current so that the final value of V_{PD} is still within $V_{PDRange}$ and amplitude calibration is achieved. Conversely, if the magnitude of the discharging current is so large that the corresponding V_{extra} is larger than the voltage difference between V_{VCO1} and V_{VCO2} , V_{PD} will fall below V_{REF1} after the CP is turned off. In that case, CP will be turned on again and start another charging process. Hence the final value of V_{PD} is the same as that of a normal charging process.

It is recommended to set $V_{VCOrange}$ to be $2 \cdot V_{extra}$ and $V_{PDRange}$ to be $4 \cdot V_{step}/\pi$ correspondingly. Theoretically with this setting, the final value of V_{VCO} should be at the center of $V_{VCOrange}$. Consequently, the final value of V_{PD} is at the center of $V_{PDRange}$ rather than near the edge. This gives a $2 \cdot V_{step}/\pi$ voltage margin for V_{PD} to tolerate the variation of V_{PD} or V_{ADJ} due to the noise or charge leakage effect as well as the input offset voltage of the comparator. Using Eq. (7) and ideal value of K_{PD} , relationship between ΔV_{PD} and ΔV_{ADJ} can be expressed as

$$\Delta V_{PD} = \frac{4}{\pi} \cdot \Delta V_{ADJ} \cdot gm \cdot R_{tank} \cdot K_{PD} = \frac{8}{\pi^2} \cdot \Delta V_{ADJ} \cdot gm \cdot R_{tank} \quad (20)$$

If variation of V_{PD} is large enough so that V_{PD} leaves $V_{PDRange}$, self-oscillation will occur. According to Eq. (20), for $2 \cdot V_{step}/\pi$ voltage margin, maximum tolerable ΔV_{ADJ} is $\pi \cdot V_{step}/(4 \cdot gm \cdot R_{tank})$.

Based on this transient analysis, an AAC VCO can be designed in these steps:

- (a) Design and determine the VCO's frequency range and the optimum amplitude range ($V_{VCOrange}$).
- (b) Design the PD and choose the optimum gm_{PD} . gm_{PD} should be chosen with consideration on power consumption of the PD and the K_{PD} . Based on this gm_{PD} and the frequency range of the VCO, choose a proper load capacitance C_I for the PD so that $C_I \cdot f / gm_{PD}$ is close to 1.
- (c) Based on $V_{VCOrange}$ and K_{PD} , calculate $V_{PDRange}$. Refer to Eq. (2), V_{REF1} and V_{REF2} can then be determined.
- (d) Use $V_{PDRange}$ to determine V_{extra} so that $4 \cdot V_{step}/\pi \leq V_{PDRange}$.
- (e) Decide the value of C_{CP} so that ΔV_{ADJ} due to charge sharing effect is less than $4 \cdot V_{step}/(\pi \cdot gm \cdot R_{tank})$.
- (f) Use $V_{step} = 4 \cdot I_{CP} \cdot gm \cdot R_{tank} / (\pi \cdot f \cdot C_{CP})$ to decide CP current I_{CP} and the transconductance of M_3 .

6. Measurement Results of the Proposed AAC VCO

The proposed AAC VCO is fabricated in GlobalFoundries CMOS 0.18 μ m technology. The die photograph of the circuit is shown in Fig. 10. As shown in the photograph large area is occupied by C_{CP} whose value is 200 pF.

Fig. 10: Die photograph of the proposed AAC VCO

Measured frequency range of the proposed AAC VCO is 2.25 GHz to 2.54 GHz. Fig. 11 shows the measured frequency of the oscillation versus amplitude while Fig. 12 shows the measured frequency and the total current consumption (I_{AACVCO}) versus reference voltage V_{REF1} . As expected, the total current consumption increases as the reference voltage increases due to the larger amplitude level.

Fig. 11: Measured oscillation amplitude versus frequency for various values of V_{REF1}

Fig. 12: Measured oscillation frequency and current consumption versus V_{REF1} for various values of V_{tune} Fig. 13: Worst case locking time for V_{ADJ} .

In all measurement, V_{REF2} is set to be 5 mV higher than V_{REF1} . According to Eq. (2), $V_{REF2} - V_{REF1} = K_{PD} \cdot (V_{VCO2} - V_{VCO1})$ and consider $K_{PD} = 2/\pi$, this means the maximum peak amplitude variation is 7.85 mV in ideal case. For all measurement, maximum peak amplitude variation is 9 mV. Frequency variation due to the change of reference voltage

when the AAC is on is less than 5 MHz. Compare with the oscillation frequency of 2.4 GHz, this variation is less than 0.25% , which can be easily tracked by the PLL.

The locking time of the proposed AAC VCO can not be measured, simulation result is shown instead. As shown in Fig. 12, for standard C_{CP} value, the worst case locking time is 10.5 μ s. If we vary C_{CP} , locking time will also be varied. Discharging rate is inversely proportional to C_{CP} , which is expected as shown Eq. (7). Analysis in Section 5 shows that smaller C_{CP} leads to larger V_{step} and predicted if this V_{step} is so large that $2 \cdot [C_I \cdot f / g m_{PD}] \cdot V_{step} / \pi \geq V_{REF2} - V_{REF1}$, then AAC may self-oscillate. This is clearly shown in Fig. 13 when C_{CP} is reduced to 70% of standard value.

As shown in Table 1, compare with other published works, this work achieves comparable FOM. Ref. 13 has a better FOM mainly due to its triode region biased current source VCO design. However this structure requires extra LDO voltage regulator. Hence the circuit will be much more complex and should be carefully designed to avoid stability problem in the AAC loop.

Table 1: State-of-the-art AAC VCO Comparisons

	Ref. 12	Ref. 13	Ref. 14	This Work
Technology (μ m)	CMOS 0.18	CMOS 0.18	CMOS 0.18	CMOS 0.18
Center Frequency (GHz)	7.2	5	3.1	2.4
Phase Noise (dBc/Hz)	-82	-104.8	-102	-105
Offset Frequency	100 kHz	100 kHz	100 kHz	100 kHz
Total Power (mW)	4.32	7.56	1.57	4.5*
FOM	178.2 dB	197.9 dB	191 dB	192 dB

$$FOM = 10 \cdot \log_{10} \cdot \left[\left(\frac{f_0}{\Delta f} \right)^2 \cdot \frac{1}{L \{ \Delta f \} \cdot P_{dc}} \right]$$

*: AAC loop=0.8 mV, VCO core=3.7 mW. Output buffer (for measurement purpose)=6.3 mW

□

7. Conclusion

In this paper, a novel AAC VCO is presented. The proposed AAC VCO employs a novel hybrid type AAC loop and targets for ISM application. It is implemented in 0.18 μ m CMOS technology with on chip LC tank. The proposed AAC loop can also prevent the AAC from injecting extra noise into the VCO and avoid stability problem which is common for conventional AAC loop. Detail transient analysis of this AAC VCO is derived. Based on this analysis, design steps applicable for such type of AAC loop is obtained. Simulation result shows the peak amplitude variation over the operation range is less than 9 mV. Phase noise achieves -105 dBc/Hz at 100 kHz offset frequency. Power

consumption of the proposed AAC VCO is 10.8 mW, where 6.3 mW is consumed by the output buffer for measurement and 0.8 mW is consumed by the loop.

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