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Current-Limited Voltage Control Strategies for Multiple-Input Buck Converters Applied in Renewable Energy Hybrid Systems

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Abstract—Current-limited voltage control strategies (CLVCSs) are required by kinds of renewable energy hybrid systems. For small-scaled loads such as portable electronic devices and electric vehicles, multiple-input buck converters (MIBCs) are the preferred candidate, if introducing renewable energy sources to power them. In this paper, three CLVCSs—*independence CLVCS*, *addition CLVCS*, and *subordination CLVCS*—which are applied in the input-capacitor-added (ICA) MIBC topology, are put forward and compared based on the simulation stage. The results show, when designing the CLVCS structure, the consideration of building up a proper connection of the duty cycles, as the subordination CLVCS did, is able to improve the stability and robustness of the controlled output voltage of the ICA MIBC, whereas at the expense of less control accuracy of limiting the output current of the power source.

Keywords—multiple-input converters; renewable energy hybrid systems; current-limited voltage control

I. INTRODUCTION

In the recent decade, multiple-input converters (MICs) are attracting more and more attentions from the areas of power electronics and renewable energy techniques, because of their irreplaceable advantages such as comparative higher efficiency, less component count, lower cost and simpler control method comparing with those conventional hybrid-used converter structures. Thus, MICs are widely concerned and utilized in field of renewable energy hybrid systems (REHSSs) recently. Renewable energies, or called alternative power sources, such as wind, solar, fuel cells (FCs), etc. possess some specialized characteristics on their electrical properties. For instance, photovoltaic cells have a maximum power point which varies with different external circumstances; fuel cells in high power level have an apparent time-delay features on responding to sudden changes of load demand. Therefore, keeping input currents (or input powers) of these power sources constant or under proper control, when putting them into REHSSs, appears significant to the stability, economy, and efficiency of the entire system.

In the recent several years, researches and studies on control strategy (CS) for MICs are emerging and becoming active. One-cycle control (OCC) for double-input buck

converter (DIBC) was proposed in [1] to eliminate the interactions of the control loops and simplify the design of the controllers. The two control loops are independent of each other and no current regulator is required. The experiments shows the output voltage and the current of the power source 1 are able to be maintained. Multiple-input (MI) SEPIC proposed in [2] is able to successfully perform line and load regulation for both voltage and current simultaneously with a simple decentralized PI control scheme. Without neglecting any cross interactions, several analysis techniques for multivariable control systems are used to assess the nominal stability, nominal performance, robust stability and robust performance of the closed-loop system. The analysis in [3] was based on regulating the output voltage while simultaneously tracking a fixed input power at one source in a multiple-input buck-boost (MIBB) converter with ripple correlation control method. Experimental results show good control performance and correlation of the system. A switching strategy called modified-time-sharing switching technique for MIBB is presented and analyzed in [4]. With this technique, the MIBB can be reduced to an equivalent-single-input converter for analysis and its output voltage can be regulated by a single PI controller. [5] proposed a single inductor MI boost converter combined with an automatic digital control method and a universal tracking algorithm. The function was to deliver maximum power from the various sources into a battery for energy harvesting purpose. The experimental results for a prototype showed the maximum power transferred efficiency was over 95%.

In this paper, three CSs for both control targets (output voltage and input current of one of the two power sources) on an input-capacitor-added (ICA) MI buck converter (MIBC) topology are proposed, analyzed, and compared based on the simulation stage. The following contents are organized as: Section II gives the circuit topology of an ICA double-input buck converter (DIBC), whose operation principle and relevant relational expressions are analyzed as well; In Section III, the three control schemes for the closed-loop linear feedback control system of ICA DIBC are presented; Comparisons among these three methods on their electrical characteristics and control performances are put forward based on the

MATLAB/Simulink environment. Finally, Section V draws the concluding remarks.

II. ICA DIBC

A. Circuit Topology

Compared with other types of MICs (MIBBs, MI SEPICs, MI Ćuks, MI boost converters, etc.), MIBCs have advantages on expected cost and reliability [6], and are very suitable for FCs, wind turbines, and photovoltaic cells to power the loads with relative low voltage such as electric vehicles and portable electronic devices. Therefore, MIBCs are selected in this paper. Taken two power sources for instance, an ICA DIBC topology is proposed as Fig. 1 shows.

Figure 1. Proposed ICA DIBC circuit topology.

Two separated power sources $S\#1$ and $S\#2$ are parallel connected as converter's inputs. The sharing inductor is L . M_1 and M_2 are the MOSFETs, responding for switching on/off of $S\#1$ and $S\#2$, respectively. The gate control signal S_1 is put on M_1 and S_2 on M_2 . Moreover, $S\#1$ ($S\#2$) is parallel connected with a capacitor C_1 (C_2) for being charged by the source when S_1 (S_2) is off and supplying power in company with the source when S_1 (S_2) is on. Therefore, no interrupted current status in operation will come out and the current (or power) control strategy can be implemented. The reference positive directions of voltage or current of each component are assumed and marked in Fig. 1 as well.

B. Operation Principle

The operation principle of the ICA DIBC can be sorted into three modes. The corresponding switching patterns used in the paper are described in Fig. 2. T denotes one switching periodic time.

Figure 2. Switching patterns of ICA DIBC.

The relation of D_1 , D_2 , and D_3 is expressed as

$$\sum_{i=1}^3 D_i = 1 \quad (1)$$

If the system is in stable operation, it can be considered that the variation of inductor current in one operation cycle is zero, thus the following equation therefore can be derived

$$v_o = \sum_{i=1}^2 D_i v_i \quad (2)$$

where v_o denotes the output voltage of ICA DIBC, v_i denotes the output voltage of $S\#i$. From (2), it is clear that v_o is related to both output voltages of the two power sources.

Through the complex derivation and calculation, we also find the mathematical expression for average output current of $S\#1$ with respect to the operation time t , as follows:

$$I_{s1} = \frac{v_{s1} - v_o}{2Lf} D_1^2 + I_{Lmin} D_1 \quad (3)$$

where I_{Lmin} is the initial value at which the inductor current starts to climb in a periodic operation, f is the switching frequency of the gate control signals. One can see from (3) that I_{s1} is determined by D_1 only, assuming v_{s1} , v_o , f , I_{Lmin} and L are constants.

It can be easily verified that to make the two parameters of the DIBC v_o and i_{s1} be under control simultaneously, by finding a proper combination of D_1 and D_2 , is achievable.

III. CONTROL STRATEGIES

As is mentioned in Section I, for high reliability and economical efficiency of a REHS, the output current of the source is expected to be maintained at a desired value point, such as at maximum efficiency point (MEP) of a FC stack, or at maximum power point (MPP) of photovoltaic cells [7-9], in purpose of which we need to propose and design a specific CS. In this paper, $S\#1$ is considered as the master device to provide base-loaded part of the demand, while $S\#2$ is served as a slave device to compensate intermittent or fluctuating rest part. Thus, the CS basically focuses on maintaining the input current of $S\#1$ on condition that v_o is stable. Three closed-loop linear feedback CSs are hereby proposed to realize the target applied in the proposed ICA DIBC topology:

- Independence control strategy (ICS);*
- Addition control strategy (ACS);*
- Subordination control strategy (SCS).*

All the above three strategies apply PI controllers for their regulators and sample the feedback values of v_o and i_{s1} for generating the corresponding gate control signals. The difference lies on the control structures of the three ones. The details on control principles of these three CSs are presented as follows:

A. Independence Control Strategy

As Fig. 3 shows, the control objectives i_{s1} and v_o are controlled by the two independent regulators Re#1 and Re#2, respectively. There is no relation between the two regulators.

Re#1 generates D_1 to take charge of i_{s1} ; Re#2 generates D_2 to take charge of v_o . D_2 is compared with D_1 via a relational operator module in order to prevent S_1 and S_2 from switching on simultaneously. After limited by saturation (D_2), D_1 and D_2 are directly put on S_1 and S_2 as the gate control signals, respectively.

Figure 3. Block diagram of ICS principle.

B. Addition Control Strategy

As Fig. 4 shows, the control objectives i_{s1} and v_o are controlled by the two regulators Re#1 and Re#2, respectively. Re#2 generates D_v to take charge of v_o ; Re#1 generates D_1 to take charge of i_{s1} . Then, D_2 is determined by the following additive relation:

$$D_v = D_1 + D_2 \quad (4)$$

After that and saturation (D_2), D_1 and D_2 are put on S_1 and S_2 as the gate control signals, respectively.

Figure 4. Block diagram of ACS principle.

C. Subordination Control Strategy

As Fig. 5 shows, the control objectives i_{s1} and v_o are controlled by the two regulators Re#1 and Re#2, respectively. Re#2 generates D_v to take charge of v_o ; Re#1 generates D_{1temp} . Then D_1 , which takes charge of i_{s1} , is determined by the following algorithm:

$$D_1 = D_v D_{1temp} \quad (5)$$

Actually, by applying this control algorithm, D_1 can be guaranteed as part of D_v and D_{1temp} represents the degree of this subordination. Then, D_2 is determined by (4) as ACS performs.

Figure 5. Block diagram of SCS principle.

IV. SIMULATION ANALYSIS AND COMPARISON

MATLAB/Simulink simulation software is utilized to build up and emulate the circuit models and their controllers for analyzing and comparing the control and operation performances of the three CSs. The parameters set in the simulation models are listed in Table I.

TABLE I. PARAMETERS SETTING FOR SIMULATION MODELS

Para.	Value	Para.	Value
V_{s1}	35 V	V_{s2}	45 V
f	10 kHz	L	4.225×10^{-5} H
C	1×10^{-3} F	V_{ref}	30 V
I_{ref}	5 A		

A. Load Changes Test

In this test, 3-18-5-1.8-4.5Ω-pure-resistance step load changes with 0.1s-intervals are connected to the DIBC with the three CSs, respectively. The simulation time of one test is set as 0.5 s. Fig. 6 and Fig. 7 illustrate the voltage and current dynamics of the DIBC with the three CSs, respectively. Fig. 8 shows the output power dynamics during 0.2-0.3 s. Furthermore, Fig. 9 gives the details on duty cycles dynamics in the whole test for convenience of analysis.

Figure 6. Voltage dynamics of DIBC with ICS, ACS, and SCS.

From Fig.6, we see, as for the control performance of v_o , the ICS gets the worst result while the SCS obtains the best. The ICS has an over-2V-ripple on v_o during 0.2-0.3 s and many over-1V-ripples during 0.2-0.4 s. From Fig. 10, we conclude the reason is the actual value of (D_1+D_2) is beyond the constraint presented in (1), as the prevention measurement described in Fig. 3, D_2 is restrained to maintain the validity of (1), which breaks the casual relation between D_2 and v_o . The ACS considers the relevance between D_1 and D_2 in (4), resulting better v_o -controlled curve. But from Fig. 9, we see D_1 is bigger than D_v sometimes; D_2 is negative in (4) and no signal outputs in practice due to the saturation module, causing occasional instability on v_o . The SCS, taking both the relevance and the D_2 -negative problems into consideration, gets the most ideal control performance of v_o , however, at the cost of larger ripples of i_{s1} (1 A) than another two CSs' (less than 1 A).

Figure 7. Current dynamics of DIBC with ICS, ACS, and SCS.

Within 0.1-0.2 s, the load demand (18 Ω /1.67 A) becomes lower than I_{ref} (5 A) and the output voltages of the ICS and the ACS are out of control, because D_2 , which is responsible for controlling v_o , reduces to zero. However, v_o is always under control through the SCS, because it changes D_1 into D_v via (5) to control v_o , though D_2 is zero. The overlap phenomenon of D_1 and D_v during 0.1-0.2 s can be observed in Fig. 9.

Figure 8. Output power dynamics of DIBC with ICS, ACS, and SCS during 0.2-0.3 s.

From Fig. 8, one can see the output power response results of the three CSs when the load demand has a step up change (1.67-6 A). The powers have about 18W-overshoots after the load changes in the ICS and the ACS models, while the SCS has a gradual-rise response. That is because the former two models are out of control during 0.1-0.2 s, and the sudden increase of the load demand asks for higher response requirements from the CSs than the SCS one, like a heavy-loaded system startup. On the other hand, the SCS is in operation within 0.1-0.2 s and never stop to output signals in

the test, which makes the power response to the sudden load change more gently. Fig. 9 clearly supports the above analysis.

Figure 9. Duty cycles dynamics of DIBC with ICS, ACS, and SCS.

B. Source Voltage Change Test

In this test, V_{s2} is set to step down by 2 V for 0.01 s and step up back to 45 V at 0.02 s when the DIBC is operating in 200 W, testing its operating stability and anti-disturbance performance. Fig. 10 and Fig. 11 give the output voltage response of the DIBC and the output current response of S#1 by using the three different CSs, respectively.

Figure 10. Voltage responses of DIBC with ICS, ACS, and SCS to a 2V-step-down decrement on V_{s2} at 0.01 s and a 2V-step-up increment on V_{s2} at 0.02 s.

From Fig. 9, we can see the output voltage responses of the DIBC with ICS and ACS have an obvious 0.5V-overshoot when V_{s2} steps down. The SCS one shows no apparent regulating phenomenon. From Fig. 10, we can see all of the three show similar dynamics when V_{s2} changes. Approximate 1.2A-down-pulses appear after 0.01 s, and the SCS one shows longer adjusting time than that in the ICS and the ACS ones. About 1.5A-pulses can be observed at 0.02 s for all of the three CSs.

Figure 11. Current responses of DIBC with ICS, ACS, and SCS to a 2V-step-down decrement on V_{s2} at 0.01 s and a 2V-step-up increment on V_{s2} at 0.02 s.

V. CONCLUSION

The derived relation functions from an ICA DIBC circuit topology indicates that to regulate v_o and i_{s1} simultaneously is needed for achieving advanced control targets in some of the REHSSs, and is available to realize by finding proper combinations of D_1 and D_2 . The three CSs on the DIBC, ICS, ACS, and SCS, were proposed and simulated. The simulations showed the SCS has the most stable and robust v_o -controlled result, and the widest controlling range of v_o , at the expense of larger ripples when limiting i_{s1} . The ICS and the ACS obtained unstable v_o -controlled results, lacking of insufficient considerations on building up the interactive connection between the two duty cycles D_1 and D_2 . Considered all of the above results, the SCS on the ICA DIBC system, for regulating

v_o while limiting i_{s1} , is the best candidate from the proposed three CSs, if the control accuracy on i_{s1} is not required very high.

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