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2017

Zhou, J., Huang, X., Wang, C., Kim, T. T.-H., & Lian, Y. (2017). Energy-efficient digital and wireless IC design for wireless smart sensing. *Journal of Semiconductors*, 38(10), 105005-. doi:10.1088/1674-4926/38/10/105005

<https://hdl.handle.net/10356/105779>

<https://doi.org/10.1088/1674-4926/38/10/105005>

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Energy-Efficient Digital and Wireless IC Design for Wireless Smart Sensing

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Abstract—Wireless smart sensing is now widely used in various applications such as health monitoring and structural monitoring. In conventional wireless sensor nodes, significant power is consumed in wirelessly transmitting the raw data. Smart sensing adds local intelligence to the sensor node and reduces the amount of wireless data transmission via on-node digital signal processing. While the total power consumption is reduced compared to conventional wireless sensing, the power consumption of the digital processing becomes as dominant as wireless data transmission. This paper reviews the state-of-the-art energy-efficient digital and wireless IC design techniques for reducing the power consumption of the wireless smart sensor node to prolong battery life and enable self-powered applications.

I. INTRODUCTION

Nowadays, wireless smart sensing has been widely used in various applications such as health monitoring, smart grid, structural monitoring and wearable devices. These applications require miniaturized sensor nodes for easy installation and deployment. They also require low power consumption for prolonged battery life and reduced battery size. These requirements raise the need for energy-efficient IC design. As shown in Fig. 1, a wireless sensor node (WSN) typically consists of sensors, sensing module, digital control module, power management module and wireless transceiver module. Among these modules, wireless transceiver usually consumes significant amount of power. One reason is that the power required for wireless transmission is large. Another reason is that conventional WSNs usually transmit significant amount of raw data. To reduce the power consumption of wireless transceiver module, energy-efficient wireless IC design need to be investigated. In the meanwhile, various signal processing such as data compression, feature extraction and data analysis can be performed on the sensor node to reduce the amount of data for wireless transmission, which becomes a major difference of wireless smart sensing from conventional wireless sensing. The enhanced digital signal processing capability adds intelligence to the sensor node as well as help reduce the node power consumption.

In this paper, we will review the state-of-the-art energy-efficient digital and wireless IC design techniques for reducing the power consumption of wireless smart sensing to prolong battery life and enable self-powered applications with energy harvesters. Section II reviews the ultra-low voltage digital IC design, including device sizing, level shifter design, SRAM design and variation-resilient design techniques. Section III reviews the energy-efficient wireless IC design,

Fig. 1. Wireless sensor node system

including wireless network topologies, low power wireless standards, low power radio architectures. Section IV draws the conclusions.

II. ULTRA-LOW VOLTAGE DIGITAL IC DESIGN

Conventional low power circuit design techniques such as clock gating, power gating and dynamic voltage scaling are able to reduce the power consumption in digital ICs. However, the amount of power reduction is limited and is difficult to meet the stringent power requirement of wireless intelligent sensor nodes. A promising technique, ultra-low voltage circuit design (also known as near/sub-threshold circuit design), has been shown to be able to reduce energy consumption by 5-10 $\times$ [1][2] while meeting the performance requirement of most wireless intelligent sensing applications. As shown in Figure 1, when the power supply voltage is scaled down from nominal voltage to a voltage in the near/sub-threshold region, the dynamic energy per cycle drops quadratically with the voltage. In the meanwhile, the leakage energy per cycle decreases first and then increases due to exponentially increasing delay in the near/sub-threshold region. The decreasing dynamic energy and increasing leakage energy will balance each other in the sub-threshold region and form a minimum energy point, which is significantly smaller than the energy consumption of nominal voltage operation.

While ultra-low voltage circuit design is promising in reducing energy consumption, significant design effort is needed to ensure the functionality and reliability of circuits in the near/sub-threshold region. Firstly, some cells/blocks in the conventional digital library do not function anymore at ultra-low voltages and have to be re-designed. Typical examples include level shifter and SRAM. Other cells such as logic gates are usually functional at ultra-low voltages but with significantly degraded performance. Device re-sizing is needed for these cells to improve their performance. Other than that, circuits operating at ultra-low voltages exhibit large variations due to exponential relation between current and voltage. This cause substantial design margin in order to meet the timing

Fig. 2. Ultra-low voltage level shifters.

constraint in digital circuits, resulting in much larger power and area overhead compared with nominal-voltage design. Therefore variation-tolerant design techniques are required to reduce the overhead while ensuring the correct timing. In the following sections, the major ultra-low voltage design approaches will be reviewed.

A. Ultra-Low Voltage Device Sizing

It has been found that the logic gates usually do not have functionality problems in near-threshold or non-deep sub-threshold regions [2][3] (deep sub-threshold region is rarely used due to extremely low performance and large variability). However, compared with super-threshold operation, there is performance issue. For example, the PMOS is usually sized around twice as big as NMOS for achieving balanced rise and fall delay. However, in the near/sub-threshold region, the strength ratio of PMOS and NMOS varies a lot due to different current-voltage relation, leading to unbalanced rise and fall delay [2][3][4]. Another issue is that the impact of the parasitic effects becomes different in the near/sub-threshold region. For example, the impact of drain-induced barrier lowering (DIBL) become less due to reduced drain-to-source voltage, and the impact of reverse short-channel effect (RSCE) becomes stronger due to the exponential dependence of current on threshold voltage. Sub-threshold device sizing methods considering the change of current-voltage characteristic and parasitic effects of have been proposed to achieve optimal performance for the near/sub-threshold operation. In [4], RSCE is utilized to boost the current by using non-minimum transistor length. This also mitigates the impact of process variations due to increased transistor area. In [5], inverse

narrow width effect (INWE) is utilized to increase the current by utilizing minimum-size finger. With constant current this results in reduced load capacitance and area. The same device sizing method is combined with minimum sizing in a dual-width sub-threshold standard cell library [6]. The INWE-aware cells are used in critical paths to achieve small delay while the minimum-sizing cells are used in non-critical paths to reduce the power and area. Based on these work, future ultra-low voltage device sizing methods may further explore circuit partitioning and hybrid device sizing method to achieve co-optimized delay, power and area.

B. Ultra-Low Voltage Level Shifter

For ultra-low voltage operation, level shifter is an important circuit for bridging ultra-low voltage domains with other voltage domains. However, the conventional level shifters have issues when operating in the ultra-low voltage region. For example, for the conventional Type I level shifter (based on cross-coupled element) as shown in Fig. (a), when the input voltage is extremely low, the pull-down NMOS cannot overcome the strength of the pull-up PMOS even after heavy upsizing, which will cause functional failures. For the conventional Type II level shifter (based on current-mirror) as shown in Fig. (b), the static source current causes significant standby power, which will diminish the power saving from ultra-low voltage operation. To address these issues, ultra-low voltage level shifters have been proposed. In [7][8] the pull-up network is weakened by using reduced swing inverter (RSI) so as to prevent functional failure in Type I level shifters. However, in this topology the delay is not scalable with supply voltage as the pull-up network is constantly weakened. In [9][10], multi-stage level shifter is used to reduce the effort for wide-range level shifting. This effectively avoids the heavy upsizing of the pull-down NMOS while resulting in increased complexity and relatively long delay compared with single-stage level shifters. In [11], forward body bias is applied to help the level shifting at the price of increased area and power due to body bias control. For Type II level shifter, the major effort are spent on reducing the static current. In [12] the source current is enabled/disabled based on the detection of input transition. This significantly reduce the standby power while increasing the delay and dynamic energy due to the operation of the detection circuits. In [13], feedback control is used to cut off the source current after the output of the level shifter flips. However, the feedback structure causes output drop and charging sharing issues, resulting in non-optimal delay and energy consumption. The issues were addressed in [14] via a revised Wilson-current mirror based level shifter, which also uses mixed- V_T devices to achieve wide-range voltage conversion up to I/O voltage. While focusing on the performance optimization for ultra-low voltage operation, what is missing in the existing work is how to optimize performance over a wide range of supply voltages across sub-threshold and super-threshold region. This needs to be considered especially for wide-range dynamic voltage scaling (DVS) applications.

Fig. 3. Proposed SRAM cell with equalized bitline [16].

Fig. 4. Principle of the equalized bitline [16].

C. Ultra-Low Voltage SRAM

SRAM circuits are heavily used for data storage in digital ICs. Conventional 6T SRAM does not function well at ultra-low voltage. As the supply voltage is extremely low, the SRAM cell is sensitive to read disturbance and a read operation may accidentally change the cell content. Another issue is that the degraded I_{on} -to- I_{off} ratio may cause incorrect bitline sensing. In addition, writing data into SRAM may be a issue due to weak write strength. These issues are further worsened by increasing variability at ultra-low voltage. Some design techniques have been proposed to address the issues. In [15], a 8T sub-threshold SRAM is proposed. It decouples the read port from the write port so that the read disturbance is mitigated. Scaling supply voltage degrades I_{on} -to- I_{off} ratio, which affects read bitline sensing margin. This limits the number of SRAM cells per bitline, maximum temperature, operating supply voltage, etc. One technique to reduce the impact of bitline leakage on sensing is to equalize the bitline leakage. Fig. 3 shows an 9T SRAM that can generate same leakage regardless of the stored data. In unselected SRAM cells, either M7 or M9 is turned on while RVDD and /SEL are grounded. Compared to the conventional bitline sensing (Fig. 4(left)) where sensing margin is affected by the amount of data-dependent bitline leakage, the equalized leakage always provides sensing margin (Fig. 4(right)) with the equalized bitline leakage. In addition to read operation, write operation is critical for reliable ultra-low voltage operation due to weak write strength. Circuit techniques such as boosted wordline [16] and floating supply [16] have been used to improve write margin by enhancing the strength of write path or weakening the strength of the latch in bitcell.

D. Variation-Resilient Design Techniques

PVT variation has been one of the major challenges for digital IC design especially those using advanced technology

nodes. For ultra-low voltage design this becomes more severe. The variability at ultra-low voltages can be up to 100× compared to that for nominal voltage operation due to exponential relation between current and voltage [1], resulting in significant design margin. On-chip timing error monitoring using the replica critical paths and adaptive clock/voltage tuning have been proposed to address this issue, but is not able to deal with the local variations. In [17], razor technique is used to capture the in-situ timing error by a shadow flipflop and correct them through architectural replay. However, this requires the minimal path delay to be increased to differentiate the late arrival and early arrival signals, leading to significant area overhead due to buffer insertion. Also, its application is limited to high performance processors where architectural replay is available. In [18], canary flipflop technique is used to predict the error by monitoring artificially delayed signal. This eliminates the need for increasing minimum path delay. The drawback is there are some errors it cannot correct such as errors caused by fast variation or suddenly activated critical paths. In [19], half-path error monitoring is proposed to address the disadvantages of the razor and canary flipflop techniques. As the error is detected before the clock rising edge. It does not need to differentiate the late and early arrival signals, reducing the overhead of buffer insertion. Also, it is able to deal with errors caused by fast variations and suddenly activated critical path. Another advantage is that it is applicable to any digital designs as the error correction is done through general clock gating. For variation-resilient ultra-low voltage design techniques, the most important considerations include overhead, effectiveness and compatibility with standard design flow, which determine how the technique will be welcomed by major industry.

III. ENERGY EFFICIENT WIRELESS IC DESIGN

After the information from the sensor is acquired using low-power sensor interface circuits and processed via low-power digital circuits, the resulting data should be transmitted wirelessly to a center node. In this section, the state-of-the-art energy efficient wireless solutions will be presented, covering both the system level and the circuit level.

A. Wireless Network Topologies

Depending on how individual sensor nodes are connected to and interact with one another, the topology used in wireless sensing applications varies. The most common network topologies used in any network are star and mesh topologies, as well as a combination of these two.

Fig. 5 shows examples of different network topologies. With star topology, all the sensor nodes are connected to a central node directly. This central node, sometimes called “gateway”, “hub”, “base station” or “aggregation node”, typically has unlimited energy resource (i.e., connected to mains supply), and thus is capable of collecting and processing data from the sensor nodes, and control the operation of the sensors. In such a network, all the sensing nodes must be within the communication range of the central node, and information is transferred without relaying via another node.

With Mesh topology, sensor nodes communicate not only with a central node, but also with one another. Information collected by the sensor nodes is relayed one node to another,

and eventually reach the central node via multiple hops. In contrast to star topology, all sensor nodes need not to be within the range of the central node, and therefore the coverage of the network can be extended. Another feature of Mesh topology is redundancy. As there can be more than one route via which information can be exchanged between a sensor node and the central node, even if some of the nodes stop working (e.g. due to depletion of battery), information can be still relayed from other sensor nodes to the central node. This effectively prolongs the lifetime and enhances the reliability of the network.

In some cases, the network is configured as a hybrid between the star topology and mesh topology. The benefit of such combination is that different nodes can be optimized for different purposes. For example, the backbone of the network can be mesh topology with redundancy and range extension, while the sensor nodes are connected to the backbone directly which reduces the routing overhead and relaxes the radio specifications. This fits well in most applications, where the backbone can be computational heavy while the sensor nodes are energy constrained.

Fig. 5 Network topologies for wireless sensing.

It should be noted that the choice of network topology is not directly linked to the coverage of the network. For short-range

wireless network applications, the Bluetooth standard [20] defines star topology while ZigBee standard [21] defines mesh topology. For long-range networks, star-topology is used in the SigFox [22] and LoRaWAN [23] networks, thanks to the powerful long range base stations and low-rate data transmission.

B. Low-Power Wireless Standards

There are several industry standards that are suitable for wireless sensor network and internet of things applications. The most notable ones are briefly discussed in this section.

Bluetooth® Low Energy (BLE) [24] is often used in wearable consumer devices thanks to the widespread availability of Bluetooth-enabled smartphones. It adopts star network topology, and operates at the 2.4GHz Industrial, Scientific and Medical (ISM) band. The ISM band is partitioned into 40 channels, each separated by 2MHz. The modulation scheme is GFSK, and the data rate is 1Mb/s over the air. Compared to classic Bluetooth, the channel spacing is wider, the data-rate is lower, and the frequency hopping spread spectrum (FHSS) is less frequent, which all relax the specification of the radio hardware and therefore allow power reduction in BLE.

IEEE802.15.4 (15.4) Wireless Personal Area Networks (WPAN) standard [25] has been incorporated in other standard or proprietary networks such as ZigBee [26] and 6LoWPAN [27]. It has many variants, including the 15.4a ultra-wideband (UWB) PHY, 4c and 4d amendment for China and Japan regulations, 4f for active RFID applications, as well as 4g for Smart Utility Network (SUN) applications. As this standard only defines the PHY and MAC layer, the network topology can be either star or mesh, or a combination of both. There are many frequency band covered by the standard ranging from sub-GHz to 10GHz, but in low-power sensor network applications, sub-GHz (780MHz in China, 868MHz in Europe, 915MHz in USA and 930MHz in Japan) and 2.4GHz (worldwide) are most often used due to lower free space loss and lower power consumption in radio front-end compared to higher frequency bands. The channel spacing, modulation scheme and transmitter output power also differs in different amendments of the standard. For example, the original 15.4 standard specifies O-QPSK, BPSK and ASK modulation schemes, while the 15.4g standard specifies FSK modulation. The ZigBee standard is built on top of the original 15.4 standard, and the network topology is mesh. It is often used in short-range wireless sensing applications. For longer range, 802.15.4g-SUN standard can be considered thanks to the constant envelope modulation and lower free-space loss at sub-GHz bands. The 6LoWPAN adds IPv6 network layer on top of the 15.4 PHY and MAC layer, and it is an ideal candidate for applications where sensor nodes need to be addressed over the internet.

The IEEE802.11 WiFi standard is not a traditional contender in wireless sensing applications, but since the introduction of the 11ah amendment, it may be adopted in low-power wireless sensing and internet of things applications. Compared to conventional WiFi networks, 11ah standard specifies lower frequency band (sub-GHz), lower data rates, and longer range [28]. Similar to conventional WiFi [29], the 11ah standard adopts star topology for the end nodes, i.e., all sensor nodes

should communicate with an access point (AP), and the orthogonal frequency division multiplexing (OFDM) / PSK / QAM modulation schemes are also maintained.

For connecting sensors in, on and around human body, one should look at the IEEE802.15.6 Wireless Body Area Network (WBAN) standard [30]. Apart from wireless communication channels from 400MHz Medical Implantable Communications Service (MICS) band to 10GHz UWB, the standard also defines a 5-50MHz human body communication (HBC) band where data is sent and received using human body as a medium by modulating the electric field [31]. Strictly speaking, HBC is not wireless sensing as electrodes need to be attached to the human body, but this can be still considered as a part of a larger wireless body area network. PSK and FSK modulation schemes are specified for 400MHz – 2.4GHz narrowband PHY options for data-rate up to 2Mbps. Similar to the 15.4 standard, the 15.6 standard does not dictate which network topology should be chosen. We have yet to see a lot of wireless sensing applications based on the 15.6 standard.

Beside these low-power short-range wireless standards, there are also standards that cover much longer wider area, i.e., low-power wide area network (LPWAN). SigFox [32] is a company which deploys WPAN that connects wireless sensor nodes in cities. The network uses sub-GHz unlicensed bands such as 868MHz and 915MHz and BPSK modulation with 200Hz bandwidth (ultra-narrowband) to transmit data from the end nodes to the base station up to several km. The network topology is star for the end nodes, and the base stations are deployed by the network operators, which may be SigFox or its partners. Due to this reason, applications adopting SigFox rely on the network infrastructure provided by the network operator, which is only available in certain countries and cities as of the end of 2016. In addition, subscription to the SigFox network is not free, which may be a concern for certain applications. Another potential issue with SigFox is that the sensor nodes have to be stationary during transmission, as the bandwidth is very narrow and transmission takes long time [33].

The LoRaWAN by LoRa (Long-range Radio) Alliance [34] covers similar range as SigFox, but it is rather a standardized technology based on which wireless sensing infrastructures can be built by other companies. Apart from the relative “openness” as compared to SigFox, LoRaWAN also features higher bandwidth (up to 500kHz) and data-rate (up to 50kbps) [34].

Last, it is worth mentioning that cellular network operators are going to launch Long Term Evolution (LTE) Category NB1 (aka NB-IoT) services for internet of things and wireless sensing applications [35] with data-rates up to around 10kbps. In contrast to other standards, it uses licensed spectrum which reduces the chance of interference. However, just like SigFox, users of LTE NB-IoT technology most likely need to pay for subscription, and in some cases also need to apply for license for deploying their sensor networks.

C. Low-Power Radio Architectures

Different standards specify distinct PHY requirements that can only be met with careful architecture choice at the circuit level. In this section, several low-power transceiver architectures are studied.

To achieve the lowest possible power consumption, RF envelope detection receiver is sometimes adopted. Fig. 6 shows the block diagram of a generic envelope detection receiver. The incoming radio signal is downconverted by the envelope detector to baseband without the need for a local oscillator (LO) signal at the radio frequency. The baseband signal can be demodulated by comparing the baseband signal to a threshold voltage via the threshold detector. The low-noise amplifier (LNA) preceding the envelope detector can be removed at the cost of sensitivity degradation. The complexity and power consumption of this type of receivers is the lowest, and receivers consuming below 1 μ W [36][37] have been reported.

Fig. 6 Low-Power Receiver Architecture: Envelop Detection

An envelope detector does not distinguish frequency and phase of the input signal, it suffers from in-band interference at frequencies nearby. In [38], 2-tone envelope detection is introduced which enables in-band interference rejection in such receivers. In [39], the interference rejection is further improved by adding spread-spectrum during the 2-tone modulation. The sensitivity of envelope detection receivers is a trade-off with the power consumption of the LNA, although techniques like uncertain-IF [40] and synchronized-switching [41] can improve the sensitivity without drawing too much current. Despite achieving better sensitivity and selectivity, envelope detection receivers are still seldom used in standard-compliant applications since it does not support channelization or frequency / phase modulation schemes.

Fig. 7 Low-Power Receiver Architecture: Super-regenerative

Super-regenerative receivers (Fig. 7) are similar to envelope detection receivers since they also use an envelope detector to downconvert RF signal. However, it uses a super-regenerative oscillator to convert miniscule, amplitude-modulated RF input signal into high-swing RF signal of the oscillator with either amplitude-modulation (linear mode) or pulse-width modulation (logarithmic mode). Receivers consuming a couple of mW have been reported [42], and with the help of high-Q Film Bulk Acoustic wave Resonator (FBAR), the power consumption can be lower than 1mW [43].

Similar to envelope detection receivers, super-regenerative receivers are limited to amplitude modulation schemes and suffer from in-band interference, even to a higher degree. As

the power consumption is higher than envelope detection receivers, such receivers are less often used nowadays.

Fig. 7 Low-Power Receiver Architecture: Direct Conversion.

To support most standards with frequency or phase modulations while achieving low power, direct conversion receivers (Fig. 7) can be used. The received RF signal is amplified by the LNA, then downconverted to baseband via I/Q mixers with quadrature LO signal. Then the baseband signal is filtered by a low-power filter (LPF) to reject in-band interference, and amplified by a programmable gain amplifier which provides optimal signal level to the analog-to-digital converter (ADC). Demodulation of amplitude, phase and frequency modulated signal can be carried out in the digital domain after ADC.

To achieve low power consumption, the number of high-frequency stages in direct conversion receivers should be minimized. The LNA can be eliminated, and passive mixers can be used as the first stage [44]. In [45] the RF synthesizer is reduced to a free-running ring oscillator with automatic frequency calibration, and the complete receiver consumes only 382.5 μ W. In [46], a 400MHz IEEE802.15.6 WBAN receiver is reported, consuming less than 1.2mW, yet more than half of which is consumed by the RF synthesizer. In [47], the 400MHz LO signal is synthesized by injection locking instead of a phase-locked loop (PLL), so the power consumption can be as low as 38 μ W. Due to the versatile modulation and channelization support, direct conversion receivers are often used in standard-compliant wireless-sensing applications.

Fig. 8 Low-Power Transmitter Architecture: Direct Conversion

At the transmit side, the direct conversion (Fig. 8) and direct modulation (Fig. 9) architectures are two candidates for energy-efficient wireless. Both architectures try to minimize the number of high-frequency / RF stages, so the overall power consumption can be reduced for given output power level. In direct conversion transmitters, the complex digital baseband signals are firstly converted to I/Q analog baseband signals using digital-to-analog converters (DACs), the baseband LPFs are there to reject out-of-band noise and signal aliasing. The analog signals are then upconverted by the quadrature LO signals via the mixers, and then amplified by the power amplifier (PA) after summation. In [48], a direct conversion transmitter delivers -10dBm output Gaussian Minimum Shift Keying (GMSK) modulated signal while consuming 1.77mW, resulting in an overall power efficiency of 5.6%. The constant envelope modulation of GMSK also helps to improve the power efficiency as the PA can operate in nonlinear, high-efficiency region. For the same transmitter, when delivering non-constant-envelope modulation D8PSK signals, the output power drops to -17dBm with similar power consumption.

Fig. 9 Low-Power Transmitter Architecture: Direct Modulation

The direct modulation architecture also eliminates the I/Q baseband and explicit mixers in the transmitter. Modulation is applied directly to the RF synthesizer for frequency / phase modulations (FM / PM), and to the PA for amplitude modulation. It can be further simplified if the modulation scheme is constant envelope, or only amplitude-based. In [49], a direct modulation 2-tone transmitter is implemented with amplitude-only modulation, achieving 27.7% efficiency while delivering -6dBm output power with 0.9mW consumption. In [50], an FSK transmitter is reported with less than 100 μ W power consumption. The FSK modulation is applied by pulling the crystal oscillator at 45MHz, which is then multiplied by 9 using injection locking to the 400MHz MICS band.

Both direct conversion and direct modulation transmitters support most of modulation schemes, and thus can be used in various standard-compliant applications as long as the performance meets the specifications. They suffer from similar issues: as the LO and PA operate at the same frequency, there can be LO leakage to antenna as well as PA pulling [51] of the LO which results in higher error vector magnitude (EVM) and noise. In addition, direct modulation transmitter has limited modulation bandwidth, due to the AM / PM timing mismatch in polar modulation.

IV. CONCLUSIONS

In wireless smart sensor nodes, the power consumption of digital processing and wireless communication are dominant, making energy-efficient digital and wireless IC design important. This paper reviews the state-of-the-art energy-efficient digital and wireless IC design techniques. These techniques are able to reduce the total power consumption of wireless smart sensor nodes to achieve long battery life or enable self-powered operation with energy harvesters

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