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Le, Van Loi; Kim, Tony Tae-Hyoung

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An Area and Energy Efficient Ultra-Low Voltage Level Shifter with Pass Transistor and Reduced-Swing Output Buffer in 65nm CMOS

Van Loi Le, *Student Member, IEEE*, and Tony Tae-Hyoung Kim, *Senior Member, IEEE*

Abstract—This paper presents an ultra-low voltage level shifter (LS) with fast and energy-efficient voltage conversion from the deep subthreshold region to the superthreshold region. The proposed LS achieves better performance and higher energy efficiency by addressing the reduced swing and the slow fall transition issues in prior arts. A novel reduced-swing buffer design is proposed to obtain lower standby power consumption while a pass transistor is used for improving the speed of the fall transition. The proposed LS consists of only 11 transistors occupying $7.45 \mu\text{m}^2$, which occupies the smallest area among the state-of-the-art ultra-low voltage LSs [2-9]. Measurement results from a test chip fabricated in 65nm CMOS technology demonstrate that the proposed LS shows the maximum leakage and speed improvements of $16.3\times$ and $2.7\times$ compared to WCMLS [5]. The proposed LS also accomplishes the maximum switching energy reduction of $8.5\times$ and can convert deep subthreshold voltage as low as 100 mV to the voltage of 1.2 V.

Index Terms—Current mirror, level shifter, low voltage

I. INTRODUCTION

VOLTAGE scaling is one of the most widely used techniques for reducing power consumption in low power digital circuits and systems. In fact, digital cores on today's processors have been increasingly voltage-scaled, and the number of cores has also been significantly increased. For example, the 45nm IA processor in [1] has 48 cores and 8-core voltage domains; necessitating level shifting between different core voltage domains. Therefore, level shifters (LSs) have increasingly become one of the major concerns especially in aggressively voltage-scaled systems.

The major challenge of the conventional cross-coupled LS (Fig. 1 (a)) is the strong contention between pull-up and pull-down networks, which causes functional failures when converting from deep subthreshold to higher voltages. The cross-coupled LS in [2] enables robust voltage shifting from 0.188V to 1.2V by employing a two-stage topology with a reduced virtual supply voltage in the first stage for limiting the contention and facilitating the wide-range voltage conversion. However, this results in large delay and area. The LS in [3]

Fig. 1. Conventional LS designs: (a) cross-coupled LS (b) current mirror LS.

achieves robust and fast voltage conversion from the deep subthreshold to the above-threshold domain by effectively controlling the contention. However, it suffers from high static power and large area. A self-adapting pull-up structure is exploited in [4] so that the LS can convert from the extremely low input voltages to the nominal voltage of 1.8V with low static power, but it comes at the expense of large area and slow conversion speed.

The conventional current mirror LS as shown in Fig. 1 (b) avoids the contention by using a current mirror instead of the cross-coupled structure. However, the static current for maintaining the mirror current results in large standby power when input data consistently stay at the logic 'high' level. Several current mirror LSs [5-9] have been proposed to resolve this major drawback. The Wilson current mirror level shifter (WCMLS) [5] (Fig. 2) uses the feedback transistor M2 to prevent the static current. When the static current is cut off, the voltage swing at node $n1$ is reduced as simulated in Fig. 3; this results in high static current at I2. In addition, the speed of the fall transition also deteriorates drastically due to the input inverter I1 and the charge sharing from node $n2$ to $n3$ via M2 as highlighted in Fig. 3. The LS in [6] uses a logic error correction circuit instead to eliminate the high static current and achieve low standby power, but it suffers from large delay and area penalty. The revised LS in [7] proposes an input-controlled diode chain to avoid the voltage swing issue in WCMLS for

Fig. 2. Wilson current mirror level shifter (WCMLS) [5] utilizing the feedback transistor M2 for preventing large leakage current through M3 and M1 during the high output. However, it still results in the reduced voltage swing at $n1$, causing high static current at I2.

Fig. 3. Simulated behavior of WCMLS showing the reduced voltage swing and slow fall transition issues.

eliminating the static current, but it also induces large area and slow transition speed. A self-controlled current limiter is effectively used in [8] to reduce the standby current. However, this also comes at the price of high delay and large area. The LS in [9] achieves low power by employing a new topology based on the current mirror structure and a level-shifting capacitor. Nevertheless, it still induces large delay and area overhead. Table I summarizes the main shortcomings of the previous ultra-low voltage LSs.

In this paper, we propose an area and energy efficient LS for wide-range level conversion. The proposed LS exploits a novel reduced-swing buffer design to achieve low static power consumption while a pass transistor enhances the speed of the fall transition so that the conversion delay can be significantly improved. In addition, the proposed LS has the smallest area compared to the previous ultra-low voltage LSs [2-9].

II. PROPOSED LEVEL SHIFTER

Fig. 4 illustrates the schematic of the proposed LS for wide-range voltage conversion from deep subthreshold to above-threshold voltages. The key features of the proposed LS are highlighted in Fig. 4. As shown in Fig. 2, the high static current flows at I2 due to the reduced swing $n1$. The novel reduced-swing buffer (M6-M11) suppresses the high static current through M8 by stacking a diode-connected transistor (M7)

Fig. 4. Proposed LS utilizing a reduced-swing buffer design for eliminating the high static current at the output buffer and a pass transistor for speeding up the fall transition.

TABLE I
MAJOR DRAWBACKS OF THE PREVIOUS ULTRA-LOW VOLTAGE LSs

	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]
High Standby Power	NO	YES	NO	YES	NO	NO	NO	NO
Large Delay	YES	NO	YES	YES	YES	YES	YES	YES
Area Overhead	YES	YES	YES	NO	YES	YES	YES	YES

when the output is high. M9 recovers the full voltage swing at node $n3$ and further speeds up the fall transition. In addition, the proposed LS removes the input inverter and uses only one pass transistor (M3) for the fall transition so that the fall transition speed improves significantly. The feedback transistor (M1), added between M2 and ground, prevents the high static current in the current mirror during the high output and avoids the charge sharing problem in WCMLS [5].

Fig. 5 (a) shows the operation of the proposed LS for L→H transition. When IN goes high, M2 is turned on to generate the mirror current through M5. The mirror current charges $n1$, then $n3$ is discharged through M6 and the output goes high. The discharged $n3$ turns off M1 to cut the static current through M2 and M4; this leads to the voltage swing reduction at node $n1$. With the aid of the diode-connected transistor M7 in the reduced-swing buffer, the voltage swing at node $n2$ is also reduced as same as the voltage swing at node $n1$ as shown in the simulated behavior of the proposed LS (Fig. 6). Therefore, the high static current flowing through M8 is eliminated and the proposed LS obtains low standby power.

Fig. 5 (b) shows the operation of the proposed LS for H→L transition. M2 is switched off to disable the mirror current and the pass transistor M3 is turned on for quickly discharging $n1$. Then, $n3$ is fully charged to VDDH with the aid of M9 in the reduced-swing buffer and the output goes low. Fig. 7 compares the simulated behaviors of the proposed LS and WCMLS. The zoom-in waveforms highlight the significantly reduced fall transition delay of the proposed LS. With the use of the pass transistor and the aid of M9, the fall transition delay of the proposed LS is significantly improved compared to WCMLS.

Fig. 5. Operation details of the proposed LS for (a) L→H and (b) H→L transitions.

Table II shows the 2000-point Monte Carlo simulation results for the transition delay of the proposed LS and WCMLS when converting from 0.3 V to 1.1 V. The proposed LS achieves 3.3× smaller mean delay with less variation than WCMLS.

III. MEASUREMENT RESULTS AND COMPARISONS

The proposed LS and WCMLS [5] were implemented in a 65nm CMOS test chip for comparisons. The microphotograph of the test chip and the layout of the proposed LS are depicted in Fig. 8. Measurement results demonstrate that the proposed LS can convert from the deep subthreshold voltages as low as 100 mV to the above-threshold voltage of 1.2 V. Fig. 9 shows the measured waveform of the proposed LS when converting from 200 mV to 1.2 V.

Fig. 10 shows the measured delay of WCMLS and the proposed LS when sweeping VDDL from 0.3 V to 1.0 V and VDDH = 1.2 V. With the use of the pass transistor and the aid of M9, the proposed LS exhibits 2.3× faster delay than WCMLS when converting from 0.3 V to 1.2 V. When VDDL = 0.6 V - 1.0 V, the proposed LS shows up to 2.7× delay improvement compared to WCMLS.

Fig. 11 exhibits the measured leakage power of the two LSs versus VDDL and VDDH = 1.2 V. From the leakage power measurement results, the proposed LS shows the maximum leakage reduction of 16.3× compared to WCMLS when VDDL = 0.6 V. The leakage improvement is achieved by the aid of the proposed reduced-swing buffer design.

Fig. 6. The proposed reduced-swing buffer design creates a voltage reduction at node $n2$ as same as the voltage drop at node $n1$ for preventing the high static current at the output buffer.

Fig. 7. With the use of the pass transistor and the aid of M9, the fall transition delay of the proposed LS is significantly improved compared to WCMLS.

TABLE II

2000-POINT MONTE CARLO SIMULATION RESULTS FOR TRANSITION DELAY

Parameters	WCMLS	Proposed LS
Normalized Mean Delay (μ)	1.00	0.30
Normalized Standard Deviation (σ)	0.50	0.10
Variation (σ/μ)	50.0%	33.3%

Temperature: 27°C

VDDL = 0.3 V

Normalized mean delay and standard deviation: ratio normalized by WCMLS's delay

N = 2000 points

VDDH = 1.1 V

Fig. 12 and Fig. 13 show the measured total power and switching energy per transition of the two LSs over various VDDL values at VDDH = 1.2 V and the input frequency $f_{IN} = 1\text{MHz}$. By exploiting the reduced-swing buffer and the pass transistor for speeding up the fall transition, the proposed LS has shorter transition time than WCMLS without extra transistors. Thus, the proposed LS consumes less power and energy per transition. In terms of total power consumption, the proposed LS shows 5.3× and 8.5× total power improvement vs. WCMLS at VDDL = 0.7 V and VDDL = 1.0 V, respectively. Regarding energy per transition, the proposed LS exhibits 4.5× and 8.5× switching energy reduction over WCMLS when VDDL = 0.3 V and VDDL = 0.8 V, respectively.

Table III compares the proposed LS with the several state-of-the-art ultra-low voltage LSs. With the smallest number of transistors as in [2, 5, 8] and the smallest area among the compared state-of-the-art ultra-low voltage LSs [2-9], the

Fig. 8. Microphotograph of the test chip in 65nm CMOS and layout of the proposed LS.

Fig. 9. Measured waveform of the proposed LS (VDDL=0.2V, VDDH=1.2V).

Fig. 10. Measured delay versus VDDL (VDDH=1.2V).

proposed LS provides the highest level shifting speed. In terms of energy consumption per transition, the proposed LS shows the minimum switching energy compared to the LSs in [4-7]. The LSs in [3, 8, 9] have slightly lower switching energy than the proposed LS, but it comes at the expense of larger delay, area [3, 8, 9], and higher static power [3]. The proposed LS obtains lower standby power vs. the LSs in [3, 5]. Compared to [4, 6-9], the proposed LS has higher leakage power. The main reason for the high leakage power is the difference between the voltage swing at node $n1$ and $n2$. Due to process variations, the voltage swing at node $n1$ and $n2$ are not relatively close as simulated. It leads to considerable leakage at the output buffer. One possible solution is to analyze the effect of process variations on the voltage reduction at node $n1$ caused by the

Fig. 11. Measured leakage power versus VDDL (VDDH=1.2V).

Fig. 12. Measured total power versus VDDL (VDDH=1.2V).

Fig. 13. Measured energy per transition versus VDDL (VDDH=1.2V).

feedback transistor M1 and the reduced swing at node $n2$ due to the diode-connected transistor M7 through extensive Monte Carlo simulations. Thus, a better sizing strategy could be achieved for improving the robustness of the similarity between the voltage swing at node $n1$ and $n2$ over the process variations, significantly reducing leakage power. The LS in [4] shows the lowest static power among all of the compared LSs. However, it comes at the price of large delay, switching energy and area. The LSs in [6-9] also have lower static power compared to the proposed LS, but they have slower speed, larger area [6-9], and higher switching energy [6, 7].

TABLE III
MEASUREMENT COMPARISON OF THE PROPOSED LS AND THE STATE-OF-THE-ART ULTRA-LOW VOLTAGE LSS

Parameters	Proposed LS (This work)	S. Lütkeimer, TCAS-II 2010 WCMLS [5] *Re-implemented	Y. Osaki, JSSC 2012 [6]	J. Zhou, TCAS-I 2015 [7]	L. Wen, TCAS-II 2016 [8]	M. Lanuzza, TVLSI 2015 [3]*Post layout	M. Lanuzza, TCAS-II 2017 [4]	E. Maghsoudloo, TCAS-I 2017 [9]	S. N. Wooters, TCAS-II 2010 [2]
Technology	65nm	65nm	350nm	180nm	65nm	90nm	180nm	180nm	130nm
Conversion range	0.1V - 1.2V	0.1V - 1.2V	0.23V - 3V	0.21 - 3.3V	0.1V - 1.2V	0.1V - 1V	0.1V - 1.8V	0.33V-1.8V	0.188V-1.2V
Type	Current mirror	Current mirror	Current mirror	Current mirror	Current mirror	Cross coupled	Cross coupled	Current mirror	Cross coupled
Strategy	Reduced-swing buffer and pass transistor	Feedback control	Logic error correction	Input-controlled diode chain	Self-controlled current limiter	Self-adapting pull-up network	Self-adapting pull-up network	Level-shifting capacitor	Double stages with reduced virtual supply
Transistor count	11	11	16	18	11	15	14	13	11
Delay (ns) @VDDL	7.5 @0.3V	17.5 @0.3V	10000 @0.4V	186.3 @0.3V	13.7 @0.2V	16.6 @0.2V	31.7 @0.4V	29 @0.4	57.9 @0.2V
Energy per transition (fJ) @VDDL - f_{IN}	123.8 @0.3V-1MHz	552 @0.3V-1MHz	5800 @0.4V-0.01MHz	954 @0.3V-0.1MHz	90.9 @0.2V-1MHz	77 @0.2V-1MHz	173 @0.4V-0.1MHz	61.5 @0.4V-0.5Mhz	N.A.
Leakage power (nW) @VDDL	2.64 @0.3V	20.4 @0.3V	0.23 @0.4V	0.97 @0.3V	1.24 @0.2V	8.7 @0.2V	0.055 @0.4V	0.33 @0.4V	N.A.
Cell Area (μm^2)	7.45	9.94	1880	153.01	31.3	37.3	108.8	229.5	96

By utilizing the reduced-swing buffer design for preventing the high static current, the proposed LS significantly reduces the standby power compared to WCMLS [5]. In addition, the use of the pass transistor considerably shortens the transition delay and minimizes the switching energy. Compared to the recently proposed ultra-low voltage LSs [2-9], the proposed LS has the highest level shifting speed with the smallest number of transistors and the smallest area.

IV. CONCLUSION

In this paper, we presented a novel fast and energy-efficient LS for wide-range voltage conversion from the deep subthreshold voltage as low as 100mV to the above-threshold voltage of 1.2V. By exploiting the reduced-swing buffer design for eliminating the high leakage current and the pass transistor for speeding up the fall transition, the proposed LS significantly improves the conversion speed and reduces static power consumption. Measurement results from a test chip fabricated in 65nm CMOS technology demonstrate that the proposed LS achieves the maximum leakage and delay reductions of 16.3 $\times$ and 2.7 $\times$ compared to WCMLS. The proposed LS also exhibits the maximum switching energy reduction of 8.5 $\times$. In addition to the power and speed improvements, the proposed LS occupies only 7.45 μm^2 , which is the smallest area among the compared state-of-the-art ultra-low voltage LSs [2-9]. Therefore, the proposed LS is applicable to many low-power digital systems where multiple aggressively scaled voltage domains are employed for power and energy efficiency.

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