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Single-Event-Transient Resilient Memory for DSP in Space Applications

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Abstract—We present a radiation-hardened-by-design (RHBD) memory design that mitigates Single-Event-Transients (SETs), Single-Event-Upsets (SEUs) and Dual-Event-Upsets (DEUs), hence significantly enhancing the reliability of digital signal processors (DSPs) for space applications. We achieve these attributes by combining a Triple-Interlocked Cell (TICE) SRAM cell array and a Triple Modular Redundancy (TMR) voter. The TICE SRAM cells therein self-correct SEUs and DEUs. The TMR voter eliminates SETs. Our proposed RHBD TICE SRAM cells integrated with the TMR voter are also hardened by the layout/sizing RHBD practices. By means of the 128x9-bit memory implementation @ 65nm CMOS, we show that our memory design is inherent SEU- and DEU-tolerant, and has 94.83% SET reduction and 92.05% Triple-Event-Upset (TEU) reduction when compared to the memory design embodying the 8-transistor (8-T) SRAM cells.

I. INTRODUCTION

Space exploration, including commercial space business, has been recently and actively fueled not only by governments but also by private industry. Over the past few years, there has been a significant increase in number of satellites launched into space. To enhance the success rate for satellites to complete their critical mission, one of the key considerations is the onboard data processing capabilities [1]-[2]. This has led to using high performance digital signal processors (DSPs) which are unfortunately highly sensitive to radiation-induced soft errors [3]. Radiation-induced soft errors are generally based on the assumption of a single event effect. These include Single-Event-Upsets (SEUs) and Single-Event-Transients (SETs). SEUs are soft errors where the logic states (in sequential logic) [3] are changed by high-energy radiation particles. On the other hand, SETs are unwanted transient disturbances [4] which can cause the DSPs to malfunction, thus leading to SEUs or system deadlock. Due to shrinking feature size of transistors the occurrence of multiple events (multiple upsets) effect has increased [5]. These include dual-event-upset (DEU) and triple-event-upset (TEU).

It is important to enhance the reliability of memories inside the DSPs in satellites as they constantly store crucial intermediate data which are to be processed [6]. For example, if the storing coefficients (in memories) such twiddle factors, filter coefficients, etc., are corrupted, then DSPs could no longer perform their functions. Unfortunately, the memories are highly susceptible to soft errors including SEUs and/or

SETs. To mitigate these soft errors in memory, the design techniques for radiation-hardening, also known as Radiation-Hardened-By-Design (RHBD), are popular, ranging from the architecture level down to the circuit level and the transistor/layout level. The architecture level RHBD techniques include Triple-Modular-Redundancy (TMR) [8] and Error-Detection-and-Error-Correction (EDAC). The circuit level RHBD techniques include Dual-Interlocked-Cell (DICE) [9] and other RHBD memory cells [8]-[12]. The transistor/layout level includes transistor-up sizing, and special layout practices [3], [17]-[18]. These RHBD techniques generally incur overheads (than unhardened counterparts) and can enhance either SEUs or SETs but not both. Furthermore, when there are multiple upsets [9], memories remain vulnerable despite embodying these RHBD practices.

In this paper, we propose a SET-reduced cum DEU-tolerant RHBD memory for DSPs used in mission-critical satellite/space applications. We realize our RHBD memory in the following ways. First, we apply Triple-Interlocked Cell (TICE) memory cells [14] to prevent two event upsets or called DEU. Specifically, a TICE memory cell can self-correct up to two simultaneous upsets. To mitigate SET, we apply a TMR voter for the read outputs of TICE memory cells. To further enhance the overall reliability, we apply layout techniques to place the critical nodes [13] in TICE memory cell as far as possible. This reduces the possibility of the critical nodes being hit simultaneously, under the assumption that three simultaneous upsets are rarely occurred. We consider transistor up-sizing to protect the TMR voter, hence mitigating SET occurrence on the TMR voter itself. When compared to the standard 8-T memory cell and DICE memory cell, our proposed memory cell has the highest radiation hardness characteristics.

We realize a 128x9-bit RHBD memory @ 65nm CMOS process, and show that it is guaranteed SEU and DEU tolerant. When compared to the memory embodying standard 8-transistor (8-T) SRAM cells, our proposed memory design has 94.83% SET reduction, and 92.05% reduction in TEU.

This paper is organized as follows. Section II reviews the conventional SRAM cells and their read output buffer. Section III describe our proposed memory design embodying TICE SRAM cells and TMR voters associated with the read output buffer. Section IV presents our memory design implementation and the results. Finally, conclusions are given in Section V.

II. REVIEW: MEMORY CELL

Figs. 1 (a) to (c) depict the conventional 8-transistor (8T) SRAM cell, a conventional DICE SRAM cell [9] and a conventional TICE SRAM cell [14]. These 8T, DICE and TICE SRAM cells embody a read-decoupled port for better read static noise margin [16]. The 8T, DICE and TICE SRAM cells have 8 transistors, 14 transistors and 20 transistors respectively.

Fig 1: (a) 8-T SRAM cell, (b) Dual-Interlocked Cell (DICE) SRAM cell, and (c) Triple-Interlocked Cell (TICE) SRAM cell

The 8T SRAM cell is generally weak to both SETs and SEUs. The DICE SRAM cell has SEU-hardening at the circuit level. This is because the nodes 1 and 3 form an interlocked pair, and the nodes 2 and 4 form another interlocked pair as shown in Fig. 1(b).

In each pair, if one of the nodes is struck by radiation particles causing a temporary error, the other node will self-correct the error except in case of the interlocked pairs being simultaneously struck by irradiation. In short, the DICE SRAM cell is SEU-tolerant but not DEU-tolerant. The TICE SRAM cell is more structurally SEU and DEU hardened than the DICE SRAM cell. This is because, instead of two nodes in

the latter, the former now have 3 nodes to form an interlocked group. Particularly, from Fig. 1 (c), the nodes 1, 3, and 5 form an interlocked group, and the nodes 2, 4, 6 form the other interlocked group. In each group, a permanent error only occurs if all nodes within the group are affected simultaneously, or otherwise the unaffected node(s) will self-correct any possible error. In short, the TICE SRAM cell is DEU-tolerant but not TEU tolerant.

Fig. 2 depicts the output buffer connected with a memory array embodying SRAM cells; all 8T, DICE and TICE SRAM cells are applicable. The output buffer is merely a dynamic logic output circuit. When $En = '0'$, there is no read operation, and the output OUT is '0'. When $En = '1'$ for a read operation, the read decoupled port will discharge RBL for OUT to be '1' or otherwise to be '0' kept by the weak PMOS feedback transistor. Unfortunately, the output buffer is vulnerable to SETs, hence the overall memory embodying either 8T or DICE or TICE SRAM cells remain vulnerable to SETs.

Fig 2: The output buffer for the memory array

III. PROPOSED MEMORY DESIGN

We propose to integrate the TICE SRAM cell into a TMR voter, making the overall memory both SEU and DEU tolerant. Fig. 3 depicts our proposed TICE SRAM cell which has two additional read decoupled ports (when compared to the conventional TICE SRAM cell depicted in Fig. 1 (c)).

Fig 3: Proposed TICE SRAM cell with three read-decoupled ports

Fig. 4 depicts the output buffer having a TMR voter embedded inside. The three read-decoupled output ports are connected to the output buffers, followed by a TMR voter. Now all output buffers (including all digital voters) and the memory array(s) are closely integrated in the memory. The advantages of this integrated memory design include small areas (as many circuits are closely integrated) with good high reliability (due to its voting mechanism to self-correct SETs, SEUs and DEUs). We now explain why the proposed TICE SRAM cell(s) with the TMR output buffer are collectively to mitigate SETs, SEUs and DEUs.

Fig 4: Proposed TMR output buffer for the memory array

First, the proposed TICE SRAM cell is effective to mitigate SEUs (i.e. single event) and DEUs (dual events). Hence, the probability of having an upset is extremely low. Second, the TMR voter is effective to filter any SETs, whether they are induced in the any of the read-decoupled ports or at the proposed TICE SRAM cell per se.

We remark that the TMR voter (e.g. the AND and OR gates) and the inverters must be radiation-hardened or otherwise SETs are still possibly induced. To make the TMR voter and the inverters to have high radiation hardness, we adopt transistor up-sizing, making their aspect ratio large.

We realize our RHBD memory design using a commercial 65nm CMOS process. Fig. 5 depicts the layout view of our proposed TICE SRAM cell with three read-decoupled ports. The area of the SRAM cell is $6.2\mu\text{m} \times 4.45\mu\text{m}$. We also adopt the layout-level RHBD practices [17]-[18] to realize the TICE SRAM cells. Particularly, guard rings are used to mitigate

single-event-latch-up and isolation. The guard rings for the SRAM cell are shown in the thick (dark green) lines.

Fig 5: Layout view for our proposed TICE SRAM cells where layout-level RHBD practices are used

The nodes shown in the odd number (blue) are within a pair/group, and those shown in the even number (purple) are within another pair/group. The nodes within the same pair/group are placed in different (isolated) guard ring regions, minimizing the SEU error possibility on the cell because radiation particles might only be localized in the area near one node therefore not affecting other.

IV. IMPLEMENTATION AND RESULTS

We realize a 128x9-bit memory design (@65 nm CMOS process) embodying our proposed TICE SRAM cells and the TMR output buffer. We partition the memory array into two blocks, even and odd. The data-width is 8-bit and 1 parity bit. This memory design is targeted for a mission-critical microcontroller for satellite applications. Figs. 6 (a) and (b) depict the layout view and the microphotograph of the prototype chip.

Fig 6: 128x9-bit RHBD memory embodying our TICE SRAM cells and TMR Output buffer: (a) layout view and (b) microphotograph for the prototype

For comparison, we also designed two 128x9-bit memories embodying the 8-T SRAM cells and the DICE SRAM cells.

RHBD practices, including layout-level practices, are similarly applied. Table I tabulates several characteristics of the 128x9-bit memories embodying the conventional 8-T SRAM cells, the DICE SRAM cells, and our proposed TICE SRAM cells integrated with TMR voter (TICE+TMR Memory). Where applicable, their results are normalized with respect to that embodying the 8-T SRAM cells (which are not SET and SEU hardened), and the normalized results are shown in the parenthesis.

As expected, the silicon area of the memory embodying the 8-T SRAM cells is the smallest, followed by that embodying the DICE SRAM cells, and the largest for TICE+TMR Memory. Specifically, the memory embodying the DICE and the TICE+TMR memory are respectively 1.33× and 1.79× bigger than that embodying the 8-T SRAM cells. Not unexpectedly, in most cases, in terms of electrical characteristics (e.g. speed, power), the memory embodying the 8-T SRAM cells is the most competitive, followed by that embodying the DICE SRAM cells, and the least competitive for the TICE+TMR memory.

It is also of interest to remark that the TICE+TMR memory has a better write delay than the memory embodying the DICE SRAM cells. This is largely because a TICE SRAM cell has three writing paths (instead of two writing paths in a DICE SRAM cell), hence reducing the charge-fighting feedback when all the three writing paths are turned simultaneously.

To qualify the radiation hardness – one important figure-of-merit for this work, we define a hardness factor (F), as the ratio of the sensitive drain/source areas of the transistors over the total drain/source areas of the transistors as shown in Equation (1) below, n is the number of upset events.

$$F = \left(\frac{\text{Sensitive cross - section area}}{\text{Total drain/source cross - section area}} \right)^n \quad (1)$$

The sensitive drain/source areas are defined as the diffusion area when hit by radiation particles can result in SETs or SEUs at the given output logic. The total drain/source areas are the all diffusion areas except those connected to V_{DD} or Gnd. The memory embodying 8-T SRAM cells is prone to SETs, SEUs, DEUs and TEUs. The memory embodying the

DICE SRAM cells is slightly less prone to SETs and SEUs, but not to DEUs and TEUs.

However, the probability of 2 bit upset on 1 and 3 or 2 and

4 nodes simultaneously are highly unlikely which is evident from Table II. The hardness factor F for DEUs for DICE is 71.8% lower than 8T SRAM cell but the DICE SRAM is still vulnerable SETs (only marginally 3.34% lower than 8T SRAM cell). Similarly, the TICE+TMR memory is only prone to TEUs (3 event upsets simultaneously) when striking on nodes 1, 3, 5 or 2, 4, 6 simultaneously; see Fig. 3.

Since the TICE SRAM cell is integrated with the TMR voter SET on one or two nodes are not seen on the output. Moreover, the voter is designed to mitigate SETs due to strike on the TMR voter itself as explained in Section II. The only way to cause an SET on the proposed design is if a TEU occurs and the likelihood of that happening extremely unlikely which is evident from Table II. The hardness factor F for SETs on TICE+TMR memory is 94.83 % lower than that of 8T SRAM cell and similarly the chances of an TEU is 92.05% lower than that of 8T SRAM cell.

Compared to memories embodying 8T and DICE SRAM cells the proposed TICE+TMR memory not only can mitigate SEUs and DEU but also reduces the chances of SETs occurrence significantly, thus making it a very highly reliable memory for DSP used in mission-critical satellite/space application.

V. CONCLUSIONS

A new SRAM memory was proposed by integrating TICE-SRAM cell with TMR voter (TICE+TMR). A 128x9-bit memory was realized using the proposed TICE+TMR memory and compared with two other similar 128X9-bit memories constructed using 8T-SRAM and DICE-SRAM cells respectively. Although considering conventional performance parameters of the memories embodying the 8T and DICE SRAM cell are better, it has been shown that the proposed TICE+TMR memory is free from SEUs, DEUs and least prone to SETs and TEUs. Therefore, it is the best radiation hardness characteristics memory candidate to be used in mission-critical DSP for satellite/space applications.

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TABLE I:

COMPARISON OF THREE 128X9-BIT MEMORIES EMBODYING 8T SRAM CELLS, DICE SRAM CELLS AND PROPOSED TICE SRAM CELLS +TMR VOTER

	Process	Voltage	RHBD Layout	Power @ 1MHz	Read Delay	Write Delay	Area
8T	65nm	1.2V	Yes	2.9uW (1.0×)	0.78ns (1.00×)	1.67ns (1.00×)	47704um ² (1.00×)
DICE	65nm	1.2V	Yes	7.8uW (2.7×)	0.90ns (1.15×)	2.30ns (1.38×)	63368um ² (1.32×)
TICE + TMR	65nm	1.2V	Yes	11.9uW (4.1×)	1.07ns (1.37×)	2.16ns (1.29×)	85224um ² (1.78×)

TABLE II:

RADIATION HARDNESS CHARACTERISTICS OF THE THREE 128X9-BIT MEMORIES EMBODYING 8T SRAM CELLS, DICE SRAM CELLS AND PROPOSED TICE SRAM CELLS +TMR VOTER

	SET	SEU	DEU	TEU
8T	0.4340	0.282	0.2820	0.2820
DICE	0.4193 (3.34% ↓)	0 (100 % ↓)	0.0795 (71.80 % ↓)	0.0795 (71.80 % ↓)
TICE + TMR	0.0224 (94.83% ↓)	0 (100 % ↓)	0	0.0224 (92.05 % ↓)

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