Energy-efficient spread second capacitor capacitive DAC for SAR ADC

Kim, Ju Eon; Lee, Sung-Min; Yoo, Taegeun; Jo, Yong-Jun; Baek, Kwang-Hyun

2017

Kim, J. E., Lee, S.-M., Yoo, T., Jo, Y.-J., & Baek, K.-H. (2017). Energy-efficient spread second capacitor capacitive DAC for SAR ADC. *Journal of Semiconductor Technology and Science*, 17(6), 786-791. doi:10.5573/JSTS.2017.17.6.786

<https://hdl.handle.net/10356/106771>

<https://doi.org/10.5573/JSTS.2017.17.6.786>

© 2017 The Author(s) (published by The Institute of Electronics and Information Engineers).
This is an open-access article distributed under the terms of the Creative Commons
Attribution License.

Downloaded on 26 Apr 2023 18:59:48 SGT

Energy-efficient Spread Second Capacitor Capacitive DAC for SAR ADC

Ju Eon Kim¹, Sung-Min Lee¹, Taegeun Yoo², Yong-Jun Jo¹, and Kwang-Hyun Baek¹

Abstract—An energy-efficient capacitive digital-to-analog converter (C-DAC) switching with spread second capacitor is proposed for low power successive approximation register analog-to-digital converters (SAR ADCs). In the proposed spread second capacitor capacitive digital-to-analog converter (SSC C-DAC), all capacitors except the most significant bit (MSB) capacitor are switched after the second bit decision. Because the burden of the second capacitor switching is shared with all capacitors except the MSB capacitor, the number of unit capacitors and the burden of driving V_{CM} are reduced. The proposed SSC C-DAC achieves 98.1% more efficient switching energy and can be comprised of the number of quarter unit capacitors, contrary to that in conventional schemes. The fabricated differential-type SAR ADC with SSC C-DAC has a 10-bit resolution and 10-MS/s sampling speed in 0.18- μm CMOS process. The test results show a SFDR of 60.9 dBc, a SINAD of 53.1 dB and an ENOB of 8.5 bit.

Index Terms—Low power, energy efficient DAC, SAR ADC, capacitive DAC, switching energy

I. INTRODUCTION

Successive approximation register analog-to-digital converters (SAR ADCs) are preferred for low-power

applications such as wearable and biomedical sensor systems because of its simple architecture. Although the semiconductor fabrication processes have evolved considerably over the years, the analog blocks of ADCs cannot fully take advantage of the advanced technology and remains as power-hungry components because of accuracy and speed requirements. Therefore, studies for reducing the switching energy of the capacitive digital-to-analog converter (C-DAC) which is the most power consuming block of SAR ADCs have been published and these efforts have led to the development of various switching schemes of C-DAC [1-11]. These trials are based on the fact that switching energy is proportional to capacitance as expressed by the equation below (1) [1].

$$E = -CV_X (V[2] - V[1]) \quad (1)$$

The switching energy (E) is required when the potential difference of capacitor (C) is changed from $V[1]$ to $V[2]$ and V_X is reference voltage on bottom plate of each capacitor. Therefore, the effective method to decrease total switching energy of C-DAC for SAR ADCs is reducing the switching energy required by switching capacitors that have relatively larger capacitance among the capacitors array [2].

Fig. 1 shows the energy efficient switching on the first and the second conversion steps of previous C-DACs [2]. In this scheme, the most significant bit (MSB) ($2C$) capacitor is switched from ground to V_{REF} in the first conversion step and no switching energy is consumed. Subsequently, the MSB capacitor is switched from V_{REF} to $V_{CM}(V_{ref}/2)$ or the second MSB ($1C$) capacitor is switched from V_{REF} to ground in the second conversion, where a switching energy of $0.25CV_{REF}^2$ and $0.75CV_{REF}^2$

Manuscript received Jun. 6, 2017; accepted Nov. 19, 2017

¹ School of Electrical and Electronics Eng., Chung-Ang University, 84 Heukseok-ro, Dongjak-gu, Seoul, Korea

² School of Electrical and Electronic Eng., Nanyang Technological University, Singapore

E-mail : kbaek@cau.ac.kr

Fig. 1. Energy efficient switching on first and second conversion step in previous scheme [2].

is consumed for each case, respectively. However, switching the largest capacitor (2C) from V_{ref} to V_{CM} causes a large size (W/L) switch.

II. ARCHITECTURE

In the proposed spread second capacitor capacitive digital-to-analog converter (SSC C-DAC) scheme, all capacitors except the MSB capacitor are switched at the second conversion step. Fig. 2 shows the examples of the second conversion for the proposed SSC C-DAC. Each case shows two switching cases after the second comparison. In the second conversion step, all bottom node voltages of the capacitors except for the MSB capacitor are switched from V_{REF} to V_{CM} , which results in a $1/4V_{REF}$ voltage change at the top plate of the capacitors ($V_{Y2} = V_{X2} - 1/4V_{ref}$). Fig. 3 shows the examples of the switching procedure of a 4-bit SSC C-DAC. At the sampling phase, all capacitors except the MSB capacitors are connected to V_{REF} , and the MSB capacitors are connected to ground. The sampling phase is then followed by the conversion phases. At the first conversion step, the bottom plate of the MSB capacitor in the capacitive array that has a lower top plate voltage (V_N or V_P) is switched from ground to V_{REF} . For simplicity, only one case ($V_P - V_N > 0$) is shown. The first conversion step does not require switching energy. At the second conversion step, the bottom plates of all

Fig. 2. Block diagram of the proposed transmitter.

capacitors except the MSB capacitor of only one side of the capacitive array that has a higher top plate voltage (V_N or V_P) are switched from V_{REF} to V_{CM} . At the third conversion steps, the merged capacitor switching (MCS) scheme [3] is partially applied to all capacitors that are connected to V_{CM} . If the capacitors that are connected to V_{CM} are in the V_P C-DAC array and $V_P > V_N$, the bottom plate of the capacitor in the V_P C-DAC array is switched from V_{CM} to ground. If $V_P < V_N$ for the same scenario, the bottom plate in the V_P C-DAC array is switched from V_{CM} to V_{REF} . If the capacitors that are connected to V_{CM} are in the V_N C-DAC array and $V_P > V_N$, the bottom plate in V_N C-DAC array is switched from V_{CM} to V_{REF} . If $V_P < V_N$ for the same scenario, the bottom plate in the V_P C-DAC array is switched from V_{CM} to ground. The switching method of remaining conversion steps is the same with that of the third conversion step. Fig. 4 shows a 10-bit C-DAC configuration of the proposed SSC scheme. Because a role of capacitors for second conversion steps are spread from $64C$ to C with top plate sampling, the total number of unit capacitors can be reduced by a quarter compared to conventional C-DAC. As a result, the proposed switching scheme does not require to connecting the MSB capacitors to V_{CM} unlike previous switching schemes [2, 3]. Therefore, the burden of switches for driving the MSB capacitors can be reduced.

III. MEASUREMENT RESULTS

The proposed switching scheme was fabricated in a 0.18- μm process. The differential-type 10-bit SAR ADC operating at 1.8 V and 10-MS/s with an ADC core area

Fig. 3. Examples of switching procedure of 4-bit SSC C-DAC.

Fig. 4. C-DAC of the SSC scheme with a 10-bit SAR ADC.

occupying $0.479 \times 0.482 \mu\text{m}^2$ was fabricated. Fig. 5 shows the chip die photo of the SAR ADC. Fig. 6 shows the dynamic performance of the SAR ADC. The test result shows an SFDR of 60.9 dBc, a SINAD of 53.1 dB and an ENOB of 8.5 bit. Fig. 7 shows the ENOB trend according to the input frequency from 1 MHz to 5 MHz. Fig. 8 shows the static performance of the SAR ADC. The DNL and INL is 2.8/-1 and 3.7/-3.6 LSB, respectively. The switching energy of the proposed SSC C-DAC for SAR ADCs is verified in MATLAB. Fig. 9 compares the switching energy of the proposed SSC C-DAC with previous switching methods for C-DAC of SAR ADCs. The average switching energies reported in

Fig. 5. SAR ADC die photo.

Fig. 6. Dynamic test results at 1 MHz input frequency and 4096 FFT points.

Fig. 7. Dynamic test results using 1 MHz to 5 MHz input frequency FFT points.

Fig. 8. Static performance of the SAR ADC.

Fig. 9. Switching energy versus output code.

[2, 3] are $21.3CV_{REF}^2$ and $82.1CV_{REF}^2$, respectively. The average switching energy of the proposed scheme is $26.4CV_{REF}^2$. Compared to the conventional scheme, the proposed scheme saves switching energy by 98.1%. Table 1 shows the comparison table of the switching scheme for a 10-bit SAR ADC. The number of total unit capacitors is also reduced by 75% compared to conventional C-DAC. Table 2 shows the performance

Table 1. Comparison of switching energy for a 10-bit SAR ADC

Switching scheme	Average Energy (CV_{REF}^2)	Energy saving	Total Unit Capacitor
Conventional	1363.3	Reference	2048
MCS[3]	82.1	93.7%	1024
Sanyal[2]	21.3	98.4%	512
This work	26.4	98.1%	512

Table 2. Performance summary of an ADC

Specification	
Process	0.18 μ m CMOS
Supply voltage	1.8 V
Resolution	10-bit
Sampling rate	10-MS/s
ENOB	8.5 bit
DNL/INL	2.8/-1 LSB / 3.7/-3.6 LSB
Sampling capacitor	5 pF
Active area	0.23 mm ²
Power consumption	3.8 mW

summary of an ADC.

IV. CONCLUSIONS

An energy-efficient SSC C-DAC is proposed. In the proposed switching scheme for low power consumption, the burden of the switches making V_{CM} can be mitigated. The switching energy and the number of total unit capacitors are reduced by 98.1% and 75%, respectively, when compared to conventional C-DAC. This proposed switching scheme was verified with SAR ADCs operating at 1.8 V and 10-MS/s with the ADC core area of $0.479 \times 0.482 \mu\text{m}^2$, fabricated using the 0.18- μm CMOS process. The dynamic performance of the SAR ADC shows a SFDR of 60.9 dBc, a SINAD of 53.1 dB and an ENOB of 8.5 bit at a 1MHz input frequency.

ACKNOWLEDGMENTS

This work was supported by the Technology Innovation Program (or Industrial Strategic Technology

Development Program (10077381, Royalty Free Processor & Software Platform Development for Low Power IoT & Wearable Devices) funded By the Ministry of Trade, Industry & Energy (MOTIE, Korea) and this research was supported by the Chung-Ang University Graduate Research Scholarship in 2017.

REFERENCES

- [1] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC", *IEEE ISCAS*, May. 2005, pp.184-187
- [2] A. Sanyal and N. Sun, "SAR ADC architecture with 98% reduction in switching energy over conventional scheme," *Electronics Letters*, vol. 49, no. 4, 14th Feb. 2013.
- [3] V. Hariprasath, J. Guerber, S.-H. Lee and U.-K. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency", *Electronics Letters*, vol. 46, no. 9, 29th Apr. 2010.
- [4] Chun-Cheng Liu, Soon-Jyh Chang, Guan-Ying Huang, Ying-Zu Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure", *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731-740, Apr. 2010.
- [5] Ju Eon Kim, Seong-Jin Cho, Yong Sin Kim, Seok Lee and Kwang-Hyun Baek, "Energy-efficient charge-average switching DAC with floating capacitors for SAR ADC", *Electronics Letters*, vol. 50, no. 16, pp. 1131-1132, 31st July. 2014.
- [6] Chang-Yuan Liou and Chih-Cheng Hsieh, "A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with Charge-Average Switching DAC in 90nm CMOS", *IEEE ISSCC Dig. Tech. Pap.*, San Francisco, CA, USA, February 2013, pp. 280-281.
- [7] Liangbo Xie, Guangjun Wen, Jiaxin Liu and Yao Wang, "Energy-efficient hybrid capacitor switching scheme for SAR ADC", *Electronics Letters*, vol. 50, no. 1, pp.22-23, 2nd Jan. 2014.
- [8] Yabo Ni, Lu Liu and Shiliu Xu, "Mixed capacitor switching scheme for SAR ADC with highest energy efficiency", *Electronics Letters*, vol. 51, no. 6, pp.466-467, 19th Mar. 2015.
- [9] C. Yuan and Y. Lam, "Low-energy and area-efficient tri-level switching scheme for SAR ADC", *Electronics Letters*, vol. 48, no. 9, 26th Apr. 2012.
- [10] Y. Li, Z. Zhang and Y. Lian, "Energy-efficient charge-recovery switching scheme for dual-capacitive arrays SAR ADC", *Electronics Letters*, vol. 49, no. 5, 28th Feb. 2013.
- [11] Liangbo Xie, Jian Su, Jiaxin Liu and Guangjun Wen, "Energy-efficient capacitor-splitting DAC scheme with high accuracy for SAR ADCs", *Electronics Letters*, vol. 51, no. 6, 19th Mar. 2015

Ju Eon Kim received the B.S. and M.S. degrees at School of Electrical and Electronics Engineering from Chung-Ang University (CAU), Seoul, Korea, in 2012 and 2014, respectively. He is currently working toward the Ph.D. degree in electrical and electronics engineering at CAU. His research interests include low-voltage low-power successive approximation register (SAR)-type and high-speed, high resolution hybrid-type analog-to-digital converters (ADC). He is also interested in high-performance image sensor and display driver IC designs.

Sung-Min Lee received the B.S. degrees at School of Electrical and Electronics Engineering from Chung-Ang University (CAU), Seoul, Korea, in 2015, where he is currently working toward the M.S. degree in electrical and electronics engineering.

His research interests include ultra low-power SAR ADCs for bio-medical applications.

Taegeun Yoo received the B.S., M.S., and Ph. D. degrees in electrical and electronics engineering from Chung-Ang University, Seoul, Korea, in 2009, 2011, and 2015 respectively. From 2015 to 2016, he was also with the Chung-Ang University as a

Research Professor. In 2016, he joined the Nanyang Technological University, Singapore, as a Research Fellow. His research interests include low-power data converters and high-efficiency power management ICs.

Yong-Jun Jo received the B.S. degrees at School of Electrical and Electronics Engineering from Chung-Ang University (CAU), Seoul, Korea, in 2017, where he is currently working toward the M.S. degree in electrical and electronics engineering.

His research interests include SAR ADCs for automotive applications.

Kwang-Hyun Baek received the B.S. and M.S. degrees from Korea University, Seoul, Korea, in 1990 and 1998, respectively. He received the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign (UIUC),

IL, USA, in 2002. From 2000 to 2006, he was with the Department of High-Speed Mixed-Signal ICs as a senior scientist at Rockwell Scientific Company, formerly Rockwell Science Center (RSC), Thousand Oaks, CA, USA. At RSC, he was involved in development of highspeed data converters (ADC/DAC) and direct digital frequency synthesizers (DDFS). He was also with Samsung Electronics from 1990 to 1996. Since 2006 he has been with the School of Electrical and Electronics Engineering, Chung-Ang University (CAU), Seoul, Korea, where he is a faculty member. His research interests include high-performance analog and digital circuits such as low-power ADCs, high-speed DACs, hybrid frequency synthesizers (PLLs, DDFSs), highspeed interface circuits (CDRs, SerDes), PMIC, and near threshold-voltage (NTV) circuits.