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Ma, Chuang; Jin, Tianli; Liu, Xiaoxi; Piramanayagam, Seidikkurippu Nellainayagam

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Switching domain wall motion on and off using a gate voltage for domain wall transistor applications

Chuang Ma,^{1,a)} Tianli Jin,^{2,a)} Xiaoxi Liu,^{1,b)} and S. N. Piramanayagam^{2,b)}

¹Department of Electrical and Computer Engineering, Shinshu University, Wakasato 4-17-1, Nagano, 380-8553, Japan

²Division of Physics and Applied Physics, School of Physical and Mathematical Sciences, Nanyang Technological University, 637371, Singapore

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Spintronic devices such as magnetic random access memory and domain wall (DW) memory are attracting significant attention. Spin-field effect transistor devices have been proposed and researched for logic applications. In domain wall memory, the information is stored in magnetic domain states, which can be moved with a current above a certain threshold value. So far, the domain wall motion is only determined by the current density for most of the DW devices. Here, we demonstrate experimentally that a significant change in domain wall mobility can be achieved by applying a gate voltage. By applying a positive gate voltage, we show that the threshold current density for DW motion can be reduced by more than 10%. By choosing a suitable operating current, the domain wall motion can be switched on or off by the use of a gate voltage. These results are promising for designing high performance domain wall based transistor devices with faster operation speed and lower power consumption. *Published by AIP Publishing.*

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Spintronic devices based on domain wall (DW) motion, such as DW racetrack memory^{1–14} and DW logic devices,^{15,16} have attracted great interest of both academic and industry researchers. DW racetrack memory shows great potential for high capacity and low power dissipation, surpassing those of hard disk drives, due to the absence of mechanical parts.^{1,14} In DW racetrack memory, the information is written by applying a magnetic field or current and is read out by moving the domain walls to a sensor such as a magnetic tunnel junction. To cause DW motion, an external force, such as a magnetic field or current, is required to overcome the intrinsic pinning. To achieve a miniaturized device, driving the domain walls by using a current is preferred over using a magnetic field.¹⁷ In the case of current-induced domain wall (CIDW) motion, the applied current has to be larger than a threshold current (J_{th}) to move the domain wall. In a DW device, J_{th} depends on the depinning potential, which can be divided into the intrinsic pinning potential of the material used and the extrinsic pinning potential, which may be induced by defects, edge damages, or artificial pinning sites.^{6,18–21} A reduction of J_{th} helps in increasing the DW velocity and in reducing the power consumption. Therefore, domain wall dynamics is an interesting topic of investigation which has yet to be fully explored.²²

Application of voltage has been used to tune the magnetic anisotropy of materials in the recent past.^{4,23–27} This phenomenon can, in principle, be used to control DW motion^{28–33} and skyrmion motion.^{34,35} The DW motion in the presence of a voltage has attracted attention due to the potential of reducing energy consumption and increasing DW velocity in DW memory.^{29,31,33,36–39} A few studies have reported about the

effect of the electric field on DW dynamics in the magnetic system with perpendicular magnetic anisotropy (PMA), such as Pt/Co/oxide^{38,40} and Ta/CoFeB/oxide.^{24,41} A significant modulation of DW velocity under gate voltages has been demonstrated in the creep regime at relatively low speed and the depinning regime at high speed under a magnetic field.^{41,42} Velocity modification over an order of magnitude has been demonstrated (from 0.4 to 4 $\mu\text{m s}^{-1}$) in Co or CoB wires by Schellekens *et al.*³² Lin *et al.* have reported a change in velocity from 0.4 to 40 $\mu\text{m s}^{-1}$ in Ta/CoFeB/MgO devices.⁴¹ The depinning field has been shown to be reduced as a function of gate voltage. However, these studies were performed when the domain walls were driven by an applied magnetic field in the presence of a gate voltage. For practical applications, employing a current to drive the domain walls is preferred, but current driven domain wall motion in the presence of a gate voltage is not well investigated yet.⁴³ In this study, we have investigated the effects of a gate voltage on spin-current induced domain wall motion in the Co₅₀Ni₅₀ alloy and Pt-based multi-layered devices with a PMA. We show that the application of a gate voltage enhances the DW motion velocity and reduces the threshold current. We also find that the coercivity (H_c) decreases with gate voltage and reduces the effective pinning field.

Figure 1(a) shows the hysteresis loops of the Pt (1 nm)/[Co₅₀Ni₅₀ (0.5 nm)/Pt (0.5 nm)]₂ multilayer samples, measured in out-of-plane (OOP) and in-plane (IP) directions. A perpendicular magnetic anisotropy with an anisotropy field of about 5 kOe can be clearly seen. From the inset of Fig. 1(a), the coercivity (H_c) is about 85 Oe. In Figs. 1(b) and 1(c), we show the cross-section and a schematic illustration of the device that was prepared for this investigation. The width of the wire is 5 μm , and the length is 25 μm . The wire was lithographically fabricated on the top center of the

^{a)}C. Ma and T. Jin contributed equally to this work.

^{b)}Authors to whom correspondence should be addressed: liu@cs.shinshu-u.ac.jp and prem@ntu.edu.sg.

FIG. 1. Schematic illustration of the sample and devices used in this study. (a) Hysteresis loops of $\text{Co}_{50}\text{Ni}_{50}/\text{Pt}$ multilayers, measured in two directions. The inset indicates that the samples have a perpendicular magnetic anisotropy. (b) The cross-section and (c) schematic illustration of the device prepared for voltage-controlled domain wall investigations. (d) Measurement of the domain wall velocity by Kerr microscope images. (d1) was taken before the application of a current pulse and (d2) after the current pulse ($3.3 \times 10^{11} \text{ A/m}^2$) with a duration of $1 \times 10^{-6} \text{ s}$.

electrode pad of $100 \mu\text{m}$ by $200 \mu\text{m}$. Current pulses were applied across the two electrodes on the left and right sides. The gate voltage was applied by depositing a bottom electrode with ITO and SiO_2 . The local area magnetic properties of the device were measured by a micro-magneto-optical Kerr effect (μ -MOKE) system. The μ -MOKE uses a laser beam (532 nm) focusing on a spot of around 400 nm . A polar-MOKE microscope was used to observe the magnetic domain structure and to monitor domain wall motion on the device, as shown in Fig. 1(d). To measure the domain velocity, an image using a polar Kerr microscope was taken before applying a current pulse [Fig. 1(d1)]. Subsequently, a current pulse with a density of $3.3 \times 10^{11} \text{ A/m}^2$ and a duration of $1 \times 10^{-6} \text{ s}$ was sent through the device, and an image was taken [Fig. 1(d2)]. The above process was repeated 10 times for the same current pulse. The domain wall velocity was calculated from the average domain wall displacements (ΔD) and the current pulse width ($1 \times 10^{-6} \text{ s}$). A current pulse rather than the continuous current was used in order to avoid the Joule heating effect.

Figure 2(a) shows the OOP hysteresis loops of the device, as measured by the μ -MOKE in the polar mode, with different values of gate voltage V_G . We can notice that the hysteresis loops become narrower with the increase in V_G . The hysteresis loops start from a perfect square loop and change into tilted loops at $V_G = 8.5 \text{ V}$, which indicates that

FIG. 2. (a) Hysteresis loops of the device sample, as a function of applied gate voltage, V_G . A clear perpendicular magnetic anisotropy is seen for all the cases. (b) The reduction of coercivity, H_c , as a function of V_G .

the perpendicular anisotropy decreases. Figure 2(b) shows the coercivity as a function of V_G . The results indicate that the coercivity of these samples decreases as the gate voltage is increased.

At first, we decided to investigate the depinning field and pinning potential of our device, following previous investigations.^{24,31,40–42} We measured the domain wall velocity v as a function of the applied magnetic field (H) for various values of current density (J). It should be noted that the current density is much smaller than the threshold current density. Figure 3(a) shows the values of v for $V_G = 0 \text{ V}$. It can be noticed that the domain wall velocity increases with the applied field H . The data fits to Eq. (1) very well. In our specific experimental setup, we denote a positive magnetic field as the one that expands the bright Kerr contrast domains (with magnetization pointed up) and a negative magnetic field as the one that expands the black Kerr contrast of the domains. It is well known that the spin-transfer torque will always tend to move the domain wall to the opposite direction of the electrical current. If we denote the current from left to right as positive, we found that positive magnetic field-induced DW propagation is assisted by sending a negative current with a current density of $-0.8 \times 10^{10} \text{ A/m}^2$. On the other hand, positive magnetic field-induced DW propagation is hindered by sending a positive current density of $+0.8 \times 10^{10} \text{ A/m}^2$. The results show that the magnetic field-induced DW velocity is modulated by the current direction. Figure 3(b) shows a fitting of $\ln(v)$ to Eq. (2). We extracted $\ln(v)$ from the domain wall velocity equation under the low magnetic field, which is described by the creep law as⁴⁴

$$v = v_0 \exp \left[-\frac{U_c}{k_B T} \left(\frac{H_{\text{dep}}}{H} \right)^{\frac{1}{4}} \right], \quad (1)$$

$$\ln(v) = \ln(v_0) + \left[\left(-\frac{U_c}{k_B T} \right) (H_{\text{dep}})^{\frac{1}{4}} \right] H^{-\frac{1}{4}}, \quad (2)$$

where v_0 is the velocity scaling pre-factor related to the lateral length of the small section of the domain wall, U_c is a

FIG. 3. Domain wall velocity as a function of the applied magnetic field, for gate voltages of (a) 0 V and (c) 8.5 V . Plots of $\ln(v)$ as a function $\mu_0 H$ to determine the pinning strength in the creep regime are shown in (b) and (d).

characteristic energy related to the disorder-induced pinning potential, k_B is the Boltzmann constant, T is the temperature, and H_{dep} is the depinning field below which the creep regime occurs. The exponent $1/4$, which has been determined theoretically and experimentally,^{24,41} fits the data well.

The creep regime allows us to determine the values of $U_c(H_{\text{dep}})^{1/4}/(k_B T)$ by fitting $\ln(v)$ with $H^{-1/4}$ linearly. The slope describes the pinning strength defined as $\mu_0 H_{\text{deff}} = (U_c/k_B T)^4 \mu_0 H_{\text{dep}}$. The slope obtained from such a fitting has the lowest value (-4.93) for $J = -0.8 \times 10^{10}$ A/m². When the current density was increased to $+0.8 \times 10^{10}$ A/m², the slope increased to -4.41 , indicating that the magnetic field and spin-current exert an opposite force on the DW motion. Similar results were obtained for $V_G = 8.5$ V, and the slope increased from -4.24 to -4.02 when the current density J increased from -0.8×10^{10} A/m² to $+0.8 \times 10^{10}$ A/m². These results indicate that the application of a gate voltage can be used to reduce the effective depinning field, which results in a larger DW velocity.

As a next step, we investigated the domain wall motion as a function of the applied current in the absence of an external magnetic field. Figure 4 shows the schematics of the domain wall motion measurements [Figs. 4(a)–4(c)] and the measured domain wall velocity v for various values of current density J and gate voltages $V_G = 0$ V and 8.5 V [Fig. 4(d)]. From Fig. 4(d), we can notice that the domain wall velocity is larger when a gate voltage was applied. We can also notice that the domain wall velocity increases with the increase in current density J . The onset of domain wall motion appears at a lower J_{th} in the case of a positive gate voltage (V_G). It is interesting to note that for a current density J of about 5.4×10^{11} A/m² [in the center region of the operating window shown in Fig. 4(d)], the domain wall can be made to move or stop by applying or not applying a gate voltage. These results indicate that such a device could be used as a domain wall transistor. In an alternative perspective, the application of a gate voltage V_G helps in reducing the threshold current (J_{th}) required to cause domain wall motion. As a result, the power consumption in domain wall devices may be reduced by applying a gate voltage.

FIG. 4. Domain wall velocity measurements of the device under this study. (a) and (b) A schematic of the domain wall velocity measurements for $V_G = 0$ V and 8.5 V. (c) The Kerr imaging of domain walls to measure the domain wall velocity. (d) A plot of the domain wall velocity, v , as a function of current density J , for two different gate voltages V_G (0 V and 8.5 V). The colored box represents the operating region for the domain wall transistor.

FIG. 5. Plot of the threshold current density, J_{th} , to drive domain wall motion and coercivity H_c of the device as a function of applied gate voltage.

FIG. 6. The illustration of transistor on/off based on DW motion.

To get an insightful understanding of this effect, we measured the threshold current J_{th} required to move the domain walls for various gate voltages V_G . In Fig. 5, we plot J_{th} along with the coercivity H_c of the device. We noticed that there is a strong correlation between J_{th} and H_c from this measurement. A reduction in anisotropy, arising due to the application of an electric field, is a well reported phenomenon.^{23,24,30,39,45} Both the coercivity and the domain wall motion by spin currents are related to the anisotropy constant of the magnetic material. Therefore, we conclude that the voltage-induced reduction in anisotropy is the cause of the observed larger domain wall velocity and lower threshold current.

Despite the fact that we have made use of optical Kerr measurements to understand the domain wall propagation, a practical all-electronic device may be realized as illustrated in Fig. 6. In this case, there are two readers, in the form of magnetic tunnel junctions (MTJs), at the edges of the transistors.^{46–50} The domain wall motion through the gate may be monitored using the voltage output of these two MTJ read sensors. The results shown in this paper open a path to the realization of such a device.

To summarize, we have shown that the application of a gate voltage causes a reduction in the perpendicular magnetic anisotropy of the $\text{Co}_{50}\text{Ni}_{50}/\text{Pt}$ quadruple layers. We have shown that this phenomenon helps to reduce the threshold current required to drive domain wall motion. The reduction of the threshold current density can be interpreted by the reduction of the pinning potential due to the gate electric field. The gate voltage can also be used to switch the domain wall motion between ON and OFF states, making the realization of a domain wall transistor possible.

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