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Fabrication and characterization of germanium-on-insulator through epitaxy, bonding, and layer transfer

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A scalable method to fabricate germanium on insulator (GOI) substrate through epitaxy, bonding, and layer transfer is reported. The germanium (Ge) epitaxial film is grown directly on a silicon (Si) (001) donor wafer using a "three-step growth" approach in a reduced pressure chemical vapour deposition. The Ge epilayer is then bonded and transferred to another Si (001) wafer to form the GOI substrate. The Ge epilayer on GOI substrate has higher tensile strain (from 0.20% to 0.35%) and rougher surface (2.28 times rougher) compared to the Ge epilayer before transferring (i.e., Ge on Si wafer). This is because the misfit dislocations which are initially hidden along the Ge/Si interface are now flipped over and exposed on the top surface. These misfit dislocations can be removed by either chemical mechanical polishing or annealing. As a result, the Ge epilayer with low threading dislocations density level and surface roughness could be realized. © *2014 AIP Publishing LLC*.
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I. INTRODUCTION

Bulk silicon (Si) complementary metal-oxide-semiconductor (CMOS) devices have been the dominant components in the microelectronic industry for decades. Rigorous device scaling methods have been driving the industry to maintain device performance, lower the power consumption, and reduce cost per transistor.[1,2] However, device scaling is expected to reach the limit soon. As the benefits of scaling subside, one approach to extract performance gains may be to attempt to improve the carrier transport, mainly through increased mobility. There are several approaches that are being used to increase mobility relative to bulk Si devices.[3,4] One of the approaches is to simply replace Si as the channel material with Ge, which possesses a 2 times increase in electron mobility and 4 times increase in hole mobility.[5]

On the other hand, silicon-on-insulator (SOI) has several key benefits over bulk technologies. The structure of the SOI substrate allows for smaller device area and increased packaging density. The SOI substrate also reduces the parasitic capacitances and short channel effects.

Germanium-on-insulator (GOI) substrate therefore has all the technical merits described above and can potentially become a suitable candidate for future semiconductor industry. GOI substrate can be fabricated by many techniques, e.g., Ge condensation techniques,[6] liquid phase epitaxy,[7] etc. Most of the techniques have drawbacks and hence limit the applications.[8] Another common technique used to fabricate the GOI substrate is *Smart Cut*™, but it is not easily scalable to wafer size larger than 200 mm.[9,10] In this manuscript, we present a scalable method to fabricate GOI wafer. The fabrication involves Ge epitaxial layer growth directly on Si (001),[11–13] fusion bonding, and layer transfer to another Si handle wafer. Subsequently, the materials and electrical properties of the GOI substrate are analyzed and discussed.

II. EXPERIMENTAL DETAILS

In this experiment, the silicon (001) wafer (diameter = 150 mm, *p*-type, resistivity = 0.01–0.025 Ω cm) was cleaned using RCA solution followed by drying the wafer using an IPA dryer. The clean wafer was loaded into a N_2-purged load-lock of ASM Epsilon 2000 reduced pressure chemical vapour deposition (RPCVD) reactor. To initiate the growth, the wafer was transferred to the growth chamber and baked in hydrogen (H_2) at 1000 °C for 2 min to desorb the thin surface oxide that is detrimental to the epitaxy process. 10% dilute germane (GeH_4) in H_2 balance was used as the Ge precursor. A three-step Ge growth was introduced and the target thickness was 1.3 μm. The three-step in the growth sequence were: (i) low temperature growth at 400 °C to obtain a rather smooth and continuous Ge seed layer as growth template; (ii) low to high temperature ramping from 400 °C to 600 °C at a rate of 6.5 °C/min; (iii) high temperature growth at 600 °C. The approach has been described in detail in previous publications.[11,12] Thermal cycling was introduced immediately after step (iii) to enhance the surface mobility of Ge atoms in order to control the surface roughness and reduce the threading dislocation density (TDD). The thermal cycling was performed by H_2 annealing between 680 and 825 °C for a repetition of 8× with 10 min annealing at 825 °C. The Si wafer that was used to grow Ge

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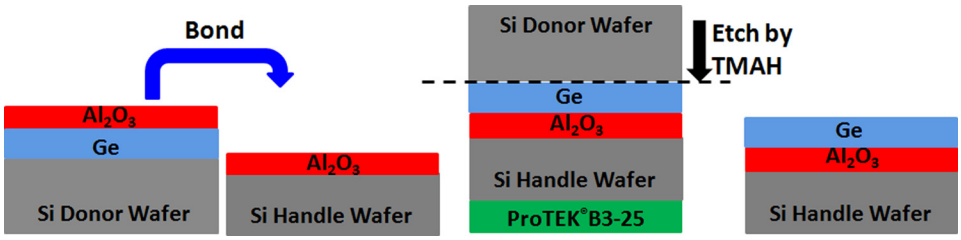

FIG. 1. Schematic flow of the fabrication of GOI substrate.

epilayer was termed as donor wafer in the subsequent section of this manuscript.

Aluminum oxide (Al_2O_3) with a thickness of ~10 nm was deposited on both donor wafer and another Si (001) handle wafer (diameter = 150 mm, *p*-type, resistivity = 0.01–0.025 Ω cm) using the atomic layer deposition (ALD). Al_2O_3 was chosen due to its higher thermal conductivity than SiO_2 (30 W m^{-1} k^{-1} vs. 1.4 W m^{-1} k^{-1}). Prior to bonding, both wafers were subjected to O_2 plasma exposure for 15 s, followed by rinsing them with deionized water and then spin-dried in a spin rinse dryer (SRD). O_2 plasma exposure could increase the surface hydrophilicity of the dielectric. The rinsing step was necessary to clean the wafers surfaces and to populate the surface with hydroxyl (OH) group at a sufficiently high density to initiate wafer bonding. After bonding, the bonded wafer pair was annealed at 300 °C in an atmospheric N_2 ambient for 3 h to further enhance the bond strength.

ProTEK®B3–25 was spin coated on the backside of handle wafer to act as a protective layer during the removal of the Si donor wafer in the tetramethylammonium hydroxide (TMAH) solution. The Ge epilayer acted as an etch-stop layer as the etching selectivity of Ge over Si is high in the TMAH solution. The etching was carried out at 80 °C until the Si was completely removed with no reaction bubbles were observed. The ProTEK B3-25 protective coating was then removed in O_2 plasma with power of 800 W. The GOI fabrication steps were summarized in the schematic flow as shown in Fig. 1.

The Ge epitaxial film on the GOI sample was characterized by various characterization techniques. The Ge RMS roughness was determined by atomic force microscope (AFM) from Veeco/Digital Instrument Dimension 3000 with tapping mode. Transmission Electron Microscopy (TEM) from Philips CM200 with operating voltage of 200 kV was used to study the dislocations. X-Ray Diffraction (XRD) from Bruker D8 Discover was used to determine the crystallinity and strain of the Ge epilayer. Rocking curve based on Si (004) was used in the XRD measurement. To further confirm the strain and quality of Ge film, Raman spectroscopy from WITec confocal Raman microscope alpha 300 was used. The excitation laser wavelength of 532 nm was used with both focus length and objective lens magnification at 80 cm and 100×, respectively. The model of the Time-of-Flight Secondary Ion Mass Spectroscopy (TOF-SIMS) used was Ion TOF's TOF. SIMS. The primary beam and energy used are Cs+ and 2 KeV, respectively. The beam raster size is 300 μm × 300 μm and the analysis area is 100 μm × 100 μm. The Capacitance-Voltage (*C-V*) of Metal-Oxide-Semiconductor (MOS) structure was measured on Cascade/Suss Microtec PM8PS Probe Station using Keithley 4200-SCS semiconductor characterization system.

III. RESULTS AND DISCUSSION

The TEM images in Fig. 2 show the cross-sectional view of GOI substrate and the bonding interface of the two Al_2O_3 layers on each wafer (donor and handle wafers). From Figs. 2(a) and 2(b), the thickness of the Ge epitaxial film and Al_2O_3 is ~1.3 μm and ~20 nm, respectively. These values closely matched with the targeted thickness of Ge and Al_2O_3 of 1.3 μm and 20 nm, respectively. Fig. 2(a) also shows that the misfit dislocations, which are previously "hidden" along the Ge/Si interface, are now accessible from the top surface. This provides the ease to remove the misfit dislocations by chemical mechanical polishing (CMP) or annealing. In addition, the treading dislocations might be removed once the misfit dislocations are removed. Hence, a Ge epilayer with typically low TDD ($<10^7$ cm^{-2}) could be realized and this is useful for subsequent III–V integration and device fabrication. As shown in Fig. 2(b), the two Al_2O_3 layers from each wafer are bonded uniformly with no sign of a microvoid. This confirms that a seamless bond at the microscale has been successfully achieved. In addition, the difference in contrast within the Al_2O_3 layer can be attributed to the O_2

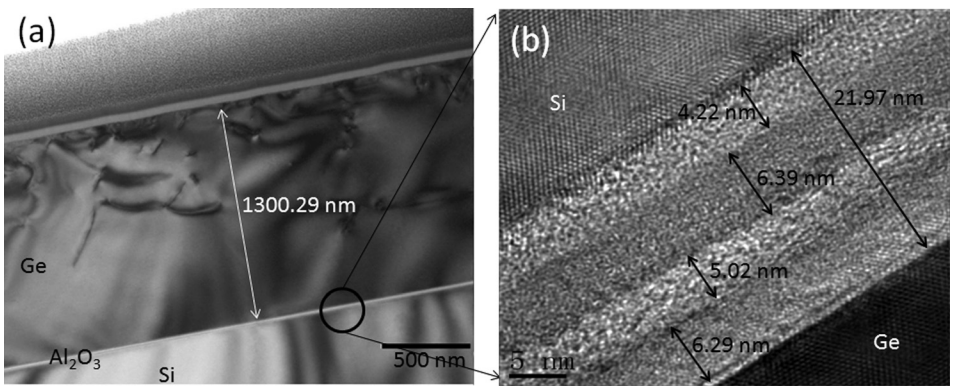

FIG. 2. Cross-sectional TEM bright field images show (a) the overall view of GOI substrate and (b) the bonding interface between the Al_2O_3 layers.

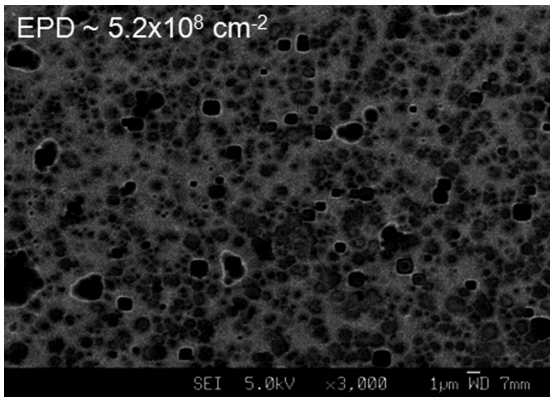

FIG. 3. The EPD determination for GOI sample.

plasma activation, which modifies the stoichiometry of the Al_2O_3. The actual underlying root-cause is still under careful investigation.

To quantify the TDD of the GOI sample, field emission scanning electron microscope (FESEM) is used. The sample is etched in an iodine solution for 1 s. Since the dislocations are etched much faster in the etchant, etch pits are delineated and can be observed. The estimated etch pits density (EPD) of the GOI sample is $5.2 \pm 0.45 \times 10^8$ cm^{-2} as shown in Fig. 3. The EPD is increased by at least one order of magnitude as compared to the initial Ge/Si, which is $\sim 3.2 \pm 0.26 \times 10^7$ cm^{-2}.[11] This is because the misfit dislocations are now exposed on the top surface.

Since the strain state of the Ge epilayer has important consequences on its electrical and optical properties, XRD study is performed to estimate the strain level of the Ge epilayer. The XRD analysis in Fig. 4 shows that the crystal quality of Ge epilayer on GOI substrate does not change significantly as signified by the peak intensity and curve shape that are comparable with that of the Ge on Si wafer. Both of the Ge peaks signals are asymmetric and show clear shoulder at the side towards higher incidence angle. This is due to Ge/Si intermixing at the interface during the thermal processing that perturbs the abrupt interface, which results in

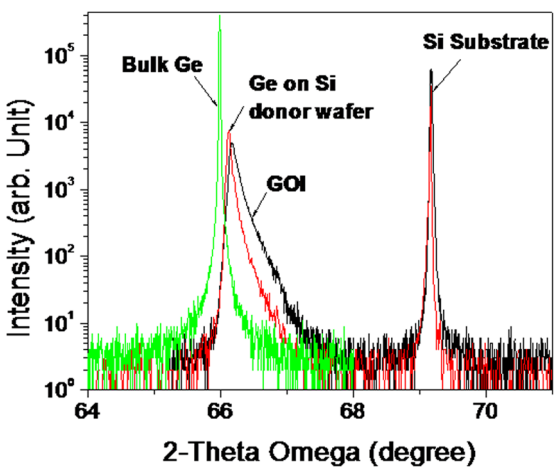

FIG. 4. HRXRD profile illustrates the crystallinity and the strain state of the Ge epitaxial films on GOI substrate and Ge on Si donor wafer with reference to bulk Ge.

an intermediate $Si_{1-x}Ge_x$ layer. The Ge peaks are shifted to the right with reference to the Ge bulk substrate as a result of a tensile strain. The tensile strain is thermally induced in the Ge epilayer during cooling after high temperature growth as the Ge (5.8 ppm/°C) and Si (2.6 ppm/°C) have different linear coefficient of thermal expansion (CTE).[14]

The perpendicular lattice constant ($a^{\perp}$) of epilayer in the growth direction can be calculated from the XRD diffraction peak using Bragg's law as follows:

$$a^{\perp} = \frac{2\lambda}{\sin\left(\frac{\omega_{Ge}}{2}\right)}, \tag{1}$$

where λ is the incident wavelength of the radiation (Cu $K_{\alpha 1}$ line, $\lambda = 1.5406$ Å) and ω_{Ge} is the angular position of Ge peak from the high resolution x-ray diffraction (HRXRD) of Si (004).

The in-plane lattice constant can be defined as

$$a^{\parallel} = \left(\frac{1+\upsilon}{2\nu}\right)\left[a_{Ge} - a^{\perp}\left(\frac{1-\upsilon}{1+\nu}\right)\right], \tag{2}$$

where υ is the elastic modulus of Ge, $\upsilon = 0.271$, and the unstrained Ge lattice constant, $a_{Ge} = 5.6576$ Å.

Finally, the residual strain of Ge epilayer can be calculated by the following equation:

$$\varepsilon = \frac{a^{\parallel}_{Ge} - a_{Ge}}{a_{Ge}}. \tag{3}$$

The positive and negative values of ε represent that the Ge epilayer has either tensile or compressive strain. From the calculation, the Ge layer on GOI substrate has higher tensile strain of 0.35% than the Ge on Si wafer of 0.20%. The discrepancy is not fully understood and likely due to the huge amount of misfit dislocations on the Ge surface.[15]

Raman spectroscopy is used to determine the quality and properties of the Ge epitaxial film by measuring the alloy composition and strain. In Fig. 5(a), no signal originated from the Si-Si vibration mode is observed indicating that the Si from the donor wafer has been removed completely in the TMAH solution. A strong Si-Ge vibration peak is expected due to the Ge/Si intermixing at the interface during the thermal cycling process. In Fig. 5(b), a red shift of Ge-Ge vibration peak position is clearly observed in the GOI substrate (291.79 cm^{-1}) relative to the Ge on Si wafer (300.14 cm^{-1}) and bulk Ge reference (peak at 301.09 cm^{-1}). Ge-Ge peak of both samples has shifted to lower wavenumber (with reference to the Ge bulk), indicating that they are under tensile strain. This observation agrees with the earlier XRD finding. In addition, the Ge-Ge peak from the GOI substrate is shifted to a smaller wavenumber than that of Ge on Si wafer, signifying a higher tensile strain in the Ge epilayer after transferring to form the GOI substrate.

Fig. 6 shows that the RMS roughness of Ge epilayer on the GOI substrate is 4.2 nm from a scan area of $10\,\mu m \times 10\,\mu m$, which is rougher than the Ge on Si wafer of 1.28 nm. The rougher surface is expected because the misfit dislocations are now exposed on the top surface.

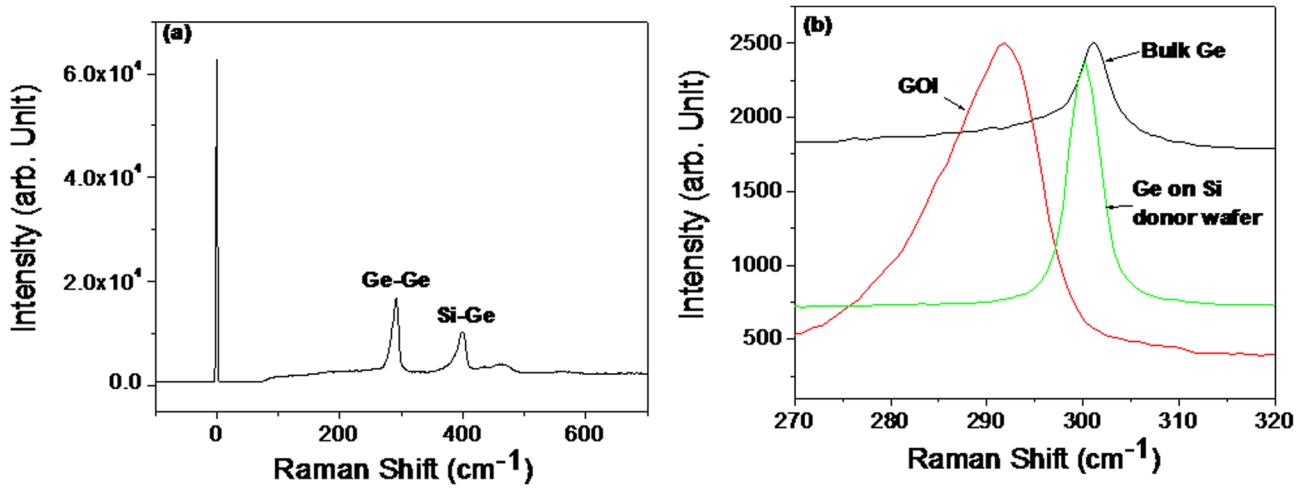

FIG. 5. Raman spectroscopy illustrates (a) the alloy composition and (b) the strain of the Ge epilayers on GOI substrate and Ge on Si wafer with reference to bulk Ge.

The TOF-SIMS depth profile is summarized in Fig. 7. There is carbon (12C) and oxygen (16O) contaminations on the Ge surface as the GOI substrate is exposed to ambient prior to SIMS analysis. No substantial aluminum (Al) atoms are out diffused from the Al_2O_3 layer to the Ge layer and Si layer. Boron (B) atoms are detected at the interface of Ge/Al_2O_3 due to the residual dopants from the chamber during the epitaxy growth of Ge on Si wafer. Based on the TOF-SIMS profile, a distinct level of Ge signal in the epitaxial film that tapers off rapidly in the Al_2O_3 layer can be observed. Similarly, the Si signal decays rapidly as it crosses the Al_2O_3/Si interface into the Al_2O_3 film. The Si signal starts increasing near the Ge top surface due to the Ge/Si intermixing during the thermal cycling process.

MOS structures are fabricated on the GOI substrate as shown in the subset figure of Fig. 8(a). The gate electrode is TiN with a thickness of ~150 nm and the gate dielectric stack consists of Al_2O_3 (thickness of ~10 nm) and interfacial GeO_xN_y (thickness of ~2 nm). The *C-V* and *I-V* measurements are done on a 200 μm × 200 μm MOS structure and the results are shown in Figs. 8(a) and 8(b). From Fig. 8(a), the leakage current of GOI substrate is lower than the Ge on Si wafer due to the presence of Al_2O_3 insulating layer. In addition, double plateau are observed from the *C-V* curve of GOI substrate because of the presence of two oxide layers (from MOS and GOI) as shown in Fig. 8(b). Even though the Ge layer is not intentionally doped during epitaxial growth, a *p*-type behavior is clearly seen. This observation is a result of background doping due to the residual boron in the CVD reactor. A four-point probe mapping tool is used to measure the sheet resistance of the Ge epilayer on Si, which can be used to estimate the boron (B) doping concentration in the Ge epilayer. The sheet resistance of the Ge epilayer on Si substrate is ~154 Ω/sq, which corresponds to B doping concentration of about $\sim 1.6 \times 10^{17}/cm^3$. At low frequency between 10 and 100 kHz, bumps are clearly observed in the *C-V* plots due to weak inversion of minority carrier response behavior. Ge is a low bandgap semiconductor, and at low frequencies, the GOI MOSCAP would show an admittance contribution due to the presence of interface traps at the mid bandgap. This contribution results in a significant exchange

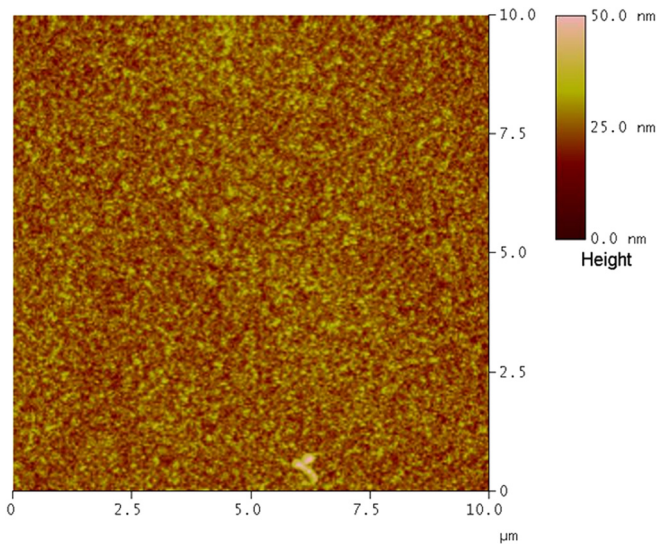

FIG. 6. 2-D AFM scan (dimension: 10 μm × 10 μm) showing the RMS roughness of the Ge epilayer on GOI substrate.

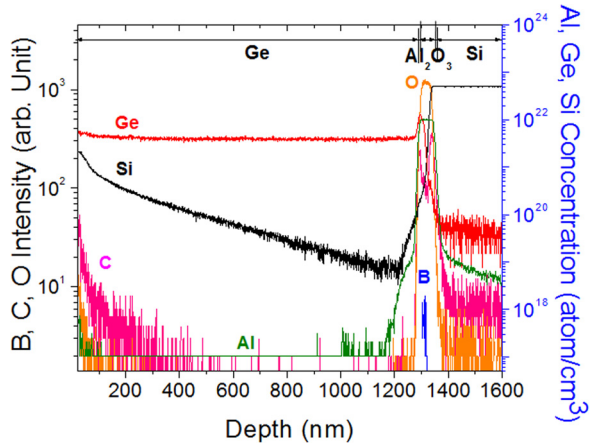

FIG. 7. TOF-SIMS analysis for elements of interest such as carbon (12C), oxygen (16O), silicon (28Si), germanium (74Ge), boron (11B), and aluminum (27Al) for Ge epilayer on GOI substrate.

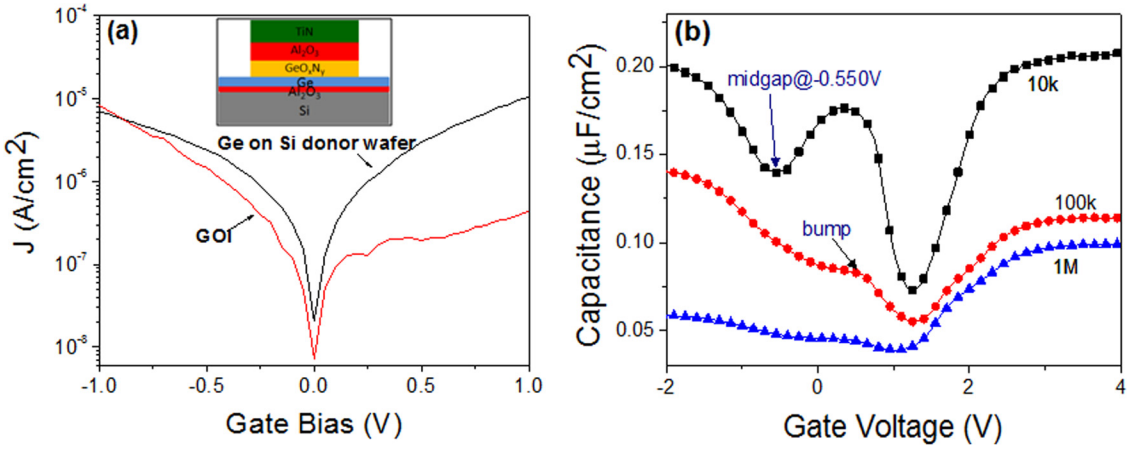

FIG. 8. (a) IV and (b) CV measurements on MOS structure fabricated on Ge epilayer on GOI substrate.

of carriers between traps and both the majority and minority carrier bands at the measured frequencies, typically within the range of 1 kHz–1 MHz. This exchange of carriers results in an increase in the capacitance as weak inversion response that causes the typical bum in the low frequency. At a high frequency of 1 MHz, frequency dispersion is observed for the sample, and the measured accumulation capacitance is lower than that at low frequency. This might be due to the dislocations on the Ge surface, which could form interface traps along the dielectric/Ge that leads to slow response in the high frequency and affects the measured capacitance. Both the midgap voltage (V_{midgap}) and flatband voltage (V_{FB}) of the GOI ($V_{midgap} = -0.55$ V, $V_{FB} = -1.64$ V) are lower than the Ge/Si (Ref. 16) ($V_{midgap} = 0.358$ V, $V_{FB} = 0.23$ V). In addition, the calculated interface state density (D_{it}) for GOI ($1.83 \times 10^{12}\,cm^{-2}/V$) is also higher than the Ge/Si (Ref. 16) ($4.7 \times 10^{11}\,cm^{-2}/V$). The effective oxide charge in the buried oxide (based on MOSCAP on TiN-Al_2O-Si) is measured and calculated as -7.72×10^{10} unit/cm^3, which is reasonably low and its effect to the *C-V* curve is not a cause for concern. Hence, the above observation is mainly due to the dislocation density that is higher in the GOI than Ge/Si substrate.

The study shows that the properties of Ge epilayer in the GOI substrate are degraded after the Ge epilayer is transferred. This is mainly due to the presence of high density misfit dislocations that are now exposed on the top surface and easily accessible. Despite this observation, this GOI structure provides ease to remove the misfit dislocation as well as the TDD by techniques CMP or annealing. Hence, a typically low level of TDD and surface roughness of Ge epilayer could be realized.

IV. CONCLUSION

In summary, GOI substrate is fabricated through epitaxy (the growth of Ge on Si wafer), bonding, and layer transfer. The Ge epilayer on GOI substrate has higher tensile stain (from 0.20% to 0.35%) and 2.28 times rougher surface compared to the Ge on Si wafer. This is because the misfit dislocations which are previously "hidden" along the Ge/Si interface are now accessible from the top surface. This GOI structure provides a possible path to remove the misfit dislocations through physical or chemical means. Unlike the *Smart Cut* technique, this method is scalable to any wafer sizes and makes the subsequent III–V integration and device fabrication on large Si wafer size becomes possible.

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