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Optical chirp *z*-transform processor with a simplified architecture

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Abstract: Using a simplified chirp *z*-transform (CZT) algorithm based on the discrete-time convolution method, this paper presents the synthesis of a simplified architecture of a reconfigurable optical chirp *z*-transform (OCZT) processor based on the silica-based planar lightwave circuit (PLC) technology. In the simplified architecture of the reconfigurable OCZT, the required number of optical components is small and there are no waveguide crossings which make fabrication easy. The design of a novel type of optical discrete Fourier transform (ODFT) processor as a special case of the synthesized OCZT is then presented to demonstrate its effectiveness. The designed ODFT can be potentially used as an optical demultiplexer at the receiver of an optical fiber orthogonal frequency division multiplexing (OFDM) transmission system.

OCIS codes: (130.3120) Integrated optics devices; (070.2025) discrete optical signal processing; (070.7145) Ultrafast processing.

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1. Introduction

This work is an extension of the author's recent article [1]. By direct realization of the CZT algorithm (which is referred to as the non-simplified CZT algorithm), a novel reconfigurable OCZT processor synthesized using the silica-based PLC technology has been presented, to the author's knowledge, for the first time in [1]. As the first important application of the designed tunable OCZT processor in [1], [2] has presented the design of a tunable ODFT processor (which is a special case of the tunable OCZT processor in [1]) and its application as a tunable optical demultiplexer at the receiver of an optical fiber OFDM transmission system. Several case studies of the author's novel tunable ODFT-based OFDM demultiplexer have been investigated to demonstrate several of its unique capabilities over the existing non-tunable ODFT-based OFDM demultiplexers [2]. However, in [1], the architecture of the tunable OCZT processor was rather complex because the design was based on the non-simplified CZT algorithm (in which no simplifications were made on the algorithm) that involved a very large number of $N \times L$ multiplications and additions. As appeared in Eq. (2), N is the number of input discrete-time samples $x[n]$ to be transformed into L number of output frequency samples $X[k]$ due to the CZT operation. As such, the number of optical components in the synthesized adaptable OCZT processor was very large (especially when N and L were large) and that there were a number of waveguide crossings or intersections which would make fabrication difficult [1].

To overcome these drawbacks in [1], this paper presents a more simplified CZT algorithm based on the discrete-time convolution method to come up with a much simpler architecture of the tunable OCZT processor design. The simplified CZT algorithm only requires $\sim (N+L)\log_2(N+L)$ multiplications and additions which are much smaller than those of the non-simplified CZT algorithm in [1], as described above. Hence, it is shown that the number of optical components in the simpler architecture of the tunable OCZT processor in this work is much less than those in [1]. Furthermore, unlike in [1], the adaptable OCZT processor with a simpler architecture in this work has no waveguide crossings or intersections and this will make fabrication much easier. Section 2 presents the simplified CZT algorithm using the discrete-time convolution technique. Using the simplified CZT algorithm, section 3 describes the synthesis of the reconfigurable OCZT processor with a simpler architecture using the silica-based PLC technology. Section 4 presents the design of an ODFT as a special case of the synthesized OCZT and its potential application. Conclusion is given in Section 5.

2. Simplified CZT algorithm

This section presents a simplified CZT algorithm based on the discrete-time convolution technique [3−6]. An input analog complex-valued signal $x(t)$ is sampled at the sampling period T (or unit-time delay of a filter) to yield a discrete-time N-point sequence $x[n]$ so that

$x[n] = x(nT) = x(t)\big|_{t=nT;\ n=0,1,\ldots,N-1}$ (see Fig. 4(a) of [1]). The unilateral N-point z-transform of $x[n]$ is given by [3−6]

$$X(z) = \sum_{n=0}^{N-1} x[n] z^{-n} \ , \tag{1}$$

where the z-transform parameter is defined as $z = \exp(j\omega T)$, where $j = \sqrt{-1}$ and ω is the angular frequency. It is assumed that the sum in Eq. (1) converges for all z except at $z = 0$. In Eq. (1), $x[n]$ is transformed into its complex-plane representation $X(z)$ which is the spectrum of $x[n]$. By computing Eq. (1) at a set of L equally-spaced frequency samples on an arbitrary contour in the z plane, i.e., $z = \{z_k\} = \{z_0\ z_1 \ldots z_{L-1}\}$, the L output frequency samples $\{X[k]\} = \{X[0]\ X[1] \ldots X[L-1]\}$ are given by [3−6]

$$X[k] = X(z)\big|_{z=z_k} = \sum_{n=0}^{N-1} x[n] z_k^{-n};\ k = 0,1,\ldots,L-1, \tag{2}$$

where N and L are arbitrary integers and

$$z_k = \left[r_0 \exp(j\theta_0)\right]\left[R_0 \exp(j\phi_0)\right]^k , \tag{3}$$

where $0 \le \theta_0 \le 2\pi$, $0 < \phi_0 < 2\pi$, and r_0 and R_0 are positive real numbers. The variables in Eq. (3) have been defined in [1]. The non-simplified CZT algorithm is described by Eqs. (2)−(3) [1]. Figure 1 of [1] shows the graphical meaning of Eq. (3). A plot of Eq. (3) for several case studies is shown in Fig. 2 of [1]. The simplified CZT algorithm derived using the discrete-time convolution technique is described as follows. Putting Eq. (3) into Eq. (2), the CZT of $x[n]$ is given by [3−6]

$$X[k] = \sum_{n=0}^{N-1} x[n]\left(r_0 \exp(j\theta_0)\right)^{-n} V^{-nk};\ k = 0,1,\ldots,L-1, \tag{4}$$

where

$$V = R_0 \exp(j\phi_0). \tag{5}$$

Putting the ingenious identity

$$nk = \frac{1}{2}\left[n^2 + k^2 - (k-n)^2\right] \tag{6}$$

into Eq. (4) gives

$$X[k] = V^{-k^2/2} \sum_{n=0}^{N-1} g[n] V^{(k-n)^2/2};\ k = 0,1,\ldots,L-1, \tag{7}$$

where

$$g[n] = x[n]\left(r_0 \exp(j\theta_0)\right)^{-n} V^{-n^2/2};\ n = 0,1,\ldots,N-1. \tag{8}$$

The use of the elegant identity defined in Eq. (6) makes it possible to express Eq. (4) (which is called the non-simplified CZT algorithm [1]) into a form that involves the convolution operation and hence the derivation of the simplified CZT algorithm, as explained next. To express Eq. (7) as a convolution, replace k by n and n by k in Eq. (7) to give

$$X[n] = V^{-n^2/2} \sum_{k=0}^{N-1} g[k] V^{(n-k)^2/2};\ n = 0,1,\ldots,L-1. \tag{9}$$

Let

$$h[n] = V^{n^2/2}, \tag{10a}$$

$$h[n-k] = V^{(n-k)^2/2}. \tag{10b}$$

Putting Eq. (10b) into Eq. (9) gives

$$X[n] = V^{-n^2/2} \cdot y[n];\ n = 0,1,\ldots,L-1, \tag{11}$$

where

$$y[n] = \sum_{k=0}^{N-1} g[k] h[n-k];\ n = 0,1,\ldots,L-1, \tag{12a}$$

$$y[n] = g[n] * h[n];\ n = 0,1,\ldots,L-1, \tag{12b}$$

where * denotes the convolution operation. Equations (12a) and (12b) mean that the output discrete-time sequence $y[n]$ is given by the discrete-time convolution of an input discrete-time sequence $g[n]$ with the discrete-time impulse response $h[n]$ of a linear time-invariant system which is here a finite-impulse response (FIR) filter. Then $y[n]$ is multiplied by the sequence $V^{-n^2/2}$ to give the CZT output $X[n]$ according to Eq. (11). In Eqs. (11) and (12a), the range of $g[k]$ is $k = 0,1,\ldots,N-1$ and the ranges of both $X[n]$ and $y[n]$ are $n = 0,1,\ldots,L-1$. Using these results, it can be easily shown from Eq. (12a) that the range of $h[n]$ in Eq. (10a) is given by $-(N-1) \le n \le L-1$. Hence

$$h[n] = V^{n^2/2};\ -(N-1) \le n \le L-1. \tag{13}$$

In Eq. (13), $-(N-1) \le n \le L-1$ corresponds to the right number (i.e., no more and no less) of filter coefficients in the impulse response $h[n]$, avoiding the use of extra or redundant filter

coefficients for structural simplicity. In Eq. (13), $h[n]$ for $n < 0$ corresponds to a non-casual filter which is not practical for real-time implementation. To make $h[n]$ a casual impulse response for real-time implementation (i.e., $h[n]$ for $n \geq 0$), delay $h[n]$ by $(N-1)$ samples to become $h[n-(N-1)]$ and a new variable $h_1[n]$ is thus defined as $h_1[n] = h[n-(N-1)] = h[n-N+1]$. Substituting this expression into Eq. (13) gives

$$h_1[n] = h[n-(N-1)] = V^{(n-N+1)^2/2}; \quad 0 \leq n \leq L+N-2. \tag{14}$$

Note that $-(N-1) \leq n \leq L-1$ in $h[n]$ in Eq. (13) has been changed to $0 \leq n \leq L+N-2$ in $h_1[n]$ in Eq. (14) because $h[n]$ has been delayed by $(N-1)$ samples to give $h_1[n]$. Putting $h_1[n] = h[n-(N-1)]$ from Eq. (14) into Eqs. (12a) and (12b) gives

$$y[n] = \sum_{k=0}^{N-1} g[k] h_1[n-k]; \; n = 0,1,\ldots, L+N-2, \tag{15a}$$

$$y[n] = g[n] * h_1[n]; \; n = 0,1,\ldots, L+N-2. \tag{15b}$$

Since $h[n]$ in Eq. (13) and hence Eq. (12) have been delayed by $(N-1)$ samples, $y[n]$ in Eq. (12) must also be delayed by the same $(N-1)$ samples because $g[k]$ $(k = 0,1,\ldots, N-1)$ in Eq. (12) remains unchanged. Hence, in Eqs. (15a) and (15b), $n = 0,1,\ldots, L+N-2$ for $y[n]$ because $h_1[n]$ in Eq. (14) also has $n = 0,1,\ldots, L+N-2$. Since $y[n]$ has been delayed by $(N-1)$ samples according to Eq. (15), $X[n]$, the chirp factor $V^{-n^2/2}$ and $y[n]$ in Eq. (11) must also be delayed by the same $(N-1)$ samples such that

$$X[n] = V^{-(n-N+1)^2/2} \cdot y[n]; \; n = 0,1,\ldots, L+N-2. \tag{16}$$

Since $X[n]$ in Eq. (16) has been delayed by $(N-1)$ samples, the L useful (or correct) output frequency samples $X_{\mathrm{u}}[n]$ correspond to the samples of $X[n]$ that are $(N-1)$ samples in advance such that

$$X_{\mathrm{u}}[n] = X[n+N-1]; \; n = 0,1,\ldots, L-1. \tag{17}$$

Equation (8) can be written as

$$g[n] = x[n] \times \left[a[n] \exp(j\alpha[n]) \right]; \; n = 0,1,\ldots, N-1, \tag{18a}$$

where

$$a[n] = \left(r_0^{-n} \right) \left(R_0^{-n^2/2} \right), \tag{18b}$$

$$\alpha[n] = -\left(n\theta_0 + \frac{n^2}{2}\phi_0 \right). \tag{18c}$$

Putting Eq. (5) into Eq. (14) gives

$$h_1[n] = b[n]\exp(j\beta[n]);\ n = 0,1,\ldots,L+N-2, \tag{19a}$$

where

$$b[n] = R_0^{(n-N+1)^2/2}, \tag{19b}$$

$$\beta[n] = +\frac{(n-N+1)^2}{2}\phi_0. \tag{19c}$$

Putting Eq. (5) into Eq. (16) gives

$$X[n] = y[n]\times\left[c[n]\exp(j\gamma[n])\right];\ n = 0,1,\ldots,L+N-2, \tag{20a}$$

where

$$c[n] = R_0^{-(n-N+1)^2/2}, \tag{20b}$$

$$\gamma[n] = -\frac{(n-N+1)^2}{2}\phi_0, \tag{20c}$$

$$X_{\mathrm{u}}[n] = X[n+N-1];\ n = 0,1,\ldots,L-1. \tag{20d}$$

Note that Eq. (20d) is the same as Eq. (17). Equation (20a) gives all (i.e., $L+N-1$) the output frequency samples. However, the L useful output frequency samples are $\{X_{\mathrm{u}}[0]\, X_{\mathrm{u}}[1]\ldots X_{\mathrm{u}}[L-1]\} = \{X[N-1]\, X[N]\ldots X[L+N-2]\}$ according to Eq. (20d) while $\{X[0]\, X[1]\ldots X[N-2]\}$ in Eq. (20a) are the redundant or non-useful output frequency samples which should not be implemented to simplify the architecture. In summary, Eqs. (18a), (15a), (15b), (19a), (20a) and (20d) describe the simplified CZT algorithm using the discrete-time convolution method and its block diagram representation is shown in Fig. 1. The FIR filter with an up-chirp impulse response $h_1[n]$ defined in Eq. (19a) is called a *chirp* filter for the following reason. The algorithm is called the simplified *chirp z*-transform (CZT) algorithm because $h_1[n]$ is a complex exponential sequence with linearly increasing frequency. These kinds of signals (or impulse responses) are called *chirp* signals (or impulse responses) in radar systems and hence the name *chirp* in the simplified CZT algorithm [3−6]. Hence the FIR filter with $h_1[n]$ defined in Eq. (19a) is called the *chirp* filter. Radar and sonar signal processing systems similar to the simplified CZT system shown in Fig. 1 have been widely used for pulse compression [3−6]. The simplified CZT algorithm basically consists of three operations in the following sequential order (see Fig. 1): (i) pre-multiply down chirp; (ii) convolution; and (iii) post-multiply down chirp. Down chirp means that there is a negative sign in $\alpha[n]$ [Eq. (18c)] and also in $\gamma[n]$ [Eq. (20c)] while up chirp means that there is a

positive sign in $\beta[n]$ [Eq. (19c)].

3. Synthesis of a reconfigurable OCZT processor with a simplified architecture

Using the simplified CZT algorithm described in Section 2, this section presents the synthesis

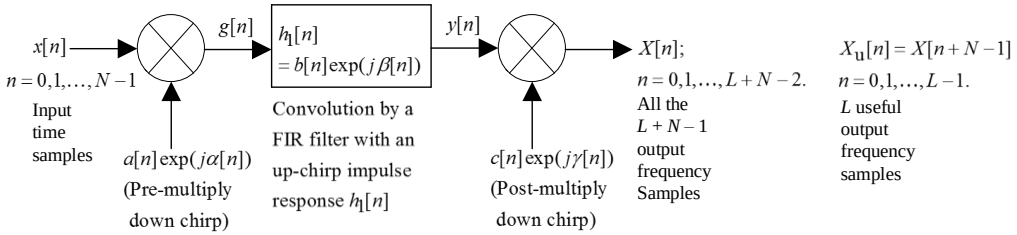

Fig. 1. Block diagram representation of the simplified CZT algorithm using the discrete-time convolution method.

of a reconfigurable OCZT processor using the silica-based PLC technology [7−12]. Other integrated-optic technologies (e.g., the silicon-on-insulator (SOI) platform which is compatible with the complementary metal-oxide-semiconductor (CMOS) technology) could also be employed for the implementation of the reconfigurable OCZT processor [13,14]. Two designs of the tunable OCZT processor based on the same architecture are presented here to cater for different application requirements. The optical synthesis of $a[n]$ and $\alpha[n]$ is described as follows. As explained in the texts below Eq. (27b) and also in Eq. (33), the phase angle $\alpha[n]$ defined in Eqs. (18a) and (18c) can be realized using a thermo-optic-based tunable phase shifter (PS) [7−11]. While the amplitude $a[n]$ defined in Eqs. (18a) and (18b) can be realized using a thermo-optic-based tunable coupler (TC) with a coupling coefficient of between 0 and 1 (inclusive) [7−11, 15]. Applying $a[n] \le 1$ on Eq. (18b) gives

$$r_0 \ge \frac{1}{R_0^{n/2}}; \quad n = 0,1,\ldots,N-1, \tag{21a}$$

or

$$R_0 \ge \frac{1}{r_0^{2/n}}; \quad n = 0,1,\ldots,N-1. \tag{21b}$$

Note here that $a[n]$ has been designed to be in the range of $0 \le a[n] \le 1$ (rather than $a[n] > 1$) so that it can be realized using a TC, eliminating the need to use an optical gain element which will be much more difficult to fabricate. Comparing Eq. (19b) with Eq. (20b) gives

$$b[n] = \frac{1}{c[n]}; \; n = 0,1,\ldots,L+N-2, \tag{22}$$

from which two possible designs are

$$\text{Design 1: if } b[n] \le 1 \text{ then } c[n] \ge 1 \text{ and} \tag{23a}$$

$$\text{Design 2: if } b[n] \ge 1 \text{ then } c[n] \le 1. \tag{23b}$$

These designs have $a[n] \le 1$ and they are described in Sections 3.1 and 3.2, respectively.

3.1 Design 1: $a[n] \le 1,\ b[n] \le 1,\ c[n] \ge 1$

In this Design 1, applying $b[n] \le 1$ on Eq. (19b) gives

$$0 < R_0 \le 1. \tag{24}$$

Applying Eq. (24) on Eq. (21a) gives

$$r_0 \ge 1. \tag{25}$$

This Design 1 requires $c[n] \ge 1$, and to avoid using an optical gain element to realize $c[n] \ge 1$, the following approach is employed. Also, $c[n] \ge 1$ cannot be implemented using a TC with a coupling coefficient of between 0 and 1 (inclusive) unless $X[n]$ in Eq. (20a) is normalized. Thus, normalize $X[n]$ in Eq. (20a) to give

$$X[n] = c[n]_{\max} \left[y[n] \times c'[n] \times \exp(j\gamma[n]) \right], \tag{26}$$

where $c[n]_{\max}$ ($c[n]_{\max} > 1$) is the maximum value of $c[n]$ and $c'[n] = c[n] / c[n]_{\max}$ where $0 \le c'[n] \le 1$. Now $0 \le c'[n] \le 1$ can be implemented using a TC with a coupling coefficient of between 0 and 1 (inclusive), and this is the same situation as $0 \le a[n] \le 1$, as described above. The optical synthesis of $0 \le a[n] \le 1$ and $0 \le c'[n] \le 1$ using the TC is explained below. In Eq. (26), $c[n]_{\max} > 1$ can be implemented using gain provided by an erbium-doped fiber amplifier (EDFA), as explained below.

Using Eqs. (18a), (15a), (15b), (19a), (20a) and (20d) and Fig. 1, Fig. 2 shows the schematic diagram of the synthesized reconfigurable OCZT processor based on the silica-based PLC technology. Without loss of generality, the waveguide loss is neglected for ease of analysis. In Fig. 2(b), in assigning the notations $\{x[0]\, x[1] \ldots x[N-1]\}$ at the inputs of the $g[n]$ block, the splitting loss of the $1 \times N$ splitter in the serial-to-parallel converter is ignored for ease of analysis. Similarly, in Fig. 2(d), in assigning the notations $\{y[N-1] \ldots y[L+N-3]\, y[L+N-2]\}$ at the inputs of the $X[n]$ block, the splitting loss of the $1 \times L$ splitter in the serial-to-parallel converter is neglected for ease of analysis. However, these splitting losses will be taken into consideration below as shown in Eq. (27). The serial-to-parallel converters and the samplers shown in Figs. 2(b) and 2(d) are described below. The splitters and combiners in Figs. 2(b)−2(d), which consist of the cascade of Y-branch waveguides arranged in a binary fashion, can be designed using the wavefront matching method [12]. This type of splitter/combiner is better than a slab splitter/combiner, including a star coupler and a multi-mode interference (MMI) splitter/combiner, in terms of the uniformity of the splitter ratio [8]. To compensate for the splitting losses of the three splitters in Figs. 2(b)−2(d), the two G terms (the intensity gains) are provided by an EDFA at the input and another EDFA at each output:

$$\left(\sqrt{G}\right)\left(\frac{1}{\sqrt{N}}\right)\left(\frac{1}{\sqrt{L+N-1}}\right)\left(\frac{1}{\sqrt{L}}\right)\left(\frac{1}{c[n]_{\max}}\right)\left(\sqrt{G}\right)=1, \tag{27a}$$

$$G=\sqrt{N}\cdot\sqrt{L+N-1}\cdot\sqrt{L}\cdot c[n]_{\max}, \tag{27b}$$

where $1/\sqrt{N}$ is the splitting loss of the splitter in Fig. 2(b), $1/\sqrt{L+N-1}$ is the splitting loss of the splitter in Fig. 2(c), and $1/\sqrt{L}$ is the splitting loss of the splitter in Fig. 2(d). In Fig. 2(a), the tunable PS is a thin-film heater loaded on the waveguide and utilizes the thermo-optic effect to induce a phase change of the optical carrier by φ_n [7−11]. The PSs are used in Figs. 2(b)−2(d). In Fig. 2(a), the TC is a symmetrical Mach-Zehnder interferometer that consists of two 3-dB directional couplers (DCs), two waveguide arms of equal length and a thin-film heater, with a carrier phase change of φ_n, deposited on one of the arms for controlling the desired coupling coefficient [7−11], [15]. The TCs are used in Figs. 2(b)−2(d). The OCZT processor is reconfigurable due to the tunable features of the tunable PSs and TCs. The TC's transfer function is given by [15]

$$C_n=|C_n|\exp\left(j\angle C_n\right)=0.5\left[\exp\left(j\varphi_n\right)-1\right]. \tag{28}$$

The desired TC's coupling coefficient is given by

$$|C_n|=\sqrt{0.5-0.5\cos\left(\varphi_n\right)}, \tag{29}$$

which can be controlled to a desired value by adjusting the phase shift value of the tunable PS according to

$$\varphi_n=\cos^{-1}\left[1-2|C_n|^2\right]. \tag{30}$$

Accordingly, the TC's output phase is given by

$$\angle C_n=\tan^{-1}\left[\sin(\varphi_n)/\left(\cos(\varphi_n)-1\right)\right]. \tag{31}$$

The coupling coefficient $|C_n|$ and output phase $\angle C_n$ of the TC, both of which repeat themselves at every cycle of 2π, can be continuously tuned from 0 to 1 (inclusive) and from $\pi/2$ to 0, respectively, when φ_n is varied from 0 to π [15]. The optical synthesis of $a[n]$ and $\alpha[n]$ in Eq. (18) and Fig. 2(b) is explained as follows. From Fig. 2(b), $a[n]$ in Eq. (18b) is given by

$$a[n]=\left|C_{a[n]}\right|, \tag{32}$$

where $\left|C_{a[n]}\right|=|C_n|$. From Fig. 2(b), $\alpha[n]$ in Eq. (18c) is given by

$$\alpha'[n] = \alpha[n] - \angle C_{a[n]}, \tag{33}$$

where $\angle C_{a[n]} = \angle C_n$. Similarly, the optical synthesis of $b[n]$ and $\beta[n]$ in Eq. (19) and Fig. 2(c) is described as follows. From Fig. 2(c), $b[n]$ in Eq. (19b) is given by

$$b[n] = \left|C_{b[n]}\right|, \tag{34}$$

where $\left|C_{b[n]}\right| = \left|C_n\right|$. $\beta'[n]$ in Fig. 2(c) relates to $\beta[n]$ in Eq. (19c) according to

$$\beta'[n] = \beta[n] - \angle C_{b[n]}, \tag{35}$$

where $\angle C_{b[n]} = \angle C_n$. Similarly, the optical synthesis of $c'[n] = c[n] / c[n]_{\max}$ in Eqs. (26) and (20b) and $\gamma[n]$ in Eq. (20c) and Fig. 2(d) is explained as follows. From Fig. 2(d), $c'[n]$ in Eq. (26) is given by

$$c'[n] = \left|C_{c'[n]}\right|, \tag{36}$$

where $\left|C_{c'[n]}\right| = \left|C_n\right|$. $\gamma'[n]$ in Fig. 2(d) relates to $\gamma[n]$ in Eq. (20c) according to

$$\gamma'[n] = \gamma[n] - \angle C_{c'[n]}, \tag{37}$$

where $\angle C_{c'[n]} = \angle C_n$.

3.2 Design 2: $a[n] \le 1,\ b[n] \ge 1,\ c[n] \le 1$

In this Design 2, just like Design 1 described in section 3.1, $a[n] \le 1$, and $a[n]$ and $\alpha'[n]$ in Fig. 2(b) are described by Eqs. (32) and (33), respectively. In this Design 2, $b[n] \ge 1$ and applying this condition on Eq. (19b) gives

$$R_0 \ge 1. \tag{38}$$

Applying Eq. (38) on Eq. (21a) gives

$$0 < r_0 \le 1. \tag{39}$$

Since $b[n] \ge 1$ in this Design 2 cannot be realized using a TC with a coupling coefficient of between 0 and 1 (inclusive), normalize $h_1[n]$ in Eq. (19a) to give

$$h_1[n] = b[n]_{\max}\left[b'[n]\exp(j\beta[n])\right], \tag{40}$$

where $n = 0,1,\ldots,L+N-2$, $b[n]_{\max}$ $(b[n]_{\max} > 1)$ is the maximum value of $b[n]$ and

$b'[n] = b[n]/b[n]_{\max}$ where $0 \le b'[n] \le 1$. Now $0 \le b'[n] \le 1$ can be implemented using a TC, and this is the same situation as $0 \le c'[n] \le 1$ in Design 1. In Fig. 2(c), the notation $b[n]$ for Design 1 must be changed to $b'[n] = b[n]/b[n]_{\max}$ for Design 2 according to Eq. (40). Hence

$$b'[n] = \left|C_{b'[n]}\right|, \tag{41}$$

$$\beta'[n] = \beta[n] - \angle C_{b'[n]}, \tag{42}$$

where $\left|C_{b'[n]}\right| = \left|C_n\right|$ and $\angle C_{b'[n]} = \angle C_n$. Also, in Fig. 2(d), the notation $c'[n]$ for Design 1 must also be changed to $c[n]$ since $c[n] \le 1$ for Design 2. Thus

$$c[n] = \left|C_{c[n]}\right|, \tag{43}$$

$$\gamma'[n] = \gamma[n] - \angle C_{c[n]}, \tag{44}$$

where $\left|C_{c[n]}\right| = \left|C_n\right|$ and $\angle C_{c[n]} = \angle C_n$. Similarly, in Eq. (27b), replacing $c[n]_{\max}$ for Design 1 with $b[n]_{\max}$ for Design 2 gives

$$G = \sqrt{N} \cdot \sqrt{L+N-1} \cdot \sqrt{L} \cdot b[n]_{\max}. \tag{45}$$

In Fig. 2(b), the N input discrete-time samples $\{x[0]\, x[1] \ldots x[N-1]\}$ at the inputs of the $g[n]$ block can be generated using a serial-to-parallel converter and N gate-based optical samplers [7−10]. Together with the serial-to-parallel converter, the optical gates (or samplers) must synchronously sample the input continuous-time signal $x(t)$ over the time slot T and convert it into its discrete-time representation $\{x[0]\, x[1] \ldots x[N-1]\}$ [Fig. 2(b)]. The optical gates can be implemented using electro-absorption modulators (EAMs) [7−10]. In Fig. 2(b), $x(t)$ is equally split (by a $1 \times N$ splitter) into N signals which are relatively delayed (using delay lines in the delay array 1) by integer multiples of T and then time gated (by the optical samplers) so that the discrete-time samples $\{x[0]\, x[1] \ldots x[N-1]\}$ will arrive at the respective input ports of the $g[n]$ block at the same time slot of T to achieve time synchronization according to Eq. (18a). In the delay array 1, the top waveguide has the largest delay of $(N-1)T$ to slow down $x[0]$ most because it is the fastest sample. Conversely, the bottom waveguide has the smallest delay to speed up $x[N-1]$ most because it is the slowest sample. As such, all the samples $\{x[0]\, x[1] \ldots x[N-1]\}$ will simultaneously arrive at the inputs of the $g[n]$ block at the same time slot of T. In the delay array 2 of the $g[n]$ block, the delay lines differ by integer multiples of T so that the neighbouring samples of $g[n] = \{g[0]\, g[1] \ldots g[N-1]\}$ at the output of the $N \times 1$ combiner are separated by T. $a[n]$ $\alpha'[n]$ in the $g[n]$ block implement Eqs. (32) and (33), respectively, and thus the $g[n]$ block is realized. However, to fabricate the whole device on the silica-based PLC platform, the optical gates shown in Fig. 2(b) are moved to the output ports of the tunable OCZT processor

as shown in Fig. 2(d), without affecting the device characteristics due to its linearity property. The FIR filter shown in Fig. 2(c) is the implementation of Eqs. (15), (19), (34) and (35). In Fig. 2(d), the $X[n]$ block implements Eqs. (26), (36) and (37) and $X[n+N-1]$ relates to $X_{\mathrm{u}}[n]$ according to Eq. (20d). Similar to the function of the serial-to-parallel converter in Fig. 2(b), the L input discrete-time samples $y[n]=\{y[N-1]\ldots y[L+N-3]\, y[L+N-2]\}$ (which are some of the FIR filter's total $L+N-1$ output time samples in Fig. 2(c)) at the input of the serial-to-parallel converter in Fig. 2(d) are equally split (by a $1\times L$ splitter) into L discrete-time samples which are relatively delayed (using the delay lines in the delay array 1) by integer multiples of T so that $\{y[N-1]\ldots y[L+N-3]\, y[L+N-2]\}$ will arrive at the respective input ports of the $X[n]$ block at the same time slot of T to achieve time synchronization according to Eqs. (26) and (20d). In the delay array 1, the top waveguide has a larger delay of $(L-1)T$ to slow down $y[N-1]$ more because it is a faster sample. Conversely, the bottom waveguide has the smallest delay to speed up $y[L+N-2]$ most because it is the slowest sample. As such, all the samples $\{y[N-1]\ldots y[L+N-3]\, y[L+N-2]\}$ will simultaneously arrive at the respective input ports of the $X[n]$ block at the same time slot of T. In the delay array 2 of the $X[n]$ block, the delay lines differ by integer multiples of T so that $X[n]$ defined in Eqs. (26) and (20d) can be realized. At the outputs, the L useful output frequency samples are $X_{\mathrm{u}}[n]=X[n+N-1]$ $(n=0,1,\ldots,L-1)$ according to Eq. (20d). To obtain time synchronization so that all the input time samples $\{x[0]\, x[1]\ldots x[N-1]\}$ in Fig. 2(b) propagate in synchronism from one stage to the next, the waveguides (on which the TCs and PSs are placed) and the Y-branch waveguides inside the splitters and combiners must have the same delay. As such, the L useful output frequency samples $\{X_{\mathrm{u}}[0]\, X_{\mathrm{u}}[1]\ldots X_{\mathrm{u}}[L-1]\}$ will simultaneously appear at the respective output ports (i.e., before the gates and the EDFAs) of the tunable OCZT processor at the same time. Furthermore, on each waveguide path, the TC's coupling coefficient $|C_n|$ can also be adjusted to compensate for any non-uniform splitting ratio of the splitters and also for any non-uniform combining ratio of the combiners. On each waveguide path, the PS's phase shift value can also be adjusted to be slightly more or less (if needed) than the designed value to compensate for any length deviation due to fabrication error of the waveguide path. A waveguide can be fabricated to the precision of 1 μm using the silica-based PLC technology [11].

From Table 1, it is clear that the proposed tunable OCZT architecture is much simpler than that reported in [1]. The choice of the L and N values depends on the application requirements [1,2].

One important application example of the proposed tunable OCZT processor based on the simplified CZT algorithm is described as follows. As explained in [1] (see Fig. 2(b) of [1]) and [2] (see sections 2 and 3 and Table 1 of [2]), by putting $r_0=R_0=1$ into Eq. (3) (it is also Eq. (3) in [1,2]), a new tunable ODFT processor can be designed as a special case of the tunable OCZT processor based on the non-simplified CZT algorithm. The ODFT processor is tunable because θ_0 and ϕ_0 in Eq. (3) can be continuously tuned to be within $0\le\theta_0\le 2\pi$ and $0<\phi_0<2\pi$, respectively. While the current non-tunable ODFT processors designed using the fast Fourier transform (FFT) algorithm [7−10] also have $r_0=R_0=1$ but θ_0 and ϕ_0 cannot be tuned and must take the fixed values of $\theta_0=0$ and $\phi_0=2\pi/N$ with $N=L$ (see Fig. 2(a) of [1]). As such, the current non-tunable ODFT processors (such as those described

in [7−10]) are a special case of the tunable ODFT processor of [1,2]. Table 1 of [2] provides a summary of the unique advantages of the tunable ODFT processor based on the non-simplified CZT algorithm over the current non-tunable ODFT processors designed using the FFT algorithm. These unique advantages over the current non-tunable ODFT processors are also enjoyed by the proposed tunable ODFT/OCZT processor based on the simplified CZT algorithm in this work. The only difference is that the proposed tunable OCZT processor based on the simplified CZT algorithm here has a simpler architecture than that of the tunable OCZT processor based on the non-simplified CZT algorithm in [1,2].

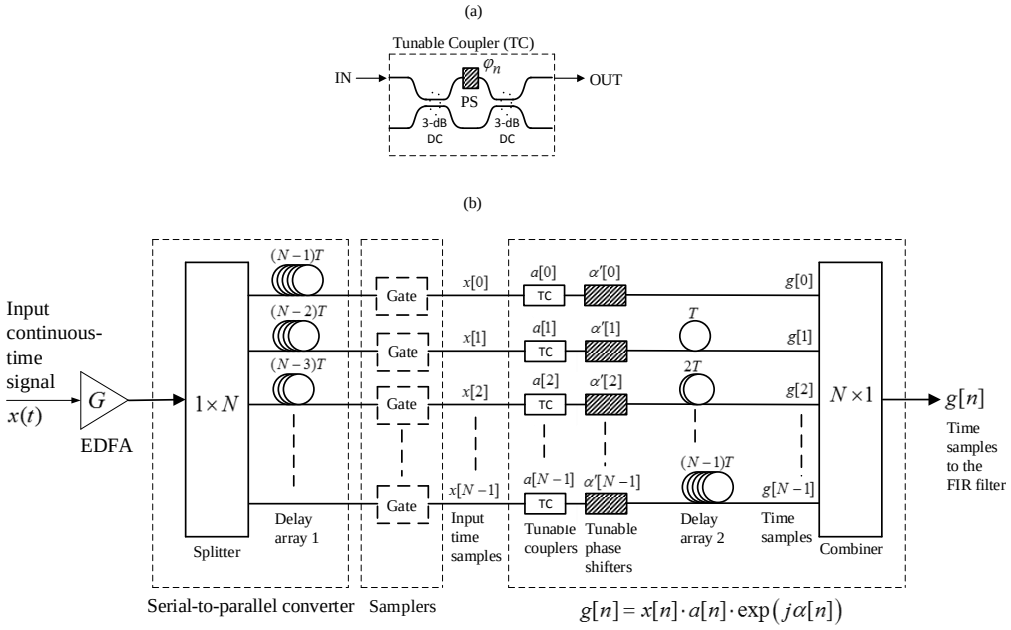

Fig. 2 (a) and (b).

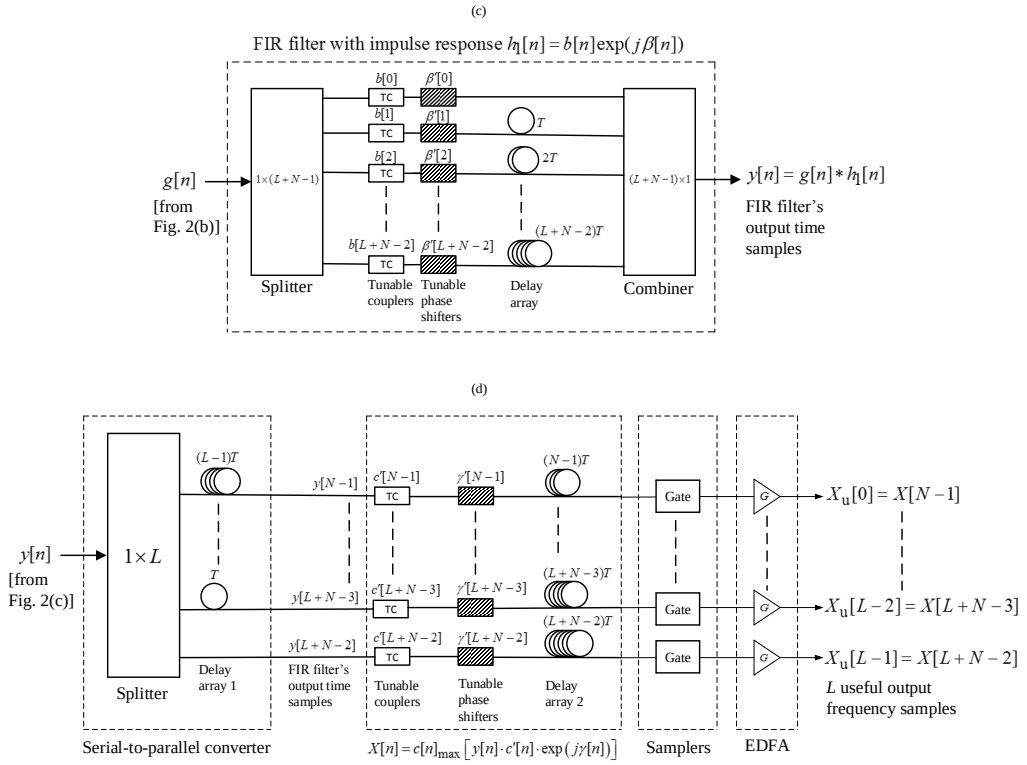

Fig. 2. Schematic diagram of the synthesized reconfigurable OCZT processor using the silica-based PLC technology. TC: tunable coupler; PS: tunable phase shifter; DC: directional coupler; and EDFA: erbium-doped fiber amplifier. (a) Tunable coupler (TC). (b) $g[n]$, as defined in Eqs. (18), (32) and (33). The gates (or samplers), as shown, are for illustration only and should be removed when fabricating the device. These gates are moved to Fig. 2(d) for structural simplicity, without affecting the device performance. (c) $y[n]$, as defined in Eqs. (15), (19), (34) and (35). (d) $X[n]$, as defined in Eqs. (26), (36) and (37), and $X_{\mathrm{u}}[n] = X[n+N-1]$ $(n = 0,1,\ldots,L-1)$ as defined in Eq. (20d).

Table 1. The Tunable OCZT Architecture using the Simplified CZT Algorithm in this paper is Much Simpler than that using the Non-simplified CZT Algorithm Reported in [1]

Tunable OCZT processor with a complex architecture using the non-simplified CZT algorithm in [1].	**Tunable OCZT processor with a simpler architecture using the simplified CZT algorithm in this work.**
$N \times L$ multiplications and additions are required which are very large, especially for large N and L values [5,6].	$\sim (N+L)\log_2(N+L)$ multiplications and additions are required which are much smaller [5,6].
The required number of components in the tunable OCZT processor is very large, especially for large N and L values: 1 $1\times N$ serial-to-parallel converter, N 1 × L splitters, L N × 1 combiners, L × N waveguides, L × N TCs, L × N PSs, L gates, and L EDFAs.	The required number of components in the tunable OCZT processor is much smaller: 1 $1\times N$ serial-to-parallel converter, 1 $1\times L$ serial-to-parallel converter, 1 $N\times 1$ combiner, 1 $1\times(L+N-1)$ splitter, 1 $(L+N-1)\times 1$ combiner, $N+(L+N-1)+L$ waveguides, $N+(L+N-1)+L$ TCs, $N+(L+N-1)+L$ PSs, L gates, and L EDFAs.
There are a number of waveguide crossings or intersections (which may induce crosstalk and additional loss) that makes fabrication difficult. A tapered waveguide with an adiabatically larger width at the intersection may be used to overcome this problem [9].	There are no waveguide crossings or intersections, making fabrication much easier.

4. A design example and its potential application

This section presents the design of a new type of optical discrete Fourier transform (ODFT) processor as a special case of the synthesized OCZT presented in Section 3 to demonstrate its effectiveness. The designed ODFT can be potentially used as an optical demultiplexer at the receiver of an optical fiber orthogonal frequency division multiplexing (OFDM) transmission system [7−10]. Putting $r_0 = R_0 = 1$ (as required by an ODFT) into Eqs. (4)−(5) gives

$$X_k(\omega) = \sum_{n=0}^{N-1} \exp\left(j\theta_{k,n}\right) \cdot x(nT); \quad k = 0,1,\ldots,L-1 \tag{46}$$

where $X_k(\omega) = X[k]$, $x(nT) = x[n]$, and $\theta_{k,n} = -n\left(\theta_0 + k\phi_0\right)$. In the continuous-time domain, Eq. (46) is given as

$$X_k(t) = \sum_{n=0}^{N-1} \exp\left(j\theta_{k,n}\right) \cdot \left[\delta(t-nT) * x(t)\right] \tag{47}$$

where $\delta(t)$ is the Dirac delta function, * denotes the convolution operation, $X_k(\omega) = \mathrm{FT}\left[X_k(t)\right]$, $X(\omega) = \mathrm{FT}\left[x(t)\right]$, and FT denotes the Fourier transform operation. Taking the FT of Eq. (47), the transfer function of a novel type of ODFT (for the

*k*th output frequency sample $X_k(\omega)$; $k = 0,1,\ldots,L-1$) is given by

$$H_k(\omega) = \frac{X_k(\omega)}{X(\omega)} = \frac{1}{N} \cdot \sum_{n=0}^{N-1} \exp\left(j\theta_{k,n} \right) \cdot \exp\left[-jn\omega T \right] \qquad (48)$$

In the conventional ODFTs, $r_0 = R_0 = 1$, $N = L = 2^p$; $p = 1,2,\ldots$, $\theta_0 = 0$, and $\phi_0 = 2\pi / N = 2\pi / L$ [7−10]. In the new ODFT presented here, $r_0 = R_0 = 1$; however *N* and *L* are arbitrary integers, θ_0 can be chosen to be within $0 \le \theta_0 \le 2\pi$, and ϕ_0 can be chosen to be within $0 \le \phi_0 \le 2\pi$ provided that $\phi_0 \ge 2\pi / N$ to avoid overlapping of the neighbouring channels in the magnitude response. The chosen values of θ_0 and ϕ_0 must satisfy the fact that the *L* channels must lie within one normalized free spectral range (FSR) of 2π. Hence, the conventional ODFTs [7−10] are a special case of the new ODFT. As a design example, the new ODFT has $r_0 = R_0 = 1$, $N = 8$, $L = 7$, $\theta_0 = 50^\circ$, and $\phi_0 = 45^\circ$. The magnitude responses over one normalized FSR of 2π obtained using Eq. (48) for $L = 7$ channels (i.e., $|H_k(\omega)|^2$; $k = 0,1,\ldots,6.$) are shown in Fig. 3. For $r_0 = R_0 = 1$, $a[n] = b[n] = c[n] = 1$ according to Eqs. (18b), (19b) and (20b), respectively. Hence Design 1 and Design 2 are the same design according to Eqs. (22)−(23). Thus Design 1 is discussed here. It is a straight forward task to compute the values of the parameters shown in Fig. 2 using Eqs. (18b), (18c), (19b), (19c), (20b), (20c) and Eqs. (28)−(37) of Design 1.

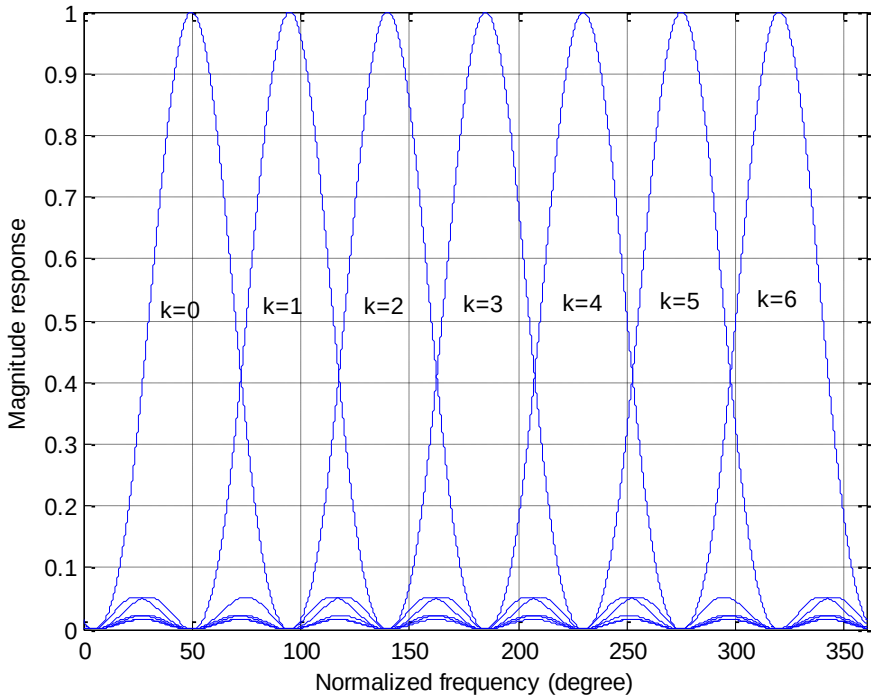

Fig. 3. Magnitude response of the new ODFT design as a special case of the synthesized OCZT with $r_0 = R_0 = 1,\ N = 8,\ L = 7,\ \theta_0 = 50^\circ$, and $\phi_0 = 45^\circ$.

5. Summary

This paper has presented a simpler architecture of an integrated-optic-based reconfigurable OCZT processor using the simplified CZT algorithm based on the discrete-time convolution method. Compared to the more complex architecture of the reconfigurable OCZT processor in [1], the proposed reconfigurable OCZT architecture is much simpler, requiring much less number of components and eliminating the waveguide crossings that would otherwise make fabrication difficult. The simpler architecture of the proposed reconfigurable OCZT processor makes it even more attractive for future research and development, especially on its numerous potential applications that are yet to be discovered because it is a fundamentally important real-time and high-speed all-optical signal processing device. As a special case of the synthesized OCZT, a novel ODFT design and its potential application as an optical demultiplexer at the receiver of an optical fiber OFDM transmission system has been presented. Is it possible to simplify or reduce the computational complexity of the already-simplified CZT algorithm presented in this work and hence a simpler OCZT architecture? This suggestion is worth considering as a future work.