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Electron velocity of 6×10^7 cm/s at 300 K in stress engineered InAlN/GaN nano-channel high-electron-mobility transistors

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A stress engineered three dimensional (3D) Triple T-gate (TT-gate) on lattice matched In_{0.17}Al_{0.83}N/GaN nano-channel (NC) Fin-High-Electron-Mobility Transistor (Fin-HEMT) with significantly enhanced device performance was achieved that is promising for high-speed device applications. The Fin-HEMT with 200-nm effective fin-width (W_{eff}) exhibited a very high I_{Dmax} of 3940 mA/mm and a highest g_m of 1417 mS/mm. This dramatic increase of I_D and g_m in the 3D TT-gate In_{0.17}Al_{0.83}N/GaN NC Fin-HEMT translated to an extracted highest electron velocity (v_e) of 6.0×10^7 cm/s, which is $\sim 1.89 \times$ higher than that of the conventional In_{0.17}Al_{0.83}N/GaN HEMT (3.17×10^7 cm/s). The v_e in the conventional III-nitride transistors are typically limited by highly efficient optical-phonon emission. However, the unusually high v_e at 300 K in the 3D TT-gate In_{0.17}Al_{0.83}N/GaN NC Fin-HEMT is attributed to the increase of in-plane tensile stress component by SiN passivation in the formed NC which is also verified by micro-photoluminescence (0.47 ± 0.02 GPa) and micro-Raman spectroscopy (0.39 ± 0.12 GPa) measurements. The ability to reach the $v_e = 6 \times 10^7$ cm/s at 300 K by a stress engineered 3D TT-gate lattice-matched In_{0.17}Al_{0.83}N/GaN NC Fin-HEMTs shows they are promising for next-generation ultra-scaled high-speed device applications. © 2015 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4906970>]

By lateral and vertical scaling, researchers have enabled 20-nm gate-length depletion mode (D-mode) Al_xGa_{1-x}N/GaN high-electron-mobility transistors (HEMTs) on SiC substrates to reach a maximum drain-current density (I_{Dmax}) ~ 4000 mA/mm and an enhanced electron-velocity (v_e) $\sim 2.7 \times 10^7$ cm/s.¹ However, further scaling of the gate-length results in poor electrostatic gate control, which would lead to high-gate-leakage current, short-channel effects such as high drain induced barrier lowering (DIBL), low $I_{\text{ON}}/I_{\text{OFF}}$ ratio, and poor sub-threshold swing (SS) of the devices. To realize superior gate control, sub-nm fins were formed on silicon to move towards realizing a theoretical limit of SS (~ 60 mV/dec).²⁻⁵ To further improve the switching speed in the logic circuits, the carrier velocity can be increased by introducing high mobility materials GaAs, AlAs, InAs, InP, and its related alloys.^{6,7} Recently, sub-nm In_xAl_{1-x}N/GaN nano-ribbon three dimensional (3D) triple I-shape gate Fin-FETs on SiC was demonstrated.⁸ In this letter, we report a stress engineered 3D Triple T-gate (TT-gate) on In_{0.17}Al_{0.83}N/AlN/GaN nano-channel (NC) Fin-HEMT on Si substrate with significantly improved transport properties. The proposed Fin-HEMTs exhibited a very-high I_{Dmax} and highest g_{mmax} which are correlated to the extracted v_e of 6.0×10^7 cm/s at 300 K. This is the highest value ever reported in literature. The high v_e in the 3D TT-gate NC Fin-HEMT is attributed to the

increase of in-plane tensile stress component by SiN passivation in the formed NC which is also verified by optical measurements.

The In_{0.17}Al_{0.83}N/AlN/GaN HEMT structure was grown on high-resistivity ($>6000 \Omega \text{ cm}$) Si(111) by metal-organic chemical-vapor-deposition. The inset 1 of Fig. 1(a) shows the cross-sectional high-resolution transmission-electron-microscopy (HR-TEM) image of In_{0.17}Al_{0.83}N/AlN/GaN heterostructure with individual layer thicknesses. An average two dimensional electron gas (2DEG) charge density (n_s) of $2.74 \times 10^{13} \text{ cm}^{-2}$ and an average 2DEG mobility (μ_H) of $760 \text{ cm}^2/\text{Vs}$ were measured using Hall-van der Pauw structures at 300 K. After the mesa-isolation and ohmic-contact formation, the NC fins were formed between the source and drain contacts by electron-beam-lithography (EBL). The InAlN/AlN channel was completely etched by BCl₃/Cl₂ plasma. The dimensions of the formed NC fins were measured using cross-sectional HR-TEM and Scanning-Electron-Microscopy (SEM). Figure 1(a) shows the cross-sectional TEM image of a single fin-width $W_{\text{Fin}} = 314$ nm. The energy dispersive X-ray (EDX) area mapping revealed the material composition of InAlN/GaN NC. From Fig. 1(a), it is confirmed that the NC fins were formed using the dry etching process. The fin-widths (W_{Fin}) were 176 and 314 nm while the height was 12 nm. The effective fin-width was calculated using, $W_{\text{eff}} = [\text{number of fins} \times \{ (W_{\text{Fin}} + (2 \times H_{\text{Fin}})) \}]$. The T-gate on NC fins was formed using a process similar to that of conventional HEMTs. The fabrication details of the

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FIG. 1. (a) Cross-sectional HR-TEM image of InAlN/GaN HEMT structure [effective Fin width $W_{\text{eff}} = W_{\text{Fin}} + 2(H_{\text{Fin}}) = 339$ nm], cross-sectional area EDX mapping for different elements in the InAlN/GaN nano-channel (NC), *Inset 1*: cross-sectional HR-TEM image of InAlN/AlN/GaN heterostructure, *Inset 2*: Cross-sectional HR-TEM image of T-gate NC Fin-HEMT [y-axis cut of Fig. 1(b)]; (b) Three dimensional schematic view of Triple T-gate on InAlN/GaN nano-channel; (c) Schematic cross-section of T-shape gate configuration with different stress regions [(i) SiN/Au/Ni stress layers, (ii) SiN/Au/Ni/SiN stress layers and (iii) SiN/SiN stress layers] to InAlN/GaN nano-channel.

conventional HEMTs can be found in Ref. 9. Figure 1(b) shows the 3D schematic diagram of the fabricated triple T-gate InAlN/GaN NC Fin-HEMT on Si substrate. Three different stress regions are involved as a result of introducing T-shape gate structures to the NC Fin-HEMTs. Figure 1(c) shows the three different stress regions [(i) SiN/Au/Ni stress-layers, (ii) SiN/Au/Ni/SiN stress-layers, and (iii) SiN/SiN stress-layers] of T-gate InAlN/GaN HEMTs. For comparison, conventional HEMTs with $L_g = 170$ nm were also fabricated on the same wafer with gate-widths, W_g of $(1 \times 25) \mu\text{m}$, $(2 \times 25) \mu\text{m}$, and $(2 \times 75) \mu\text{m}$. For this study, the device dimensions of source-gate distance (L_{sg}) = 850 nm; gate-drain distance (L_{gd}) = 1800 nm; and $L_g = 170$ nm were maintained for both NC Fin-HEMTs and conventional HEMTs. To study the influence of stress by SiN on NC Fin-HEMT and on conventional HEMT, four types of devices were fabricated, *Device-A*: 3D TT-gate InAlN/GaN NC Fin-HEMT with SiN passivation (stressed), *Device-B*: 3D TT-gate InAlN/GaN NC Fin-HEMT without SiN passivation (un-stressed), *Device-C*: Conventional InAlN/GaN HEMT with SiN passivation (stressed), and *Device-D*: Conventional InAlN/GaN HEMT without SiN passivation (un-stressed). The capacitance-voltage (C-V) characteristics of the Schottky diode were also measured at 1 MHz. The v_e of the NC Fin-HEMT and conventional HEMT were also estimated using a previously investigated 2D model for GaN transistors.¹⁰ To study the stress in the formed NC with and without SiN stress layer, micro-Photoluminescence (PL) and micro-Raman measurements were carried out. The measurement details can be found in the supplementary file.¹¹

Figure 2 shows (a) $I_{\text{DS}}-V_{\text{DS}}$ (b) transfer [$I_{\text{D}}(g_m)$, $|I_g|-V_g$] characteristics of 3D TT-gate NC Fin-HEMT (*Device-A*), and Conventional HEMTs (*Device-C*) on Si substrate. Though, the forward gate current (I_g) at 2 V is high for NC Fin-HEMTs, the device did not breakdown. The Fin-HEMT and conventional HEMT exhibited I_{Dmax} of 3940 mA/mm and 1225 mA/mm at $V_g = +1$ V, respectively. Furthermore, the 3D TT-gate NC Fin-HEMTs also exhibited record-high g_{mmax} of 1417 mS/mm at $V_{\text{D}} = 6$ V. The observed I_{Dmax} and

g_{mmax} values are the highest ever reported in the literature for NC Fin-HEMTs on Si(111). Previous investigations of Fin-FETs with I-shape gate suggested that the improvement in I_{D} and g_m could be due to an un-changed source resistance (R_s) even at high I_{D} conditions.⁸ However, the measured R_s of NC Fin-HEMT is not un-changed with the increase of I_{D} .¹¹ Hence, we do not expect any enhancement in I_{D} or g_m due to R_s . To investigate the improved transport properties, we extracted the v_e for both NC Fin-HEMT (*Device-A*) and conventional HEMT (*Device-C*) using the measured $I_{\text{D}}-V_g$ characteristics [Fig. 2(b)]. Effective gate voltage at the source end of the gate was calculated directly from the $I-V$ characteristics, $V_{g,\text{internal}} = V_g - R_s \times I_{\text{D}}(V_g)$, where $V_{g,\text{internal}}$ is the gate-channel voltage, V_g is the applied gate voltage, and I_{D} is the measured drain current. The effective gate voltage 2DEG density at the source end of the gate was extracted from the measured C-V characteristics by integrating the C-V curve. The v_e is estimated using the formula:¹⁰ $v_e(V_g) = I_{\text{D}}(V_g) / \{en_s(V_{g,\text{internal}})\}$. Figure 2(c) shows v_e versus n_s for both conventional HEMTs (*Device-C*) and 3D TT-gate NC Fin-HEMTs (*Device-A*) with $W_{\text{eff}} = 200$ nm. The experimental curves are compared with the theoretical v_e as a function of $n_s (= 1 \times 10^{12} - 8 \times 10^{12} \text{ cm}^{-2})$, estimated using a previously investigated 2D model for GaN transistors.¹⁰ For conventional HEMTs (*Device-C*), we found the experimental v_e matches the theoretical prediction well. In contrast, for the 3D TT-gate NC Fin-HEMTs (*Device-A*), the extracted v_e of $6.0 \times 10^7 \text{ cm/s}$ is much higher than the reported drift-velocity of $\sim 3.2 \times 10^7 \text{ cm/s}$ at high electric-fields.¹² The extracted v_e ($\sim 3.17 \times 10^7 \text{ cm/s}$) of conventional HEMT (*Device-C*) is closer to the reported drift-velocity at high electric-fields.¹² Danilchenko *et al.*¹³ extracted a drift-velocity of $6.8 \times 10^7 \text{ cm/s}$ in AlGaIn/GaN heterostructure at a high electric-field (0.3 MV/cm) by measuring a current from dumbbell-shaped sample only at 4.2 K with rectangular contacts. Since our transistors are having non-uniform electric-field, we have not discussed the extracted v_e as a function of electric-field. The higher v_e correlated well with the higher I_{Dmax} and g_{mmax} in these 3D TT-gate NC Fin-HEMTs (*Device-A*). The v_e in 3D TT-gate NC Fin-HEMT (*Device-A*)

FIG. 2. (a) I_D - V_{DS} (b) transfer [$I_D(g_m), |I_g|$]- V_g characteristics of conventional InAlN/GaN HEMTs and 3D TT-gate InAlN/GaN NC Fin-HEMTs. (c) Calculated electron velocity (v_e) for 3D TT-gate InAlN/GaN NC Fin-HEMT, conventional HEMT, and 2D model.

at $V_D = 6$ V values are $\sim 2 \times$ higher than that of the conventional HEMT (*Device-C*). While the experimental data unequivocally suggests the high v_e ($\sim 6 \times 10^7$ cm/s), the underlying cause of this can be explained as follows: Normally, the v_e depends mainly on (i) the optical-phonon scattering rate and (ii) the change in electron effective mass. Therefore, we believe that one of these two factors is significantly changed in the case of the NC transistors. The observation of higher v_e could be a modification in the optical-phonon spectrum or scattering rates, possibly due to the 3D geometry or due to the effective mass being altered by the stress caused by lateral scaling (fin formation) and the induced in-plane stress by the PECVD deposited SiN films and T-shape gate. One hypothesis to explain the highest reported v_e is that variable stress along the nano-channel leads to significant variations in the conduction-band-edge.

Such variations could lead to an electron launcher effect, leading to quasi-ballistic transport across the channel, resulting in higher v_e . Since the gate metallization with T-shape prevents probing below the gate region, further work would be needed to investigate and confirm this effect.

To understand the stress related effects induced by SiN, DC characteristics, and extraction of v_e were also carried out on both NC Fin-HEMTs [$W_{eff} = (2 \times 339) = 678$ nm] and conventional HEMTs with and without SiN stress layers (*Device-A* and *-B* for NC Fin-HEMT and *Device-C* and *-D* for conventional HEMT). Figure 3 shows I_D - V_{DS} (a) and transfer [$I_D(g_m)$]- V_g (b) characteristics of conventional HEMT with (*Device-C*) and without (*Device-D*) SiN stress layers. For the conventional HEMT without SiN stress layer (*Device-D*), it exhibited a decrease of I_D (~ 100 mA/mm) at $V_g = +1$ V and g_m (~ 30 mS/mm) at $V_{DS} = 6$ V [Figures 3(a)

FIG. 3. (a) I_D - V_{DS} and (b) Transfer characteristics of conventional InAlN/GaN HEMT on Si substrate with and without SiN stress layers. (c) Transfer characteristics of 3D TT-gate InAlN/GaN NC Fin-HEMT with SiN stress layer (*Device-A*). (d) Extracted v_e for 3D TT-gate InAlN/GaN [$W_{eff} = (2 \times 339) = 678$ nm] NC Fin-HEMT with SiN stress layer (*Device-A*) and conventional InAlN/GaN [$W_g = (2 \times 75) \mu m$] HEMT with and without SiN stress layer (*Devices C and D*).

FIG. 4. Micro-PL spectrum of InAlN/GaN nano-channel (a) without and (b) with SiN stress layer.

and 3(b)]. The increase of I_D and g_m has also been observed and reported for AlGaIn/GaN HEMTs and InAlN/GaN HEMTs with SiN stress layers (passivation).^{14–17} Figure 3(c) shows the transfer [$I_D(g_m)-V_g$] characteristics of 3D TT-gate NC Fin-HEMT ($W_{\text{eff}}=678$ nm) with SiN stress layers (*Device-A*). The Fin-HEMT without SiN stress layer (*Device-B*) exhibited poor device characteristics (not shown here) which are due to the high access resistance in the NC. To validate the increase of I_D and g_m by SiN stress layer, the v_e was also extracted for the devices with and without SiN stress layer (*Devices A, C, and D*). Figure 3(d) shows the extracted v_e versus n_s for 3D TT-gate InAlN/GaN Fin-HEMT ($W_{\text{eff}}=678$ nm) with SiN stress layers (*Device-A*) and conventional HEMT with and without SiN stress layers (*Devices C and D*). Very small decrease of v_e (2.76×10^7 – 1.78×10^7 cm/s) was observed in conventional HEMTs without SiN stress layer (*Device-D*). However, the 3D TT-gate NC Fin-HEMT with SiN stress layers (*Device-A*) exhibited very high v_e of 5.44×10^7 cm/s. From this experimental evidence, we can conclude that the stress layer SiN is inducing large amount of tensile stress to the 3D TT-gate NC Fin-HEMT (*Device-A*) when compared to conventional HEMTs (*Device-C*).

To investigate the influence of stress in the NC by SiN passivation, micro-PL and micro-Raman measurements were carried out on the NC with and without SiN passivation. To address stress-induced band-gap shifts, the nature of the

2DEG UV-PL which is basically the band-edge PL peak of GaN was studied from line scan across the NC along the source-gate-drain contacts [see insets of Figs. 4(a) and 4(b)]. Figure 4 shows the micro-PL spectrum acquired in the buffer, side-walls of the NC and top of the NC (a) without SiN (*Device-B*) and (b) with SiN passivation (*Device-A*). The induced amount of tensile stress can be calculated using the expression: $\Delta E = K\sigma$, where K is the proportionality factor of 21.2 ± 3.2 meV/GPa and σ is the in-plane stress component.¹⁸ The SiN interface between InAlN/GaN NC and the etched GaN region is different [see the trace 3 and 1 of Fig. 4(b)]. The peak-shift of about 16.5 meV is clearly seen in the micro-PL line scan of SiN passivated NC region [Fig. 4(b)]. From the ~ 10 meV peak-shift of the SiN covered NC with respect to the SiN covered conventional HEMT surface,¹¹ an additional in-plane stress component of about 0.47 ± 0.02 GPa can be estimated. The characteristics of PL spectra are explained in the supplementary data.¹¹

UV-visible micro-Raman measurements were also performed on the HEMT structure to probe the nature of stress at the 2DEG interfaces. The in-plane stress can be determined from the relationship:¹⁹ $\Delta\omega = K_R\sigma$, where $K_R = 4.3$ cm⁻¹/GPa⁻¹. To address the vibrational properties of top interfaces, 325 nm UV-Raman measurements were performed. The UV-Raman spectra were fitted with Lorentzian curves to extract the peak-shifts within the spectral resolution of the instrument.¹¹ Figure 5(a) shows the typ-

FIG. 5. (a) Micro-Raman spectrum of InAlN/GaN nano-channel and conventional InAlN/GaN HEMT structure without SiN stress layer and (b) zoomed E_2 -High peak of Fig. 5(a).

ical UV-Raman spectrum of the conventional HEMT surface including E_2 -high mode at 565.7 cm^{-1} , and the related interface vibration modes. Due to the thick SiN passivation layer, the UV-Raman signal from interface is weak and difficult to resolve. Therefore, a comparative analysis is done from the NC after the removal of SiN and the UV-Raman line scan shows a variation of E_2 -high phonon peak in the range of $563.5\text{--}564.5\text{ cm}^{-1}$. Even after the removal of SiN stress layer, the NC region shows an E_2 -high peak-shift, of $\sim 1.7\text{ cm}^{-1}$ [Fig. 5(b)], which is significant with respect to the surface of as-grown conventional HEMT structure. This confirms the existence of induced tensile stress of $0.39 \pm 0.12\text{ GPa}$ in the NC by SiN passivation.

In summary, we demonstrated a stress engineered 3D triple T-gate $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ NC Fin-HEMTs with record-high performances. The dramatic increase of I_D and g_m in the Fin-HEMT are correlated with highest v_e of $6.0 \times 10^7\text{ cm/s}$ at 300 K. The high v_e at 300 K in 3D TT-gate NC Fin-HEMT is therefore attributed to the increase of in-plane tensile stress component by SiN passivation in the formed NC which is also confirmed by micro-PL ($0.47 \pm 0.02\text{ GPa}$) and micro-Raman ($0.39 \pm 0.12\text{ GPa}$) measurements. The ability to reach highest $v_e = 6 \times 10^7\text{ cm/s}$ at 300 K by a stress engineered 3D TT-gate $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ NC Fin-HEMTs opens up new frontiers to further achieve higher performance in nano-scale III-Nitride materials and its devices.

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- ¹¹See supplementary material at <http://dx.doi.org/10.1063/1.4906970>. Figure S1 shows the R_s/R_{s0} measured at $I_D = 0\text{ A/mm}$ versus I_{DS} . Inset shows the setup to measure R_s at different I_{DS} . Experimental details of micro-PL and micro-Raman measurements. Figure S2 shows Micro-PL line-scan results from the InAlN/GaN nano-channel (a) with and (b) without SiN.
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