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Effect of OFF-state stress induced electric field on trapping in AlGaN/GaN high electron mobility transistors on Si (111)

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The influence of electric field (EF) on the dynamic ON-resistance (dyn-$R_{DS[ON]}$) and threshold-voltage shift (ΔV_{th}) of AlGaN/GaN high electron mobility transistors on Si has been investigated using pulsed current-voltage (I_{DS}-V_{DS}) and drain current (I_D) transients. Different EF was realized with devices of different gate-drain spacing (L_{gd}) under the same OFF-state stress. Under high-EF ($L_{gd} = 2\,\mu m$), the devices exhibited higher dyn-$R_{DS[ON]}$ degradation but a small ΔV_{th} (~120 mV). However, at low-EF ($L_{gd} = 5\,\mu m$), smaller dyn-$R_{DS[ON]}$ degradation but a larger ΔV_{th} (~380 mV) was observed. Our analysis shows that under OFF-state stress, the gate electrons are injected and trapped in the AlGaN barrier by tunnelling-assisted Poole-Frenkel conduction mechanism. Under high-EF, trapping spreads towards the gate-drain access region of the AlGaN barrier causing dyn-$R_{DS[ON]}$ degradation, whereas under low-EF, trapping is mostly confined under the gate causing ΔV_{th}. A trap with activation energy 0.33 eV was identified in the AlGaN barrier by I_D-transient measurements. The influence of EF on trapping was also verified by Silvaco TCAD simulations.
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AlGaN/GaN high electron mobility transistors (HEMTs) on Si has emerged as a promising solution for cost-effective high-power switching electronics.[1] Leveraging on the availability of 200-mm diameter GaN-on-Si wafers and maturity of Si-CMOS process, GaN-on-Si is now an attractive choice for commercialization.[2] Though various research groups have demonstrated excellent performances of AlGaN/GaN HEMTs on Si, reliability issues such as current-collapse[3,4] and dynamic ON-resistance (dyn-$R_{DS[ON]}$) degradation[3,5] still persist. For high-voltage switching operations, it is very important to have control over dyn-$R_{DS[ON]}$ of the device.[6] Chu *et al.*[7] achieved low dyn-$R_{DS[ON]}$/stat-$R_{DS[ON]}$ ratio (1.6 at 600 V) in normally off AlGaN/GaN MISHEMTs on Si by employing multiple field-plates. Huang *et al.*[8] demonstrated reduction of dyn-$R_{DS[ON]}$ degradation in AlGaN/GaN HEMTs by AlN passivation. Recently, we demonstrated low dyn-$R_{DS[ON]}$ (0.58 mΩ-cm^2) in AlGaN/GaN HEMTs, achieved by ammonium-sulphide [$(NH_4)_2S_x$] treatment followed by SiN passivation.[9] High-EF stress to the device induces both temporary and permanent current-collapse due to electron trapping and mechanical strain in GaN HEMTs.[10] Meneghesso *et al.*[11] investigated the high-EF reliability and the role of surface/bulk traps by analysing the threshold-voltage shift (ΔV_{th}) and increase of access resistance in un-passivated AlGaN/GaN HEMTs on SiC. However, most of these reports have not discussed the effect of EF on the trapping location which influences dyn-$R_{DS[ON]}$ and V_{th}. Although both dyn-$R_{DS[ON]}$ degradation and ΔV_{th} are consequences of trapping, we believe that the EF generated in the device during an applied-bias plays a vital role by influencing these two effects separately. Eventhough EF can be varied by changing the applied-bias, we have chosen to vary EF by varying device L_{gd}, under the same OFF-state stress. This gives us a better understanding of the effects of EF in the optimization of device dimensions for power-switching applications. HEMTs with $L_{gd} = 2$ to $6\,\mu m$ were used in this study. By treating the I_D-dispersion in the linear and saturation regions of the pulsed I_{DS}-V_{DS} characteristics as two separate events, this work explains the EF related electron trapping mechanisms and its effects on dyn-$R_{DS[ON]}$ and V_{th} in AlGaN/GaN HEMTs on silicon. Dyn-$R_{DS[ON]}$ degradation and ΔV_{th} were quantified from pulsed I_{DS}-V_{DS} and pulsed-transfer (g_m-V_G) characteristics. Additionally, temperature dependent I_D-transient measurements were used to study the trap properties. Finally, the experimental results were validated using 2-D numerical simulations (Silvaco TCAD).[12]

The GaN HEMT structure {inset of Fig. 1(a)} was grown by metal-organic chemical vapor deposition on 100-mm high-resistivity Si (111) substrate.[13] After mesa isolation by BCl_3/Cl_2 plasma etching, non-gold metal stack (Ta/Si/Ti/Al/Ni/Ta) was deposited as ohmic contacts. This metal scheme exhibited a low R_C (0.24 Ω-mm) after annealing at 800 °C for 30 s.[14] After ammonium sulphide [$(NH_4)_2S_x$] treatment,[15] 120-nm-thick SiN was deposited by plasma-enhanced chemical vapor deposition (PECVD). The non-gold gate electrode was formed using Ni/Al/Ta (50/400/50-nm) metal stack after etching SiN by CF_4/O_2 plasma. Finally, the devices were passivated with 120-nm-thick PECVD grown SiN. The devices had an L_{gd} of 2 to 6 μm, source-to-gate spacing (L_{gs}) of 1 μm, and a gate length (L_g) of 2 μm. DC and pulsed I_{DS}-V_{DS} measurements were performed using Kiethley 2636 A source meter and Accent DiVA D265, respectively. Quiescent-bias (Q-bias)

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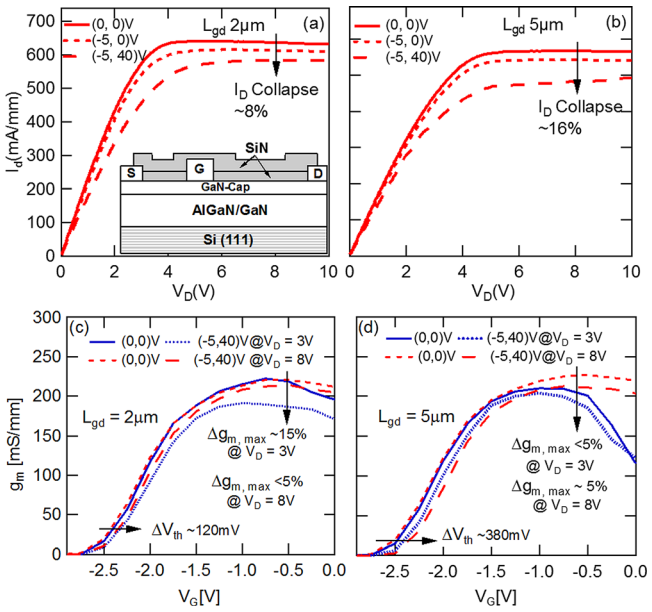

FIG. 1. Pulsed I_{DS}-V_{DS} characteristics measured at Q-bias conditions (−5,0) V and (−5,40) V for HEMTs with (a) $L_{gd} = 2\,\mu m$ [inset—device cross-section] and (b) $L_{gd} = 5\,\mu m$; Pulsed g_m-V_g characteristics at (0,0) and (−5,40) V for HEMTs with (c) $L_{gd} = 2\,\mu m$ (d) $L_{gd} = 5\,\mu m$, measured at $V_D = 3$ V and 8 V, respectively. Device dimensions: $L_{sg}/L_g/W_g = 1/2/(2 \times 100)\,\mu m$.

conditions for gate-lag and gate- and drain-lag were $(V_{GS0},V_{DS0}) = (-5,0)$ V and (−5,40) V, respectively, with a pulse-width ranging 0.2 μs to 10 μs and pulse-separation of 1 ms. Short pulse-duration was chosen to mitigate self-heating effects[4] from the gate-lag and gate- and drain-lag measurements. The stat-$R_{DS[ON]}$ and dyn-$R_{DS[ON]}$ were measured from the slopes (linear region at $V_D \leq 3$ V) of DC and pulsed I_{DS}-V_{DS} characteristics, respectively. The dyn-$R_{DS[ON]}$/stat-$R_{DS[ON]}$ ratio serves as a measure of dyn-$R_{DS[ON]}$ degradation. I_D-collapse corresponding to ΔV_{th} was measured in the saturation region ($V_D \geq 8$ V) of the pulsed I_{DS}-V_{DS} characteristics. The temperature dependent I_D-transient measurements (from 20 °C to 120 °C, increment of 20 °C) were performed using Agilent 1505 A power device analyser.

The device DC breakdown and stat-$R_{DS[ON]}$ characteristics are discussed elsewhere.[9] The pulsed I_{DS}-V_{DS} characteristics measured under (−5,0)V and (−5,40)V Q-bias conditions are shown in Figs. 1(a) and 1(b) for devices with $L_{gd} = 2$ and 5 μm, respectively. Under gate-lag condition, both devices exhibited ~3% I_D-collapse ($V_D = 8$ V) and negligible dyn-$R_{DS[ON]}$ degradation. Since the samples went through $(NH_4)_2S_x$ treatment followed by SiN passivation,[15] the devices exhibited negligible *virtual gate effect*.[16] Since the surface related traps were mitigated through passivation, any further trapping under the fully OFF-state stress condition is related to the AlGaN barrier region.[11]

To quantify I_D-collapse in the linear and saturation regions of pulsed I_{DS}-V_{DS} characteristics separately, the pulsed-transfer (g_m-V_G) characteristics of the HEMTs were measured at $V_D = 3$ V and 8 V, respectively. Figures 1(c) and 1(d) show the pulsed (pulse-width/pulse-separation = 0.2 μs/1 ms) g_m-V_G characteristics at (−5,40)V Q-bias condition for HEMTs with $L_{gd} = 2$ and 5 μm, measured at $V_D = 3$ V and 8 V. The g_m-dispersion was high (~15%) for HEMTs with $L_{gd} = 2\,\mu m$ [Fig. 1(c)] at $V_D = 3$ V, whereas the g_m-dispersion at $V_D = 8$ V was negligible. However, an overall ΔV_{th} of ~120 mV was observed. For the HEMTs with $L_{gd} = 5\,\mu m$, the g_m-dispersion (~5%) is small in both regions, but a large ΔV_{th} of ~380 mV was observed. The 15% g_m-dispersion, corresponding to dyn-$R_{DS[ON]}$ degradation observed in devices with $L_{gd} = 2\,\mu m$, is attributed to electron trapping in the gate-drain access region, whereas the larger ΔV_{th} observed in devices with $L_{gd} = 5\,\mu m$ corresponds to electron trapping under the gate.[11]

To understand the trap dynamics, pulsed I_{DS}-V_{DS} measurements were performed at different pulse-widths and fixed pulse-separation. Figure 2(a) shows the I_D-collapse (ΔV_{th}) and the dyn-$R_{DS[ON]}$/stat-$R_{DS[ON]}$ ratio of HEMTs as a function of device L_{gd} under (−5,40)V Q-bias for pulse-widths: 0.2 μs and 10 μs. The I_D-collapse (ΔV_{th}) increased with increasing L_{gd}. Under 0.2 μs pulse-width range, devices with $L_{gd} = 2$ and 5 μm exhibited an I_D-collapse of 8% and 16%, respectively ($V_D = 8$ V). Increase of I_D-collapse with increasing L_{gd} was attributed to L_{gd} dependent trapping effects by Lee *et al.*[17] However, the dyn-$R_{DS[ON]}$ degradation exhibited an opposite trend with increasing L_{gd}. No comparative analysis of dyn-$R_{DS[ON]}$ degradation and ΔV_{th} based on EF can be found in literature. Fig. 2(b) shows the dyn-$R_{DS[ON]}$/stat-$R_{DS[ON]}$ ratio of HEMTs with $L_{gd} = 2,3,4$ and 5 μm under (−5,40)V Q-bias for pulse-widths: 0.2 μs to 10 μs. All devices exhibited smaller dyn-$R_{DS[ON]}$ degradation (dyn-$R_{DS[ON]}$/stat-$R_{DS[ON]} \sim 1.04$) in the longer pulse-width (≥2 μs) range. However, in the shorter pulse-width (<2 μs) range, the HEMTs with $L_{gd} = 2$ and 3 μm exhibited larger dyn-$R_{DS[ON]}$ degradation (dyn-$R_{DS[ON]}$/stat-$R_{DS[ON]} \sim 1.27$). This increase of dyn-$R_{DS[ON]}$ degradation for smaller L_{gd} devices can be attributed to increased trapping due to activation of additional trapping centres caused by high-EF in the gate-drain region.[18] This behaviour follows the Poole-Frenkel field-dependent emission process where the rate of electron detrapping from the traps experiencing high-EF substantially increase due to potential barrier lowering given by

$$\Delta \emptyset_{PF} = \left(\frac{q^3}{\pi\varepsilon}\right)^{1/2} \sqrt{EF}, \tag{1}$$

where q is the electronic charge and ε is the dielectric constant of AlGaN. Also, the rate-of-change of the dyn-$R_{DS[ON]}$/stat-$R_{DS[ON]}$ ratio with pulse-width is very high for devices

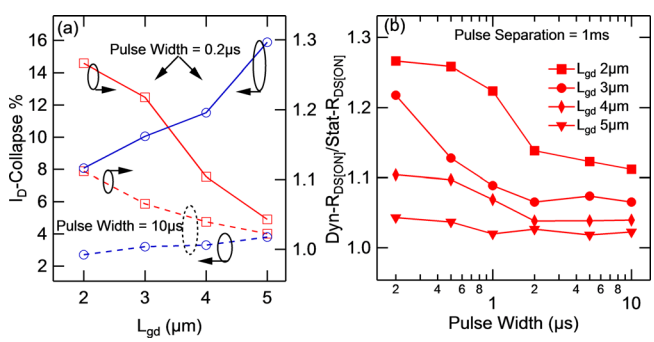

FIG. 2. (a) Dyn-$R_{DS[ON]}$/Stat-$R_{DS[ON]}$ ratio for devices of $L_{gd} = 2$ to 5 μm measured at different pulse-widths. (b) Dyn-$R_{DS[ON]}$/Stat-$R_{DS[ON]}$ ratio and I_D-collapse as a function of device L_{gd} under (−5,40) V Q-bias for pulse-widths 0.2 μs and 10 μs. Device dimensions: $L_{sg}/L_g/W_g = 1/2/(2 \times 100)\,\mu m$.

with smaller L_{gd} [Fig. 2(b)]. This corresponds to the exponential increase in electron emission rate [*e(EF)*] from the traps with the square-root of EF given by

$$e(EF) = e\,(0)\exp\left(\frac{\Delta \emptyset_{PF}}{kT}\right). \quad (2)$$

Trapping analysis was done by temperature dependent I_D-transient measurements. The devices were stressed with a filling pulse of $V_G = -5$ V and $V_D = 40$ V for 1000 ms. The I_D-transient signals were measured at very low $V_D = 1.5$ V (linear region) and $V_G = 0$ V, in-order to eliminate the effects of self-heating during measurements. The effects of self-heating due to applied bias have been reported by Albahrani *et al.*[19] The I_D-transients (normalized to final steady-state value) measured at room temperature for devices with $L_{gd} = 2$ and 6 μm are shown in Fig. 3(a). Under OFF-state stress, the devices with $L_{gd} = 2\,\mu$m show higher I_D-collapse at $V_D = 1.5$ V (linear region). The collapsed-I_D recovered through a similar de-trapping process for both devices. Figure 3(b) shows the I_D-transients of AlGaN/GaN HEMTs with $L_{gd} = 6\,\mu$m at different measurement temperatures. Figures 3(c) and 3(d) show the corresponding differential signals with amplitudes A1 and A2 for devices with $L_{gd} = 2$ and 6 μm, respectively. Both devices exhibited a thermally activated detrapping time constant, with an activation energy (E_a) of 0.33 ± 0.05 eV and capture cross-section 1.2×10^{-20} cm^2, obtained from Arrhenius plot [Fig. 3(e)]. The observed trap with $E_a = 0.33$ eV is commonly accepted to be located in AlGaN barrier.[20,21] For further confirmation, the 2-D transient simulations were performed using TCAD. An additional differential rate equation was solved for simulating the emission and capture processes. The experimentally determined trap parameters were incorporated into the model. Similarly, an OFF-state stress of $(V_G,V_D) = (-5,40)$V was applied for 1000 ms. The simulated I_D-transients (I_D/I_{Dmax}) for HEMTs with $L_{gd} = 2$ and 5 μm in the linear region [$V_D = 3$ V] and the saturation region [$V_D = 8$ V] are shown in Figs. 4(a) and 4(b), respectively. From simulations, the I_D-collapse in the linear and saturation region for device with $L_{gd} = 2\,\mu$m is 12% and 7%, respectively; and for HEMTs with $L_{gd} = 5\,\mu$m is 6% and 11%, respectively. Both simulation and experiment show high I_D-collapse for the device with $L_{gd} = 2\,\mu$m in the linear region {represented as dyn-$R_{DS[ON]}$ degradation in Fig. 2(a)}, whereas high I_D-collapse in the saturation region for the device with $L_{gd} = 5\,\mu$m. The opposite trend of I_D-collapse for the devices with $L_{gd} = 2$ and 5 μm is due to the difference in the distribution of the lateral electric field in the gate-drain access region {See Fig. 4(c)}.

Under negative gate-bias, electrons tunnel through the gate contact barrier[22] into the AlGaN barrier by a tunnelling-assisted Poole-Frenkel (TAPF) conduction mechanism.[23] Mitrofanov *et al.*[22] reported that the potential-well-height of the trap is lowered by ~0.2 to 0.25 eV under the influence of EF. The difference between the Schottky barrier height (0.61 eV) in the devices-under-test and the reduced potential-well-height closely matches with our experimentally determined E_a (0.33 eV). The simulated average-EF in the AlGaN barrier as a function of device L_{gd} under (−5,40)V bias is shown in Fig. 4(c). The device with $L_{gd} = 2\,\mu$m (~3.4MV/cm) experiences ~2-times higher EF than the device with $L_{gd} = 5\,\mu$m (~1.4 MV/cm). For the device with $L_{gd} = 2\,\mu$m, due to high-EF in the gate-drain access region, the tunnelled gate electrons which face a higher Coulomb force of attraction are drawn and trapped in the extrinsic region of the AlGaN barrier [see Fig. 4(d)], causing higher dyn-$R_{DS[ON]}$ degradation [~15% g_m-dispersion in Fig. 1(c)]. On the contrary, for HEMTs with $L_{gd} = 5\,\mu$m experiencing low-EF, extent of the tunnelled electrons being drawn and trapped into the gate-drain access region is much lesser [see Fig. 4(e)]. Thus, most of the trapping is confined to the AlGaN barrier directly under the gate, resulting in ΔV_{th} [~380 mV in Fig. 1(d)]. This shows that the EF plays a vital role in

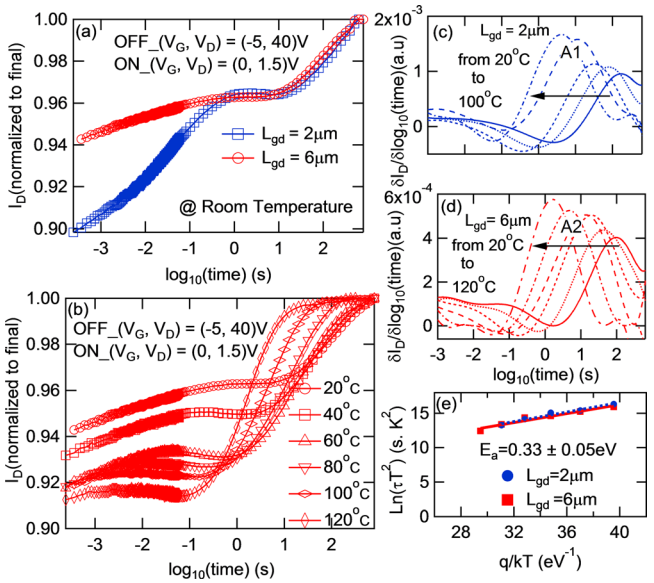

FIG. 3. I_D-transients (normalized) after an OFF-state stress of $(V_G,V_D) = (-5,40)$ V for HEMTs with (a) $L_{gd} = 2$ and 6 μm, (b) temperature dependent I_D-transient for HEMTs with $L_{gd} = 6\,\mu$m. The related differential signals for device with (c) $L_{gd} = 2\,\mu$m, (d) $L_{gd} = 6\,\mu$m, and (e) Arrhenius plot.

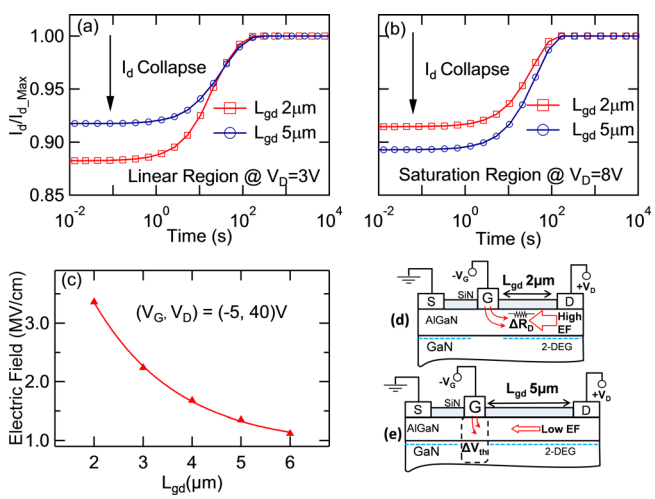

FIG. 4. 2D-transient TCAD simulations (normalized) for AlGaN/GaN HEMTs with $L_{gd} = 2$ and 5 μm; at (a) linear region ($V_D = 3$ V), (b) saturation region ($V_D = 8$ V). (c) Simulated average-EF in the AlGaN barrier under (−5,40) V Q-bias condition for HEMTs as a function of L_{gd}; Electron injection from gate metal into the AlGaN barrier under (−5,40) V Q-bias condition for HEMTs with (d) $L_{gd} = 2\,\mu$m, (e) $L_{gd} = 5\,\mu$m.

governing the location of electron trapping affecting the dyn-$R_{DS[ON]}$ or V_{th} of the devices.

The influence of EF on dyn-$R_{DS[ON]}$ and V_{th} in AlGaN/GaN HEMTs on Si has been investigated using pulsed I_{DS}-V_{DS} and I_D-transient measurements. The dyn-$R_{DS[ON]}$ degradation and I_D-collapse (ΔV_{th}) follow an opposite trend for the devices with $L_{gd} = 2$ and 5 μm, respectively. Under OFF-state stress, the electrons from the gate are injected and trapped in the AlGaN barrier by tunnelling assisted Poole-Frenkel conduction mechanism. The obtained traps with $E_a = 0.33 \pm 0.05$ eV originate from the AlGaN barrier. Under high-EF ($L_{gd} = 2\ \mu$m), the trapping is pronounced in the gate-drain access region of the AlGaN barrier resulting in dyn-$R_{DS[ON]}$ degradation. Under low-EF ($L_{gd} = 5\ \mu$m), the trapping is mostly confined in the AlGaN barrier under the gate. The experimental results are in good agreement with the TCAD transient model. The observed anomalies in dyn-$R_{DS[ON]}$ and V_{th} can be mitigated through proper EF-profile engineering and optimized growth conditions, especially in the AlGaN barrier.

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