High frequency electrical properties of copper interconnects patterned by resolution enhanced lithography

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**HIGH FREQUENCY ELECTRICAL PROPERTIES
OF COPPER INTERCONNECTS PATTERNED BY
RESOLUTION ENHANCED LITHOGRAPHY**

HIGH FREQUENCY ELECTRICAL PROPERTIES OF COPPER INTERCONNECTS
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High Frequency Electrical Properties of Copper Interconnects Patterned by Resolution Enhanced Lithography

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School of Electrical & Electronic Engineering

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STATEMENT OF ORIGINALITY

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

Rakesh Kumar

16 March, 2008

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ABSTRACT

Signal integrity problems associated with on-chip interconnects have become very significant with increase in device integration and circuit frequency. Copper and low- κ dielectric materials are used to improve electrical performance of interconnects for integrated circuits. At radio and microwave frequencies, the signal propagation behaviour of on-chip interconnects are complex to analyze and predict especially for lossy low-resistivity silicon substrates. Interconnects behave as transmission lines, and signal delay, transients, crosstalk and power dissipation become critical. In addition, integration of mesoporous dielectrics and scaling of feature size has made the patterning and processing of damascene interconnects far more challenging than initially anticipated. The fabrication, high-frequency characterization and modeling of copper interconnects are the objectives of this thesis.

This work is divided into two parts. First, the fabrication of deep submicron (100-250 nm) copper interconnects with porous ultra low- κ dielectrics in a damascene process is addressed. Resolution enhanced optical lithography is used to pattern copper interconnects in a step and scan system with a 248 nm excimer laser source. A mask with alternating phase shifted sub-resolution assist features is designed to enhance the resolution and process latitude of the lithography process. The spurious reflections associated with deep ultraviolet exposure of transparent film stacks and resist poisoning effects are systematically studied and solutions demonstrated. In addition, the effects of plasma processing on the structure, composition and electrical properties of an ultra low- κ dielectric and the microstructure of barrier layer deposited on it are investigated.

The second part investigates the high frequency electrical properties of a large set of test structures corresponding to local, intermediate and global interconnects by S-parameters measurements up to 40 GHz. The signal propagation mode is found to be slow wave at low frequencies and quasi transverse electromagnetic wave at high frequencies consistent with earlier theoretical predictions. A wide band equivalent circuit with frequency independent lumped elements is used for interconnect modeling by standard circuit simulators. The model predictions are experimentally validated in both the frequency and time domains. It is shown that the wide-band model accurately represents the dispersive behaviour of copper interconnects and can predict both propagation delay and signal rise time. Finally, a novel modeling methodology based on measured S-parameters is developed for coupled interconnects. Using this, the benefits of ultra low- κ dielectrics for crosstalk reduction are experimentally verified.

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Chapter 1

Introduction

1.1 INTERCONNECT SCALING TRENDS AND HIGH FREQUENCY OPERATION

Over the last four decades, the complexity and operating speed of integrated circuits (ICs) have increased many folds. The need for miniaturization of ICs arises from the significant cost and performance advantages. The increase in the number of transistors with scaling, coupled with large chip sizes enables the incorporation of more functionality in ICs, thus enhancing their performance. The speed of an IC is determined by the resistance-capacitance (RC) delay of the transistors in a circuit. Fig.1.1 shows the gate and interconnect RC delays as a function of the technology generation node [1]. Scaling reduces the intrinsic gate delay due to a reduction in the gate and channel lengths. The

Fig. 1.1 RC delay for different generation technology nodes

transistor gate delay reduces continuously with scaling of complimentary metal oxide semiconductor (CMOS) devices while the interconnect delay increases. With the use of low resistivity materials such as copper instead of aluminum and low dielectric constant (κ) materials, the interconnect delay can be reduced.

The increase in interconnect RC delay is mainly due to denser and longer interconnects at the global levels [1-2]. The interconnect density is increased by reduction of line-width and pitch. The reduction in line-width reduces interconnect cross-section area with corresponding increase in resistance. On the other hand, decreasing interconnect pitch adversely impacts interconnect parasitic capacitance. For each technology generation, assuming a constant aspect ratio and no change of conductor or dielectric materials, the feature size reduces by a factor of 0.7 and interconnect delay degrades by a factor of 2 [1]. Decreasing pitch also increases the capacitive coupling between neighbouring interconnects, thus increasing the probability of spurious signals or crosstalk.

The operating frequency of digital ICs is doubling every 1.5 year in accordance with Moore's law. The on-chip local clock frequency of micro processing unit (MPU) is expected to reach 23 GHz by the year 2013 for 32 nm (metal 1-half pitch) technology node. There is also a strong interest in using CMOS technology for radio frequency (RF) and microwave applications due to its lower power consumption and lower costs. Si and SiGe technologies are fast replacing III-V compound semiconductors for millimeter wave devices as shown in Fig. 1.2 [3]. At high frequencies, interconnect behaviour is governed by transmission line effects as the length of interconnects becomes a significant portion of wavelength. One of the major impediments in using CMOS technology for RF applications is the low-resistivity of silicon, which at high frequency causes significant losses.

Fig. 1.2 Evolution of mixed-signal technologies for mm-wave applications [3].

Furthermore interconnect signal integrity issues such as delay, crosstalk, reflections, distortions and ringing are exacerbated at high frequencies. It is also necessary for interconnect behaviour at high frequencies to be accurately modeled and simulated using circuit simulators in order to facilitate the reliable design of high frequency and high performance circuits. In the following, the relevant factors and issues associated with interconnect scaling and high frequency operations are discussed.

1.2 ISSUES WITH INTERCONNECT SCALING

1.2.1 Propagation Delay

An interconnect can be represented as a distributed RC network ignoring the inductance effects at low frequencies. The propagation delay (τ) of this interconnect can be approximately represented as:

$$\tau = RCL^2 \quad (1.1)$$

where R and C are per unit length (p.u.l.) line resistance and capacitance, respectively and L is the length of the interconnect. The line is represented by a single RC network with RL as its resistance and CL as the capacitance. Using a simple RC model, the propagation delay can be derived as:

$$\tau = \rho \varepsilon \frac{L^2}{t_m t_d} \quad (1.2)$$

where ρ and t_m are resistivity and thickness of the conductor, and ε and t_d are permittivity and thickness of the inter-level dielectric (ILD) material respectively. From this expression, it is clear that in the case of ideal scaling where line width, thickness and length are scaled by the same factor, there would not be any change in delay. However, interconnects do not follow ideal scaling at all levels of interconnect hierarchy.

Interconnects can be categorized into local and global interconnects. Local interconnects are typically used for communication within a functional block while global interconnects are for clock and signal distribution between the functional blocks of an IC. The interconnect delay scales differently for local and global interconnects [4]. The line-width, spacing and thicknesses of global and local wires, and ILD thickness scale by the same factor, irrespective of whether the interconnects are local or global as shown in Table 1.1. However, the length of global and local interconnects scale differently with technology scaling. If the technology scaling factor is S , local interconnects will scale down by the same scaling factor S , whereas global interconnect scale up by $1/\sqrt{S}$. This is due to the fact that the length of a global wire is set by the chip-side length as well as the size of functional units, and it does not directly shrink with gate dimensions. This amount

Table 1.1 Technology scaling scenarios for local and global interconnects [4]

	Ideal scaling (scaling factor, S)	
	Local wires	Global wires
Linewidth and spacing	S	S
Wire thickness	S	S
ILD thickness	S	S
Wire length	S	$1/\sqrt{S}$
Resistance (per unit length)	$1/S^2$	$1/S^2$
Capacitance (per unit length)	1	1
RC Delay	1	$1/S^3$
Current density	$1/S$	$1/S$

to ~20 % increase in length for each technology generation. Taking different scaling factors for length of interconnects into consideration; the RC delay is expected to remain constant for the local interconnect, while global RC delay will increase by a factor of $1/S^3$ as derived from equation (1.2). With a scaling factor of S of 0.7 from one technology generation to the next, this translates to 192% rise in RC delay with each technology generation.

Table 1.2 shows the impact of scaling on the transistor intrinsic gate delay and

Table 1.2 MOSFET switching and interconnect intrinsic delays with technology scaling [5]

Technology	MOSFET switching delay ($t_d = CV/I$)	Intrinsic delay of minimum scaled 1 mm long interconnect
1.0 μm (Al, SiO ₂)	~20 ps	~5 ps
0.1 μm (Al, SiO ₂)	~5 ps	~30 ps
35 nm (Cu, low- κ)	~2.5 ps	~250 ps

propagation delay of a minimum scaled interconnect [5]. The transistor intrinsic gate delay reduces from ~ 20 ps to ~ 2.5 ps as transistor gate length is scaled from $1\text{ }\mu\text{m}$ to 35 nm, On the other hand, the interconnect intrinsic propagation delay increases substantially from ~ 5 ps to ~ 250 ps.

It is worthwhile to mention here that the scaling factors given in Table 1.1 were predicted by assuming aluminum and silicon dioxide are used for the fabrication of interconnects. Thus, the change of materials to copper and low- κ dielectrics will alter the trend. The interconnect length is not scaling up as $1/\sqrt{S}$ as chip area is not increasing as expected. The resistance is assumed to increase with scaling as both line width and height scale down; however, the height is actually scaling down at a much slower rate. Therefore, these scaling factors may not be realistic in the long term as such.

1.2.2 Crosstalk

With the reduction in the pitch of interconnects, the lines are placed very close to each other resulting in strong capacitive coupling between neighboring wires. For coupled interconnects, voltage change in one wire (aggressor) can cause spurious change in the voltage of a neighbouring wire (victim). The crosstalk noise is a parasitic shift of the victim line voltage due to a concurrent transition of the aggressor signal. Capacitive and inductive coupling between the two interconnect lines can cause the signal in a node to deviate from its proper logic levels of V_{dd} or ground.

Crosstalk is interconnect scaling dependent. In [5], it is observed that for a 1 mm long coupled interconnects, scaling the line-width and spacing from $1\text{ }\mu\text{m}$ to 50 nm increases peak crosstalk voltage (V_n) to supply voltage (V_{dd}) ratio on the victim line by a factor of 500 (~ 0.0002 to 0.1) for a rise time of 1 ns. Furthermore, the maximum

interconnect coupling length at which crosstalk begins to exceed 10 % of V_{dd} decreases from ~3.3 mm to ~0.3 mm as technology scales from 0.25 μm to 0.05 μm . The inductance of interconnects becomes very significant at GHz frequencies for long and wide interconnects [6-8] and inductive coupling effects should be included for accurate crosstalk noise analysis [9]. Fig. 1.3 shows the peak noise voltage as a function of linewidth for coupled interconnects. As line-width increases to 2.4 μm , the peak noise voltage caused by inductive coupling, starts to exceed the capacitive coupling.

Fig. 1.3 Absolute peak noise voltage vs. linewidth for capacitive, inductive, and a combination of capacitive and inductive coupling [9]

1.2.3 Power dissipation

The total dissipated power in an IC can be expressed as [10]:

$$P_{total} = P_{dynamic} + P_{sc} + P_{static} + P_{passive} \quad (1.3)$$

where $P_{dynamic}$ is the dynamic power associated with logic gates as they switch states. During switching, power supplies must charge internal capacitance associated with the gate of a transistor. In addition, the gate must charge any external, or load capacitances that comprise parasitic wire capacitances and input capacitances associated with downstream logic-gate inputs. P_{sc} is the short circuit power dissipated during abrupt switching transients when both n-channel MOS (NMOS) and p-channel MOS (PMOS) devices are on. P_{static} is the power dissipated by sub-threshold and gate tunneling leakage of MOS transistors and $P_{passive}$ represents the power dissipated by passive elements in the circuit which is normally negligible.

The total power dissipation of interconnects, P_{int} is the sum of dynamic power dissipated as a result of the charging and discharging of its parasitic capacitances and the total power consumed by repeaters used in the circuit. It can be represented as:

$$P_{int} = S_w C_{int} V^2 f + P_{repeaters} \quad (1.4)$$

where S_w is the switching activity factor representing the probability of interconnects switching during a clock cycle, C_{int} is the total interconnect capacitance, V is the voltage to which an interconnect charges, f is the operating frequency and $P_{repeaters}$ is the total power consumed by the repeaters in the circuit.

Chandra et al. [11] estimated that total interconnect power dissipation at 180 nm node is about 46% of the total chip power consumed for signaling interconnects out of which 4% power is consumed by repeaters. With scaling, the interconnect power dissipation is expected to increase. However, its relative contribution to total power

dissipation in a chip will decrease as the power dissipation for logic and memory transistors is expected to increase with an increase in the total number of transistors by a greater proportion. Shin et al. [12] in their analysis of the 70 nm to 180 nm technology nodes showed that in case of optimally buffered interconnect systems 70%–80% of the total power is consumed by transistors while the remaining power is dissipated as heat in interconnects. According to the international technology roadmap for semiconductors (ITRS) [3], the maximum allowable average power for the MPUs is estimated to be 198 W. This is projected to remain constant for various technology nodes from 2008 to 2020, possibly with the use of innovative design and cooling methodologies.

1.2.4 Electromigration (EM)

EM refers to the phenomenon of mass transport in metals due to the momentum transfer between conducting electrons and diffusing atoms. It is characteristic of metals biased with a very high current density. When current flows through the interconnect metal, an electron wind force is set up in a direction opposite to that of the current flow. The electron wind, on colliding with the metal ions can impart sufficient momentum to displace and to enhance the diffusion of metal ions with neighbouring vacancies in the direction of wind force. These vacancies condense to form voids that result in the increase of interconnect resistance or open circuit conditions [13]. The interconnect reliability degradation is mainly due to the electromigration (EM) phenomenon [14].

Joule heating in global lines increases the resistance of conductors and is an additional contributor to the interconnect reliability [15]. Non-uniform temperature distributions along global wires in high-performance ICs have significant implications for interconnect performance [16]. The maximum current density (J_{max}) at 105°C for

intermediate level interconnects is expected to rise from 2.08 MA/cm^2 for the 65 nm technology node in the year 2007 to 8.08 MA/cm^2 for the 32 nm technology node in 2013 [3]. The introduction of low- κ dielectrics with lower thermal conductivity adversely affects the EM reliability. With the use of low- κ dielectrics, temperature of metal lines increases further and makes them more susceptible to high current failures [17].

The resistivity of copper interconnects is increased as the interconnect feature size approaches the mean free path of electrons in copper due to the scattering of electrons at the metal surfaces. Also the barrier metal, engulfing an interconnect, does not scale in the same proportion as the feature size of interconnects. Since the resistivity of the barrier metal is large as compared to copper, current conduction mainly takes place through copper metal lines. This results in the reduction of the effective area of cross-section of metal lines for a specific technology node. Designers are typically given a maximum allowable root mean square (rms) current density value for assuring a specific EM lifetime of the conductors. This value is derived from the reliability studies of the interconnect. This maximum allowable rms current density is reported to reduce with the increase in resistance [17].

1.3 SOLUTIONS FOR INTERCONNECTS PERFORMANCE ENHANCEMENT

1.3.1 Circuit Design Solution Using Repeaters

The Elmore delay is the most widely used model for delay approximation for RC lines [18]. For RC interconnects, the delay is proportional to the square of line-length (equation 1.2). Repeaters are CMOS inverters/buffers that convert this quadratic dependency on length into a linear one. An interconnect is divided into a number of

segments and a repeater is inserted after each segment to improve the delay and signal transition times.

Fig. 1.4 shows a k -segmented interconnect of length L with p.u.l. resistance R and p.u.l. capacitance C . Therefore, the total resistance and capacitance of the line are $R_t = RL$ and $C_t = CL$, respectively. If the numbers of segments are very large, capacitance is scaled by a factor of 0.5 to approximate a fully distributed scenario, where the distributed resistance only sees the downstream capacitance. The delay τ of such a line can be expressed as:

$$\tau = \frac{RC}{2} L^2 \quad (1.5)$$

Fig. 1.4 Division of an RC interconnect into k -segments and insertion of repeaters

The interconnect can be sub-divided into k segments with a length of each section as

$l_{segment}$ where:

$$L = l_{segment} \cdot k \quad (1.6)$$

If k repeaters with zero delay are inserted in the line, the total delay with repeaters $\tau_{repeater}$ is given as:

$$\tau_{repeater} = \frac{RC}{2} (l_{segment})^2 \cdot k \quad (1.7)$$

Combining equations 1.5 and 1.6,

$$\tau_{repeater} = \frac{RC}{2} l_{segment} \cdot L \quad (1.8)$$

Thus, delay can be made proportional to the line length as shown in the equation 1.8 with insertion of repeaters. Several strategies for optimizing the number of repeaters and size of repeaters in relation to wire size have been proposed in literature [19-28].

At high frequencies, inductive effect becomes significant. Therefore, a RC representation of interconnects cannot describe the propagation behaviour accurately. So a RLC representation is necessary. This inductive behaviour of interconnects is beneficial as far as ‘delay’ is concerned. Delay is estimated to reduce with inductance, and therefore the optimum number of repeaters inserted to minimize the total interconnect delay can be reduced [29-30].

Although repeaters offer a viable solution to reduce interconnect delay, additional power is consumed by repeaters in the process of delay minimization [31-33] and reduction of effective silicon area for logic blocks [34]. It is estimated that about 2.5 to 10 million repeaters are needed for 50 nm technology node and they can consume close to 60 W of power [35]. The contribution of global interconnects is estimated to be about 10% of total power dissipation in a chip and repeaters can contribute as much as 50% [35, 36]. Repeaters take up a significant portion of silicon and reduce the effective chip area for circuit layout due to via blockage [37]. In reference [34], it is estimated that for the 45 nm and 35 nm technology nodes, repeater count as a percentage of total cells in an IC can be as high as ~35% and ~70% respectively.

1.3.2 Reverse Scaling of Interconnects

Reverse scaling [38, 39] refers to the concept where metallization layers do not scale down with technology scaling. In reverse scaling scheme, interconnects are short and densely packed at the local level, and long and wide at the global level. Thus, at the global layer of metallization, wire cross-section areas and pitch are increased or reverse scaled to minimize the RC delay. Fig. 1.5 shows a cross-section scanning electron micrograph (SEM) of an Intel 65 nm chip with reverse scaling implemented at metal-6 to metal-8 global levels [40]. In comparison with alternatives such as new materials and processes, the compelling advantages of reverse scaling are: minimal time to implementation and low cost of implementation [38]. The problems with reverse scaling are: increase in the number of metallization layers, larger chip size and higher manufacturing costs associated with increased layers of metallization and chip size. For the near term, reverse scaling provides a practical solution to mitigate global interconnect latency, however alternative solutions will still be needed for the advanced technology nodes extending to and beyond 35 nm.

The key to optimal reverse scaling is the capability to predict the complete stochastic interconnect density distribution for a projected next-generation product [38].

Fig. 1.5 Copper interconnects with low- κ dielectrics for Intel 65 nm chip [40]

For a logic circuit, the Rent's rule [22] relates the total number of input and output (I/O) signal terminals (T) to the number of logic gates (N) in a random logic network through an empirical formula $T = kN^p$ where k is a constant related to the type of devices and p is an empirical constant between 0.5 and 1. Based on the Rent's rule, Meindl et al. [38] derived the interconnect length distribution as well as the average interconnect length for logic circuits. Knowing this, an optimal architecture for a multilevel interconnect network that minimizes macrocell area, power dissipation, clock cycle time, or number of wiring levels can be derived.

1.3.3 Process Solution Using Copper and Low- κ Dielectrics

Historically, aluminum has been the preferred material for interconnect metallization with silicon dioxide as a dielectric material. The resistivity of aluminum is $2.65 \mu\Omega\text{-cm}$ compared to $1.67 \mu\Omega\text{-cm}$ for copper at 25°C . Even though resistivity of aluminum is higher than copper, it has been a material of choice due to its ease of deposition and patterning. The main issue with the introduction of copper had been the difficulty of dry etching of copper within the permissible thermal budget of IC processing. With the introduction of dual damascene technology, copper patterning became feasible without the need for the etching process and this has enabled copper metallization to become mainstream for high performance integrated circuits below 130 nm technology node [41, 42]. One other problem with copper is that the copper ions are highly mobile in SiO_2 and it can diffuse through the silicon. Thus, in absence of any barrier layer, copper ions can reach the active layer and cause the failure of the device. Therefore, integration of suitable barrier materials is necessary to stop this copper diffusion through a dielectric.

There are many schemes for dual damascene interconnect patterning. Some of the commonly used schemes are: via first, trench first and self aligned. Via first scheme is the most promising due to its reduced process complexity and capability of scaling down to the next generation of devices. In the via first scheme as shown in Fig. 1.6, via is masked through two layers of dielectrics by deep UV lithography. Via masking is usually done using a bottom antireflective layer (BARC) to suppress thin film interference effects. The dielectrics can be same or different at via and trench level. The dielectrics are typically separated by an etch stop layer. During trench masking, the trench mask is aligned with via and a trench is formed by reactive ion etching. During etching, via is filled by an organic BARC film to prevent the etching of the copper capping dielectric film at the bottom of via. The etching process terminates after the desired trench depth has been

Fig. 1.6 Via first dual damascene scheme for copper interconnects: (a) after via masking (b) after via etch and resist strip (c) after trench masking and (d) after trench etch, and resist strip (e) after barrier/seed layer deposition and copper electroplating and (f) after chemical mechanical planarization

etched. The copper cap dielectric is etched next, followed by cleaning in a solvent to remove any polymer or copper residues on the sidewalls of patterned structure. Thereafter, copper diffusion barrier layers such as Ta or TaN are deposited, followed by a copper seed layer and electroplating of copper. Electroplated copper surface is then planarized by chemical mechanical planarization (CMP) process to form the final conductor. The whole sequence of steps is repeated for next level of metallization.

At present, copper interconnects are used together with low- κ dielectric materials to reduce the interconnect RC delay. Many dielectrics are available for low- κ applications such as fluorine or carbon doped oxides, hydrogen silsesquioxane, organic polymers, nanoporous silica, porous polymers, poly tetrafluoroethylene, amorphous carbon [43, 44]. However, the use of copper and low- κ materials has also brought in many new issues, which need to be addressed for the successful integration of these materials into manufacturing [44]. The first significant criterion for selection of a low- κ dielectric is its dielectric constant. However, the dielectric should also be able to withstand the temperature experienced during the processing as well as under normal operating conditions of the fabricated device. It should not deform during processing. Thus, low- κ materials must also have good thermal and mechanical properties. These properties are dependent on the chemical structure of the material. Materials with strong individual bonds and high density of bonds have better thermal and mechanical properties. The problem is that strong bonds are often more polarizable and that increases the dielectric constant of the material. Organic polymeric materials have lower bond density as well as lower individual polarizability. However they have poor thermal stability. They can decompose at typical back-end of line processing temperatures (≥ 400 °C) as their C-C bonds are much

weaker than Si-O bonds. Due to weaker bond strength, organic materials are mechanically inferior to oxides. There are no suitable dense polymers available with κ less than 2.5 [45]. Therefore, porosity needs to be introduced in the materials structure. However, porosity creates voids in the material structure and this will compromise the thermo-mechanical stability of porous materials. The dual damascene process used for fabrication of interconnects involves a large number of critical processes such as lithography, etching, metallization and planarization. Lithography, etching, photoresist stripping and wet cleaning processes have greater potential of damaging a porous material due to the diffusion of the reactive species into the pores. Porous dielectrics are also very prone to damage from stress inducing processes such as CMP and thermal processes as they have relatively weak mechanical strength compared to dense dielectrics.

In ITRS 2005 [3], ultra low- κ (ULK) dielectrics with dielectric constant less than 2.4 were expected to be introduced by year 2007. However, in the 2006 ITRS update, this has been postponed to 2009. The difficulties in processing porous dielectrics and the accompanied reliability issues have delayed the introduction of ULK dielectrics materials by at least one technology generation. ITRS 2005 also lists the most difficult challenges for interconnects process technologies for near term (2005-2011) and long term (2012-2020). Some of the most difficult challenges listed for interconnects are: integration of porous dielectrics, size effects leading to increase in resistivity due to scattering, reduced feature sizes and pattern dependent processes, and high aspect ratio nano structure patterning.

Another approach towards lowering of κ is the integration of copper with air-gaps ($\kappa = 1$) created using sacrificial films [46-47]. However, incorporation of air gaps and maintaining the mechanical and electrical integrity of the structure is extremely

challenging [46] and a lot of effort is needed before this approach can be seriously looked into as a potential interconnect solution.

1.3.4 Three Dimensional (3-D) Interconnects

In spite of the rapid progress in copper interconnect technology, increased interconnect delay and power consumption for 2D planar ICs have posed severe limitation on their performance [49]. If IC dies can be stacked in the third dimension, there could be considerable saving in chip area, power consumption and the propagation delays can be reduced due to shorter wire lengths [50]. It has been reported that the aggregate wire length can be reduced by 30%-50% through 3-D wafer scale integration and this corresponds to a reduction in interconnect power consumption by 21% -39% for stacking of two to five wafers [51, 52]. In another study, a 2-layer 3-D integration achieves nearly 40% area reduction with 18% interconnect delay reduction as compared to a standard 2-D structure, while 4-layer integration achieves 70% area reduction and 40% interconnect delay reduction [53]. 3-D stacking can be realized at various levels. In a 3-D system in package (SIP), the stacking is done by interconnecting stacked chips through the I/O pads. A higher level of 3-D connectivity can be achieved by stacking the functional blocks on each other and connected with interconnects within a chip without the need of going through I/O pads. This scheme is termed 3-D system on-a-chip (SOC). The ultimate integration is at transistor level where transistors can be stacked vertically with 3-D interconnects at the local level. The ICs stacked vertically at transistor level are known as 3-D ICs.

Several technologies have been proposed for 3-D integration [54-59]. The challenges for 3-D integration are in the integration and maintaining of mechanical and electrical integrity of 3-D stack. Industry is still working on several potential solutions to

solve these issues. Fig. 1.7 shows some examples of 3-D interconnect integration schemes being investigated. 3-D technologies also enable heterogeneous integration of ICs fabricated in different technologies such as analog, digital, logic, memory etc. where each technology is optimized for best performance. This can facilitate integration of non-silicon substrates such as III-V compounds with Si for applications such as photonics.

Fig. 1.7 Three Dimensional (3-D) Interconnects Integration schemes

1.4 MODELING AND ELECTRICAL CHARACTERIZATION OF INTERCONNECTS

In the early 80's, gate parasitic were much larger than the interconnect parasitics, primarily because gate dimensions at that time were greater than $1\ \mu\text{m}$. Interconnect parasitics were thus largely ignored, and interconnects were modeled as short circuits. As transistor gate dimensions were scaled downwards, interconnect capacitance became larger than gate capacitance. Therefore, it became necessary to model the interconnect as a single

lumped capacitance element. With continued transistor scaling, interconnect dimensions also shrank and the resistance of interconnects increased to a point where it was no longer possible to ignore it. Therefore, interconnect models made a transition from a lumped capacitance model to a RC model.

In the past, circuit frequencies were such that parasitic inductance was negligible in comparison to resistance and capacitance of interconnects. Today, IC frequencies have reached the multi-gigahertz range and the length of interconnects has increased. Global interconnects that are used as high frequency data buses, and for carrying control and clock signals, have lower resistance due to larger cross-section dimensions and replacement of aluminum interconnects by low resistivity copper. Therefore, the line resistance for global interconnects has further decreased and inductive effects have become more prominent. These inductance effects can manifest as a distortion of signal waveforms with overshoots and undershoots adversely affecting signal integrity [60, 61]. Therefore inductance of interconnects is very critical to IC performance [62-68] at high frequencies and RLC representation of interconnects has become necessary to accurately model the behaviour of interconnects.

It is now a standard practice in VLSI circuit design to extract full-chip interconnect resistance and capacitance after completing the physical design and before performing the timing analysis as shown in Fig. 1.8 [69-70]. Of significant concern to analog/custom IC design flows is the sensitivity to inductance, which increases with frequency, especially in high-frequency RF designs [70]. Comprehensive silicon modeling is done to handle inductive effects for RF circuits. Since the interconnect design affects every stage of the

design flow, fast and accurate full-chip level parasitic extraction and delay estimations are becoming increasingly important.

Fig. 1.8 Interconnect parasitic extraction in a VLSI design flow

As shown in Fig. 1.2, silicon technology is fast becoming the preferred choice for RF communication with signal frequencies in GHz range. At high frequencies, an interconnect can be represented as a transmission line, as its length becomes a significant proportion ($> 10\%$) of the wavelength of the signal propagating through it [71, 72]. At 30 GHz, the free space wavelength of light is equal to 10 mm and it is about 5 mm in a SiO_2 dielectric medium ($\epsilon_r \sim 4$). Therefore, any interconnect with line-length greater than 0.5 mm can be regarded as a transmission line for analog signals. If the signal is sinusoid, it is generally agreed that signal does not change much over an interval equal to one twentieth of its period. For example, consider a sinusoidally varying signal $x(t) = A \sin(2\pi t/T)$ where t is the time, A is its amplitude and T is the period of the signal. The maximum

change in signal amplitude occurs when the signal goes from a time $t = \alpha T/2$ to $t = -\alpha T/2$ where α is the fraction of period. So in one-twentieth of period ($\alpha = 0.05$) signal, the signal can change by 16% of its maximum possible change in value ($x(t) = \pm A \sin(0.05\pi) = \pm 0.16 A$) [71]. Therefore, it is considered as safe to use a lumped circuit model to represent an interconnect, when its line length is less than one-twentieth of the wavelength of the signal. When the interconnect length is between 5% and 10 % of the wavelength of signal, there is a grey area. In this range, the decision whether an interconnect is to be represented as a transmission line or a lumped element circuit can be taken based on the accuracy needed for a particular application.

For digital circuits, the rise time of a pulse waveform is used to determine if the interconnect needs to be represented as a transmission line. The highest operating frequency can be determined from the rise/fall time of the signal. The relationship between the maximum operating frequency f_{max} and rise/fall time t_r can be expressed as $f_{max} \approx 0.35/t_r$. The rise and fall times for digital circuits are currently approaching a few tens of pico-seconds. This implies that f_{max} would be in the GHz range. For example, f_{max} is equal to about 7 GHz for a 50 ps rise/fall time. The corresponding wavelength for this signal will be 21.4 mm in a dielectric medium. Thus, for an interconnect which is longer than 2.14 mm, transmission line effects will be significant. Interconnects at the intermediate level are typically a few mm long, while interconnects at global levels can be as up to 30 mm long [38]. Hence, for current and future IC generations, interconnects must be modeled as transmission lines.

Transmission lines have been studied extensively in literature. However in the context of interconnects, the lossy nature of silicon makes it very difficult to accurately predict the electrical behaviour of a transmission line due to substrate loss and signal dispersion. Therefore, accurate understanding of loss mechanism and modeling of transmission lines on lossy silicon substrate is required. In 1971, Hasegawa published a seminal paper identifying three fundamental wave propagation modes on silicon viz. quasi-TEM mode, the slow-wave mode, and the skin-effect for a microstrip line based on silicon substrate resistivity and frequency [73]. Since then, there have been tremendous advances in interconnect models used for IC design and modeling. Full wave [74-75] or quasi-static electromagnetic [76-77] approaches have been used for characterization of transmission line parameters. However these techniques require extensive computational resources and are not practically viable for computer aided design of high density ICs. Closed form expressions have also been proposed for the characterization of single and coupled transmission lines which enables faster designs and design scalability of ICs [78-83]. However the accuracy of closed form expressions does not always match the real chip environment. It is therefore, necessary that these models are validated by experimentation to ensure successful chip designs.

1.5 MOTIVATION AND RESEARCH OBJECTIVES

1.5.1 Motivation

Copper metallization and low- κ dielectrics were brought in for substantial performance improvements specifically in interconnect RC delay at the beginning of this decade. To successfully integrate low- κ dielectrics in IC processing, a tremendous effort has been made by the research community to develop low- κ /ULK material with suitable

mechanical, chemical, thermal and electrical properties. Integration of these materials to form reliable interconnects has turned out to be very difficult. A measure of this effort is evident in the dominance of research papers covering material synthesis, characterization, and process integration aspects of interconnects.

In the last few years, a lot of theoretical modeling and simulation work has been undertaken to predict and improve the performance of interconnects. However, there are few experimental reports on electrical characterization of interconnects particularly at high frequencies, and with submicron features. Yu et al. [84] proposed a loop based inductance extraction methodology and validated the results using coupled lines with linewidth of 1 μm and spacing of 2 μm up to a frequency of 50 GHz. Yang et al. [85] and Sia et al. [86] studied the propagation characteristics of microstrip lines and coplanar waveguides. Ktata et al. [87] studied effect of substrate conductivity and influence of ground line position on lines electrical properties. Taek et al. [88] proposed a compact distributed circuit model and validated it by S-parameters measurement of microstrip lines of width 0.6 μm and 0.7 μm up to 20 GHz. Ong et al. [89] did experimental investigations of interconnects down to 1.5 μm using S-parameters measurements. Janezic et al. [90] developed a methodology for extraction of frequency dependent dielectric constant of low- κ materials till 40 GHz for line-width down to 0.36 μm . However no crosstalk or time domain analysis was done. Cregut et al. [91] studied the low- κ influence on crosstalk and Bermond et al. [92-93] studied the effect of oxide and ULK dielectrics and air gap on coupled lines performance.

In 2000, Kapur et al. [94] studied the technology and reliability constraints of copper interconnects and found that p. u. l. resistance values for 35 nm technology node are 90%, 145% and 192% greater than that obtained using ideal copper resistivity for

global, semiglobal and local wires, respectively. They also predicted that at some point copper effective resistivity will become higher than that of aluminum. This raises concerns as to how long the performance improvements that are being seen with copper interconnects will continue.

As the fabrication and characterization of test structures for copper and low- κ technology is very demanding due to severe integration difficulties, there is a paucity of experimental data for submicron test structures. Therefore, there is a need for experimental characterization of the different categories of copper interconnects (local, intermediate and global) at high frequencies to critically evaluate their performance with low- κ and ULK dielectrics.

In the area of interconnect modeling, there is also a lack of compact and scalable models suitable for circuit design. Therefore, there is a need for developing suitable lumped circuit model for extraction of circuit parameters that can be validated by experimentation. The extracted parameters can then be used for the simulation and the design of a circuit.

1.5.2 Research Objectives

The main objective of this work is to identify, study and resolve the critical process integration issues that come into play with feature size scaling of interconnects and develop suitable interconnect models for characterization of single and coupled interconnects at high frequencies. The specific objectives are:

- (a) To form an aerial image that can be used to pattern trench structures down to 100 nm for fabrication of nanoscale copper/low- κ interconnects by extending the resolution of a 248 nm deep ultra violet (DUV) lithography system by design of a

suitable resolution enhancement scheme and to mitigate the effect of reflections and DUV resist contamination during processing of damascene structures.

- (b) To study the impact of plasmas chemistries on the surface and bulk properties of the ultra low- κ material when subjected to etching and stripping plasmas during processing and to investigate the effectiveness of an ultra-thin dielectric film deposited as pore sealing and diffusion barrier layer on the electrical properties of the ultra low- κ materials. To study the morphology and electrical properties of a Ta barrier metal layer deposited on an ultra low- κ material.
- (c) To study the propagation characteristics of a single line interconnect down to 100 nm fabricated using copper/oxide and copper/ULK test structures.
- (d) To develop a compact wide band lumped circuit model as an accurate representation of the interconnect propagation behaviour.
- (e) To develop a compact lumped element coupled line model of the interconnect for predicting crosstalk and to study the impact of ULK on crosstalk. Experimental validation of both single line and coupled line interconnect models by frequency and time domain measurements.

1.6 MAJOR CONTRIBUTIONS OF THE THESIS

1.6.1 Alternating Phase Shifted Sub-Resolution Assist Features for Resolution Enhancement

We designed a novel phase shift mask with alternating phase shifted sub-resolution assist features, to enhance the resolution of a 248 nm DUV exposure system with NA of 0.68. Through simulation, we found that three sets of 40 nm alternating phase shifted scattering bars with separation of 120 nm are most optimum for forming an aerial image in

terms of higher peak intensity, lower side lobe intensity and smaller full width of half maxima (FWHM). Simulation results are verified experimentally and we patterned isolated trenches with critical dimension (CD) target of $120\text{ nm} \pm 10\%$. The patterned CD target of 120 nm corresponds to a k_1 factor of 0.33 for an exposing wavelength of 248 nm , a sigma of 0.31 and an NA of 0.68. The results of resolution and process latitude enhancement with such a mask are reported for the first time in the literature [95]. The design was extended to the patterning of 100 nm copper interconnect test structures.

1.6.2 Dual Dielectric Bottom Antireflective Coating (DARC) for Damascene Processing

A novel two layers DARC scheme for dual damascene copper and low- κ process was developed to reduce thin film interference effects. Comprehensive lithography simulations were used to design a dual layer dielectric antireflective scheme and the performance was verified through experiments. The dual DARC performed considerably better in controlling the substrate reflectivity with variations in underlying optically transparent films thicknesses as compared to organic bottom antireflective coating (BARC) or single layer DARC. The effectiveness of the dual DARC scheme was demonstrated experimentally on a SiC/SiOC/SiC film stack typically used in a VFDD process integration scheme.

1.6.3 Mechanism of DUV Resist Contamination

Process methodologies have been developed for minimizing resist poisoning effect in dual damascene patterning after systematic investigation of DUV resist patterning process. A process integration solution involving additional baking and time link between

processes is proposed for eliminating base contamination caused by post via etching solvent cleaning process.

1.6.4 Process Interaction and Electrical Properties of ULK dielectrics

We investigated the modification in structure, composition, and electrical properties of a porous methyl-silsesquioxane (P-MSQ) ULK dielectric film ($\kappa = 2.2$) when exposed to different gas plasmas viz. O_2 , H_2/N_2 , C_4F_8 , and H_2/He . Both leakage current density and breakdown voltages deteriorated after the plasma treatment. The worst case was that of a combination of fluorocarbon etching and H_2/He stripping plasmas. The leakage current was partially reduced by adding an ultra-thin (10 nm) dielectric capping layer to the plasma-treated film. The Ta barrier film microstructure deposited on the plasma-treated P-MSQ correlated with the surface roughness of the film. The Ta film deposited on fluorocarbon plasma-treated samples had the largest surface roughness and relatively less crystalline microstructure compared to that deposited on nonfluorocarbon-based, plasma-treated samples.

1.6.5 Interconnect Behaviour at Microwave Frequencies and Wide Band Model

The interconnect electrical characteristics were measured at microwave frequencies by line parameters from S-parameter data using a large sample set with a comprehensive range of feature sizes and dielectric materials. The relationship between feature size, frequency and inductance has been established to determine when inductance effects become prominent enough to be included in interconnects modeling. A fully lumped element model is developed for the wideband on-chip interconnects, and its scalability is verified for line-lengths up to 8000 μm , and line-widths down to 100 nm. We show that both the series and shunt lumped elements of model can be determined based on the

frequency asymptotic technique without any optimization. The equivalent lumped circuit is derived and verified to efficiently recover the frequency-dependent parameters up to 40 GHz. The lumped element model can be directly used in the SPICE-compatible simulation for the wide-band frequency applications in the design of RF integrated circuits.

1.6.6 Measurement Based Modeling for Single and Coupled Interconnects and Experimental Validation

A modeling methodology is proposed for coupled interconnects based on measured S-parameters. In the proposed coupled line model, single line model parameters extracted from a wide-band model can be extended for modeling of the coupled lines, and only a couple of model parameters need to be changed due to the proximity effect. The time-domain crosstalk is measured for Cu/oxide and Cu/Ultra low- κ interconnects and analyzed using the proposed model. A good agreement is found between the simulated and measured results in both the frequency and the time domains for different lengths, widths and spacing (for coupled-lines) confirming the accuracy of the modeling methodology. The compact modeling approach presented here facilitates accurate characterization and modeling of coupled interconnects based on measured data. To the best of our knowledge, this is the first attempt in modeling the coupled lines in both frequency and time domain with the same set of model parameters.

We show that the proposed wide-band model accurately represent the dispersive behaviour of interconnects and can be used for prediction of delay and rise time. The delay shows a linear dependence with the length for lines wider than 1 μm . The wide ($>1 \mu\text{m}$) and long lines ($> 500 \mu\text{m}$) lines can be modeled as RC interconnects, if the rise/fall times are large ($>50 \text{ ps}$). The simulated and measurement waveforms shows a good match for a

pulse input validating the accuracy of wide-band model for estimating the interconnect delay and rise time.

1.6.7 Experimental Verification of Crosstalk Reduction with ULK Dielectrics

Using a coupled line model, we verified the advantages of ULK dielectrics for crosstalk reduction. A decrease in coupling capacitance in the range of ~25-36% is observed for the coupled lines with ULK dielectric. The simulated reduction in the coupling capacitance value from USG to ULK is found to be ~22-47%. The difference between the experimental and simulated results may be due to dimensional tolerances of the fabricated structures as well as due to a possible degradation of ULK dielectric constant during wafer processing.

1.7 ORGANIZATION OF THE THESIS

This thesis consists of nine chapters. Chapter 1 explains the background and motivation as well as objectives and major contribution of this thesis. Chapter 2 describes a novel phase shift lithographic methodology developed for patterning of nano-scale interconnects using a 248 nm DUV exposure system. Chapter 3 comprises the simulation and experimental results of the development of antireflective coating schemes. Chapter 4 describes the problems and solutions for minimizing resist poisoning in DUV patterning of dual damascene interconnects. Chapter 5 focuses on the effects of process interactions on the structure, composition and electrical properties of ultra low- κ dielectrics. Frequency independent lumped element circuit models are proposed for simulating the electrical behaviour of Cu/oxide and Cu/ULK interconnects at microwave frequencies in chapter 6. In chapter 7, the rise time and signal delay of copper interconnects are measured and evaluated using the interconnect models developed. An enhanced model for crosstalk

evaluation of coupled interconnects is developed and validated by time domain characterization in chapter 8. Chapter 9 gives overall conclusions of this thesis as well as proposed future work.

Chapter 2

Resolution Enhanced Optical Lithography by Alternating Phase Shifted Assist Features

2.1 INTRODUCTION

Nanoscale copper interconnect test structures are required for our study of their electrical properties and signal propagation behaviour at high frequencies. It is, therefore, necessary to have the lithographic patterning capability for the fabrication of nanoscale test structures down to 100 nm in width. The resolution of an optical lithography system follows Rayleigh's equation, which is given by $R = k_1 \cdot \lambda / NA$, where k_1 is a process dependent factor, λ is wavelength of the light and NA is numerical aperture of the objective lens. Typically advanced optical lithography operates at a k_1 factor in the range of 0.37 to 0.42 under optimized conditions [96]. This translates into a half pitch resolution of 135-153 nm using a 248 nm DUV lithography system with an NA of 0.68. However, this is not sufficient for patterning features close to 100 nm for forming nanoscale copper interconnects. Therefore, a study was carried out to develop appropriate resolution enhancement techniques to lower the value of k_1 for a 248 nm DUV exposure system.

The interconnect test structures that were used in our study were either isolated or semi-isolated. Patterning of dense, and isolated or semi-isolated features requires different lithography approaches. Lithographic patterning of dense lines with a pitch of 160 nm has been demonstrated with off-axis illumination in a 193 nm exposure tool with a k_1 value of 0.31 and a further enhancement of line/space resolution was reported by using a double

exposure technique [97]. Typically, in conventional aluminum/oxide IC integration scheme, poly gate and metal-1 patterning are the most critical and challenging layers for lithographers as these require patterning of the smallest feature sizes at the tightest pitch in the whole mask set. Therefore, most of the resolution enhancement efforts have been spent in improving resolution and CD control for these two layers [98-100]. The invention of damascene technology has changed the polarity of metal patterning from clear to dark field with a trench replacing the line. Due to changes in mask polarity, trench patterning methodologies are different from those for a line and this poses new lithography challenges [101]. Trench patterning is accomplished using a dark field mask, where trench features allow transmission of light and the rest of the field area is opaque. For polysilicon or aluminum metal lines patterning, clear-field masks are used. For a clear-field mask, a very fine isolated feature can be printed with mask-less lithography using a phase edge change. However this would not be possible in a dark field mask as the field area is opaque [102]. Therefore, patterning techniques developed for clear-field mask cannot be implemented for the patterning of isolated or semi-isolated lines.

Patterning of very fine trench structures is typically accomplished using shrinkage techniques such as dielectric gap fill [103], spacer [104-106] and e-beam lithography [107]. In the gap fill scheme, a trench is first etched and then a dielectric liner is deposited over the trench to reduce its size. In the spacer scheme, a hard mask is patterned first and then a metallic spacer is deposited. This is followed by anisotropic etching of bottom of the spacer. The metal on the side walls reduces the CD of hard mask and this is then used for patterning of trenches. For both of the above schemes, it is very difficult to have a conformal deposition of dielectrics or metals over the trenches or hard masks to reduce the

feature sizes. Adapting these techniques for mass production is difficult due to increased process complexity and cost resulting from an increased number of process steps. With e-beam lithography, it is possible to make feature sizes even below 30 nm. However, e-beam lithography has the classical problem of low throughput, and thus it has very limited potential for use as a mass production patterning tool.

In this chapter, we present the design of a novel phase-shift-mask (PSM) with alternating phase shifted assist features to improve the lithographic resolution of isolated/semi-isolated trenches patterned during copper metallization using damascene processing. This technique enhances the resolution of a DUV exposure system. Assist features are sub-resolution features on the mask that reduce the critical dimension (CD) bias, which is a difference between the CDs of isolated/semi-isolated and dense features, by creating an electric field at the image plane resembling a dense pattern environment. Assist features are incorporated in the mask and they surround the primary isolated or semi-isolated features that need to be printed. As dimensions of assist features are below the resolution capability of the lithography system, only primary patterns are printed.

The use of assist features in the semiconductor industry has been limited to line patterning as this has been the most challenging due to patterning of polysilicon gates [108]. Lin patented a method of forming widely spaced line/space patterns and isolated lines using attenuated phase shifted assist features [109]. Chen et al. described a method to improve the depth of focus (DOF) range using sub-resolution assist features for line patterning and optical proximity correction for semi isolated and isolated line patterns [110]. Assist features that are typically used by lithographers are binary in nature. In case of binary assist features, the phase of light transmitting through the primary and assist

features is the same. Phase shifted assist features, where primary and assist features are 180° out of phase are described in the literature [111]. We have studied the lithographic performance of multiple pairs of alternating phase shifted assist features where assist features are not only 180° phase shifted with respect to primary feature, they are also phase shifted with respect to each other. The three types of assist features are shown in Fig. 2.1 for three pairs of assist features.

There are no reports on the patterning results of a phase shift mask with alternating phase shifted assist features in the literature. We report the lithography performance of phase shift mask with alternating phase shifted assist features and demonstrate that this provide a better resolution and process latitude as compared to binary or phase shifted assist features.

Fig. 2.1 Cross section of a mask with primary and sub-resolution assist features of the type (a) binary, (b) phase shifted and (c) alternating phase shifted

2.2 THEORY OF ALTERNATING PHASE SHIFTED ASSIST FEATURES

A one dimensional analytical description of how assist features to improve the lithographic performance has been given by Petersen [111] based on Fourier optics [112]. Fig. 2.2 shows a cross-sectional view of an isolated space on a photo-mask. At the mask plane, the electric field $m(x)$ is given by a rectangular function, $\text{rect}(x)$. The diffraction pattern of the E-field emerging from the mask is given by the Fourier transform of the mask function. Fourier transform expresses the diffraction pattern as the sum of its weighted sinusoidal frequency components. Thus at the pupil plane of the lens, the electric field can be represented as Fourier transform of electric field at the mask plane and is defined as $M(\nu) = F(m(x))$. In a lithography system, the objective lens would perform the inverse Fourier transform of diffraction pattern entering into it, and form an image of the mask pattern at the focal plane by collection of diffracted frequency components.

The Fourier transform of a single isolated space shown in Fig. 2.2, with a mask function $m(x)$ is equal to $\text{sinc}(\nu)$ where $\text{sinc}(\nu) = \sin(\nu)/\nu$, where ν is the normalized

Fig. 2.2 Electric field at mask and image plane for an isolated space pattern

frequency.

The Fourier transform $M(\nu)$ of mask function $m(x)$ can be expressed as,

$$M(\nu) = F(m(x)) = \int_{-\infty}^{\infty} m(x) \cdot e^{-i2\pi x \cdot \nu} \cdot dx \quad (2.1)$$

Electric field or intensity plot at the mask and pupil plane are conventionally plotted as a function of normalized frequency ν , where the spatial frequency of the periodic mask pattern is normalized by the highest frequency that is possible by coherent imaging. For the imaging of periodic patterns, the minimum resolvable pitch for coherent imaging is given by the expression λ/NA . Therefore, the highest frequency possible by coherent imaging would be an inverse of λ/NA . Normalized frequency ν is plotted in the range $-n \cdot NA/\lambda$ to $+n \cdot NA/\lambda$ where typical values of n ranges from 1 to 10.

Fig. 2.3 shows a primary feature of width W_p surrounded symmetrically on both sides by sub-resolution features of width W_A . The center to center distance between the primary and the assist feature is equal to Δx . The total electric field at the pupil plane can be found by superposition of the contributions of both the primary and assist features. If

Fig. 2.3 Cross-section of mask with an isolated space and sub-resolution assist features

the transmission of electric field at the primary and assist features is T_p and T_A respectively, then the Fourier transform $F(m(x))_{bin}$ at the pupil plane for binary assist can be expressed as

$$F(m(x))_{bin} = T_p W_p \text{sinc}(\pi \nu W_p) + T_A W_A \text{sinc}(2\pi \nu W_A) \left(e^{+2i\pi \nu \Delta x} + e^{-2i\pi \nu \Delta x} \right) \quad (2.2)$$

The first part of the equation 2.2 denotes the contribution due to primary feature at $x = 0$ and the second part denotes the contribution at a distance $\pm \Delta x$ due to assist features on either side of the primary feature.

Using Euler's equation, the expression (2.2) becomes,

$$F(m(x))_{bin} = T_p W_p \text{sinc}(\pi \nu W_p) + 2T_A W_A \cos(2\pi \nu \Delta x) \text{sinc}(2\pi \nu W_A) \quad (2.3)$$

We used Mathematica software to evaluate the intensity at the pupil plane, with and without the use of assist features for a primary feature size of 125 nm. The width of assist feature used for this evaluation was chosen as 40 nm which is much below the resolution capability of 248 nm DUV systems. The value of Δx was 162.5 nm.

It can be seen from the Fig. 2.4 that the use of assist features provides higher image intensity of an isolated primary feature as compared to patterning without assist features. The disadvantage of using assist features is the side-lobe generation. These side lobes are generated due to light transmission through the assist features. If the intensity of side-lobes is sufficiently high and above the threshold light intensity for resist dissolution, they may cause thinning of resist or even print as unwanted features. Therefore, the challenge for the design of assist features is to improve the intensity profile and to keep the intensity of the side-lobe as low as possible.

Fig. 2.4 Intensity profile of an 125 nm isolated pattern with and without use of assist features

Petersen [111] analyzed equation 2.2 and showed how various parameters W_p , W_A , T_p , T_A and Δx modify the maximum amplitude of central and side lobes features. Increase of W_p increases both of the magnitudes and ratio of central and side lobes intensity. It was also shown that adding additional pairs of assist features spaced at integral multiples of Δx will help reducing the minimum between the lobes. With proper optimization, primary isolated features can be made to print as the same size as dense patterns.

If the assist features are shifted 180° out of phase with respect to primary, then the central intensity profile is found to be improved and side lobes intensity is decreased. The electric field due to phase shifting assist features $F(m(x))_{ps}$ is given as,

$$F(m(x))_{ps} = T_p W_p \text{sinc}(\pi v W_p) - 2 T_A W_A \cos(2\pi v \Delta x) \text{sinc}(2\pi v W_A) \quad (2.4)$$

Equation 2.2 for binary assist features can be modified to represent the intensity profile for three pairs of alternating phase shifted assist features. The reason for choosing

three pairs is described in the next section on simulations. If the assist features are separated from each other by a distance W_A , then the electric field at the pupil plane is given by the expression,

$$F(m(x))_{Alter. Assist Features} = T_P W_P \text{sinc}(\pi \nu W_P) - T_A W_A \text{sinc}(2\pi \nu W_A) \left[\left(e^{+2i\pi \nu \Delta x} + e^{-2i\pi \nu \Delta x} \right) - \left(e^{+2i\pi \nu (\Delta x + 2W_A)} + e^{-2i\pi \nu (\Delta x + 2W_A)} \right) + \left(e^{+2i\pi \nu (\Delta x + 4W_A)} + e^{-2i\pi \nu (\Delta x + 4W_A)} \right) \right] \quad (2.5)$$

The intensity profiles for 3 pairs of binary, phase-shifted and alternating phase shifted masks were calculated using Mathematica and plotted as a function of normalized frequency ν as shown in Fig. 2.5. It can be observed in Fig. 2.5 (a) that the assist features

Fig. 2.5 Intensity profile of an isolated 125 nm feature with 3 pairs of assist features (a) primary and binary/phase shifted assist features and (b) primary and alternating phase shifted assist features

intensity is same for either the binary or phase shifted assist features. However, it is much higher than the intensity of the primary feature, which is not desirable as it would lead to side lobe printing. With use of the alternating phase shifted assist features, intensity of primary feature increases significantly over the assist features (Fig. 2.5 (b)). This would prevent printing of side lobes.

Fig. 2.6 shows the normalized total intensity profiles of the sum of primary and assist features, for all the 3 types of assist features viz. binary, phase shifted and alternating phase shifted. Using alternating phase shifted assist features, the zero order diffraction pattern is fully suppressed. Higher order diffraction patterns intensities are very small in comparison to those of the binary or phase shifted assist features. The pattern is formed

Fig. 2.6 Normalized intensity profile with 3 pairs of binary, phase shifted and alternating phase shifted assist features for a primary feature size of 120 nm

mainly by interference of +1 and -1 orders. This reduces the probability of diffracted rays with non-optimal angles interfering to form the image resulting in higher depth of focus of the primary feature. Thus, alternating phase shifted assist features provide a better image quality than the binary or phase shifted assist features.

2.3 SIMULATION

The lithography simulations were carried out using the PROLITH 3D (Positive Resist Optical lithography) simulation software [113]. The imaging conditions used in simulations were: (1) exposure wavelength of 248 nm, (2) NA of 0.68 and (3) partial coherence of 0.31. The criteria for evaluating the lithographic performance of the mask were based on peak intensity (I_{peak}), side lobe intensity (I_{sl}), full width at half maximum (FWHM), and normalized image log slope (NILS) values of the simulated intensity profile. NILS has been in use by lithographers for a long time as an indirect measure of exposure latitude (expressed as change in exposure with respect to change in line-width) [114]. The NILS is a measure of the information content of the aerial image and represents an intensity gradient at the position of the nominal line edge. Larger NILS means that feature edge placement is close to the mask pattern. The information from the aerial image propagates to resist through exposure and development, converting NILS into a normalized dissolution rate gradient which affect the CD control and exposure latitude.

The normalized image log slope is given by the expression

$$NILS = w \cdot \frac{\partial(\ln I(x))}{\partial x} \quad (2.6)$$

where w is the width and $I(x)$ is the aerial image intensity of the feature.

2.3.1 Optimization of Primary Feature Width, Assist Features Width and Their Separation

Three different designs of a phase shift mask, with varying numbers of pairs of alternating phase shifted assist features were simulated. The designs of mask with primary and alternating phase shifted assist features are shown in Fig. 2.7.

Fig. 2.7 Design of a mask with varying numbers of alternating phase shifted assist features (a) 1 pair (b) 2 pairs and (c) 3 pairs

(a) Single Set of 180° Phase Shifted Assist Features

First, the simulations were carried out for a primary isolated trench with one set of phase shifted assist features. The primary feature width was chosen to be 125 nm corresponding to a target k_1 value of 0.34. The width of assist features was varied from 40 nm to 80 nm. The assist features below 40 nm were not considered due to difficulties of making masks for such small features. The separation between the primary features to assist features and between the assist features was varied from 60 to 150 nm in steps of 10 nm.

Fig. 2.8 (a) shows the effect of assist feature width on I_{peak} , I_{sl} and CD. I_{sl} values at the image plane increases with the width of assist features. A separate study was carried out to find out the optimized separation between the primary and assist features. A separation of 120 nm was found to be optimum within the experimental space. The I_{sl} values were 0.1, 0.2, 0.25 and 0.27 for assist feature widths of 40, 50, 60 and 70 nm respectively. I_{peak} remains constant for 40 nm, 50 nm and 60 nm. For 70 nm and 80 nm assist features width, I_{peak} increase slightly and that causes CD to change by 3-4 nm. Thus, CD seems to be very sensitive to I_{peak} intensity. As shown in figure 2.8 (b), ratio of I_{peak} / I_{sl} is maximum for 40 nm assist feature width. The higher I_{peak} / I_{sl} ratio is expected to result in an improvement of the image quality of primary feature and decrease in the possibility of the printing of side lobes. Thus, simulation results show that for the patterning of 125 nm primary features using a single set of phase shifted assist features, optimum lithographic performance is obtained when the line-width of assist features is 40 nm and separation between the center primary and assist feature is 120 nm.

Fig. 2.8 (a) I_{peak} , I_{sl} , CD, and (b) I_{peak} / I_{sl} as a function of width of one pair of phase shifted assist features

(b) Multiple Sets of Alternating Phase Shifted Assist Features

Simulations were carried out with multiple sets of alternating phase shifted assist features. The dimensions of assist features and the separation between primary and assist features were kept constant at 40 nm and 120 nm respectively. For multiple pairs of assist features, the features were phase shifted by 180° as illustrated in Fig. 2.6 (b) and 2.6 (c).

The impact on CD, I_{peak} and I_{sl} with increase in number of pairs of alternating phase shifted assist features is shown in Fig. 2.9. I_{sl} values were found to decrease very slightly when the number of assist features were increased from two to three pairs. However, it remained constant with any further increase in number of pairs. I_{peak} was almost constant for two, three and four pairs of assist features and increased slightly for five, six and seven pairs. With this increase in I_{peak} , primary CD was found to increase by about 3 nm. This trend is similar to what was observed for single pair of assist features in section 2.3.1 (a). For both three and four pairs of assist features, the primary feature CD is

Fig. 2.9 I_{peak} , I_{sl} and CD as a function of number of pairs of alternating phase shifted assist features

131 nm. The CD increases and saturates at 133 nm for four to seven pairs of assist features. This indicates that the additional assist features do not contribute much in shaping the primary feature, as they are placed too far away from the primary feature to be effective.

Fig. 2.10 shows NILS as a function of the number of pairs of alternating phase shifted assist features. Simulation results show a NILS value of 1.12, 1.25, 1.76 and 1.76 for one, two, three and four pairs of assist features respectively at threshold intensity ($I_{threshold}$) of 0.3. Any photoresist exposed to light intensity above the threshold intensity level is expected to be dissolved away during the development process forming a resist image. As mentioned earlier in section 2.3, a higher NILS value is a measure of better process latitude [114]. It was observed that NILS values are saturated for three or more pairs of assist features. Therefore, three pairs of alternating phase shifted assist features are found to be optimum for patterning a trench with design CD of 125 nm. Increasing the number of assist features further does not yield any improvement in process latitude.

Fig. 2.10 NILS as a function of number of pairs of alternating phase shifted assist features

2.3.2 Binary, Phase Shifted and Alternating Phase Shifted Assist Features

Simulations were carried out to compare the lithographic performances of binary, phase shifted, and alternating phase shifted assist features. Fig. 2.11 shows the computed aerial image intensity of a primary feature of width 125 nm for the three cases. The distance between primary feature to adjacent assist and assist features pitch is 240 nm. A significant increase in I_{peak} and a reduction in FWHM of the aerial image were observed in alternating phase shifted assist features as compared to binary assist features. I_{peak} for the binary, phase shifted and alternating phase shifted assist features are 0.36, 0.51 and 0.58 respectively. FWHM is 199.2 nm for binary assist features, 148.3 nm for phase shifted assist features, and 139.7 nm for alternating phase shifted assist features. Smaller FWHM is a metric of good aerial image profile and better process latitude. This is because a

Fig. 2.11 Aerial image intensity profiles of a 125 nm primary feature with three pairs of 40 nm wide alternating phase shifted, phase shifted and binary assist features

smaller FWHM provides steep aerial image profile as can be seen in Fig. 2.11

There is a slight increase in the side lobe intensity for alternating phase shifted assist features as compared to phase shifted and binary assist features. However as long as the intensity of side lobes is less than the threshold value dissolution of resist, the side lobes will not be printed. Fig. 2.12 shows the normalized image log slope (NILS) values as a function of focus for the three cases. NILS values are 2.20, 2.01 and 0.99 for alternating phase shifted assist features, phase shifted assist features and binary assist features respectively at best focus. It is also observed from Fig. 2.12 that for alternating phase shifted assist features, the NILS of 2.20 is maintained within a wide focus range of $0.8\ \mu\text{m}$ ($\pm 0.4\ \mu\text{m}$), which is considered to be quite acceptable for advanced lithography.

Fig. 2.12 Normalized image log slopes of a 125 nm primary feature with three pairs of 40 nm wide alternating phase shifted, phase shifted and binary assist features

2.4 EXPERIMENTAL RESULTS AND DISCUSSION

2.4.1 Experimental Details

The experiments were conducted using a Nikon 248 nm DUV (KrF excimer laser) step and scan exposure system as shown in Fig. 2.13. During exposure, NA of 0.68 and partial coherence of 0.31 were chosen. The mask with phase shifted assist features was made by Hoya Corporation. These exposure parameters were the same as those used for the simulations in section 2.3. Patterning of the isolated trenches was carried out on 200 mm silicon wafers. TEL ACT-8 photoresist coater and developer system was used for resist processing. Wafers were coated with 60 nm of organic bottom anti-reflective coating (BARC- Shipley AR3) and 210 nm of DUV resist (JSR M221Y). Silicon etch was done in a STS deep RIE tool. Top down CD of trench was measured using Hitachi CD SEM S-9200 at a threshold value of 20 %.

Fig. 2.13 Photograph of a Nikon S208, 248 nm DUV step and scan system

2.4.2 Effect of Single and Multiple Pairs of Assist Features on Resist Profile of Trench

Isolated trenches with one, two and three pairs of binary and alternating phase shifted assist features were evaluated experimentally. Top view pictures at different focus values for different number of pairs of alternating phase shifted assist features are shown in Fig. 2.14 (a), (b) and (c). For the evaluation of image quality, we define an acceptable

(a) One pair of phase shifted assist features

(b) Two pairs of alternating phase shifted assist features

(c) Three pairs of alternating phase shifted assist features

Fig. 2.14 Top-down scanning electron micrographs (SEMs) of isolated resist trench patterns across the focus with (a) one pair (b) two pairs and (c) three pairs of alternating phase shifted assist features. Primary feature size on mask is 125 nm

focus range as one in which CD is within $\pm 10\%$ of the average value and there is no distortion of the printed feature. For one and two pairs of alternating phase shifted assist features, isolated trench patterns meeting this criterion were obtained only within a focus range of $0.3\ \mu\text{m}$. For three pairs, focus range was increased to $0.5\ \mu\text{m}$.

The image of trenches could not be resolved when assist features were not used as well as when binary assist features were used. This can be explained by the relatively smaller aerial image I_{peak} and wider FWHM of binary assist features as discussed in section 2.3.2.

Fig. 2.15 (a) is the top down CD SEM profile of resist trench at best dose and focus with CD at the bottom of trench as $117\ \text{nm}$. Fig. 2.15 (b) is the cross-section SEM resist profile after trench patterning. The resist profile looks quite vertical and smooth. There is a CD difference of $8\ \text{nm}$ between top down CD SEM ($117\ \text{nm}$) and cross-section SEM ($125\ \text{nm}$). This could be due to electron beam charging of non-conducting resist features, making resist lines appear larger and trenches smaller under top down SEM measurements. In a top down SEM measurement, the primary electron beam incident on

Fig. 2.15 SEM profiles of isolated trenches using three pairs of alternating phase shifted scattering bars at best dose and focus a) top down resist profile, b) cross-section resist profile and (c) cross-section profile after 200 nm silicon trench etch

the sample would charge the photoresist and underlying dielectric as both are insulators. The net charge could be positive or negative, depending on the number of emitted secondary electrons. If the secondary electrons are less than the number of incident electrons, the surface in the region of the scanning beam would acquire excess negative charge. On the other hand, if the secondary electron yield is larger than the impinging primary electrons, the surface would be positively charged. This localized field would cause the incident beam trajectory to be disturbed, degrading the image focus and consequently, leading to an error in CD measurement. Fig. 2.15 (c) is the trench profile after etching of 200 nm of silicon. A trench bottom CD of 118.4 nm with smooth sidewall profile was obtained.

2.4.3 Effect of Number of Alternating Phase Shifted Assist Features on Depth of Focus (DOF) and Exposure Latitude (EL)

Bossung curve is an important tool to evaluate the process window of a lithography process. It determines the EL that can maintain CD values for a specified structure within 10 percent of its nominal value within an acceptable focus range. Bossung curves of one, two and three pair(s) of alternating phase shifted assist features are shown in Figures 2.16 (a), (b) and (c) respectively.

It is observed that CD uniformity across focus with different exposure doses is much more uniform for three pairs of alternating phase shifted assist features as compared to one and two pair(s). Total process window is shown by dotted rectangles in Fig. 2.16. The pattern with three sets of alternating phase shifted assist features has a DOF of 0.4 μm for a target CD of 120 nm $\pm$ 10 %, while one and two sets of alternating phase shifted assist features have a DOF of 0.1 μm and 0.2 μm respectively. These results show fairly

Fig. 2.16 Experimental Bossung curves for a) one, b) two and c) three pairs of alternating phase shifted assist features

large and acceptable process latitudes with the use of three pairs of alternating phase shifted assist features in terms of DOF, EL and profile. These results are in line with simulated improvement seen in NILS for three pairs of alternating assist features as discussed in section 2.3.2.

2.4.4 Performance of 1:1 Dense Pattern Using the Same Process Conditions as those of an Isolated Trench

We evaluated an alternating phase shift mask pattern for a dense pattern with equal line and space at a pitch of 240 nm using the same process conditions as those used for the processing of the isolated trench pattern in section 2.4.3. Fig. 2.17 shows the Bossung

Fig. 2.17 Experimental Bossung curves for 1:1 dense trench pattern at 240 nm pitch. The process window is shown by dotted rectangle

curves for patterning of dense trenches. We achieved a DOF of 0.5 μm for a CD target of 120 nm $\pm$ 10%. For the isolated trench with three pairs of alternating phase assist features, DOF was found to be 0.4 μm . The CD target and the exposure dose range were kept the same as those for the dense pattern in computation of this DOF value.

Thus, both isolated and dense trenches can be patterned using the same process conditions with acceptable process latitude. Resist top down profiles of dense trench across the focus range is shown in Fig. 2.18.

Fig. 2.18 Top-down SEM images of 1:1 dense trenches of 240 nm pitch across the focus at exposure dose of 76 mJ/cm²

2.5 FABRICATION OF DAMASCENE TRENCH PATTERNS USING ALTERNATING PHASE SHIFTED ASSIST FEATURES

We successfully patterned damascene trenches with nominal trench width of 120 nm, 150 nm and 250 nm using the alternating phase shifted mask lithography technique. The cross-section profiles of these trenches are shown in Fig. 2.19. The fabrication process is described in further details in chapter 6.

The scheme was extended to 100 nm structures by optimization of exposure dose and focus. The SEM cross-section structure of 100 nm patterned Cu damascene trench

Fig. 2.19 Cross-sectional TEM profile of isolated Cu damascene trench for nominal CD of (a) 120 nm, (b) 150 nm and (c) 250 nm

Fig. 2.20 Cross-sectional TEM profile of an isolated Cu damascene trench for nominal CD of 100 nm

pattern is shown in Fig. 2.20. The test structures down to 100 nm were subsequently evaluated for their electrical performance as discussed in Chapters 6 to 8.

2.6 SUMMARY

A novel scheme for enhancing the resolution of DUV exposure tools for backend of line (BEOL) trench pattern lithography making use of a phase shift mask with alternating phase shifted assist features is proposed. We have shown by theory, simulations and experimentation that phase shift mask with alternating multiple assist features is more advantageous as compared to binary or phase shifted assist features, for resolution enhancement. The printed CD achievable with this methodology corresponds to a k_1 factor of 0.33.

We have demonstrated the printing of isolated and semi-isolated trench patterns down to 120 nm with $\pm 10\%$ CD tolerances using a 248 nm DUV lithography exposure system with an NA of 0.68 with wide process latitude. We found that three pairs of assist features are optimum to pattern isolated/semi-isolated trench patterns. We achieved 0.4 μm DOF for a nominal design CD of 115 nm using three pairs of alternating phase shifted assist features. Both isolated and dense trenches can be printed together using the same process conditions and CD target. With only conventional or annular illumination for nominal design trench size of 125 nm with binary assist features, it was not possible to pattern isolated features. The alternating assist features scheme was applied for damascene printing of isolated copper test structures down to 100 nm in width.

Chapter 3

Reflection Control for Copper Damascene Process

3.1 INTRODUCTION

Copper dual damascene technology has changed the traditional integration scheme for back-end metallization. Apart from material changes from aluminum to copper and silicon oxide to low- κ dielectrics, there are substantial changes in the way these materials are integrated in the process flow. During the fabrication of nanoscale interconnects, one of the main challenges encountered is reflectivity control during the lithography process. In chapter 2, a novel mask with alternating phase shifted assist features was proposed with considerable improvement in resolution and exposure latitude for patterning of nanoscale isolated or semi-isolated trench structures for copper metallization. The lithography process latitude for such a scheme can be further enhanced by having a good reflection control during the lithography processes. Therefore, a study was carried out to understand the underlying issues which make reflectivity control difficult in dual damascene technology and to propose appropriate solutions for a better control.

There are two main factors which make reflectivity control more difficult for copper/low- κ interconnect process as compared to the aluminum interconnect process. Firstly, copper metallization is typically used for sub 0.13 μm technology nodes and therefore the resolution requirement necessitates the use of 248 nm or 193 nm DUV lithography systems. For aluminum interconnect patterning, 365 nm (I-line) exposure tools are used. Padmanaban et al. [115] reported that compared to g-line (436 nm) exposure, reflectivity from silicon into a typical resist film is higher by about 78% at 365 nm, 132%

at 248 nm and 157% at 193 nm. Since reflectivity increases with a decrease in the exposure wavelength, reflectivity control is more difficult with the use of DUV systems. Secondly, the patterning process changes from subtractive patterning for aluminum interconnects to additive patterning for copper interconnects. In the subtractive aluminum process, buried layers underneath the aluminum have very little influence on the substrate reflectivity as the surface to be patterned is covered with a blanket film of highly reflective aluminum layer. In contrast, in an additive damascene process, patterning is carried out on a film stack consisting of transparent dielectric films as well as buried reflective metal or polysilicon films. As a result, in a copper damascene process, incident light is reflected back at multiple interfaces during the via and trench lithography as shown in Fig.3.1. This reflected light from various interfaces then interferes with the incident light causing so called thin film interference (TFI) effects.

Fig. 3.1 Multiple light paths for incident and reflected light in a dual damascene film stack

3.1.1 Thin Film Interference (TFI)

TFI manifests itself as two major effects which degrade the resist profile and cause variations in the CD of a patterned structure. These effects are known as i) standing waves effect and ii) swing effect. Standing waves effect is well documented in the literature [116-119] and it arises due to interference of incident and reflected light beams resulting in sinusoidal intensity variation with depth in the resist. Due to this effect, the resist profile contains a periodic ripple on its side walls after the development of exposed pattern. As can be observed in Fig. 3.2, the resist profile is deteriorated and such a profile results in large variation in the CD of etched patterns.

Fig. 3.2 Cross-section profile of a resist structure showing standing wave effect

Mack [120, 121] has proposed the following approximate expression for the standing wave intensity $I(z)$ in the resist as a function of depth,

$$I(z) = \left[e^{-\alpha z} + R e^{-\alpha(2D-z)} \right] - 2\sqrt{R} e^{-\alpha z} \cos(4\pi n(D-z)/\lambda) \quad (3.1)$$

Here λ is the wavelength of light source, α , n and D are respectively the absorption coefficient, refractive index and thickness of the resist, and R is the substrate reflectivity.

In the above equation, the first part indicates absorption of light in the resist and the second part accounts for the sinusoidal variations of intensity in the resist profile.

The swing effect causes variations in a lithography parameter such as CD due to changes in the total light energy coupled to the resist. This arises as intensity and phase of reflected light in a damascene film stack varies with the thickness of resist as well as that of the transparent dielectric films. The extent of variation is assessed using the term ‘swing ratio’ which is defined as peak to valley change in a given lithographic parameter as a function of thickness divided by its average value. Fig. 3.3 (a) shows the simulated variation in resist reflectivity with the thickness of resist and Fig. 3.3 (b) shows the simulated effect of such a reflectivity variation on the CD of the developed image.

Swing ratio is an important figure of merit used for characterization of lithography performance. Lithographers always try to optimize the process so as to minimize the swing ratio. Brunner has developed an analytical expression for the swing ratio [122]. Consider a light incident normally on a substrate through a resist. The incident light then goes through a series of reflections between the resist and substrate interface as well as the resist and air

Fig. 3.3 (a) Resist reflectivity and (b) CD swing curves

interface. The incident and the reflected light waves interfere constructively if they are in phase and destructively if they are out of phase. The theory of such a film stack, also known as Fabry-Perot etalon, is well established. According to this theory, the intensity of light at the bottom of resist, I_b is given as:

$$I_b = I_{avg} (1 - 2|F| \cos(\phi + \delta)) \quad (3.2)$$

where δ is the phase change of the reflected light at the resist/substrate interface, ϕ denotes the phase change in resist, I_{avg} is the average intensity in the resist and F is a complex coefficient.

$$I_{avg} = \frac{4n_r}{(n_r + 1)^2} e^{-\alpha D} \cdot (1 + R_b) \quad (3.3)$$

$$\phi = \frac{4\pi n_r D}{\lambda} \quad (3.4)$$

$$|F| = \sqrt{R_t R_b} e^{-\alpha D} \quad (3.5)$$

Here n_r is the refractive index of the resist, D is resist thickness, and R_t and R_b are the reflection coefficients at the resist-air and resist substrate interfaces respectively.

The peak and valley value for intensity at the bottom of resist can be found from equation 3.2 by using the maximum value of cosine function.

$$I_{peak-valley} = I_{avg} (1 + 2|F|) - I_{avg} (1 - 2|F|) = I_{avg} \cdot 4|F| \quad (3.6)$$

Swing ratio, S is calculated by dividing equation 3.6 for peak to valley intensity by equation 3.3 for the average intensity I_{avg} ,

$$S = \frac{I_{peak-valley}}{I_{avg}} = 4|F| \quad (3.7)$$

Equations (3.5) and (3.7) yield,

$$S = 4\sqrt{R_t R_b} e^{-\alpha D} \quad (3.8)$$

Equation (3.8) is also known as Brunner's formula.

As seen from the Equation 3.8, swing ratio can be minimized either by reducing the resist to substrate interface reflectivity or resist to air interface reflectivity or both. Organic or dielectric bottom antireflective coatings (BARC) or top antireflective coatings (TARC) can be used for this purpose. In literature, dual antireflective layers consisting of two different layers deposited on the substrate as BARC are also discussed for mitigating the effects of reflectivity [123-128]. In a typical dual antireflective BARC scheme, the bottom layer is typically a thick light absorbing layer with a high absorption coefficient while the upper antireflective layer minimizes reflectivity by a combination of absorption and destructive interference of light. Chen et al. [123] proposed a dual BARC scheme consisting of a 248 nm DUV resist and an organic resist BARC material for ArF (193 nm) reflection control applications. Ying et al. [124] discussed the design of dual layer BARC as universal antireflective layer while Min et al. [125] discussed its use for KrF applications. In addition Lin et al. [126] applied dual $\text{SiO}_x\text{N}_y\text{:H}$ DARC as an oxide hard mask application. Lee et al. [127] and Chou et al. [128] proposed dual layer SiO_xN_y antireflective schemes for the formation of damascene structures. Although the literature describes the principle and design of dual antireflective layers, not much has been reported on the effects of additional diffusion barrier layers or CMP etch stop layer layers on a dual damascene process.

There are two types of antireflective coatings, organic and inorganic films. The former are normally spin coated. With feature sizes shrinking below 100 nm, it is

becoming very difficult to spin coat organic antireflective layers with good planarization and conformality for small features in an interconnect process. The inorganic antireflective coatings also known as dielectric anti-reflective coatings (DARC) have the advantage of conformal deposition by plasma enhanced chemical vapour deposition (PECVD). Their optical properties and thickness can be modified during deposition to obtain the appropriate phase shift and amplitude for destructive interference.

In this chapter, we report a systematic study of the lithographic performance of three different BARC films using simulations and experimentation. We studied three different types of BARC schemes viz. i) organic BARC film, ii) single layer SiO_xN_y DARC and iii) dual layers SiO_xN_y DARC. The film stack chosen for evaluation was based on a via-first-dual damascene (VFDD) integration scheme [129]. The lithography simulator PROLITH/3D version 6.1 [113] was used to design and evaluate the performance of the three antireflective schemes. This was followed by extensive experimental evaluation of their lithographic performance with particular emphasis on the dual SiO_xN_y DARC scheme. We also discuss the results of development of a PECVD process for deposition of DARC films with required optical constants.

3.2 DESIGN AND SIMULATION OF THE ANTIREFLECTIVE SCHEMES

The main objective of design and simulations of antireflective films is to minimize surface reflectivity and CD swing ratio caused by multiple reflections and variation in underlying film thickness. It is also desirable that the optimized antireflective scheme performance is not degraded with change in the underlying substrate materials. The second objective is to design a BARC scheme that is not very sensitive to variations in optical properties and layers thickness so that a large process latitude can be obtained.

3.2.1 Effect of Substrate Reflectivity on CD Swing Ratio

CD, dose to clear (E_0), and resist reflectivity (RR) are important metrics for evaluating the performance of a lithography process. E_0 refers to the amount of exposure energy required that just clears the resist in a large clear area for a given process. Equation 3.7 can be generalized to evaluate variations in CD, E_0 and RR as a function of resist thickness. A generalized equation for computation of swing ratio for a given swing curve is given by the expression:

$$S_x = \frac{(X_{\max} - X_{\min})}{(X_{\max} + X_{\min})/2} \times 100\% \quad (3.9)$$

Here S_x is the swing ratio corresponding to parameter X , which can be CD or E_0 or RR. $X_{\max}$ is the average value for two consecutive maxima and $X_{\min}$ is the minimum value in between. It is desirable to have minimum variation or least swing ratio as a function of change in resist thickness and underlying films thicknesses. For a $\pm 5\%$ variation in the value of parameter X from its average value, the swing ratio would change by 10%. As an example, for CD tolerance to be within $\pm 5\%$ of nominal value, swing ratio should not exceed more than 10%.

Simulations were used to find the relationship between substrate reflectivity and swing ratio. To get a variable substrate reflectivity, a dummy layer of SiC with variable thickness, n and k values and a DUV resist deposition of thickness 540 nm on Si substrate were considered. The optical parameters and thickness of the dummy SiC layer were adjusted to achieve a substrate reflectivity in the range 1-10 %. Isolated 0.18 μm trench patterns were simulated for exposure by a 248 nm, 0.68 NA DUV system. The swing ratios for RR, E_0 and CD, derived from simulation data as a function of substrate reflectivity, are

shown in Fig. 3.4. It is found that all the swing ratios increase with substrate reflectivity. As the maximum allowable S_{CD} should be less than 10 % for a $\pm 5\%$ CD control, the substrate reflectivity needs to be controlled within 2% as shown in Fig. 3.4.

Fig. 3.4 RR, E_0 and CD swing ratio as a function of substrate reflectivity

3.2.2 Optimum Thickness (t), Refractive Index (n) and Extinction Coefficient (k) of Antireflective Layers

A low- κ film stack consisting of Si substrate, SiC, low- κ SiOC and SiC cap layer was defined in the simulations. The SiC cap layer acts as a copper diffusion barrier layer and also protects the low- κ film from direct polishing during chemical mechanical polishing (CMP). The t , n and k of Si-substrate and various films used for simulation are shown in Table 3.1.

Simulations were carried out to optimize the optical parameters and thicknesses of the various types of antireflective coatings that result in minimum substrate reflectivity. Three different antireflective schemes viz. i) organic BARC, ii) single layer DARC and iii) dual layer DARC were simulated.

Table 3.1 n , k and t of films used in simulations of damascene film stack

Layer	n	k	t (nm)
Si	1.57	3.56	Substrate
SiC	1.99	0.05	50
SiOC	1.47	0.003	1000
SiC (cap)	1.99	0.05	60
Organic BARC	1.47	0.47	Variable
Single DARC	Variable	Variable	40
Dual DARC (bottom)	variable	Variable	40
Dual DARC (top)	2.3	Variable	Variable
Resist (UV210)	1.75	0.01	540

(a) No BARC

Fig. 3.5 shows the substrate reflectivity as a function of SiOC layer thickness without any antireflective layer. The substrate reflectivity is as high as 29%. This is much higher than the desired substrate reflectivity of less than 2% for a $\pm 5\%$ CD control. Therefore, an antireflective layer is necessary for reflection control.

Fig. 3.5 Substrate reflectivity swing curve without use of an antireflective layer

(b) Organic BARC

The n and k values for the organic BARC simulations were chosen as 1.46 and 0.47 respectively. These values correspond to those of a commercially available organic BARC for 248 nm dual damascene applications. A substrate reflectivity of less than 2% was found at a BARC thickness of 80-85 nm as shown in Fig. 3.6.

Fig. 3.6 Substrate reflectivity as a function of organic BARC thickness

(c) Single layer DARC

The thickness of the SiO_xN_y DARC was set at 40 nm so that the combined thickness of SiC cap and DARC film is about 100 nm. This thickness was chosen to ensure that sufficient SiC remains in the stack after CMP to protect the underlying low- κ SiOC film. Also it is not desirable to have thicker layers as it will increase the aspect ratio of the film stack, creating difficulties in patterning and filling of via with copper. As shown in Fig. 3.7, n and k in the range of 2.3-2.5 and 0.05-0.25 respectively will keep the substrate reflectivity below 2.5%.

Fig 3.7 Contour plots of substrate reflectivity as a function n and k for single DARC layer of thickness 40 nm

(d) Dual layer DARC

The dual DARC scheme is simulated with two different layers of SiO_xN_y DARC films. The dielectric stack for dual DARC consisted of Si substrate with 50 nm of SiC, 1.0 μm of SiOC, 60 nm of SiC cap, 40 nm of bottom DARC and top DARC as shown in Fig, 3.8. The dual layer DARC scheme is simulated with two different layers of SiO_xN_y DARC films.

Variation of substrate reflectivity was studied as a function of k of the bottom DARC and thicknesses of the SiOC and SiC layers as shown in Fig. 3.9 (a) and (b) respectively. There is increase in substrate reflectivity with k . However at higher k values, the reflectivity contours become flat, indicating less sensitivity of substrate reflectivity with change in underlying films. Thus, for the absorptive bottom DARC, a k value higher than 1.2 should be chosen as this can mitigate the effect of rapid reflectivity variations seen

Fig. 3.8 Dielectric film stack for dual layer DARC simulations

Fig. 3.9 Contour plots of substrate reflectivity for bottom DARC as a function of k and t of (a) SiOC and (b) SiC

at lower k values due to thickness changes. Therefore, n and k values of 2.3 and 1.3 respectively were chosen for the bottom DARC for further simulations.

For the top DARC layer, n should be the same as that of the bottom DARC layer to minimize reflections at the top and bottom DARC interface. Fig. 3.10 shows the relationship between the bottom and top DARC layers thickness and substrate reflectivity. Refractive index is 2.3 for both bottom and top DARC layers and k is 0.3 for top DARC and 1.3 for bottom DARC. Substrate reflectivity of less than 0.5% is achieved for a wide range of top and bottom DARC layers thicknesses with a range of 15-20 nm for the top DARC and greater than 35 nm for the bottom DARC. A thickness of 40 nm for the bottom DARC and 17 nm for the top DARC were chosen for further simulations.

Fig. 3.10 Contour plot of substrate reflectivity as a function of thickness change of bottom and top DARCs for fixed n and k

3.2.3 Effects of SiC and SiOC Film Thickness on Substrate Reflectivity

The PECVD deposited dielectric film thickness can vary because of non-uniformity of the deposition process and non-uniform loss of film after CMP. The non-uniformity can be as high as 2 % and a thickness loss of 30- 100 nm for the barrier film has been reported during the CMP process [126]. Therefore, it is necessary to simulate the effect of process induced film stack thickness variations of low- κ and other dielectrics on the substrate reflectivity.

The simulated substrate reflectivity as a function of thickness changes in SiC and SiOC films are shown in Fig. 3.11. The peak to peak substrate reflectivity with changes in the thickness of SiC and SiOC layers are shown in Table 3.2. It is observed that the single layer DARC scheme is found to be the most sensitive to SiC and SiOC layers thickness variations. The dual layer DARC scheme is the least sensitive followed by the organic BARC scheme.

Fig. 3.11 Substrate reflectivity without BARC, organic BARC, single DARC and dual layer DARC as a function of thickness of (a) SiC (b) SiOC:H

Table 3.2 Peak to peak substrate reflectivity for a damascene film stack for various antireflective schemes as a function of thickness changes of SiOC and SiC layers

Film type	Peak to Peak reflectivity (%)			
	No BARC	Organic BARC	Single layer DARC	Dual Layer DARC
SiOC (960-1240 nm)	8.4	4.4	12.3	0.5
SiC (20-100 nm)	17.7	4.1	12.4	0.5

3.3 EXPERIMENTAL EVALUATION OF LITHOGRAPHIC PERFORMANCE OF DARC FILMS

SiO_xN_y films were deposited using a plasma of N₂O, SiH₄, N₂ and He with different flow rate ratios (α) of N₂O and SiH₄ in an Applied Materials Centura PECVD system. The flow rates of SiH₄, N₂ and He were kept constant at 60 sccm, 600 sccm and 2000 sccm respectively while the flow rate of N₂O was varied to achieve α values in the range 0.2 to 5. The radio frequency (RF) power was fixed at 350 W with a chamber pressure of 5 Torr. Undoped silicate glass (USG) and SiC layers were deposited in a Novellus Concept 2 Sequel PECVD reactor while SiO_xN_y and SiOC layers were deposited in an Applied Materials Centura PECVD reactor. The tetra-methyl silane (4MS) and tri-methyl silane (3MS) precursors were used for SiC and SiOC film deposition respectively. The chemical composition of the film was evaluated using a Biorad QS2200 ME Fourier transform infrared spectroscopy (FTIR) system.

The organic BARC layer coating and resist bake/development were carried out on a TEL ACT8 wafer track. The UV210 photoresist was exposed using Nikon S203 DUV step and scan system at an NA of 0.68 and a partial coherence of 0.75. The n and k values of the films at 248 nm were measured using a Thermawave Optiprobe 5240i spectroscopic ellipsometer. The n , k and t of the organic ARC layer used for the experiments were 1.46, 0.47 and 60 nm respectively. The values of n , k and t for the dual layer DARC are given in Table 3.3.

Table 3.3 Measured values of t , n and k for top and bottom DARC layers

Film type	t (nm)	n	k
Bottom DARC	40.1	2.273	1.243
Top DARC	16.6	2.353	0.304

3.4 RESULTS AND DISCUSSIONS

3.4.1 SiO_xN_y DARC Deposition Process Development

The objective was to obtain the relationship between α and n and k of the PECVD deposited films. From Fig. 3.12, it is seen that n decreases from 2.36 to 1.56 with increase in α . This implies that there is a gradual increase in the percentage of oxygen in the film because the refractive indexes of stoichiometric silicon nitride and silicon dioxide are 2.33 and 1.51 respectively [130]. Increase of oxygen content rather than nitrogen with increasing α can be explained from the fact that the dissociation energy of N₂O is lower than that of N₂; therefore the activation efficiency of N₂O in plasma is larger than that of

Fig. 3.12 n and k values of SiO_xN_y as a function of $\text{N}_2\text{O}:\text{SiH}_4$ flow rate ratio, α

N_2 . Also the bonding energy of Si-O is larger than that of Si-N. Therefore, Si atoms tend to form bond easily with O atoms rather than N atoms.

As observed from Fig. 3.12, k increases with decrease in α . Stoichiometric SiO_2 and Si_3N_4 films have very low extinction coefficient of about zero and 0.02 respectively at 248 nm [131]. At low α values of 0.16 to 0.4, the film becomes Si rich SiO_xN_y and exhibits very high k values in the range 0.61 to 0.25. A still higher value of k can be obtained at higher SiH_4 flow rates where a k value in the range 1.26 to 0.99 is obtained for an α of 0.1 to 0.3.

FTIR absorption spectra were collected for samples prepared with different α in the range of 0.2 to 5. Fig. 3.13 shows the FTIR spectra of all samples for wave numbers ranging from 400 to 4000 cm^{-1} . In the spectra, a Si-O rocking bond peak is observed at 450 cm^{-1} . A Si-N stretching mode peak is also observed and its position varies from 840- 880 cm^{-1} . In stoichiometric Si_3N_4 , this peak is at about 900 cm^{-1} [130]. In the films deposited,

Fig. 3.13 FTIR spectra of SiO_xN_y with varying $\text{N}_2\text{O}:\text{SiH}_4$ flow rate ratio, α

this peak is much lower due to the presence of Si-Si groups in the films. The intensity of this peak decreases with α and this implies a corresponding decrease in the relative atomic percentage of nitrogen. A second peak is observed between 960 cm^{-1} and 1040 cm^{-1} and it is related to the Si-O stretching mode. The position of the Si-O stretching peak depends upon the atomic percentage of oxygen in SiO_xN_y . The Si-O stretching bonds shift to higher wave number with an increase in atomic percentage of oxygen [130]. Thus, a shift to a higher wave number as observed in the films implies that there will be more oxygen in SiO_xN_y film with increase in α .

Two hydrogen stretching bonds are observed near 3350 cm^{-1} (N-H stretch) and 2200 cm^{-1} (Si-H stretch). No significant intensity is observed near $3350\text{--}3500\text{ cm}^{-1}$ (O-H stretch). The intensity of Si-H bonds increases as α decreases. With decreasing α , the peak of Si-H shifts from about 2240 to 2160 cm^{-1} . Lucovsky et al. [131] reported that the Si-H peak shifts to low wave numbers because the $\text{SiO}_x\text{N}_y\text{:H}$ films become increasingly rich in

Si. Gocho et. al reported that an increase in k value is attributed to the increase in Si in the SiO_xN_y [132]. The intensity of N-H bonds observed near 3350 cm^{-1} decreases with the decrease in α . N-H bonds play a major role in the contamination of DUV resist as N-H bonds can neutralize the photo acid generated upon exposure, making resist less soluble in the developer. This is the main limitation of SiO_xN_y and additional surface treatment such as oxygen plasma, annealing at high temperature or deposition of a thin layer of silicon oxide on top of the SiO_xN_y : H film may be necessary to solve the problem of resist contamination.

This experiment shows that the PECVD process parameters can be used to deposit DARC layers with n and k values close to the simulated values given in Table 3.3.

3.4.2 Effect of Substrate Multi-Layers on Dual DARC Performance

The experimental resist reflectivity and E_0 swing curves for the damascene stack are shown in Fig. 3.14 as a function of SiOC thickness. Resist reflectivity was measured by a spectroscopic ellipsometer system and was normalized to the reflectivity of silicon. The resist reflectivity swing ratio decreases from 51.3% to 5.5% with dual layer DARC.

Fig. 3.14 Experimental swing curves as a function of SiOC thickness (a) resist reflectivity with and without dual layer DARC, and (b) dose to clear with dual DARC

The dose to clear (E_0) swing ratio with dual layer DARC is 2.6%. These results show that the dual layer DARC is effective in mitigating the effects of the thickness variations of under-layers on the substrate reflectivity.

3.4.3 Comparison of Lithographic Performance For Organic BARC and Dual DARC Scheme

Lithographic performance of the antireflective schemes was evaluated by a comparison of RR and E_0 swing ratios. As the objective of the experiment is to compare the different antireflective layers, we chose silicon as a substrate. The RR and E_0 swing curves for bare silicon and two BARC schemes are shown in Fig. 3.15 (a) and (b) respectively. A maximum error (3σ) of 2.48% was estimated for the reflectivity based upon eight measurements for each of the resist thicknesses on three different types of substrates. This error could be caused by inaccuracies in focusing, incidence angle and roughness of the film surface. A maximum error of 0.1 mJ/cm^2 was estimated for E_0 measurements. This is equal to the incremental step used for the exposure dose in the experiment. The effects of other errors such as exposure and resist process non-

Fig. 3.15 Experimental swing curves for bare silicon, organic BARC and dual DARC on a silicon substrate (a) resist reflectivity and (b) dose to clear

uniformities were considered to be negligible due to the large incremental exposure dose of 0.1 mJ/cm^2 used in the experiment.

Table 3.4 shows the simulated and experimental results of resist reflectivity and E_0 swing ratios. The results show that both organic and dual layer DARC schemes are effective in reducing the swing ratios as comparison with bare silicon substrate.

The minimum swing ratios were obtained for the organic BARC followed by dual layer DARC. A plausible explanation is that the design of the dual layer DARC was not optimized for patterning on the bare silicon substrate so the RR swing ratios for dual layer DARC are higher than that of organic BARC. E_0 swing ratios for both schemes are small and comparable. The differences in E_0 , between the simulated and experimental data can be narrowed down further by a better tuning of chemically amplified resist parameters used for the simulation [133].

Table 3.4 Simulated and experimental RR and E_0 swing ratios without BARC, with organic BARC and dual layer DARC

ARC scheme	RR Swing ratio (%)		E_0 Swing ratio (%)	
	Simulated	Experimental	Simulated	Experimental
No BARC	129.8	73.7	67.2	50.0
Organic BARC	18.2	21.0	3.15	7.44
Dual DARC	62.7	52.4	7.8	9.88

3.5 SUMMARY

In this study, three different antireflective films viz. (i) organic BARC, (ii) SiO_xN_y single layer DARC and (iii) SiO_xN_y dual layer DARC were studied for the purpose of

reflectivity control in a backend copper process. Although all the antireflective films were found suitable, the dual DARC performed considerably better in controlling substrate reflectivity with variations in underlying optically transparent films thicknesses as compared to other antireflective films. A maximum reflectivity range of 4.4%, 12.3% and 0.5 % respectively are estimated for a 40 nm change in SiOC film thickness with use of organic BARC, single layer DARC and dual layer DARC respectively. Effectiveness of the dual DARC scheme was demonstrated experimentally on a SiC/SiOC/SiC film stack. Dual DARC reflectivity control methodology together with resolution enhancement scheme using alternating phase shifted assist features should be quite useful for nanoscale patterning of interconnects.

Chapter 4

Deep-ultraviolet Lithography of Damascene Structures and Resist Contamination Effects

4.1 INTRODUCTION

In chapters 2 and 3, methodologies to improve the resolution and process latitude for patterning of nanoscale copper interconnects were discussed. The use of phase shift mask with alternating assist features enhanced the resolution capability of the 248 nm DUV scanner and enabled resolving trench features down to 100 nm. Reflection control strategy using dual DARC provided a better exposure latitude and DOF for CD control of nanoscale features. However, these improvements are still not sufficient for patterning of nanoscale trenches and vias required for fabricating copper interconnects. One of the issues faced is DUV resist contamination or resist poisoning observed in a via-first dual damascene (VFDD) integration scheme [129, 134-138] for fabrication of copper and low- κ interconnects.

For patterning of nanoscale interconnects used in our study, it is imperative to use a DUV exposure tool with a chemically-amplified resist (CAR). CARs provide much better sensitivity, resolution and dry etch resistance as compared to traditional resists based on novolac resin and diazonaphthoquinone dissolution inhibitor. In a CAR, catalytic species generated on irradiation induce a cascade of chemical transformations which improve the gain and sensitivity of resists [139]. However CARs are inherently prone to molecular-base contamination from airborne or process-induced species. Any molecular base contaminations will terminate the chemical amplification process of a CAR making it

insoluble in a developer after irradiation and formation of resist residues. This phenomenon is known as resist contamination or resist poisoning.

Resist poisoning has been very widely reported in literature, and the problem was recognized soon after DUV resist was introduced for conventional aluminium/oxide high resolution lithography [140-145]. Resist poisoning is further aggravated in the dual damascene architecture [134-140, 146-148]. The ITRS roadmap for interconnects [3] identifies resist poisoning as one of the difficult challenges for interconnects ≥ 32 nm. In a VFDD scheme, resist contamination is normally observed after trench lithography. The via dielectric after etching, striping and cleaning processes may trap a small amount of amines or other type of molecular base contamination. Resist in the vias may be contaminated by this molecular base. This contamination appears as residue in the via region after resist development. As a result, the dielectric underneath the residual resist cannot be etched adequately for the formation of DD structures. Fig 4.1 (a) shows the problem of resist contamination in a VFDD schematic process flow. Fig. 4.1(b) and (c) depicts the top view and cross-section SEM micrographs of the poisoned via structures. Resist residue in the via region leads to the formation of unwanted crown structures due to micro-masking as shown in Fig. 4.1(d). The resist poisoning problem is further enhanced with the use of low- κ dielectrics which are relatively porous as compared to the conventional dielectrics such as silicon-dioxide. Porosity in a material makes it more susceptible to interactions with the various chemicals and gases used in the wafer processing and any molecular base contamination inside the clean room environment. Therefore, dual damascene patterning process with copper and porous low- κ materials is more prone to resist poisoning.

DUV-resist poisoning in copper interconnects process has been reported in

Fig. 4.1 (a) VFDD scheme showing resist poisoning. (b) Top view SEM (after trench lithography), (c) cross-section SEM (after trench lithography) and (d) crown formation after trench etching

the literature as one of the major problem for trench patterning. It is reported that process [149-153] as well as environmental induced base contamination [154-160] can cause resist poisoning. In [134-135, 150-152], it is observed that nitrogen containing hardmask and etch stop layers can deactivate the photoresist by consumption of photoacid. Also if a nitrogen containing reducing chemistry is used for photoresists strip, it results in the formation of amines, which can poison the resist during trench patterning. Some researchers [151, 153] have noticed that post etch cleaning can lead to photoresist poisoning as most of the post etch chemicals used in the semiconductor industry contain amines. In [150, 161], it is suggested that resist poisoning can be mitigated by the use of a

more contamination tolerant DUV resist. A negative tone resist for via patterning is also proposed as a potential solution to resist poisoning [162-164]. Some reports suggest the use of contamination trapping via gap fill material to act as a buffer between the via dielectric and resist [165-167] Shimura et al. [148] proposed a bi-layer silylation process to mitigate poisoning which is however difficult to implement. Lamy et al. [168] did a comparative study of resist poisoning caused by four different wet chemical treatments that are used for post resist strip (ashing) cleaning process with an objective of developing a contamination monitoring technique. They found that low- κ SiOC is more affected by poisoning than oxides. Surprisingly, porous low- κ materials were, however, found to be less affected as compared to non-porous SiOC materials. On the other hand, Simon et al. [169] confirmed that porous low- κ materials amplify the resist poisoning problem. They also implemented a ‘dose to clear’ compensation method for evaluating hard masks, wet and dry stripping processes, and photo-resist in terms of their poisoning sensitivity. Louveau et al. [151] advocated a combination of dry stripping processes and wet chemicals for shortening the time for wet treatment. Satyanarayana et al. [170] suggested a time link between via etching and trench lithography process, avoiding the use of N_2 containing reducing chemistry during the via ashing process, minimizing the use of high nitrogen content films, and isolating the via bottom by a BARC process.

Besides process-induced contamination of DUV resists, another potential source of contamination is airborne molecular contaminants. Organic contaminants can come from many sources in a wafer fab, such as photoresists, cleanroom materials, wafer carriers etc [154-155]. It has been reported that the level of organic contamination does not necessarily correspond to the amount of particle contamination in a cleanroom. The organic

contamination level on wafer in a class 1 cleanroom could be worse than that in a class 10 cleanroom [155]. Airborne molecular organic contamination has increasingly become a serious problem as the surface arrival rate of airborne molecular contaminants is several orders of magnitude higher than that of particles [156]. Airborne organic molecules are ubiquitous in the wafer fabrication environment. It can exist as floating organic micro-globule or vaporized organic solvents [156]. It has been reported that airborne organic contamination can result from the outgassing of the carrier case materials when the wafers are stored in a carrier box equipped with different carrier cases [157]. Various techniques have been used to characterize wafer surface contamination [134-135, 155-160].

Thus there is no single solution to resist poisoning and it is not clear whether it is dielectric materials, process interaction or environment that has a larger role to play in resist poisoning. The susceptibility of a given process, materials and environment towards poisoning is very difficult to evaluate due to several reasons. Firstly, the species that cause poisoning are not fully identified. Secondly, the quantities of contamination that can induce poisoning could be in parts per billion (ppb) [171]. Lastly, any one or a combination of the processes such as deposition, etching, photoresist stripping or cleaning can cause the poisoning. In this chapter, we have investigated the resist poisoning issue from an overall integration perspective and identified the most critical processes and materials that are responsible for poisoning. Materials such as low- κ (SiOC), cap (SiC) and antireflective DARC (SiON) dielectrics, as well as processes used for forming the DD structure (deposition, etch, stripping and cleaning) are investigated for resist poisoning. Physical mechanisms responsible for the formation of resist residues are identified.

The results of this study will enable a successful fabrication of test structures required for electrical characterization of interconnects in Chapters 6-8.

4.2 MECHANISM OF DUV RESIST CONTAMINATION

The DUV resist consists of a photo acid generator (PAG), a polymer resin, a protecting group, dyes, additives and a solvent. Aryl sulfonium salts as PAG, and tertiary butoxycarbonyl (t-BOC) protecting group are commonly used in a DUV resist. The resin is normally soluble in an aqueous base developer. However, the t-BOC group reacts with the resin and forms side chains to slow down its solubility. So without any exposure, resist is protected against development in an aqueous base. Upon exposure of DUV resist, PAG reacts to form a photoacid (CF_3COOH) as shown in the equation 4.1.

The photoacid is used for the de-protection reaction after the post exposure bake. The de-protection reaction of t-BOC is shown in equation 4.2. Here t-BOC dissociates to form soluble hydroxyl groups, making the resist soluble in a developer solution.

Concurrently, more acid (H^+ ions) is generated [138]. If there is any amine impurity present, it will quench the acid generation during the post exposure bake and de-protection will be incomplete. This will lead to DUV resist contamination.

4.3 EXPERIMENTAL

A base dielectric-film stack consisting of USG (200 nm), SiC (50 nm), and a low- κ SiOC film (1000 nm) on a silicon wafer was prepared. Two additional dielectric-film layers designated as first and second capping layers were deposited on top of this base stack to obtain a total of five different low- κ dielectric film stacks, as shown in Table 4.1.

All the deposition processes on the wafers were carried out using PECVD process. The low- κ SiOC and antireflective SiON films were deposited in an Applied Materials Centura PECVD system, while the USG and SiC films were deposited in a Novellus Concept Two Sequel PECVD system. A 60 nm thick Shipley AR3 bottom antireflective coating (BARC) was used for both via and trench lithography. Shipley UV210 DUV photoresist with a thickness of 560 nm and 480 nm was used for via and trench lithography

Table 4.1 Cap dielectrics (100 nm) deposited on a base film stack consisting of Si-substrate, USG (200 nm), SiC (50 nm) and SiOC (1000 nm)

Scheme	Capping layer 1	Capping layer 2	Remarks
a	None	None	Base stack only
b	SiC (100 nm)	None	SiC capping layer
c	SiON (100 nm)	None	SiON antireflective layer
d	USG (100 nm)	None	USG capping layer
e	SiC (100 nm)	SiON (100 nm)	SiC capping layer and SiON antireflective layer

respectively. The resist/BARC coating, bake and development processes were carried out on a Tokyo Electron ACT8 wafer-track system. The wafers were exposed in the Nikon S203 step and scan system with an NA of 0.68. The BARC and dielectric films were etched in a Tokyo Electron DRM etcher while resist stripping was carried out in a Mattson ASPEN II system. Post-etch solvent cleaning of polymer residue was performed in a Semitool Magnum solvent processor using a commercial cleaning solvent ST250.

Film thickness was measured by a Thermawave Opti-Probe 5240i spectroscopic ellipsometer. The wafer surface was inspected for contamination by a Hitachi 9200 CD SEM. Cross-section SEM analysis was carried out on a JEOL JSM6700F system. Secondary-ion mass spectroscopy (SIMS) analysis was conducted on a CAMECA IMS 6f system. Auger electron spectroscopy (AES) was performed on a JEOL JAMP 7800F system. The AES used for the analysis had a sampling depth of < 5 nm, spatial resolution of < 100 nm and an elemental sensitivity of 0.1-1.0 atomic %. Electron energy loss spectroscopy (EELS) analysis was carried out using a GATAN GIF 2001 Model 860 system attached to a Phillips CM200 FEG transmission-electron microscope (TEM). Thermal-desorption gas chromatography and mass spectroscopy (GC-MS) were performed on a HP6890 GC and a HP5973 MS systems attached to a Frontier Labs double-shot pyrolyzer system. Outgassing species from the pyrolyzer were collected in a cold trap, cooled with liquid nitrogen and introduced into the GC-MS system for analysis. Time-of-flight secondary-ion mass spectroscopy (TOF-SIMS) was performed by an ION TOF-SIMS IV system. A pulsed primary ion beam of 15 keV $^{69}\text{Ga}^+$ was used for the TOF-SIMS analysis and positive ions were detected.

4.4 RESULTS AND DISCUSSION

4.4.1 Effects of Underlying Substrate on DUV Resist Contamination

In a copper/low- κ dielectric stack, the low- κ dielectric film is typically capped with a thin dielectric film. This layer can act as a copper diffusion barrier, a hard mask to prevent the etching of under-layers and as a protection layer for direct polishing of low- κ film during the chemical-mechanical polishing (CMP) process. A variety of dielectric capping layers were studied in this chapter.

After each process step in the VFDD process, the wafers were inspected in a CD SEM system. No resist residues were seen in the exposed area after via masking and etching process for all the wafers. However, after trench masking and resist development, the exposed pattern was not completely clear of resist as it should have been for a positive resist. The CD SEM top-view images of the various film stacks after trench masking and photoresist development are shown in Fig. 4.2.

Fig. 4.2 Top-view SEM micrographs of resist contamination in vias after trench patterning of base low- κ stack for schemes (a)-(e) (Table 4.1)

Resist residues were found in the via area after trench patterning for all combination of base stack with or without different capping layers as given in Table 4.1. The amount of the resist residues found was dependent on the type of capping layers used.

The smallest amount of resist residue was seen on the base low- κ SiOC stack without any capping layers. The largest amount of resist residue was seen on the film stack with a combination of SiC and SiON capping layers. Nitrogen was used as one of the gases for deposition of SiC and SiON films. It may have caused resist poisoning as nitrogen can form amines with hydrogen present in the film or after exposure to the environment. As explained in section 4.2, a minute catalytic amount of photoacid is formed at the exposed regions. This acid can be quenched by base impurities such as amines from the environment or substrate to deactivate the chemical-amplification process making DUV-resist insoluble.

SEM cross sections were analyzed to find the amount and shape of resist residues inside the vias. A greater amount of residue was observed in the via structure at the interface of SiOC and capping layers in comparison to the bulk of the etched SiOC film.

The cross section in Fig. 4.3 clearly shows resist residue remaining inside the via after trench patterning. Since the spin-coated resist was quite thick (~ 1000 nm) in order to fill the etched via in a trench lithography process, it was suspected that the DUV exposure dose used for trench patterning might not be sufficient to completely expose the thick

Fig. 4.3 Cross-section SEM micrographs of resist poisoning in vias observed after trench patterning on (a) base low- κ stack, (b) base stack + SiC (100 nm) and (c) base stack + SiO_xN_y (100 nm)

resist. However, experiments conducted with a large range of overexposure (~165%) and overdevelopment (~200%) failed to clear the resist residues.

4.4.2 Compositional Analysis of Dielectrics and Resist Residues

In order to better understand the results observed in Fig. 4.3, two more film stacks with low- κ SiOC:H and USG films were prepared as given in Table 4.2.

Table 4.2 USG and low- κ SiOC film stacks on a silicon substrate

Scheme ^a	1 st layer	2 nd layer	3 rd layer	4 th layer	5 th layer
1	USG (200 nm)	SiC (50 nm)	USG (1000 nm)	SiC (100 nm)	SiON (100 nm)
2	USG (200 nm)	SiC (50 nm)	SiOC:H (1000 nm)	SiC (100 nm)	SiON (100 nm)

a. The data in brackets indicates thickness of the dielectric film.

After trench patterning, resist residues were again seen in the via and on the sidewalls. The amount of resist residue did not change substantially for the two dielectric materials. The USG film stacks (Fig. 4.4) had almost the same amount of resist contamination as the low- κ SiOC film stack. Therefore, it can be concluded that low- κ

Fig. 4.4 Resist contamination on a USG dielectric film stack

material, and conventional USG dielectric stacks, are equally prone to resist contamination. In order to determine the elemental compositions of the resist residue relative to those of the surrounding dielectric material, resist residue in the via was analyzed by AES. Fig. 4.5 shows the structure of a typical sample (scheme 2 - Table 4.2). Four locations indicated in the figure by a + sign were analyzed: 1) via deposit, 2) dielectric area adjacent to the deposit, 3) via dielectric wall above the deposit, and 4) plug type residue.

Fig. 4.5 Cross-section SEM micrographs of via structure used for Auger analysis

Fig. 4.6 (a) and (b) shows the direct measured and differentiated Auger spectra for the sample respectively. The differentiated Auger spectra obtained from the sample was quantified using relative-sensitivity factors (RSF) supplied by the equipment vendor. The relative concentrations (in atomic percentages) of each element found are summarized in Table 4.3. Plugs, deposits, and via walls showed a very-high elemental composition of carbon, indicating that these are photoresist residues. Nitrogen, if any, could not be detected in the sample.

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Fig. 4.6 Direct measured and differentiated Auger spectra for resist poisoned SiOC sample

Table 4.3 Compositional results of sample after AES analysis

Element location	C (atomic %)	O (atomic %)	Si (atomic %)
Deposit	59.0	11.2	29.8
Area adjacent to deposit	39.3	16.7	44.0
Via wall	60.6	10.0	29.4
Plug	70.5	8.9	20.6

TEM-EELS analysis was performed on the two samples to determine if any elemental nitrogen was present in the areas sampled. Fig. 4.7 shows the TEM micrograph of the SiOC:H sample and the locations at which EELS analysis was performed for detecting the nitrogen. The EELS spectra of the structure are shown in Fig. 4.8. No nitrogen-characteristic peak at 401.6 eV was seen at any of the locations analyzed [172].

Fig. 4.7 TEM cross-section micrograph of SiOC film stack

Fig. 4.8 TEM EELS spectra of poisoned SiOC sample

In the literature, it has been reported that amine impurities in the ppb range can cause resist contamination [171]. Even though no nitrogen was detected in the dielectric films and resist residue after trench patterning, the apparent absence of nitrogen may not necessarily imply a base contamination-free process as the amount of nitrogen present in the dielectric stack could be simply below the detection limit of the analytical tools. Hence, there is a need for more-sensitive techniques for detecting the nitrogen which may have caused resist poisoning.

4.4.3 Effects of the Processes used for Forming DD Structures on Resist Contamination

A further experiment was devised to identify the processing conditions that could lead to the contamination of the DUV resist. Most of the standard processes used for dielectric, resist, and BARC etching use nitrogen as one of the processing or carrier gases. As nitrogen is suspected to be the main cause of resist contamination, an effort was made to investigate the effects of nitrogen-containing chemistry, as used in dielectric etching, resist/BARC stripping, and solvent cleaning processes on the resist contamination.

For this study, silicon wafers with 200 nm of USG, 50 nm of SiC and 850 nm of SiOC:H films were prepared. During via patterning, two different sets of recipes were used. One set of etch recipe was nitrogen free, while the other set had nitrogen as one of the process gases. Table 4.4 shows the two sets of recipes. To evaluate the impact of post via etching solvent cleaning process on resist contamination, two different conditions, with and without ST 250 solvent cleaning, were used after completion of via dielectric, resist, and BARC-etching processes. Four samples were studied altogether.

Table 4.4 Etch recipes used for BARC stripping, photoresist stripping and SiOC film etching

Process	Recipes without N ₂	Recipes with N ₂
BARC etch	Ar, O ₂	N ₂ , O ₂
SiOC etch	Ar, O ₂ , CHF ₃ and CF ₄	C ₄ F ₈ , Ar, O ₂ , N ₂ and CF ₄
Photoresist ashing	O ₂	He, N ₂

After the DD trench etching process, DUV resist contamination was evaluated by CD SEM inspection. The results showed that there is no obvious contamination of wafers processed with nitrogen free etching recipes and without a solvent-cleaning process. Some resist residues were observed on wafers processed with nitrogen containing etching recipes but without a solvent cleaning process. Large amount of resist contamination was found on wafers processed with nitrogen free etching recipes followed by a solvent cleaning process. The worst-case residues were observed on wafers processed with nitrogen containing etching recipes followed by a solvent cleaning process. The CD SEM top-view micrographs for the above four conditions are shown in Fig. 4.9. Similar results were seen with the use of another commercial cleaning solvent (NE14 from Ashland Chemicals) that is recommended for post-etching polymer-residue removal in a DD process. From our results, it seems that the solvent cleaning process has caused some contamination of the dielectric films or made dielectric more susceptible to environmental contamination. Therefore, a baking step was introduced to check if the contaminants introduced by the solvent-cleaning can be removed by baking. In this additional experiment, the wafers was baked at 325° C for 30 minutes on a hot plate after solvent-cleaning. This was followed by trench lithography. The patterning results after the bake are shown in Fig. 4.10. After

Fig. 4.9 CD SEM top-view micrographs of SiOC film stack after the trench patterning. The processing conditions are a) nitrogen free process chemistry without solvent cleaning, b) nitrogen containing process chemistry without solvent cleaning, c) nitrogen free process chemistry and solvent cleaning, and d) nitrogen containing process chemistry and solvent-cleaning

baking, no resist contamination was observed on the wafer. This implies that base molecular contaminants introduced in the film may have desorbed during high-temperature baking. Similar results were seen at a lower baking temperature of 205°C for 60 seconds. The baking experiment was repeated three times on three different days. The results consistently showed resist-poisoning-free vias.

It was suspected that the deionized (DI) water used for rinsing the wafers and/or the nitrogen used for the wafer-drying process, during the solvent cleaning process could have interacted to form amines leading to resist contamination. Therefore, one wafer was cleaned with DI water instead of the cleaning solvent and no baking was carried out after the cleaning process. No resist contamination was seen on this wafer after the DD-trench patterning. Therefore, it can be concluded that the moisture present during the wet-cleaning process does not cause any contamination.

Fig. 4.10 CD SEM top-view micrographs after the via patterning for wafers treated with solvent (a) 30-minutes baking at 325° C and (b) no baking

4.4.4 Chemical Analysis of Samples With and Without Solvent-Cleaning Process

The purpose of this analysis was to identify the contaminants causing DUV-resist contamination after the post-via etching solvent-cleaning process. The wafer samples with and without the solvent-cleaning process were analyzed by GC-MS for identification of contaminants. Fig. 4.11 shows the gas-chromatography spectrum for samples with and without cleaning at two different temperature ranges. The two samples analyzed at 60° C - 150° C did not show any major difference, except that for the samples cleaned with solvent, there is a relatively small increase in the amount of hydrocarbons of $C_{12} - C_{15}$ outgassing from the samples (Figure 4.11 (a)). The outgassing compounds were identified from their molecular mass spectrum and comparison against the library data base in the mass spectrometer. For the temperature range between 150° C -350° C, hydrocarbon intensity was found to have increased relative to 60° C -150° C baking. A small peak due to a very weak base 1,3-diazine or pyrimidine ($C_4H_4N_2$) with molecular weight of 80.089 was

Fig. 4.11 GC-MS spectra for the SiOC film stack with and without solvent-cleaning at two different temperature ranges of (a) 60-150°C and (b) 150-350°C. The GC peaks marked with B are due to column bleeding

detected for the sample treated with solvent (Figure 4.11 (b)). Pyrimidine has a boiling point of 123-124°C and it is a nitrogen-containing, single-ring, basic compound [173]. Although the intensity of the pyrimidine peak is very small, it is suspected that even a trace amount of pyrimidine could have neutralized the photoacid generated during the post-exposure bake of the DUV-resist.

An experiment was conducted to verify if pyrimidine could have caused resist contamination. Two wafers were prepared with a SiOC film stack. Both wafers were baked after the via solvent-cleaning step at 180°C for 15 minutes in N₂ atmosphere. Thereafter, one of the wafers was treated with 0.1 volume % of pyrimidine in a solution of isopropyl alcohol. The treatment consisted of spraying this pyrimidine solution on the

wafer, soaking the wafer for 5 seconds and spin drying the wafer in a spray processor. After trench lithography was performed, the wafers were inspected in a CD SEM for resist contamination. Fig. 4.12 shows the results of CD SEM inspection. DUV-resist contamination, in the via areas, showed up in the wafer treated with pyrimidine, while no contamination was observed on the wafer without pyrimidine treatment.

This experiment showed that pyrimidine can neutralize the photoacid generated in the DUV resist. As pyrimidine evaporates at 123-124° C, a high temperature baking at 205° C will outgas it from the dielectric stack. This explains why no substantial DUV resist contamination was observed on the wafer subjected to the high-temperature baking process after the solvent-cleaning (section 4.4.3, Fig. 4.9). As some contamination is also observed on the samples treated with nitrogen-containing recipes, it can be concluded that the use of nitrogen-free recipes and baking after the solvent-cleaning process can provide a solution to the problem of resist contamination.

Fig. 4.12 CD SEM top-view micrographs of via after trench patterning (a) no pyrimidine treatment and (b) pyrimidine treatment

4.4.5 Study of Dielectric Film Stack Contamination Using TOF-SIMS

In order to trace the pyrimidine in the solvent treated wafer, TOF-SIMS analysis was performed on two freshly prepared SiOC:H film stack samples with and without solvent cleaning. As shown in Fig. 4.13 (a), no significant amount of amines could be detected on both types of samples. TOF-SIMS analysis was also carried out on the two samples after leaving them in the wafer storage boxes for a week. The amount of amines detected on the sample which had gone through the cleaning process was found to have increased significantly as shown in Fig. 4.13 (b). However, there was no significant

Fig. 4.13 TOF-SIMS spectra of the SiOC samples with and without solvent-cleaning (a) same day and (b) one week after the cleaning process

increase in the surface amines for the sample which did not go through the cleaning process. The intensities of amines are normalized against the intensity of Si and the results of the two samples before and after cleaning are summarized in Table 4.5.

When the samples were left in the sample boxes, these samples were not exposed to any chemicals, nor were they in direct contact with any other surfaces. The gradual build-up of the amines on the sample surface can only be explained by airborne molecular contamination.

GC-MS analysis showed a small amount of hydrocarbons on the SiOC:H samples subjected to cleaning. These hydrocarbons on the dielectric can facilitate the gradual build-up of amines on the dielectric surface. Wafers which were not cleaned with the solvent were not affected by the storage conditions. Thus, it is important to minimize storage time of the wafers after the solvent cleaning process. A long storage time between the post via-etching solvent cleaning and DD trench patterning can lead to more resist poisoning for the DD process.

Table 4.5 Intensities of the amine fragments normalized to the intensity of silicon

	Range of intensities ^a			
	Freshly-prepared samples		After one week in wafer box	
	No cleaning	With cleaning	No cleaning	With cleaning
CH₄N (30)^b	0.92-0.99	0.99-1.02	0.59-0.76	7.77-8.28
C₂H₆N (44)	2.82-3.04	2.99-3.15	1.16-1.42	35.5-37.09
C₃H₈N (58)	5.85-6.12	5.88-6.07	2.12-2.50	84.73-92.94
C₄H₁₀N (72)	2.02-2.09	2.07-3.14	0.78-0.90	46.34-48.69

a. Each sample is analyzed three times and the range of intensities measured is presented here.

b. The data in brackets are the masses of the ion fragments.

4.5 SUMMARY

DUV resist contamination is a serious issue in the VFDD integration scheme for the fabrication of copper interconnects. Recognizing the severity of problem for nanoscale interconnects fabrication, a systematic investigation was carried out to identify its cause and to find a solution. This would enable patterning of interconnects down to 100 nm needed for subsequent study. DUV-resist contamination was observed on the dielectric film stacks after trench patterning. The study showed that there is no significant difference in DUV-resist contamination seen on low- κ SiOC:H dielectric and conventional PECVD-deposited USG films stacks. The amount of contaminated resist residue after DD trench patterning differs with various dielectric capping layers (SiC, USG, and SiON). SiON, which is used as dielectric anti-reflective layer and SiC capping layers showed maximum-resist poisoning at the interface between capping layer and underlying-dielectric stack. The cause of contamination was investigated. It was found that post via-etching solvent cleaning treatment can make dielectric stack more susceptible to amine contamination and induce resist contamination. The problem was resolved by a high-temperature baking step after the post via etching solvent cleaning process. It was also found that wafers treated with solvent are much more susceptible to amine contamination as compared to untreated wafers. Therefore, it is necessary to have a minimal delay between the post via-etching solvent cleaning and the high temperature baking process before trench-patterning in order to minimize resist contamination. It was observed that nitrogen-containing process chemistry used for dielectric, BARC, and resist-etching processes also induced some DUV-resist poisoning. However, the amount of poisoning was much less than the amount observed after the solvent cleaning.

Chapter 5

Etching and Barrier Metallization of Nanoporous Low- κ Dielectrics

5.1 INTRODUCTION

The patterning of damascene interconnects is not complete until lithographically defined patterns are etched to form interconnect vias and trenches. The etching of low- κ materials and in particular porous low- κ materials is not trivial as the plasma processes and etch chemistries that are used have a detrimental effect on the dielectric constant of the film. In a dual damascene process, plasma chemistries are employed for photoresist stripping, and etching of organic and inorganic low- κ /ULK dielectric films together with a suite of hard masks, etch stops and capping films. Plasmas are also used for removal of polymer residues and native copper oxide before the deposition of a barrier layer. Process interactions between the processing plasmas and low- κ dielectrics have been reported to degrade chemical composition and structure of dielectrics and increase the moisture uptake, surface roughness, κ value and leakage current [174-178].

In the ITRS roadmap (2006 update) a porous methyl-silsesquioxane (P-MSQ) with a κ value of 2 to 2.5 has been identified as a potential dielectric for back-end interconnects beyond the 45 nm technology node. Compared to dense low- κ dielectric such as organosilicate glass (SiOC:H), plasma effects are more severe for porous dielectrics because pores allow permeation of reactive chemical species into the material structure and degrade their thermal and mechanical properties [179-181]. This makes integration of

porous materials much more challenging as compared to dense low- κ materials. P-MSQ is one of the most promising ULK candidates available today. Therefore, we have chosen a P-MSQ with a κ value of ~ 2.2 to study the effect of plasma process interaction on the ULK dielectric properties.

MSQ belongs to a family of silsesquioxane based spin-on-glasses (SOGs) such as hydrogen silsesquioxane (HSQ), and hybrid organo siloxane polymer (HOSP) films. The low- κ property of silsesquioxane materials is due to the replacement of tetrahedral Si-O bonds in organosilicate (OSG) glass with low polarizability Si-R bonds where R is an organic functional group such as $-\text{CH}_3$. Due to the similarity of structure with SiO_2 , MSQ based dielectrics have good thermal stability, gap-filling capability, low moisture absorption, and process compatibility with conventional etching processes. The introduction of nanopores into these material helps in further reducing the κ values below 2.4 [182].

Several previous studies have been conducted to study the effect of various gas plasmas on the properties of low- κ and ULK films [183-201]. It has been reported that oxygen plasma that is typically used in a photoresist stripping process, increases the κ value of ‘carbon containing’ low- κ materials due to carbon depletion after plasma processing [183]. In reference [184], it is mentioned that densification of a thin top layer of porous ULK dielectric by ion bombardment helps in reducing carbon depletion. Researchers used a combined small angle x-ray scattering and specular x-ray reflectivity technique to characterize the mass density profile and pore size of a P-MSQ ULK material after subjecting it to an oxygen plasma treatment with significant ion bombardment. The results showed that a thin densified layer is formed rapidly at the surface region of the film

and that this densified layer protected the methyl groups in the rest of the layer from being further oxidized. Recently Xu et al. [202] studied various kinds of stripping plasmas and suggested optimized chemistry and process conditions for reducing dielectric damage. A pre-treatment with H_2 , He or NH_3 plasma, before stripping the resist in oxygen plasma, has been proposed to minimize the increase of the dielectric constant [186-190]. Alternatively, it is proposed to use a reducing plasma such as H_2/N_2 and H_2/He for photoresist stripping to avoid carbon depletion [191-195]. ULK damage is found to be greatly reduced by remote N_2 or H_2 discharges. However, resist stripping needs to be carried out at a high substrate temperature of 250°C or above to obtain a practical resist removal rate [195]. Post photoresist stripping treatments with hexamethyldisilazane (HMDS), ammonia (NH_3), trimethylchlorosilane (TMCS), trimethyldisilane (TMDs) and supercritical carbon-dioxide (CO_2) have been advocated to restore and stabilize the dielectric constant of low- κ /ULK materials [196-198, 203-204]. However, none of the above treatments is fully effective in reducing the detrimental effects of plasma etching.

Most studies on process interactions of plasmas have concentrated mainly on reducing damage to dielectrics caused by a plasma resist stripping process. The damage to a ULK material induced by a stripping plasma can be mitigated by devising a suitable process integration scheme so that direct contact of plasma with ULK material is avoided during the processing. One such scheme is the dual hard mask scheme that can effectively isolate the ULK dielectric from direct exposure to the resist stripping plasma [205]. However, damage caused by etching plasmas to the sidewalls or dielectrics underneath the etched structure cannot be mitigated by a hard mask integration scheme. Therefore, it becomes imperative to study how etching plasma will modify the properties of ULK

materials. There are reports on the effect of fluorocarbon etching plasma on ULK film properties [180, 198-200]. Researchers have suggested oxygen free fluorocarbon plasma to reduce plasma damage and to achieve in-situ sealing of pores by deposition of fluorocarbon polymers [201]. However this may cause difficulties in controlling the etched structure profile. Also fluorine in the fluorocarbon polymer may react adversely with barrier metals.

After plasma etching, copper barrier layer and seed layers need to be deposited in succession into the via/trench formed during the damascene process. Deposition of barrier films (metallic or dielectric) on ULK dielectrics is not straightforward. Porous ULK dielectrics have a relatively high surface roughness as compared to dense dielectrics and the roughness can be worsened by the etching process. The morphology of metallic barrier films deposited by a physical vapor deposition (PVD) process has been reported to follow the long range surface topography of the underlying porous dielectric film [208]. Connectivity of the pores in the ULK material also has a significant effect on the quality of deposited barrier films. For mesopores with mesoconnectivity, the pores of the substrate can act as a template and result in pores within a barrier layer and increase the sheet resistance of the film [208]. On the other hand, mesopores with microconnectivity do not give rise to this effect. It has been reported that even in the case of dense organic polymers, precursors for barrier metals such as WF_6 and NF_3 can easily diffuse through the free volume of the polymer [209]. This diffusion becomes worse with porous materials. Thus, proper sealing of the ULK dielectric prior to barrier layer deposition is absolutely necessary. Many organic [210-211] and inorganic dielectrics have been reported as a suitable pore sealing and Cu diffusion barrier layer for porous ULK materials [212-215].

To stop the diffusion of barrier metal precursors, a thin densified layer can be created by plasma treatment, sealing the surface of a low- κ polymer. However, this sealing property is reported to be lost at elevated temperatures ($> 300\text{ }^{\circ}\text{C}$) [209].

There are three main objectives in this study of process interaction of plasmas with ULK materials. Firstly, modifications to the surface and bulk properties of the P-MSQ due to etching and stripping plasmas are investigated. Secondly, the effect of a silicon carbon nitride (SiCN) pore sealing layer on the electrical properties of the P-MSQ is investigated. Lastly, the relationship between the morphology of the etched P-MSQ and the microstructure and electrical properties of Ta barrier metal is studied.

5.2 EXPERIMENTAL

LKD5109 (P-MSQ based ULK dielectric) from JSR Corporation was spin coated on two sets of 200 mm, (100) oriented, p-type silicon wafers using a TOK spin coater. This was followed by a curing step in N_2 ambient at 400°C for 30 minutes in a TEL vertical furnace (Alpha 8S-Z). The thickness and refractive index of the film at 632.8 nm were measured by a Thermawave Optiprobe 5240i spectroscopic ellipsometer. The wafers were subjected to a variety of plasma treatments as given in Table 5.1

H_2/He plasma treatment was performed in an Applied Materials Endura physical vapour deposition (PVD) system and all other plasma treatments were carried out in a TEL DRM reactive ion etching (RIE) system. Chemical bonding of the spin coated ULK films before and after plasma treatments was analyzed using a Biorad QS2200 ME Fourier transform infrared spectroscopy (FTIR) system. The dielectric constant, leakage current and breakdown voltages of the films were measured using a SSM 495 Hg probe CV/IV measurement system. Surface roughness of the film was measured using a Dimension 1500

Table 5.1 Plasma treatment conditions for P-MSQ processing

Process	Plasma Chemistry	Plasma Time (min.)	Etch rate of P-MSQ (nm/min.)
Experiment 1			
Stripping (Resist removal in an oxidizing environment)	O ₂	1	5.9
Stripping (Resist removal in a reducing environment)	H ₂ /N ₂	1	17.1
Stripping/Reactive pre-clean (Removal of Cu oxide, polymer residues & resist)	H ₂ /He	5	8.4
Etching (Etching organo-silicates and MSQ dielectrics)	C ₄ F ₈ /Ar//N ₂	1	96.3
Etching followed by Stripping	C ₄ F ₈ /Ar/N ₂ , H ₂ /He	1, 5	-
Experiment 2			
Etching followed by Stripping	C ₄ F ₈ /Ar/N ₂ , H ₂ /N ₂	0.5, 0.5	-
SiCN liner deposition (10nm & 20 nm)	3MS/He/NH ₃	0.11, 0.22	NA

atomic force microscope (AFM) and contact angle by a NRL goniometer. Surface morphology of the films was analyzed using a JEOL JSM6700F field emission scanning electron microscope (FE-SEM). X-ray photoelectron spectroscopy (XPS) analysis was performed in a VG ESCALAB 220i-XL system utilizing a monochromatic Al-K $_{\alpha}$ x-ray source. XPS depth profiling was achieved using an Ar⁺ ion beam sputtering at 3 keV and 1.0 μ A/cm² for 2 minutes. Secondary ion mass spectrometry (SIMS) depth profile analysis was performed using a CAMECA 6f system. A primary O₂⁺ ion beam with net impact energy of 10 keV and beam current of 50 nA was used. X-ray diffraction (XRD) measurements were carried out by a RIGAKU model RINT 2000 system.

In the first set of wafers (experiment 1), mainly prepared for investigating the effect of plasma treatments on the physical and chemical properties of P-MSQ, the targeted

deposition thickness of P-MSQ was 550 nm. Ta film (15 nm) was sputter deposited in an Applied Materials P5500 PVD system on P-MSQ coated wafers before and after plasma treatments. The deposition was carried out for 6 seconds at a chamber pressure of 1.9 mTorr with 2 kW of DC power and Ar gas flow of 30 sccm.

The second set of wafers (experiment 2) with 300 nm P-MSQ was prepared to evaluate the impact of etching and stripping on the electrical properties of P-MSQ material. In addition, two SiCN films of 10 nm and 20 nm thickness were deposited on two P-MSQ wafers by PECVD to study the effect of cap layers. Deposition was carried out in an Applied Materials Centura 5200 system using trimethylsilane (3MS), NH_3 and He at flow rates of 80, 160 and 200 sccm respectively at 350 °C, 300 W and chamber pressure of 3 Torr. The SiCN deposition rate at these conditions was about 3.1 nm/s.

5.3 RESULTS AND DISCUSSION

5.3.1 Surface Morphology Analysis

The SEM cross-sectional micrographs of the P-MSQ before and after different plasma treatments are shown in Fig. 5.1.

Fig. 5.1 SEM cross section of the untreated and plasma-treated samples: (a) no treatment, (b) O_2 , (c) H_2/N_2 , (d) H_2/He , (e) $\text{C}_4\text{F}_8/\text{Ar}/\text{N}_2$ and (f) $\text{C}_4\text{F}_8/\text{Ar}/\text{N}_2$ and H_2/He

There was no obvious surface damage to the ULK film after treatment with O_2 , H_2/He , and H_2/N_2 plasmas that are typically used for photoresist stripping in a damascene process. It was observed that the P-MSQ surface became very rough after partial etching in $C_4F_8/Ar/N_2$ plasma with opening up of pores and formation of micro-channels in the film as shown in Fig. 5.1(e). This was found to be more pronounced when the P-MSQ was subjected to an additional H_2/He strip plasma step after the etching plasma treatment (Fig 5.1(f)). The $C_4F_8/Ar/N_2$ etching plasma treatment also created a modified P-MSQ region with evident film damage up to a depth of about 165 nm as seen in Fig. 5.1 (f). This modified region with open pores and interconnected channels ($\sim 5\text{-}8$ nm wide) is the obvious result of plasma interactions with P-MSQ. This plasma damage could be due to a cumulative effect of bond scissioning and atomic rearrangements following bombardment by inert Ar atoms and reactive plasma radicals and ions in the plasma. The plasma damage seemed to be confined to a specific depth with partial breakdown of P-MSQ network structure. This indicates that penetration of reactive species is limited and it may depend on plasma processing conditions.

5.3.2 Chemical Bonding Analysis

Figure 5.2 shows the FTIR absorption spectra of the films before and after various plasmas treatments for experiment 1. For all the cases, intensity of both the $Si-CH_3$ stretching and rocking bonds at 778 cm^{-1} and 837 cm^{-1} were reduced after plasma treatment. The intensity was found to be the lowest for the sample treated with fluorocarbon etching followed by stripping plasma treatment. There was relatively small decrease in the $Si-CH_3$ bonds intensity after O_2 plasma treatment as compared to H_2/He and H_2/N_2 reducing chemistry treatment. This can be attributed to the relatively short O_2

Fig. 5.2 FTIR spectra of untreated and plasma treated P-MSQ films

plasma treatment time of 1 minute used in this experiment. The C-CH₃ asymmetric stretch at 2978 cm⁻¹ almost disappeared in the combined etching and stripping plasma treatments indicating a loss of carbon in the film structure. Peak intensity for the Si-O-Si cage structure at 1150 cm⁻¹ was found to be reduced after plasma treatment. This reduction of Si-O-Si cage structures and formation of dangling bonds after plasma treatment could lead to enhanced moisture absorption. This was evident from the broad spread at 3400 cm⁻¹, indicating the presence of silanol (Si-OH) bonds and H₂O for all plasma treatments except for H₂/He. This implies that H₂/He plasma is more capable of passivating the dangling bonds compared to other treatments. In all the cases, ratio of the peak intensity of Si-CH₃ (1270 cm⁻¹) to Si-O-Si (1057 cm⁻¹) bonds reduced after plasma treatments as compared to that of the untreated wafer (Table 5.2). This decrease is indicative of carbon loss in the

film. The maximum decrease was seen for the combination of etching and stripping plasma treatments (i.e. C_4F_8 followed by H_2/He).

Table 5.2 Ratio of peak intensities of Si-CH₃ (1270 cm⁻¹) to Si-O-Si network (1057 cm⁻¹) bonds

No treatment	O ₂ (1 min.)	H ₂ /N ₂ (1 min.)	H ₂ /He (5 min.)	C ₄ F ₈ /Ar/N ₂ (1 min.)	C ₄ F ₈ /Ar/N ₂ (1 min.) + H ₂ /He (5 min.)
1	0.79	0.76	0.64	0.72	0.44

5.3.3 Dielectric Constant Measurement

The dielectric constant of pristine P-MSQ was measured as 2.24. It increased to 2.53, 2.70, 2.69, 3.11, and 3.20 after O₂, H₂/He, H₂/N₂, C₄F₈ and C₄F₈+H₂/He plasma treatments respectively. This increase in dielectric constant is consistent with the loss of Si-CH₃ bonds, as seen from FTIR measurement for the corresponding plasma treatment. The increase in dielectric constant for H₂/N₂ and H₂/He plasma treatments is about the same. In this experiment, the treatment time for H₂/He plasma was five times longer (5 min.) than the H₂/N₂ treatment. Thus, dielectric constant increase normalized to plasma exposure time is higher for the H₂/N₂ plasma than the H₂/He plasma. This could be due to damage to the structure of P-MSQ caused by heavier nitrogen atoms and is evident from the almost doubling of the etching rate of the P-MSQ film (Table 5.1). An increase in the density of the O-H group at 3150-3560 cm⁻¹ was observed for the H₂/N₂ plasma treatment. Thus, it can be inferred that H₂/N₂ plasma makes P-MSQ more susceptible to moisture absorption. Overall carbon loss and corresponding increase in dielectric constant were

found to be much higher for etching (C_4F_8) plasma treatment as compared to stripping (H_2/He and H_2/N_2) plasma treatment.

5.3.4 XPS Analysis

Elemental analysis was carried out on the P-MSQ before and after plasma treatments to evaluate the effect of plasma on the atomic composition of the ULK film. Fig. 5.3 shows the XPS intensity vs. binding energy profiles for the analyzed films after 2 min. of Ar^+ sputtering. The XPS system was calibrated to etch SiO_2 at the rate of ~ 2.5 nm/min under the operating condition used for the analysis. The results of XPS analysis are tabulated in Table 5.3 and results showed depletion of carbon for all the plasma treatments at a depth corresponding to about 2 minutes of Ar^+ sputtering. Almost no signal was detected for C1s after the H_2/N_2 and C_4F_8 plasma treatments, indicating that carbon was

Fig. 5.3 XPS spectra of untreated and plasma treated P-MSQ films

almost completely depleted at the sputtered depth of the P-MSQ material. However, FTIR spectra analysis shown in Fig. 5.2 does not indicate a complete depletion of carbon. Therefore, carbon depletion is limited to a certain depth and the carbon composition beyond that may be unaffected. This finding is consistent with observations reported in [175].

Table 5.3 Elemental composition of P-MSQ analyzed using XPS

Plasma chemistry	No treatment	O ₂ (1 min.)	H ₂ /N ₂ (1 min.)	H ₂ /He (5 min.)	C ₄ F ₈ /Ar/N ₂ (1 min.)	C ₄ F ₈ /Ar/N ₂ (1 min.) + H ₂ /He (5 min.)
C (atomic %)	5.0	1.7	0.0	2.8	0.0	0.0
O (atomic %)	51.2	54.8	59.0	57.0	58.1	57.9
Si (atomic %)	43.8	43.5	41.0	40.2	41.9	40.8

5.3.5 Contact Angle Measurement

The hydrophobicity of the untreated and plasma treated ULK film was measured using water contact angle measurement at the film surface. The results are shown in Table 5.4.

Table 5.4 Contact angle measured on P-MSQ film

Plasma chemistry	No treatment	O ₂ (1 min.)	H ₂ /N ₂ (1 min.)	H ₂ /He (5 min.)	C ₄ F ₈ /Ar/N ₂ (1 min.)	C ₄ F ₈ /Ar/N ₂ (1 min.) + H ₂ /He (5 min.)
Contact angle °	90.0	24.3	32.5	34.0	90.0	25.5

The contact angle of a water droplet on top of a surface is a good indicator of its surface energy. A higher surface energy implies the presence of dangling bonds at the surface. A film having higher surface energy would have greater adhesion force which overcomes the surface tension of the water droplet. This would make the drop flatter or reduce the contact angle. In general, a hydrophilic surface has surface energy (lower contact angle) higher than that of a hydrophobic surface.

The untreated P-MSQ film was found to be hydrophobic with a contact angle close to 90° , indicating a low surface energy and the presence of stable terminating/functional groups in the bonding structure of the film. A hydrophobic surface is desirable as it has a lesser affinity towards moisture absorption, which can increase the κ value of a dielectric film. The contact angle decreased with stripping plasma treatment and this can be attributed to the breaking up of Si-CH₃ groups and the formation of silanol (SiOH) polar groups on the surface. It was found that the P-MSQ surface was hydrophobic after treatment with C₄F₈/Ar plasma. This could be due to the formation of a thin hydrophobic C_xF_y polymer film on the film surface after treatment by a fluorocarbon etching plasma. When the wafer treated with C₄F₈ etching plasma was further subjected to H₂/He stripping plasma, the contact angle reduced significantly. This implies that the thin C_xF_y polymer that was formed during fluorocarbon etch treatment was stripped off by the H₂/He plasma, thus making the surface more hydrophilic.

5.3.6 Leakage Current Density and Breakdown Field Measurements

The leakage current density and breakdown electric field were measured before and after plasma treatment on a second set of wafers (experiment 2). The results are shown in Fig. 5.4. The leakage current density of films exposed to C₄F₈ and H₂/N₂ plasmas

Fig. 5.4 Leakage current density (J) as a function of electric field (E) for untreated and plasma treated P-MSQ films (a) E vs. J (b) $\ln(J)$ vs. $E^{1/2}$ and (c) $\ln(J/E)$ vs. $E^{1/2}$

was found to be about five orders of magnitude higher than that of the untreated film at high electric fields (> 2 MV/cm). The breakdown electric field for the untreated P-MSQ was found to be ~ 4.04 MV/cm . This was reduced to ~ 3.26 MV/cm after plasma treatment.

As discussed in section 5.1, a thin dielectric layer can be used as a pore sealing and Cu diffusion barrier layer in ULK integration. Also the pore sealing dielectric needs to be denser than the porous dielectric to enable pore sealing. Therefore, its κ value would be higher compared to that of the P-MSQ. If a higher κ value pore sealing layer is used in the film stack, the effective dielectric constant of the combination of pore sealing layer and P-

MSQ would increase. Therefore, it is desirable to keep the pore sealing layer very thin in relation to the ULK dielectric to reduce the effective κ value of the film stack. In our study, SiCN layers with thickness 10 nm and 20 nm of were deposited on two wafers after subjecting them to etch and strip plasmas. A slight improvement in the leakage current density was seen for both the wafers at low electric fields (< 2 MV/cm). However at high electric field there was no significant improvement.

In order to better understand the mechanism of the leakage current in plasma etched P-MSQ, a quantitative analysis of the IV data was first carried out. For a non-porous low- κ dielectric, it has been reported that the conduction mechanism is Schottky emission (SE) at low electric field and Poole-Frenkel (PF) at high electric field [216-217]. SE conduction is due to thermionic emission across a metal-insulator interface. In the PF mechanism, conduction is due to field enhanced thermal excitation of trapped electrons into the conduction band of the insulator.

For the Schottky emission case, the relationship between the electric field, E and current density, J is given by the expression:

$$J = A^* T^2 \exp[-q(\phi_s - \beta_s \sqrt{E}) / k_B T] \quad (5.1)$$

where A^* is Richardson's constant, T is absolute temperature, $\beta_s = (q^3 / 4\pi\epsilon_0\epsilon)^{1/2}$, q is elementary charge, ϵ_0 is permittivity of free space, ϵ is high frequency relative dielectric constant, ϕ_s is the potential barrier between metal electrode Fermi level and bottom of the insulator conduction band and k_B is Boltzmann constant. For the Poole-Frenkel conduction, the current density, J is given by the expression:

$$J = \sigma_0 E \exp[-q(\phi_{PF} - \beta_{PF} \sqrt{E}) / k_B T] \quad (5.2)$$

where σ_0 is low field conductivity and $\beta_{PF} = (q^3 / \pi \epsilon_0 \epsilon)^{1/2}$ and ϕ_{PF} is barrier height of the trap potential well. To understand dielectric leakage mechanisms, $\ln(J)$ vs. $E^{1/2}$ for SE and $\ln(J/E)$ vs. $E^{1/2}$ for PF were plotted as shown in Fig. 5.4(b) and (c). The linear regions in the plots indicated a possibility of SE or PF conduction mechanisms with slopes equal to $\beta_s / k_B T$ and $\beta_{PF} / k_B T$ respectively in accordance with equations 5.1 and 5.2. The dielectric constant values assuming Schottky emission or Poole-Frenkel conduction mechanism were derived from the gradient of linear regions and are shown in Table 5.5 at

Table 5.5 κ - values before and after plasma treatments for P-MSQ derived from the gradient of linear regions of Fig. 5.4 (b) for Schottky emission and Fig. 5.4 (c) for Poole-Frenkel conduction

Plasma Treatment	Electric Field (MV/cm)	Derived κ - values	
		Schottky Emission	Poole-Frenkel Emission
Before treatment (P-MSQ)	Low field (<2)	15.52	627.11
	High Field (>2)	13.64	97.86
C ₄ F ₈ /Ar//N ₂ etch + H ₂ /He strip (P-MSQ)	Low field (<1.15)	5.01	107.27
	High Field (>1.6)	35.26	233.21
C ₄ F ₈ /Ar//N ₂ etch + H ₂ /He strip (P-MSQ +10 nm SiCN)	Low field (<0.88)	1.05	8.31
	Mid Field (0.88-2.27)	6.08	51.09
	High Field (>2.27)	37.43	Very high
C ₄ F ₈ /Ar//N ₂ etch + H ₂ /He strip (P-MSQ + 20 nm SiCN)	Low field (<0.88)	1.01	4.97
	Mid Field (0.88-2.27)	4.27	34.28
	High Field (>2.27)	37.42	Very high

low, mid and high electric fields. These extracted κ values, before and after plasma treatments, are either too high or too low in comparison to measured κ values as discussed in section 5.3.3. Therefore, it can be concluded that conduction in a porous MSQ dielectric before and after plasma treatments does not follow either a pure SE or pure PF conduction mechanism. For the untreated ULK sample, a poor fitting of the data with both SE and PF emission indicates a complex mode of conduction for the porous material which cannot be adequately described by the classical model of conduction for dielectric films with planar interfaces.

In section 5.3.1, it was observed that micro-channels are formed in the bulk of P-MSQ after etching plasma treatment. These micro-channels have a width of ~ 5 -8 nm and a depth of ~ 165 nm. It is possible that during the Hg probe IV measurement, Hg percolated into these channels causing enhanced leakage. It is to be noted that both the orientation and the aspect ratio of these channels favour field enhanced injection of carriers. In order to verify this hypothesis, further experiments were carried out with the deposition of Ta by PVD onto the P-MSQ material. Fig. 5.5 shows the SIMS depth profile of untreated and plasma treated ULK films after 15 nm Ta film deposition.

In the case of the untreated film, the Ta “peak” occurs at the Ta and P-MSQ interface and tapers off rapidly into the P-MSQ bulk material as seen in Fig. 5.5 (a). In Fig. 5.5 (b), the depletion of carbon after O_2 plasma treatment is evident at the interface of Ta and P-MSQ. However, the Ta depth profile remains unaffected. Thus, Ta diffusion in P-MSQ does not increase with O_2 plasma treatment. After C_4F_8 /Ar etching and H_2/N_2 stripping plasma treatments, there is considerable carbon depletion throughout the bulk of P-MSQ material as seen in Fig. 5.5 (c). Ta SIMS profile shows a large diffusion of Ta into

P-MSQ, until a certain depth. The increase in leakage current observed after the etching and stripping plasma treatments can thus be attributed to the penetration of Ta in P-MSQ. With the deposition of a thin (~ 10 nm) layer of SiCN as a pore sealing layer, carbon depletion and Ta diffusion were slightly reduced as seen in Fig. 5.5 (d). This also explains the slight reduction in leakage current observed at low electric fields for films capped with SiCN.

Fig. 5.5 SIMS depth profile of the untreated and plasma-treated samples with 15 nm of Ta deposition: (a) no treatment, (b) O_2 , (c) $C_4F_8/Ar/N_2$ and H_2/He strip, and (d) $C_4F_8/Ar/N_2$, H_2/He and 10 nm of SiCN film

5.3.7 Etch Process Optimization for Improved Leakage Current and Breakdown Voltage

A study was carried out to evaluate whether changes in etching plasma process conditions can reduce the leakage current and increase the breakdown voltage of the plasma treated P-MSQ dielectric. The plasma conditions used for etching of P-MSQ are given in Table 5.6. A lower RF bias power of 500 W was used in this experiment as compared to the RF bias power of 1 kW used in the leakage current study discussed in section 5.3.6. During the reactive ion etching process of an ULK dielectric using fluorocarbon chemistry, fluorocarbon deposition, fluorocarbon etching and ULK dielectric etching processes occur simultaneously. At very low RF bias i.e. low ion bombardment energy; these processes produce net fluorocarbon deposition. By increasing the RF bias power sufficiently, the etching process switches from etching of earlier deposited fluorocarbon film to the net etching of ULK dielectric. A high RF bias power leads to an immediate removal of any deposited fluorocarbon film during the etching, causing a rapid etching of the underlying ULK dielectric film by energetic ions and plasma species. This

Table 5.6 Plasma etching conditions for optimization of leakage current and breakdown voltage of P-MSQ material

Plasma condition	RF Bias Power (Watts)	Flow rate (sccm)		
		C ₄ F ₈	Ar	N ₂
Treatment 1	500	6	200	200
Treatment 2	500	6	100	100
Etching time =20 s Temperature= 40 °C Pressure=50 mT				

raises the possibility of significant damage to the ULK dielectric at high RF bias power. If RF bias power is reduced, fluorocarbon material that is deposited is removed at a slower rate. This reduces the direct high energy ion impact on the ULK film surface. Consequently damage to the ULK dielectric is expected to reduce, as a major part of ion energy and etch precursors will be used for the fluorocarbon etching.

Two different ratios of C_4F_8 gas flow rate to the total flow rate of C_4F_8 , Ar and N_2 were used in the experiment, while keeping C_4F_8 gas flow rate constant. The morphology of the structure was studied using AFM and SEM cross-sections. Leakage current and breakdown voltage measurements were carried out using a Hg probe CV/IV system.

The root mean square (rms) values of surface roughness for treatment 1 (dilute C_4F_8 plasma) and treatment 2 was found to be 0.485 nm and 0.631 nm respectively. This implies greater surface damage for treatment 2 as compared to treatment 1. The etch rates for treatment 1 and treatment 2 were 14.6 nm/s and 18.1 nm/s respectively. Micro-channels were formed in the P-MSQ material for treatment 2 (Fig. 5.6) but no such micro-

Fig. 5.6 SEM cross-section of the plasma treated P-MSQ samples (a) treatment 1 and (b) treatment 2

channels were formed after treatment 1. In Fig. 5.7, the leakage current and breakdown field for treatment 1 are much improved compared to treatment 2. The electrical data for the untreated sample is included as a reference. It is obvious the electrical characteristics have improved significantly with reduction in plasma power and flow rate ratio of C_4F_8 .

However the increase in breakdown voltage as compared to untreated sample also indicates that the film might have densified due to insufficient amount of reactive etch species (F atoms) available in the gas mixture and the bombardment by non-reactive ions and radicals may have resulted in the collapse of the network structure of the material. This densification of the film should also result in an increase in the dielectric constant. Thus there is a trade off between the two etch conditions with one leading to film densification at low F atoms concentration and the other causing excessive etching resulting in the formation of micro-channels. Clearly, the etch conditions need to be carefully optimized to minimize both the leakage current and degradation of dielectric constant of the P-MSQ film.

Fig. 5.7 Leakage current density (J) as a function of electric field (E) for untreated and etching plasmas treated P-MSQ films

5.3.8 Surface Roughness and Sheet Resistance of Ta Diffusion Barrier

The rms surface roughness of untreated and plasma treated ULK films were analyzed by AFM. No significant differences in surface roughness were observed for the stripping plasma treatment. For C_4F_8 /Ar etching plasma treatment, there was significant increase in the surface roughness as shown in Fig. 5.8. This increase in surface roughness is consistent with the earlier observation of SEM micrographs showing severe surface damage to P-MSQ after etching plasma treatment. A 15 nm thick film of Ta was sputtered on the treated and untreated P-MSQ. After Ta deposition, a significant increase in surface roughness of P-MSQ in the range of 1-3 nm was observed. The increase was the smallest for the untreated P-MSQ. A higher increase in the surface roughness with Ta deposition for the plasma treated film could be due to uneven percolation of Ta inside the P-MSQ, thus accentuating the surface roughness.

Fig. 5.8 Surface roughness of untreated and plasma treated P-MSQ films before and after Ta deposition

Resistivity values derived from the sheet resistance measurements of Ta films deposited on untreated and plasma treated P-MSQ is shown in Table 5.7. No significant change in the resistivity was observed for untreated and stripping plasma treated films. For C_4F_8 /Ar etch plasma, resistivity increased from 176 to 281 $\mu\Omega$ -cm. Since all the resistivity values were derived using the as-deposited thickness of Ta film on an untreated wafer, a possible reason for the increased resistivity could be the reduction in thickness of Ta film due to its permeation into the modified P-MSQ film after plasma treatment.

Table 5.7 Resistivity of Ta film deposited on P-MSQ before and after plasma treatments

Plasma chemistry	No treatment	O_2 Plasma (1 min.)	H_2/N_2 Plasma (1 min.)	H_2/He (5 min.)	C_4F_8 /Ar/ N_2 (1 min.)	C_4F_8 /Ar/ N_2 (1 min.) + H_2/He (5 min.)
Ta Resistivity ($\mu\Omega$-cm)	176.40	170.10	168.15	174.30	280.95	399.45

TEM cross- sections shown in Fig. 5.9 show the integrity of Ta films deposited on top of a pristine ULK film and ULK films subjected to various plasma treatments. Fig. 5.9(d) clearly shows severe permeation of Ta into the film through the micro-channels formed after etch plasma treatment. Thus, the effective Ta surface area is increased due to permeation into the P-MSQ. This would also lead to an increased surface scattering of electrons within the Ta film. Another possibility of an increase in the sheet resistance of Ta film deposited on plasma treated ULK film could be a change in the microstructure of the Ta film. This was further investigated using x-ray diffraction (XRD) measurements.

Fig. 5.9 Diffusion of Ta into the P-MSQ: (a) no treatment (b) after H_2/N_2 treatment (c) after H_2/He treatment and (d) after C_4F_8 etch plasma treatment

XRD analysis of Ta film deposited on untreated and plasma treated ULK films is shown in Fig. 5.10. The microstructure of Ta film deposited on samples before and after stripping plasma treatment was similar and show peaks at 2θ value of about 33.4° , 38.2° , 55.5° and 63.6° . XRD peak analysis using diffraction database indicates a β -Ta phase [218] for the as-deposited film. After C_4F_8 etching plasma treatment, a decrease in the intensity of β -Ta peaks was observed.

Based on the above observations, it can be inferred that Ta microstructure is surface roughness dependent and it becomes more amorphous with an increase in the surface roughness. The change in microstructure of Ta can affect its barrier properties [219] as well as the microstructure of sputter deposited copper seed film and the electroplated copper film [220].

Fig. 5.10 XRD spectra of Ta film deposited on untreated and plasma treated P-MSQ surfaces

5.4 Process Optimization and Fabrication of Interconnects for High Frequency Electrical Characterization

The ITRS 2006 [3] has identified engineering of manufacturable interconnect structures compatible with new low- κ materials and processes as one of the major (top three) challenges in interconnect technology. The successful fabrication of nanoscale interconnects is highly dependent on the integrity and robustness of various processes such as lithography, etching, metallization and CMP, as well as process integration scheme. In our earlier process optimization study, we have discussed process issues such as resist poisoning, reflectivity control of damascene film stack, and damage to ULK dielectric by plasma processes. DUV resist poisoning can deform the interconnect structure resulting in

an open circuit in the worst case. Alternatively, the shrinkage of nanoscale structures with poisoning can increase their resistivity due to scattering at the surface and grain boundaries. Plasma treatment can lead to increased dielectric constant and leakage current, and reduced breakdown voltage of a dielectric.

During the course of process development study, several issues were encountered due to non-optimization of fabrication processes. We show examples of some of these issues which can adversely impact the integrity and electrical properties of interconnects. Fig. 5.11 shows the TEM micrograph of the surface of an ULK film before and after C_4F_4 plasma etching. It is evident that nanopores which were mostly connected before the plasma treatment (Fig. 5.11 (a)), opened up to form nanochannels in the dielectric after the treatment (Fig. 5.11 (b)). Such damage can lead to increase in absorption of etch/clean precursors as well as moisture absorption by the ULK dielectric. This would lower

Fig. 5.11 Top surface TEM micrograph of ULK dielectric (a) as-deposited and (b) after C_4F_8 plasma treatment

the dielectric strength and increase the leakage current. This damage can only be reduced with optimization of etching process and protecting of ULK dielectric with a cap dielectric.

Fig. 5.12 shows the delamination of Ta layer at the Ta and Cu interface. This delamination was observed only when USG dielectric was replaced with ULK dielectric. ULK dielectric has a larger thermal coefficient of expansion (TCE) of ~ 17 ppm/ $^{\circ}\text{C}$ as compared to TCE of ~ 0.6 ppm/ $^{\circ}\text{C}$ for USG dielectric. The TCE of Ta barrier metal is ~ 6.3 ppm/ $^{\circ}\text{C}$. This mismatch in TCE of Ta and ULK dielectric and corresponding thermal stress might have caused an adhesion failure at Ta/Cu seed layer interface which appears as a weaker interface than Ta/ULK interface. The delamination of Ta barrier layer will result in increased leakage current and reduced breakdown voltage. The delamination issue was resolved after optimization of annealing temperature of electroplated copper films.

Subsequently, we investigated the electrical performance of on-chip interconnects over a wide range of dimensions suitable for intermediate and global signal/clock distribution on the chip using RF characterization tools. The representation of interconnect

Fig. 5.12 Delamination between Cu and Ta barrier film for the ULK interconnect

behavior at high frequency in terms of electrical circuit elements is strongly impacted by the physical and electrical properties of materials used for fabrication of interconnects. For example, a leaky dielectric cannot be represented by a pure capacitive element alone. Therefore, in order to find a good correlation between the modeled and experimental results, it becomes imperative to fabricate interconnects with minimum variations in their physical dimensions and electrical properties caused by fabrication process. The results of our process optimization study helped us in fabricating the interconnects which are suitable and ready for RF characterization and model development.

Though it would have been very useful to study the impact of non-optimized processes on the electrical behaviour of interconnects, it was not possible to carry out a full study due to resource constraints. However, many critical issues that can potentially affect the electrical properties of interconnects were studied. For example, the increase in dielectric constant due to plasma processing has been studied in section 3.3. Subsequently the effect of increased dielectric constant on the crosstalk is discussed in Chapter 8. The effect of cap dielectric in improving electrical leakage current and breakdown voltage was studied in section 5.3.6. The etch process was developed to further improve leakage current and breakdown voltage as discussed in section 5.3.7. The optimized process was, therefore, used to fabricate a wide range of interconnects with line widths ranging from 100 nm to 8 μm , representing intermediate and global interconnects for future technology nodes.

5.5 SUMMARY

The patterning of nano-interconnect using porous dielectrics is quite challenging due to interaction of the process plasmas with the dielectric material. It results in changes

in the dielectric chemical composition, structure, mechanical, thermal and electrical properties. In this study, the effect of different plasma treatments (O_2 , H_2/N_2 , C_4F_8 and H_2/He) on the properties of a porous ULK dielectric (P-MSQ) was studied. It was found that surface roughness, wet-ability, dielectric constant, chemical bonding and elemental composition of the P-MSQ varies with the type of plasma gas chemistry. In particular surface roughness of the film was found to have significantly increased when subjected to fluorocarbon etching plasma. Dielectric constant of the P-MSQ film increased for all of the plasma treatments used in this study. This damage to dielectric structure was also evident from the loss of $C-CH_3$ bonds and depletion of carbon in the ULK dielectric film after plasma treatment.

The microstructure of Ta film deposited on the plasma treated samples was found to be influenced by the surface roughness of the original film. Samples treated with fluorocarbon plasma showed an increased roughness and a relatively amorphous microstructure as compared to samples treated with non-fluorine based plasma. P-MSQ films exposed to etching and stripping plasmas showed a high leakage current density and a low electrical breakdown field as compared to an untreated P-MSQ film. The addition of a thin SiCN layer, used as pore sealing layer, on the etched P-MSQ film did not improve leakage current density at high electric field.

Chapter 6

High Frequency Electrical Characterization and Wide Band Model

6.1 INTRODUCTION

In chapters 2-5, we discussed the technology issues related to the fabrication of nanoscale copper interconnects using damascene technology. Problems related to lithography were resolved and a study was carried out to evaluate the damage inflicted on the low- κ /ULK dielectric during etching. In this chapter, we will study the propagation behaviour of the copper interconnects with width down to 100 nm and develop accurate models and experimental methodologies for the characterization of their high frequency behaviour.

Silicon-based CMOS is currently the most cost-effective technology for the development of advanced radio frequency (RF) and mixed-signal integrated circuits. CMOS technology has the possibility of achieving higher chip integration with RF front-end and digital/analog baseband. It is specifically advantageous for low-power active devices with high transition frequencies. Moreover, it is capable of low-cost high volume manufacturing for mixed signal/RF systems [221, 222]. With increase in the operating frequency of ICs, a fundamental and dominant requirement is to develop accurate and scalable model of the on-chip interconnects for different applications over a very wide frequency range, such as 3.1~10.6 GHz ultra-wideband (UWB) systems, 60 GHz RF systems and 77 GHz radar systems.

At GHz range frequency, inductance effect becomes dominant over the resistive behaviour of interconnects. Thus, with scaling of ICs into the sub-100 nm regime, and inductance assuming prominence at high frequency, a RLC representation of interconnects has become necessary to accurately model the behaviour of interconnects [62- 68, 223].

Kopcsay et al. [224] have shown that at high frequency, global interconnects may be modeled as transmission lines with power, signal and ground lines acting as a current return path. Interconnects as transmission lines have been studied extensively in the literature. In 1971, Hasegawa published his classical paper defining three fundamental modes of signal propagation based on silicon substrate resistivity and frequency of operation [73]. In the literature, full wave [74-75] or quasistatic electromagnetic [76-77] approaches have been used for the characterization of transmission line parameters. However these techniques require extensive computational resources and are not viable for computer aided design of high density ICs. Closed form expressions have also been proposed for the characterization of frequency dependent line parameters of single and coupled transmission lines which allow faster designs and design scalability of ICs [78-83]. Though the accuracy of closed form expressions does not always match the real chip environment, they do provide fairly close estimates of interconnect parasitics. Accurate values of these parasitics can then be obtained from test structures emulating real chip environment.

In the literature, models ranging from simple first order linear models to complex moment matching models such as asymptotic waveform evaluation (AWE) have been proposed [225]. However, all the models or closed form analytical expressions need to be verified by simulations and experiments. There are significant process variations in the

damascene fabrication process due to non-uniformities of lithography, etching and deposition processes. The pattern density variations within a chip also cause variations in the CD of the patterned structure and the thickness of films after the CMP process. The experimental approach to modeling and characterization should take care of process variations in the fabrication process. Another area of concern is higher-order effects that are difficult to model. One example is inductance; it is very difficult to predict the inductance value due to multiple current return paths that are possible for on-chip interconnects. Inductance arises from time varying currents along a path that leads to the generation of magnetic field. The magnetic flux is proportional to the area of the current loop. Since there are no clear return paths for the current, ground, power lines and silicon substrate serve as current return paths. Even the signal lines in the vicinity may act as AC grounds. Due to these multiple current return paths, it is very difficult to accurately predict the inductance effect during modeling. The partial equivalent element circuit approach has been proposed to overcome difficulties in the identification of inductance loops [224, 83, 25-26]. However these models require a huge number of circuit elements and complex inductance matrix, requiring substantial computation resources.

It is, therefore, vital to characterize the interconnect performance by experimentation in order to provide accurate information to designers for a successful chip design. In the literature, measurement based circuit models have been reported with frequency-dependent and frequency-independent model parameters [228-231]. However, there is very limited information available on the experimental characterization of nanoscale interconnects. Reports on propagation behaviour of nanoscale copper interconnects with low- κ /ULK materials in particular are lacking [93, 232-233]. We are,

therefore, motivated to develop an accurate interconnect model that is useful for circuit design and validate it by experiments.

In this chapter, we first characterize the high frequency electrical behaviour of copper interconnects modeled as lossy transmission lines using S-parameter measurement technique. S-parameter measurement technique is well established for characterization of interconnect parasitics. It provides a sound methodology for extraction of characteristic impedance and frequency dependent line parameters [228, 234-235]. A transmission line can be characterized by the generalized Telegrapher's equations with a series impedance $R(\omega) + j\omega L(\omega)$ and a shunt admittance $G(\omega) + j\omega C(\omega)$, where $R(\omega)$, $L(\omega)$, $G(\omega)$ and $C(\omega)$ are the per unit length (p.u.l) frequency-dependent distributed resistance, inductance, conductance, and capacitance respectively. We used Telegrapher's model to extract the frequency variant parameters for copper interconnects with various line widths and line lengths [228]. Thereafter, we analyzed the cross-over frequency at which inductance starts to play a dominant role. Furthermore, we developed a fully lumped element model for the wideband on-chip interconnects and verified its scalability for line-length up to 8000 μm and line width down to 100 nm. The advantage of lumped circuit representation is the frequency independence of RLGC parameters under a given geometrical and material constraint. We show that both the series and shunt elements of this model can be determined based on the frequency asymptotic technique without any optimization. The equivalent lumped circuit is used to derive the values of frequency-dependent RLGC parameters up to 40 GHz. Electromagnetic (EM) simulations were performed separately to verify the wide-band lumped model and its accuracy. The model is validated up to 40 GHz by a good agreement between the simulated and measured S-parameters. The obtained

lumped elements can be directly used in SPICE-compatible simulation of RF integrated circuits.

6.2 MODES OF TRANSMISSION ON A SEMICONDUCTOR SUBSTRATE

In 1971, Hasegawa et al. [73] described the three fundamental modes of signal propagation of a transmission line on a semiconductor substrate. The three modes, i.e. dielectric quasi TEM mode, skin-effect mode and slow-wave mode are classified based on substrate conductivity and frequency. Hasegawa analyzed the high frequency signal transmission with SiO₂ as dielectric on a silicon substrate using a microstrip model as shown in Fig. 6.1. The longitudinal and transverse propagation constants of the wave should satisfy the following relations required by the wave equation:

$$\gamma_i^2 + \gamma^2 = -\omega^2 \epsilon_i^* \mu_i^*, \quad i = 1, 2 \quad (6.1)$$

where γ_1 and γ_2 are the transverse propagation constant in the SiO₂ and Si layer respectively, and γ is the longitudinal component. $\epsilon_i^* = \epsilon_i' - j\epsilon_i''$ and $\mu_i^* = \mu_i' - j\mu_i''$

Fig. 6.1 Model of a microstrip line on a Si-SiO₂ system

denote the complex permittivity and permeability of each layer, respectively. Also, by application of transverse resonance method:

$$\sum_{i=1}^2 Z_i \tanh(\gamma_i b_i) = 0 \quad (6.2)$$

where $Z_i = \gamma_i / j\omega\epsilon_i^*$ and b_i is the thickness of each layer with $i = 1$ for the SiO₂ layer and $i = 2$ for silicon substrate.

Using the Maxwell field equations, the electric and magnetic field components in each layer can be expressed as:

$$E_{yi} = \mp \frac{\gamma}{\gamma_i} \cdot E_{z0} \cdot \frac{\cosh[\gamma_i(y \mp b_i)]}{\sinh(\gamma_i b_i)} \cdot e^{-\gamma z} \quad (6.3)$$

$$H_{zi} = \mp \frac{j\omega\epsilon_i^*}{\gamma_i} \cdot E_{z0} \cdot \frac{\cosh[\gamma_i(y \mp b_i)]}{\sinh(\gamma_i b_i)} \cdot e^{-\gamma z} \quad (6.4)$$

$$E_{si} = \mp E_{z0} \cdot \frac{\sinh[\gamma_i(y \mp b_i)]}{\sinh(\gamma_i b_i)} \cdot e^{-\gamma z} \quad (6.5)$$

Where negative sign and positive sign are applicable for $i = 1$ and 2 respectively. Also

$$E_{z0} = E_z | z = 0, y = 0.$$

At low conductivity, if the frequency becomes greater than the dielectric relaxation frequency of the semiconductor substrate, then the substrate behaves as a dielectric. This fundamental mode is known as the quasi TEM mode. If the frequency is decreased or conductivity is increased, then the substrate would behave as a metallic sheet. This mode is known as the slow-wave mode. In this case, for $b_1 \ll b_2$, a strong interfacial polarization occurs and the propagation velocity slows down. However, at high substrate conductivity and high frequency, the thickness of the silicon becomes greater than the skin depth of the

substrate. Under these circumstances, the substrate behaves like a lossy conductor wall or as an imperfect ground plane made of silicon. This mode is known as the skin-effect mode. The various characteristic frequencies of the different modes are summarized in Table 6.1.

Table 6.1 Characteristic frequencies for fundamental modes of signal propagation [13]

Dielectric relaxation frequency of Si-layer	$f_e = \frac{1}{2\pi} \cdot \frac{\sigma_2}{\epsilon_0 \epsilon_{si}}$
Relaxation frequency of interfacial polarization	$f_s = \frac{1}{2\pi} \cdot \frac{\sigma_2}{\epsilon_0 \epsilon_{SiO_2}} \frac{b_1}{b_2}$
Skin effect mode	$f_\delta = \frac{1}{2\pi} \cdot \frac{2}{\mu_0 \sigma_2 b_2^2}$
Slow-wave mode	$f_0 = \left[f_s^{-1} + \frac{2}{3} f_\delta^{-1} \right]^{-1}$

A frequency-resistivity domain chart is obtained from these characteristic frequencies as shown in Fig. 6.2. The chart is plotted for an oxide thickness of 10 μm and a silicon thickness of 750 μm . This oxide thickness is chosen to represent an equivalent thickness of ULK dielectric underneath the top metal layer for a 13 metal layers film stack with ULK dielectrics as predicted by the ITRS in the year 2013. The average thickness of metal layer is assumed to be 200 nm for local, intermediate and global wiring levels. Assuming an aspect ratio of one for the metal and via layers, the total thickness of the ULK film stack for 13 metal layers would be about 5.2 μm . This would correspond to an equivalent oxide thickness of $\sim 9.7 \mu\text{m}$, assuming a κ -value of ULK dielectric equal to 2.2.

Therefore, a 10 μm thick oxide has been chosen for plotting of frequency-domain charts and for the fabrication of test structures used in this study. In our experiments the resistivity of silicon was in the range 1-20 $\Omega\text{-cm}$ and the frequency range was 50 MHz to 40 GHz. This region is marked as “measured region” on the chart. It can be observed that for the frequency and resistivity range typically used in ICs, slow-wave mode would be dominant at low frequency and then it will change into the quasi TEM mode. For a resistivity of 1 $\Omega\text{-cm}$, the characteristic slow-wave and dielectric relaxation frequencies are 3.13 GHz and 151 GHz respectively.

Fig. 6.2 Resistivity–frequency domain chart for quasi TEM, skin-effect and slow-wave modes

The slow-wave and dielectric relaxation frequencies decrease to 0.3 GHz and 7.55 GHz respectively for a silicon resistivity of 20 $\Omega\text{-cm}$.

If the dielectric thickness is lowered, the transition region between the slow-wave and quasi-TEM mode expands and the converse is true when the thickness of dielectric is increased. For a dielectric thickness of 10 μm , we see a smooth transition from slow-wave to quasi-TEM mode over the range of frequency and substrate conductivity used in this experiment. This does not hold true for a very thin or very thick dielectric on silicon substrate. In case of a thin dielectric, propagation characteristics will show a continuous dispersion due to the presence of a large transition region. For a thick dielectric, the wave propagation velocity is expected to change abruptly from a very low velocity corresponding to a slow-wave mode to almost constant high velocity in quasi-TEM mode. The lumped element equivalent circuit of each mode is shown in Fig. 6.3 [73].

Fig. 6.3 Equivalent circuit of the (a) slow-wave mode, (b) dielectric quasi TEM mode and (c) skin-effect mode

6.3 FABRICATION OF TRANSMISSION LINE TEST STRUCTURE

A set of ground surrounded, micro-strip transmission line test structures, was designed with line width ranging from 0.10 μm to 8 μm and line length ranging from 0.5 mm to 8 mm (Table 6.2). The ITRS roadmap envisages a wiring pitch of global interconnects to be about 96 nm in the year 2013 for minimum scaled features. However,

Table 6.2 Line widths and line-lengths used for the transmission line test structure

Line widths, w (μm)	0.10, 0.15, 0.25, 0.5, 1, 2, 4 and 8
Line Lengths, l (μm)	500, 1000, 2000, 4000 and 8000

the wiring pitch for global interconnects is expected to be larger than predicted by the ITRS. The semiconductor industry has been implementing reverse scaling for global interconnects and this is expected to continue. The reverse scaling approach relieves the pressure on the circuit designers to tighten the wiring pitch continuously. With reverse scaling, interconnect resistance is reduced by an increase in cross-section area and line to line capacitance is reduced with the increase in the wiring pitch. Therefore, interconnect width and pitch at the global level is expected to be larger than the minimum scaled dimension predicted by ITRS.

A photomask with alternating phase shifted sub-resolution assist features as described in chapter 2 was designed using Cadence layout tools. The photomask with in-phase and out of phase feature defined by glass etching was fabricated by Hoya Corporation. The copper interconnect test structures were fabricated on a 200 mm, (100), 1-20 ohm-cm p-type Si-substrate using a single damascene process. Both conventional USG and ULK P-MSQ (JSR Chemicals- LKD5109) dielectrics were used. Fig. 6.4 shows the plan view of the test structure. The schematic cross section of the test structure and cross-sectional TEM micrographs of the 100 nm nominal width structure are shown in Fig. 6.5.

The test structure dimensions were chosen so that it is possible to characterize interconnect lines electrically through S-parameter measurements. The pad sizes of $70\text{ }\mu\text{m}$ x $70\text{ }\mu\text{m}$ with a pitch of $100\text{ }\mu\text{m}$ were determined based on the GSG (ground-signal-ground) probe dimensions. The ground lines were kept at a sufficiently large

Fig. 6.4 Schematic representation of ground surrounded micro-strip line test structure

Fig. 6.5 (a) Schematic representation and (b) TEM cross section of Cu/USG ground surrounded microstrip line test structure, and (c) Schematic cross-section and (d) TEM cross section of Cu/ULK ground surrounded microstrip line test structure

distance (~ 7 times) as compared to distance from the substrate in order to suppress the excitation of CPW modes. The width of $50\text{ }\mu\text{m}$ for the ground bars was chosen to provide a lossless ground for the grounding probes used in S-parameter measurements. The line widths in the range 100 nm to $8\text{ }\mu\text{m}$ and line lengths from $500\text{ }\mu\text{m}$ to 8 mm were chosen to represent the typical length of interconnects at intermediate and global levels [68]. In [236] the researchers have chosen 1 mm length to reflect a typical global interconnect length while the 1 cm length was meant to represent the longest on die interconnect for the 45 nm technology node.

All dielectric layers except the P-MSQ were deposited in a Novellus Sequel Express PECVD system. The P-MSQ was spin coated in a TR8362SD-UV TOK system followed by a thermal cure in a TEL Alpha 8S-Z vertical furnace at 400°C in N_2 environment for 30 minutes. A 50 nm thick SiC layer was used as a CMP etch stop layer to prevent direct polishing of the ULK material. A 248 nm Nikon S208 step and scan system was used for patterning of test structures using a PSM mask with alternating assist features for resolving trench structures less than 150 nm . All dielectrics were etched in a TEL DRM RIE system using C_4F_8 , Ar and N_2 plasma chemistry. In-situ resist stripping was carried out using H_2/He chemistry.

Ta barrier (15 nm) and Cu seed layer (50 nm) were sputter deposited in a physical vapor deposition (PVD) system. About 500 nm thick copper was deposited by electroplating. The electroplated copper film was subsequently annealed in a furnace at 200°C for 30 minutes in forming gas. CMP of copper overburden was carried out to define the embedded interconnect lines. A passivation layer of SiN (50 nm) and USG (300 nm) was deposited on the structure followed by pad structure aluminum metallization to

facilitate probing. The wafers were finally alloyed at a temperature of 350 °C for 30 minutes in forming gas.

Two port on-wafer S-parameter measurements were carried out using Cascade Microtech Infinity probes, and Agilent's 8510C Vector Network Analyzer (VNA) over a frequency range from 50 MHz to 40 GHz, using line-reflect-reflect-match (LRRM) technique for calibration. The measurements were carried out on a SUMMIT 9000 analytical probe station. The measurement set up is shown in Fig. 6.6. The measured data was de-embedded by subtracting open-dummy pad admittances (Y-parameters) from the admittance of the test structures. Signal propagation in the transmission line was modeled by the Telegrapher's equation and the methodology reported in [228, 235, 237] was used to extract the frequency dependent transmission line parameters.

Fig. 6.6 Measurement set up for 2-port S-parameters characterization

6.4 S-PARAMETER ANALYSIS FOR FREQUENCY DEPENDENT TRANSMISSION LINE PARAMETER EXTRACTION

A transmission line can be schematically represented as a two wire system where R , L , G and C are per unit length (p.u.l.) series resistance, series inductance, shunt conductance and shunt capacitance of the line respectively [238]. A finite length of transmission line can be viewed as a cascade of sections of the form shown in Fig. 6.7. Using Kirchhoff's voltage and current laws, the time domain form of transmission line can be represented as:

Fig. 6.7 Lumped element equivalent circuit of a transmission line

$$\frac{\partial v(z, t)}{\partial(z)} = -Ri(z, t) - L \frac{\partial i(z, t)}{\partial(t)} \quad (6.6)$$

$$\frac{\partial i(z, t)}{\partial(z)} = -Gv(z, t) - C \frac{\partial v(z, t)}{\partial(t)} \quad (6.7)$$

Equations (6.6) and (6.7) are known as the Telegrapher's equations.

For a sinusoidal steady state condition, the equations can be represented as:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \quad (6.8)$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \quad (6.9)$$

Equations (6.8) and (6.9) can be solved simultaneously for $V(z)$ and $I(z)$ as:

$$\frac{d^2 V(z)}{dz^2} - \gamma^2 V(z) = 0 \quad (6.10)$$

$$\frac{d^2 I(z)}{dz^2} - \gamma^2 I(z) = 0 \quad (6.11)$$

where γ is the complex propagation constant defined as:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (6.12)$$

The real and imaginary parts of γ , namely α and β are known as attenuation constant and phase constant of the transmission line respectively.

Using convention $z = 0$ at the load end, the solution to equation 6.11 and 6.12 can be expressed as a sum of incident and reflected voltage waves.

$$V(z) = V_o^+ e^{-(\gamma z)} + V_o^- e^{(\gamma z)} \quad (6.13)$$

$$I(z) = I_o^+ e^{-(\gamma z)} + I_o^- e^{(\gamma z)} \quad (6.14)$$

Equations (6.8) and (6.13) yields:

$$I(z) = \frac{\gamma}{R + j\omega L} \left[V_o^+ e^{-(\gamma z)} - V_o^- e^{(\gamma z)} \right] \quad (6.15)$$

Combining equations 6.12 to 6.15, the characteristic impedance (Z) of the line is given as:

$$Z = \frac{V_o^+}{I_o^+} = \frac{-V_o^-}{I_o^-} = \frac{(R + j\omega L)}{\gamma} = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}} \quad (6.16)$$

The transmission line p.u.l. parameters can be determined from the following relationships.

$$R = \text{Re}(\gamma Z) \quad (6.17)$$

$$L = \frac{\text{Im}(\gamma Z)}{\omega} \quad (6.18)$$

$$G = \operatorname{Re}\left(\frac{\gamma}{Z}\right) \quad (6.19)$$

$$C = \frac{\operatorname{Im}\left(\frac{\gamma}{Z}\right)}{\omega} \quad (6.20)$$

The frequency dependent p.u.l. distributed line parameters $R(\omega)$, $L(\omega)$, $G(\omega)$ and $C(\omega)$ can be extracted from the characteristic impedance $Z(\omega)$ and propagation constant $\gamma(\omega)$ of the transmission line. $Z(\omega)$ and $\gamma(\omega)$ can be obtained experimentally by the following methodology.

If we consider the source and load impedances as Z_0 , then the S-parameter matrix for a lossy unmatched transmission line of length l can be expressed as [238]:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{D_s} \begin{bmatrix} (Z^2 - Z_0^2) \sinh \gamma l & 2ZZ_0 \\ 2ZZ_0 & (Z^2 - Z_0^2) \sinh \gamma l \end{bmatrix} \quad (6.21)$$

where:

$$D_s = 2ZZ_0 \cosh \gamma l + (Z^2 + Z_0^2) \sinh \gamma l \quad (6.22)$$

The ABCD matrix and S-parameters are related as [238]

$$A = (1 + S_{11} - S_{22} - \Delta S) / 2S_{21} \quad (6.23)$$

$$B = (1 + S_{11} + S_{22} + \Delta S) Z_0 / 2S_{21} \quad (6.24)$$

$$C = (1 - S_{11} - S_{22} + \Delta S) / 2S_{21} Z_0 \quad (6.25)$$

$$D = (1 - S_{11} + S_{22} - \Delta S) / 2S_{21} \quad (6.26)$$

Where:

$$\Delta S = S_{11}S_{22} - S_{21}S_{12} \quad (6.27)$$

The S-parameter matrix can be converted to ABCD parameters to derive the values of Z and γ . This derivation makes use of the fact that ABCD parameters of a cascade of two linear systems are the product of ABCD parameters of individual systems.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh \gamma l & Z \sinh \gamma l \\ \frac{\sinh \gamma l}{Z} & \cosh \gamma l \end{bmatrix} \quad (6.28)$$

Combining equations 6.23 – 6.28 yields

$$e^{-\gamma l} = \left[\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm \left[\frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2} \right] \right]^{-1} \quad (6.29)$$

$$\text{and } Z = \left(Z_0^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2} \right)^{1/2} \quad (6.30)$$

Once γ and Z are determined from S-parameters, the transmission line p.u.l. parameters $R(\omega)$, $L(\omega)$, $G(\omega)$ and $C(\omega)$ can be derived from equations 6.17 to 6.20.

6.4.1 Propagation Characteristics and Frequency Dependency of *RLGC* Parameters

As discussed in section 6.2, Hasegawa et al. [73] have identified (i) skin effect mode, (ii) slow-wave mode, and (iii) quasi dielectric transverse electromagnetic (TEM) mode of propagation of a microstrip transmission line depending upon the frequency and resistivity of the substrate. The skin-effect mode is observed at a high signal frequency and low substrate resistivity. In this mode, the line behaves dispersively due to the skin effect in the substrate. In the slow-wave mode, the signal frequency is relatively low and substrate resistivity is moderate. The quasi TEM mode is dominant when both the signal frequency and resistivity of the guiding medium are high. Quasi TEM is the preferred

mode of propagation as in this mode phase velocity and impedance of the transmission line remain constant, thus minimizing signal dispersion and impedance mismatch.

The values of γ and Z of the transmission line were derived from S-parameter measurements of transmission line test structures with various width and lengths as shown in Table 6.2. Results are shown only for 0.5 and 1 mm line lengths. Results for longer lines were found to be similar.

(a) Attenuation Constant (α) and Phase Constant (β)

Fig. 6.8 shows the values of α as a function of frequency for 0.5 mm and 1 mm long Cu/USG lines. The α values increases with frequency and is also inversely proportional to the line width. This increase in α with decreasing line width may be attributed to high resistive loss with reduction in cross-section of the lines. For line width greater than 0.25 μm , α is almost constant at frequencies above 15 GHz. This implies that above a certain frequency, attenuation saturates for a specific line width. It is also found that this

Fig. 6.8 Attenuation constant α as a function of frequency for line length (a) 0.5 mm and (b) 1 mm

frequency reduces with the increase in line width. Wider lines, therefore, show less frequency dependent attenuation.

The results for β shown in Fig. 6.9 indicate a linear increase with frequency, except for the 0.10 μm , 0.15 μm and 0.25 μm wide structures at low frequency. For very small line widths, resistive effects are dominant over reactance. Under these conditions, phase constant becomes proportional to the square-root of frequency as shall be discussed in section 6.4.2.

Fig. 6.9 Phase constant β as a function of frequency for line length (a) 0.5 mm and (b) 1 mm

(b) Characteristic Impedance (Z)

As shown in Fig. 6.10(a) and (c), $|Z|$ changes from a very large value at low frequency to an almost constant value above a frequency of ~ 5 GHz for structures having line width larger than $2 \mu\text{m}$. The fact that the magnitude of Z remains constant with frequency is evidence of quasi TEM mode of wave propagation [73]. It is also observed that the frequency at which quasi TEM mode dominates decreases with an increase in the

line width. For structures with line width less than $2\ \mu\text{m}$, there is a significant variation of magnitude of Z at frequencies below 5 GHz, indicating a slow-wave mode of propagation. The slow-wave mode turns into the quasi TEM mode at a frequency of about 30-35 GHz for all line widths and lengths used in our study. It can be seen that the magnitude of Z decreases with the line width. In the quasi TEM propagation mode, the characteristic impedance of transmission lines is inversely proportional to the square-root of line capacitance. Wider lines have higher line capacitance and thus lower characteristic impedance.

Fig. 6.10 Characteristic impedance Z of the line (a) $|Z|$, $L=500\ \mu\text{m}$, (b) Phase of Z , $L=500\ \mu\text{m}$, (c) $|Z|$, $L=1000\ \mu\text{m}$ and (d) Phase of Z , $L=1000\ \mu\text{m}$

The phase of Z as shown in Fig. 6.10(b) and (d) is mostly negative except for the wide line of 8 μm , for which the phase becomes slightly positive (~ 0.03 radian). This implies that Z is mostly capacitive at low frequency and changes to inductive impedance at about 10 GHz for the 8 μm wide line. The quasi TEM mode is more evident with larger line width at higher frequency as the phase becomes close to zero. For line width less than 4 μm and frequency below 30 GHz, there is a variation of phase implying slow-wave mode of propagation. The results for 1000 μm long lines are very close to 500 μm long lines, except that a strong inductive effect is seen for line width $\geq 4 \mu\text{m}$.

(c) Slow-wave Factor

The slow-wave factor $\beta C/\omega$ is plotted as a function of frequency in Fig. 6.11 for various line widths. Below 2 GHz, the slow-wave factor is very high and then it slowly becomes constant with frequency. This behaviour is consistent with theoretical calculations of Hasegawa et al [13]. The high slow-wave factor below 2 GHz is indicative of slow-

Fig. 6.11 Slow-wave factors for Cu/USG interconnects

wave propagation and it transits to quasi TEM mode at about 30-35 GHz at which the slow-wave factor becomes constant. Wider lines show a smaller slow-wave factor which indicates that wider lines follow quasi TEM mode at a lower frequency. At 40 GHz the minimum and maximum values of slow-wave factor was found to be 1.83 and 2.24 for 4 μm and 0.1 μm wide lines, respectively.

(d) Line Parameters $R(\omega)$, $L(\omega)$, $C(\omega)$, and $G(\omega)$ for Copper/USG Interconnects

Fig. 6.12 show the extracted R , L , C , and G of interconnect lines of 0.10 to 8 μm width and line length of 500 μm . The extracted $R(\omega)$ shown in Fig. 6.12 (a) is almost

Fig. 6.12 Line parameters (p.u.l.) for 500 μm long test structure with USG dielectric (a) R , (b) L , (c) C and (d) G

constant with frequency indicating negligible skin effect. The skin depth, δ indicates the penetration depth of electromagnetic field in a conductor with infinite thickness and exponentially decreasing current density at a given frequency f . It is defined by the expression $\delta = (\pi f \mu \sigma)^{-1/2}$, where μ is magnetic permeability, and σ is conductivity of conductor. With increase in frequency, the skin depth decreases. This causes restriction of current flow to a smaller cross section area which results in an increase in the resistance of a conductor. At 40 GHz, which is the highest measurement frequency, the skin depth in Cu is about 328 nm which is greater than the thickness of Cu (220 nm) used in this experiment. There is some evidence of the skin effect in our results with marginal increase in resistance close to 40 GHz for wider lines of 4 and 8 μm . The direct current (DC) resistivity of the interconnect test structure was also measured and is given at Appendix A.

The inductance plot in Fig. 6.12 (b) shows a slight decrease of inductance with increasing frequency. At low frequency, electromagnetic field can penetrate deeper into metallic conductors and therefore the, resulting self inductance increases the total inductance of lines. In addition, the return current in the substrate spreads to reduce the line impedance, which is dominated by resistance at low frequency. This spreading of current results in a larger return current loop, increasing the inductance at lower frequency. At high frequency, skin effect in the substrate makes the current loop smaller, and correspondingly the inductance decreases. Inductance is also found to increase with a decrease in the line width. This is due to the fact that wider lines result in smaller magnetic loops and associated magnetic flux.

The p.u.l. capacitance value decreases gradually with frequency as shown in Fig. 6.12 (c). At low frequency, the dominating mode of propagation is the slow wave mode. In

this mode, electric field is mainly concentrated between the signal line and surface of the substrate, producing a very large capacitance. With an increase in frequency, the wave propagation mode changes from slow-wave to quasi-TEM mode. Silicon substrate starts to behave as a lossy dielectric as the frequency of operation becomes greater than dielectric relaxation frequency of silicon. The dielectric relaxation frequency of silicon (Table 6.1) is equal to 5.1 GHz and 30.2 GHz for silicon resistivity of 10 Ω -cm and 5 Ω -cm, respectively. In the quasi-TEM mode, the electric field starts to penetrate into silicon substrate as the carrier charge in silicon is not able to follow the signal changes. With an increase in frequency, the electrical field penetration into the substrate increases, resulting in decrease of the capacitance. The line capacitance is also found to increase with an increase in the line width as expected because the wider lines will have a higher capacitance due to an increase in the area of the conductor.

Finally, the shunt conductance is found to increase with increase in the frequency as well as the line width of the conductors as shown in Fig. 6.12 (d). This implies that shunt conductance for wider lines cannot be neglected at high frequencies. Since a wide line has a low series resistance, there will be less attenuation of the input signal due to series resistance. Higher shunt conductance for the wider line, consequently, will contribute more significantly towards the attenuation of the signal. The converse is true for the narrow lines. Their series resistance contributes more significantly towards the attenuation and the shunt conductance thus becomes less significant.

(e) Line Parameters $R(\omega)$, $L(\omega)$, $C(\omega)$, and $G(\omega)$ for Copper/ULK Interconnects

Fig. 6.13 shows the extracted values of R , L , C , and G of Cu/ULK interconnect lines of width of 0.15 μm , 0.25 μm , 1.00 μm and 4.00 μm and of length 500 μm . There is an

increase in the R for these structures as compared to structures with USG dielectric because of a larger cross-sectional area of the Cu/USG test structure as shown in Fig. 6.5. The values of L , C and G are quite close to the values measured for the USG dielectric. Thus, with ULK (P-MSQ) as an inter-level dielectric, there are no major differences in line parameters for a single line. The effect of P-MSQ would be more evident on the crosstalk behaviour of coupled lines as discussed in chapter 8.

Fig. 6.13 Line parameters (p.u.l) for 500 μm long test structure with P-MSQ ULK dielectric (a) R , (b) L , (c) C and (d) G

6.4.2 Inductance Effect in Interconnects

In section 6.4.1, it was observed that at low frequency the dominant mode of propagation is slow-wave mode. In this mode, the behaviour of interconnects is dispersive as characteristic impedance varies with frequency. The slow-wave mode was found to change into the quasi TEM mode with increase in frequency and linewidth. At frequency

exceeding ~ 35 GHz, all interconnects from 100 nm to 8000 nm wide exhibited quasi TEM mode. Inductance was found to decrease with line width and frequency. Capacitance values increased with line width as expected. The shunt conductance increased with both line width and frequency.

Fig. 6.14 shows a comparison between the extracted values of R and inductive reactance (ωL), and between conductance G and capacitive susceptance (ωC) as a function of frequency for four different line widths. The reactance (ωL) and susceptance (ωC) of interconnects increase with frequency. It is clear that for interconnects with line width of

Fig. 6.14 (a) Resistance and inductive reactance and (b) conductance and capacitive susceptance of transmission line as a function of frequency for 0.13, 0.25, 1.0 and 4.0 μm line widths. $l=500 \mu\text{m}$

0.10 μm and 0.25 μm , resistance is mostly dominant over inductive reactance over the measured frequency range (50 MHz – 40 GHz). The reactance overtakes line resistance at frequency above ~ 31 GHz for the 0.10 μm and ~ 35 GHz for the 0.25 μm wide lines. For the 1 μm wide line, inductive reactance becomes equal to resistance of the line at about 10 GHz, while for the 4 μm wide line, this frequency decreases to about 3.5 GHz. Therefore,

the frequency at which inductance effect becomes significant over resistance decreases with the line width. The highly resistive nature of narrow lines having width of 0.10 μm and 0.25 μm can potentially lead to a significant RC delay. This can become a major concern, as it is predicted that conductors with such dimensions will be used as semi-global interconnects as early as the year 2010 as per the ITRS roadmap.

Conductance (G) is negligible at all frequency as compared to capacitive susceptance ωC . The ωC values increase with increase in the line width as capacitance increases with line width.

If we consider that R is very large as compared to ωL and neglect the conductance G of the line at low frequency, equation 6.12 can be simplified as:

$$\gamma = \sqrt{j\omega RC} = \alpha + j\beta \quad (6.31)$$

$$\Rightarrow jRC\omega = \alpha^2 + 2j\alpha\beta - \beta^2 \quad (6.31)$$

Equating the real parts of equation 6.31 yields:

$$\alpha^2 - \beta^2 = 0 \quad (6.33)$$

$$\Rightarrow \alpha = \beta \quad (6.34)$$

Thus, at low frequencies, when resistance is dominant over reactance, attenuation constant α is equal to the phase constant β .

Equating imaginary parts in equation 6.31 yields:

$$RC\omega = 2\alpha\beta \quad (6.35)$$

$$\text{Or } \Rightarrow \alpha = \beta = \sqrt{\frac{\omega RC}{2}} \quad (6.36)$$

This implies that α and β are proportional to the square-root of frequency, as long as resistance is dominant over reactance.

When the inductive effect becomes significant and G is neglected, the equation 6.12 reduces to

$$\gamma = \sqrt{(R + j\omega L)(j\omega C)} = \alpha + j\beta \quad (6.37)$$

$$\Rightarrow \gamma = j\omega RC - \omega^2 LC = \alpha^2 + 2j\alpha\beta - \beta^2 \quad (6.38)$$

Equating real parts of Eq. (6.38)

$$\Rightarrow \gamma = \alpha^2 - \beta^2 = -\omega^2 LC \quad (6.39)$$

This implies that

$$\alpha < \beta \quad (6.40)$$

Thus, α lags behind β , whenever inductive reactance is dominant over the resistance.

Fig. 6.15 shows a comparison between α and β values as a function of frequency. As shown in equation 6.36, for highly resistive lines, α is numerically equal to β . However, if the inductance is significant, β will exceed value of α as shown in equation 6.40. Our results determine the frequencies at which β exceeds α for interconnects with varying line widths. The smaller the line width, the greater is the frequency at which β starts to exceed α . The separation frequency between α and β defines the RC limit above which inductance starts to dominate. For 0.10, 0.25, 1 and 4 μm line widths the cross-over frequencies were found to be about 12.6, 5.4, 1.8 and 0.5 GHz respectively, as shown in Fig. 6.16. Thus, this analysis can help in determining the line widths and frequencies at which interconnects can be modeled as RC circuit, and the effect of inductance can be neglected. For the narrower lines, RC representation remains valid up to much higher frequency, while RLC representation would be required in the same frequency range for wider lines.

Fig. 6.15 Attenuation constant α and phase constant β as a function of frequency for $L=500 \mu\text{m}$ and line widths of (a) $0.10 \mu\text{m}$ (b) $0.25 \mu\text{m}$ (c) $1.0 \mu\text{m}$ and (d) $4.0 \mu\text{m}$

Fig. 6.16 Separation frequency as a function of interconnect line width

6.5 WIDE-BAND LUMPED CIRCUIT MODEL FOR INTERCONNECTS

Wide-band is a relative term used to specify a broad-band of frequencies. In the context of our work, we refer to a wide-band spectrum ranging from 0- 40 GHz. Due to the lossy nature of the low-resistivity silicon substrate, the wideband behavior of on-chip interconnects becomes frequency-dependent. In the past, one-dimensional metal-insulator-semiconductor (MIS) transmission lines have been characterized by rigorous analytical methods and modeled as different equivalent-circuits [73, 239, 240]. In the literature, closed-form expressions are developed for up to 100 GHz, for the equivalent-circuit parameters with dominant TM₀ mode [241]. The full-wave analysis, finite difference time-domain (FDTD) method [242] and spectral domain approach (SDA) [243] are extended to characterize the MIS coplanar transmission line.

As mentioned in section 6.4, the transmission line can be characterized by the generalized Telegrapher's equation with a series impedance $(R + j\omega L)$ and a shunt admittance $(G + j\omega C)$. However, it is impractical to apply these frequency dependent parameters to the circuit-level simulators, such as Simulation Program with Integrated Circuit Emphasis (SPICE) and Advanced Design System (ADS), due to the distributed nature of the transmission lines at high frequency. Therefore, an equivalent circuit formulation of interconnects consisting of only ideal lumped elements is highly desirable [77, 244]. In [97], the equivalent-circuit parameters are extracted up to 10 GHz based on the quasi-static spectral domain EM simulation, including the frequency-dependent shunt admittance and series impedance. In [244], a partial element equivalent circuit (PEEC) integral equation based EM solver has been used to characterize the series impedance parameters and a simplified model has been derived based on effective substrate current

loops. Reference [80] uses a complex image approach to derive the approximate closed-form expressions for the series impedance parameters $R(\omega)$ and $L(\omega)$. In [245], the shunt admittance parameters $G(\omega)$ and $C(\omega)$ are derived in terms of high- and low-frequency asymptotic solutions

So far, all of the above mentioned lumped element models are limited to below 20 GHz. It is, therefore, necessary to develop fully lumped element models for a variety of wideband applications. We have investigated two different equivalent lumped circuit models for the basic cell with different series impedance configurations, as shown in Fig. 6.17. In this model, R_I and L_I represent the series resistance and inductance of the transmission line respectively. The oxide capacitance is represented by C_I , while C_2 and G_2 denote the Si-substrate capacitance and conductance respectively. The difference between

Fig. 6.17 Lumped element model for an on-chip interconnect. (a) Type-I, and (b) Type-II.

the two topologies is in the placement of a pair of series resistance (R_2) and inductance (L_2), which represents the skin effect of the conductor. As shown in Fig. 6.17 (a) and Fig. 6.17 (b), this pair is either connected in parallel with the resistance R_I , which we designate as Type-I or in parallel with the inductance L_I designated as Type II. The basic cells can be

cascaded to represent longer interconnects. Our approach is to derive the frequency independent lumped circuit parameters from frequency dependent measurements or simulation results. A methodology is developed to extract the lumped elements of the proposed wide band models based on the frequency asymptotic technique. The asymptotic values can be calculated from full-wave EM simulation or from measurement data. The recovered frequency-dependent parameters had good agreement with full wave EM simulations. The model is validated from the EM simulated and experimental results up to 40 GHz with large scalability of lengths up to 8000 μm , and widths down to 100 nm.

6.5.1 Series Lumped Elements

The frequency dependent lumped circuit representation of a single interconnect (Telegrapher's model) on a lossy silicon substrate as shown in Fig. 6.4 needs to be represented in terms of its equivalent circuits shown in Fig. 6.17. Each circuit element can be directly obtained as follows:

$$\text{Type-I: } R_1 = \lim_{\omega \rightarrow \infty} R(\omega) \quad (6.41)$$

$$L_1 = \lim_{\omega \rightarrow \infty} L(\omega) \quad (6.42)$$

$$R_2 = \frac{\lim_{\omega \rightarrow 0} R(\omega) \lim_{\omega \rightarrow \infty} R(\omega)}{\lim_{\omega \rightarrow \infty} R(\omega) - \lim_{\omega \rightarrow 0} R(\omega)} \quad (6.43)$$

$$L_2 = \frac{\lim_{\omega \rightarrow \infty} R(\omega)^2 \left(\lim_{\omega \rightarrow 0} L(\omega) - \lim_{\omega \rightarrow \infty} L(\omega) \right)}{\left(\lim_{\omega \rightarrow \infty} R(\omega) - \lim_{\omega \rightarrow 0} R(\omega) \right)^2} \quad (6.44)$$

$$\text{Type-II:} \quad R_1 = \lim_{\omega \rightarrow 0} R(\omega) \quad (6.45)$$

$$L_1 = \lim_{\omega \rightarrow 0} L(\omega) \quad (6.46)$$

$$R_2 = \frac{\lim_{\omega \rightarrow 0} L(\omega)^2 \left(\lim_{\omega \rightarrow \infty} R(\omega) - \lim_{\omega \rightarrow 0} R(\omega) \right)}{\left(\lim_{\omega \rightarrow 0} L(\omega) - \lim_{\omega \rightarrow \infty} L(\omega) \right)^2} \quad (6.47)$$

$$L_2 = \frac{\lim_{\omega \rightarrow 0} L(\omega) \lim_{\omega \rightarrow \infty} L(\omega)}{\lim_{\omega \rightarrow 0} L(\omega) - \lim_{\omega \rightarrow \infty} L(\omega)} \quad (6.48)$$

The relationship between lumped parameters and equivalent Telegrapher's line parameters $R'(\omega)$, $L'(\omega)$, $C'(\omega)$, and $G'(\omega)$ is further derived. The series impedance of the Telegrapher's model is $R'(\omega) + j\omega L'(\omega)$. Equating the series resistances of the wide-band and Telegrapher's models, we can arrive at the following expressions:

$$\text{Type-I:} \quad R'(\omega) = \frac{R_1 R_2 (R_1 + R_2) + \omega^2 R_1 L_2^2}{(R_1 + R_2)^2 + \omega^2 L_2^2} \quad (6.49)$$

$$L'(\omega) = \frac{R_1^2 L_2}{(R_1 + R_2)^2 + \omega^2 L_2^2} + L_1 \quad (6.50)$$

$$\text{Type-II:} \quad R'(\omega) = R_1 + \frac{\omega^2 R_2 L_1^2}{R_2^2 + \omega^2 (L_1 + L_2)^2} \quad (6.51)$$

$$L'(\omega) = \frac{R_2^2 L_1 + \omega^2 L_1 L_2 (L_1 + L_2)}{R_2^2 + \omega^2 (L_1 + L_2)^2} \quad (6.52)$$

Equations 6.49 to 6.52 for Type I and Type II relates the Telegrapher's model series impedance parameters with wide band model parameters. The wideband model parameters

R_1 , L_1 , R_2 and L_2 thus can be calculated from asymptotic values of Telegrapher's model parameters.

6.5.2 Shunt Lumped Elements

Similarly, the shunt lumped elements, including oxide capacitance C_1 , silicon capacitance C_2 and silicon conductance G_2 for both Type I and Type II are derived as:

$$C_1 = \lim_{\omega \rightarrow 0} C(\omega) \quad (6.53)$$

$$C_2 = \frac{\lim_{\omega \rightarrow 0} C(\omega) \lim_{\omega \rightarrow \infty} C(\omega)}{\lim_{\omega \rightarrow 0} C(\omega) - \lim_{\omega \rightarrow \infty} C(\omega)} \quad (6.54)$$

$$G_2 = \frac{\lim_{\omega \rightarrow \infty} G(\omega) \lim_{\omega \rightarrow 0} C(\omega)^2}{(\lim_{\omega \rightarrow 0} C(\omega) - \lim_{\omega \rightarrow \infty} C(\omega))^2} \quad (6.55)$$

Then, admittance elements $G'(\omega)$ and $C'(\omega)$ are given as:

$$G'(\omega) = \frac{\omega^2 G_2 C_1^2}{G_2^2 + \omega^2 (C_1 + C_2)^2} \quad (6.56)$$

$$C'(\omega) = \frac{\omega^2 C_1 C_2 (C_1 + C_2) + G_2^2 C_1}{G_2^2 + \omega^2 (C_1 + C_2)^2} \quad (6.57)$$

If the asymptotic values of $R'(\omega)$, $L'(\omega)$, $C'(\omega)$, and $G'(\omega)$ are known, either from simulation or measurements, the lumped parameters of the proposed wide band models can be calculated from equations 6.41 to 6.48 and 6.53 to 6.55.

6.5.3 Validation of Wide-Band Lumped Circuit Model by EM Simulation and Measurement

The wide band model can be validated by comparing the values of $R(\omega)$, $L(\omega)$, $C(\omega)$, and $G(\omega)$ derived from EM full wave simulation using SONNET or from VNA measured data against $R'(\omega)$, $L'(\omega)$, $C'(\omega)$, and $G'(\omega)$ recovered from lumped circuit model. Fig. 6.18 shows the flow chart that was used for the validation of a wide-band lumped circuit model.

Fig. 6.18 Flow chart for validation of wide band lumped circuit model

Fig. 6.19 shows the comparison between the $R(\omega)$, $L(\omega)$, $C(\omega)$, and $G(\omega)$ values extracted from EM simulations, and the recovered values of $R'(\omega)$, $L'(\omega)$, $C'(\omega)$, and

$G'(\omega)$ using wide-band model (Type-I) lumped parameters. The maximum relative error between the EM full wave simulation results and the values recovered from lumped parameters is smaller than 2.9 %, 1.2%, 4.7% and 2% for $R(\omega)$, $L(\omega)$, $C(\omega)$, and

Fig. 6.19 Comparison between the EM simulated and extracted frequency-dependent p.u.l parameters of an 8 μm wide and 500 μm long interconnect using wide-band lumped circuit model. (a) $R(\omega)$, (b) $L(\omega)$, (c) $C(\omega)$ and (d) $G(\omega)$

$G(\omega)$ respectively over a wide frequency range from 0.05 to 40 GHz. This validates the wide-band lumped circuit model and the lumped element extraction methodology.

The modeling technique is further validated by measuring the scattering parameters of samples, by cascading several basic cells of the wide-band circuit depending on the

length of the interconnect [233] and comparing experimental against simulated S-parameters recovered from the wide-band model. Flow chart for the validation of the wide band model by measurement is shown in Fig. 6.20.

Fig. 6.20 Validation of Frequency independent wide band lumped circuit parameters extraction methodology using S-parameter measurements

It has been reported that electromagnetic behaviour of cascaded transmission line may be captured with sufficient engineering accuracy if the length of each segment does not exceed one-tenth of the wavelength of the maximum frequency of interest [62]. In our case, for the USG dielectric ($\epsilon = 4.2$), one-tenth of the wavelength at 40 GHz is $\sim 366 \mu\text{m}$. Therefore, a minimum of 2 cascaded sections are needed for modeling the $500 \mu\text{m}$ long line.

We found that for the $500 \mu\text{m}$ long line, a lumped element model with 4 cascaded basic cells is found to have good agreement with the measurement result over all operating

frequency bands. In Fig. 6.21, the recovered results are plotted together with those from measurement. Up to 40 GHz, the scalable model exhibits very good agreement with the measurement results of the 0.1 μm , 0.5 μm , and 8 μm wide lines.

Fig 6.21 Wide-band lumped circuit model validation based on the measured results with line length of 500 μm with line width of (a) 0.1 μm (b) 0.5 μm and (c) 8 μm

6.6 SUMMARY

We have characterized the frequency dependent response of interconnects with line width ranging from 0.10 – 8 μm and line length ranging from 0.5 mm to 8 mm using the generalized Telegrapher's model. Thereafter, we analyzed the frequency at which the

inductance effect starts to play a dominant role. Finally, we developed a fully lumped element model for wideband on-chip interconnects, and verified its scalability for line length up to 8000 μm , and line width down to 100 nm. The advantage of lumped circuit representation is the frequency independence of the *RLGC* parameters under a given set of geometrical and material constraints. We show that both the series and shunt lumped elements of the model can be determined based on the frequency asymptotic technique without any optimization. The equivalent lumped circuit is derived and verified to efficiently recover the frequency-dependent parameters up to 40 GHz. We verified the wide-band lumped model and its accuracy by comparison of S-parameters derived using electromagnetic (EM) simulation as well as measurement. The model is validated up to 40 GHz by a good agreement between the modeled and measured S-parameters. The lumped elements wide-band model can be directly used in SPICE-compatible simulation for wide-band frequency applications in the design of RF integrated circuits.

Chapter 7

Interconnect Signal Integrity – Rise Time and Delay

7.1 INTRODUCTION

It is well known that transistor gate delay decreases with a reduction in feature size. In contrast, interconnect delay increases with decrease in feature size offsetting the benefits of the reduced gate delay. For high performance giga-scale IC integration, interconnect delay must be reduced by incorporating suitable modifications in IC design, materials, device and process architectures [1, 5, 64-68, 223]. The chip size of ICs has increased due to recent trends towards system-on-chip (SOC) devices with enhanced on-chip functionality. This also necessitates the need for longer wires. The length of an interconnect carrying a clock, control or data signal can be equal to the chip size. Therefore, it is necessary to model and understand the impact of interconnect delay on the electrical performance of ICs. The most widely used model for propagation delay prediction has been the Elmore delay model. However, this model does not take into account the finite input rise time and inductance of the line [245-247]. Elmore proposed a 50% RC delay (τ) where R and C are total resistance and capacitance of the interconnect. Subsequently, Wyatt proposed the delay as 0.693τ , which is considered to be more accurate than the Elmore delay [248].

With doubling of the speed of ICs every 1.5 years in accordance with Moore's law, digital circuit rise/fall times are approaching a few tens of picoseconds. Si and SiGe technologies are fast replacing III-V compound semiconductors for millimeter wave devices [3]. Thus, increasing circuit speeds have led to faster rise/fall times of the signals.

Integrity of such signals is becoming increasingly difficult to be maintained with a continuous increase in the operating frequency of ICs.

When an electromagnetic wave propagates along an interconnect, two factors can degrade the rise/fall times of a signal. The first is a change in wave amplitude as a function of its frequency. The amplitude of a wave is exponentially proportional to the attenuation constant α . As shown in chapter 6, α is frequency dependent. A high frequency signal will attenuate more than a low frequency signal as it propagates through an interconnect. The second factor is that the velocity of an EM wave increases with the wave frequency. The signal velocity (ν) in a transmission line is given as $\nu = \omega/\beta$, where ω and β are the angular frequency and phase constant respectively. For RC circuits, β is proportional to the square-root of the frequency. For digital circuits, an input pulse signal can be represented as a combination of high as well low frequency components. Thus, the velocity of a signal propagating across a transmission line will show a frequency dependent behaviour. This dispersive behaviour severely affects the shape of the wave as it transmits across the transmission line. High frequency signals travel faster than low frequency signals and at the same time get more attenuated than the low frequency signals. This results in distortion of the wave shape.

With ever increasing circuit speeds, and the use of longer and wider wires as global interconnects, the effect of inductance on signal propagation has become too important to be ignored [62, 249-252]. The effect manifests itself as changes in rise/fall time, ringing and overshoot. Ringing and overshoot can cause unwanted signal transitions in digital circuits, causing logic faults. Voltage overshoots increase power consumption of ICs and may also cause reliability problems such as gate dielectric breakdown [253].

The objective of this chapter is to determine a suitable lumped circuit interconnect model and an experimental methodology for estimating the effect of interconnect parasitics on rise/fall time and propagation delay. We compare the suitability of Telegrapher's model and the wide-band model of chapter 6 for time domain characterization by studying the match between the simulated and experimental S-parameters. The wide band model is found to be better than the Telegrapher's model. Time domain simulation and measurement are carried out for copper lines with width ranging from 100 nm to 4 μm and length ranging from 500 μm to 2 mm. Multiple sections of the model are used for accurate representation of different interconnect lengths in SPICE simulations of the delay. Effect of the interconnect inductance and resistance are clearly identifiable, thus indicating the applicability of RF models to time domain characterization.

7.2 TEST STRUCTURE FABRICATION AND MEASUREMENTS

Transmission line test structures having the GSG configuration were fabricated with width ranging from 100 nm to 4 μm and lengths ranging from 500 to 2000 μm as shown in Table 7.1. Fabrication details for the test structures were given in section 6.3. Thickness of the isolation oxide used in this experiment was 10 μm , which is in the range

Table 7.1 Line widths and line-lengths used for the test structures

Line widths, w (μm)	0.10, 0.15, 0.25, 0.5, 1, 2, and 4
Line Lengths, l (μm)	500, 1000 and 2000

of the typical dielectric thickness used in standard 10-13 metal levels processes. S-parameters were measured from 50 MHz to 40 GHz using a HP8510C network analyzer. Line-reflect-reflect-match (LRRM) techniques were used to calibrate the network analyzer. The interconnect lines were modeled as multiple cascaded sections of a standard Telegrapher's model as well as a wide-band model as discussed in chapter 6. The model parameters were extracted using IC-CAP modeling tools. The initial values of model parameters were calculated using asymptotic techniques described in section 6.5. The models were further refined using non-linear optimization routines available in IC-CAP. Typically, the rms errors in magnitude and phase between the measured and simulated S-parameters were below 3.8 %. These models were used for time domain simulation of a pulse input with varying rise/fall time. The optimized model parameter values were taken as frequency independent and used for time domain SPICE 3 simulations.

Time domain characterization was carried out using an Agilent 81134A, 3.36 GHz pulse generator and Agilent DSO81204A, 12 GHz oscilloscope. IC-CAP was used in conjunction with SPICE 3 for modeling and simulation. Fig. 7.1 shows the measurement

Fig 7.1 Time-domain measurement set up for rise time and delay estimation

set up for time-domain characterization of the interconnect test structures.

7.3 RESULTS AND DISCUSSION

7.3.1 Comparison of Telegrapher's and Wide-Band Model Using S-Parameters

Fig. 7.2 (a)-(d) shows the magnitude and phase of the S-parameters modeled using Telegrapher's model and wide-band model respectively for a typical 2 μm wide and 500 μm long interconnect line. It is discernible that the wide-band model represents the S-parameters more accurately over the entire frequency range. There is a considerable difference in the measured and simulated magnitude of S_{12} at both high and low frequencies for Telegrapher's model as compared to wide-band model. A similar trend was

Fig.7.2 Magnitude and phase of measured and simulated S-parameters for a line of $w=2\ \mu\text{m}$ and $l=500\ \mu\text{m}$, (a) S_{12} , telegrapher model, (b) S_{12} Wide-band model, (c) S_{11} , telegrapher model and (d) S_{11} Wide-band model

observed for all interconnect lines with width ranging from 100 nm to 4 μm and length ranging from 500 μm to 2000 μm . During data fitting and SPICE simulation, 3, 6 and 12 cascaded sections were used for the 500, 1000 and 2000 μm long line respectively. The maximum rms errors between measured and simulated S-parameters for the 2000 μm long lines were below 3.3 % and 1.7 % for the Telegrapher's and the wide-band model respectively as shown in Table 7.2 .

Overall, the wide-band model showed a better fit between simulated and experimental S-parameters data as compared to the Telegrapher's model. Therefore, the wide band model was used for subsequent simulation.

Table 7.2 Percentage rms errors between measured and simulated S-parameters for the wide band and Telegrapher's models

rms error (%)						
Line Width (μm) \diagdown Line Length (μm)	500		1000		2000	
	Wide band Model	Telgrapher's Model	Wide band Model	Telgrapher's Model	Wide band Model	Telgrapher's Model
0.15	1.69	2.01	1.59	1.78	1.29	1.33
1.00	1.52	2.26	1.52	2.34	1.44	3.14
4.00	1.47	2.61	1.21	2.14	1.48	3.27

7.3.2 Rise Time and Delay as a Function of Line Width and Line Length

We used SPICE simulations to perform waveform and delay analysis based on the wide band model. The lines were terminated by their characteristic impedance to avoid reflections from port 2. The input pulse had amplitude of 1 V, pulse-width of 200 ps, period of 400 ps, and rise/fall time of 20 ps. The output pulse waveforms for interconnects with line width of 100 nm, 250 nm, 1000 nm and 4000 nm, and line length of 500 μm , 1000 and 2000 μm were simulated using the best fit circuit parameters for a single line.

The simulation results are shown in Fig. 7.3.

The observed attenuation of the pulse amplitude increases with length because of an increased resistance of the interconnect line. The rise/fall times for smaller line width of 100 nm and 250 nm increases with length while for wider lines, rise/fall times were comparable to those of the input signal. For wider lines, increased inductive effect helps in maintaining a faster rise/fall time, which is a beneficial effect of inductance. However this inductive effect is masked by an increase in series resistance of the line with increase in length. This is evident in a decreased amplitude of ringing for the 1 μm and 4 μm wide lines with an increase in length as shown in Fig. 7.3 (c) and (d).

Fig. 7.4 shows the 50 % propagation delay (τ_{50}) computed from output waveforms

Fig. 7.3 Input and output pulse shapes (wide-band model) for line lengths of 500, 1000 and 2000 μm and a line width of (a) 0.10 μm , (b) 0.25 μm , (c) 1 μm and (d) 4 μm

Fig. 7.4 50% propagation delay (τ_{50}) as a function of line width and line-length. The input pulse has an amplitude of 1 V, rise/fall time of 20 ps, pulse width of 200 ps and a period of 400 ps

(Fig. 7.3) by normalizing the output signal to its steady state value. The propagation delay is highest for the smallest line width of 100 nm and increases non-linearly with line length. The propagation delay decreases with increase in line width and its dependence on length becomes almost linear for a line width of 1 μm . This linear and non-linear behaviour of interconnect delay is in line with the two primary modes of propagation of a signal through an interconnect as described in the literature [254-255]. The first mode is known as the propagation mode, which is a mode of signal travel for a lossless line such as a LC transmission line. In this mode, a signal travels at a constant velocity across the line. Therefore, delay becomes proportional to the line length. In the second mode, called diffusion mode, the signal diffuses across the line and propagation delay exhibits a quadratic dependence on length. This is the case of pure RC transmission lines. The propagation mode observed for lines wider than 1 μm changes into the diffusion mode with decrease in line width. Thus, increased inductive effect helps in reducing the propagation

delay and leads to steeper rise and fall of the signal.

7.3.3 Effect of Rise/Fall Time on Output Pulse Shape as a Function of Line width

Fig. 7.5 shows the input/output pulse shapes for rise and fall time of 20 ps, 60 ps and 100 ps (10%, 30% and 50% of the pulse width) for a line width of 100 nm. It is observed that the output pulse resembles more closely the input pulse as rise/fall time increases. A 100 nm wide line has a higher series resistance as compared to a 1000 nm wide line. A pulse with shorter input rise/fall time will have more high frequency

Fig. 7.5 Input and output pulse shapes for a line width of 100 nm (wide-band model) and with a rise and fall time of (a) 20 ps, (b) 60 ps and (c) 100 ps

components than a slow rising pulse. We have also observed that the attenuation constant α of the interconnect lines is frequency dependent and increases with frequency as shown in section 6.4.1. Therefore, the output of a pulse with a shorter input rise/fall time is attenuated more as compared to a pulse with a longer rise/fall time due to greater attenuation of high frequency components.

Fig. 7.6 shows the effects of change in the rise/fall time on an interconnect line of 4000 nm width. The wider interconnect lines have less resistance but a larger inductive effect results in ringing of the output signal as compared to a 100 nm interconnect line.

Fig. 7.6 Input and output pulse shapes for a line width of 4 μm (wide-band model) and with a rise and fall time of (a) 20 ps, (b) 60 ps and (c) 100 ps

Therefore, the effect of a longer input rise/fall time for wide lines is decrease in the overshoot/undershoot amplitude. This implies that if the rise/fall time of a signal is sufficiently long, then wide and long lines can be modeled as RC interconnects.

7.3.4 Validation of Wide-Band Model by Time Domain Measurement of Rise-Time and Delay

In time domain measurement, the interconnect line is connected to pad structures on both ends for probing. In section 7.3.2, these pads parasitics were de-embedded during SPICE simulation for computing rise/fall time and delay. However, for time domain measurements as shown in Fig. 7.1, the pads, cables, connectors and probe parasitics cannot be individually isolated. In our SPICE simulation, the cables, connectors and probe parasitics were neglected. However, the pad parasitics were computed from S-parameter measurements of open pad test structures. The interconnect test structure was modeled as multiple cascaded sections of wide band lumped circuit for SPICE simulation. The lumped circuit model of pads is shown in Fig. 7.7. The model parameters were computed by optimization of circuit elements values which results in best matching of simulated and measured S-parameters using ICCAP optimization routines. The values of pad circuit

Fig. 7.7 Time domain SPICE simulation set up

elements C_1 , C_2 and R_2 were found to be 17.07 fF, 7.76 fF and 972.2 Ω respectively.

Fig. 7.8 shows the measured and simulated input and output waveforms for a 1000 μm line with line width of 0.10 μm and 4 μm . The input pulse had amplitude of 1V, pulse width of 2 ns, period of 4 ns and rise/fall time of 80 ps. In the case of small line width, the simulated output signal amplitude is lower than that of the measured waveform (Fig. 7.8(a)). While for the 4 μm wide line, the simulated amplitude is greater than that of the measured waveform (Fig. 7.8 (b)). This mismatch in input/output waveforms can be due to cables, probes and connectors parasitics which were neglected in the simulation.

Fig. 7.8 Measured and simulated input/output waveforms for a line-length of 1000 μm and with a line width of (a) 0.10 μm and (b) 4.00 μm

7.3.5 Input /Output Waveforms and Rise/Fall Time

Fig. 7.9 shows the measured input and output waveforms for lines with width of 0.10 μm , 0.50 μm and 2 μm , and length of 500 μm , 1000 μm and 2000 μm for Cu/USG

Fig. 7.9 Measured input/output waveforms with various line widths for a line-length of (a) 500 μm , (b) 1000 μm and (c) 2000 μm

interconnects. The output signal attenuates as the line width becomes smaller and line length becomes longer due to increased resistance of the lines.

Fig. 7.10 shows the measured and simulated rise times for 0.25 μm , 1 μm and 4 μm wide lines. The simulation was carried out using the wide-band model incorporating the pad parasitics. The input pulse had amplitude of 1 V, pulse width of 2 ns, period of 4 ns and rise/fall time of 80 ps. The simulated and measured output pulses show a good rise-time match. Some discrepancy in matching can be due to the parasitics of cables, probes and connectors used in the measurement set up, which are not accounted for in the

Fig. 7.10 Simulated and measured rise times for a interconnect with line width of (a) $0.25 \mu\text{m}$, (b) $1 \mu\text{m}$ and (c) $4 \mu\text{m}$. The line lengths are 0.5 mm, 1 mm and 2 mm.

simulation. This time domain characterization validates the accuracy of wide-band model in estimating the rise/fall time of the interconnect.

We have not shown the experimental/simulated results related to ULK dielectric for delay and rise/fall time, as ULK implementation in our test structures is only as intra-line dielectric. For all the test structures, a $10 \mu\text{m}$ thick USG layer is fabricated under the metal lines, which has a major influence on the delay and rise/fall time than the intra layer thin ULK dielectric of 220 nm . The influence of ULK dielectric is mainly on cross-talk reduction as discussed in chapter 8.

7.4 SUMMARY

The Telegrapher's and wide-band models were used to study the effect of interconnect parasitics on rise time and delay. S-parameter analysis shows that wide-band model more accurately represents the dispersive behaviour of interconnects. The delay showed a linear dependence with length for lines wider than 1 μm . The resistive effect causes delay to increase non-linearly with length for narrower lines. If the rise/fall time is large, wide and long lines can be modeled as RC interconnects. It was observed that for the wider interconnects, inductance has a significant impact on the delay while for narrower interconnects, the series resistance masks the inductive effect. Wider and longer interconnect lines are more accurately represented by the wide-band model. Further, application of the models extracted using RF techniques is shown for time domain analysis. The simulated and measurement waveforms show a reasonable match for a given pulse input, validating the accuracy of wide-band model for estimating the interconnect delay and rise time.

Chapter 8

Interconnect Signal Integrity – Crosstalk

8.1 INTRODUCTION

With continuous downward scaling of interconnect feature size, and increased frequency of circuit operation, it is becoming very challenging to maintain signal integrity of integrated circuits. The two main concerns related to signal integrity are the timing and quality of signals as they propagate through an integrated circuit. The goal of a circuit designer is to ensure reliable high speed transmission with minimal delay and distortion of signal. One of the problems of signal integrity is crosstalk, which can deteriorate signal quality due to unwanted coupling between interconnects. Crosstalk originates from undesirable parasitic capacitance and inductance of the interconnects, producing spurious signals. As interconnects scale down, several factors aggravate the problem of crosstalk. Some of these factors are: (i) increase in circuit density which reduces the spacing between the interconnects, (ii) increase in the number of metal layers increasing vertical crosstalk, and (iii) increase in the aspect ratio of the interconnects enhancing lateral crosstalk. The higher levels of metallization are found to be more susceptible to crosstalk due to a decrease in the substrate capacitance, as distance to the substrate is increased [256]. It has been reported that crosstalk can be prohibitively large if interconnects have small resistance [257]. However, it is desirable to have small resistance for reducing the interconnect latency. Therefore, there is a trade off between interconnect latency and crosstalk.

Crosstalk between any two interconnects represented as channel 1 and 2 is defined as the ratio of output of channel 2, $V_o(2)$ with no input signal applied to it ($V_i(2) = 0$) to the output of channel 1, $V_o(1)$ excited by an input signal $V_i(1)$, as shown in Fig. 8.1.

Fig. 8.1 Crosstalk between the interconnects: channel 1 (aggressor) and channel 2 (victim)

Ideally, crosstalk between two channels that are not electrically connected should be zero. However, this is never the case for practical coupled transmission lines. There is always some electrical signal coupling between them, depending upon the properties of material surrounding the interconnects, their proximity to each other, and the voltage and frequency of operation.

Crosstalk between two channels 1 and 2 can be expressed in dB as [258]:

$$crosstalk = \left[20 \log \frac{|V_o(2)|}{|V_o(1)|} \right]_{V_i(2)=0} \quad dB \quad (8.1)$$

Modeling of crosstalk requires characterization of self and mutual parasitics of the interconnects, which are represented as transmission lines at high frequency. There is an extensive literature available on the characterization of single and coupled transmission

lines by full wave [74-75] or quasi-static electromagnetic [76-77] approach. However these techniques require extensive computational resources and are not practical for computer aided design of high density ICs. Therefore, closed form expressions are proposed for the characterization of frequency dependent line parameters of single and coupled transmission lines, which allow faster design and design scalability of ICs [79-83]. Measurement based circuit models have also been reported in [73, 77, 228-231, 259]. The advantage of measurement based models is that they can be more accurate by accounting for the variability in dimension and material properties introduced during the fabrication of these interconnects.

Though it is possible to use circuit simulation or numerical computation to estimate crosstalk, compact physical models are more useful to circuit designers for design optimization. So far, there are only a few reports on measurement based and SPICE compatible modeling of coupled lines. Sakurai et al. modeled interconnect lines as distributed RC lines [269], however RC representation of coupled lines resulted in substantial errors in predicting delay and crosstalk [72, 261]. Tang et al. [262] proposed RLC coupling based noise models; however these models are only applicable to the case where mutual inductance and coupling capacitances are much smaller than self inductance and substrate capacitance respectively. Zheng et al. [244] analyzed coupled lines using a ‘FAST HENRY’ algorithm where-in they validated the coupling capacitance and inductance with SPICE simulation using extracted per unit length (p.u.l.) parameters. The skin effect in metals, however, has been ignored to simplify the problem. Sung et al. [263] analyzed the coupling between two interconnects by ignoring the substrate effect. Arz et al. [264] used 4-port measurement to determine the mutual and self RLC parameters of the

coupled lines, but they do not describe a compact model. Agarwal et al. [265] used RLC parameters based on transmission line theory, ignoring the substrate effect to arrive at the coupling parameters. In addition, no measurement results are referred to in this work. Yu et al. [266] described a multiple conductor model valid up to 50 GHz, however again substrate effect was ignored. Thus, SPICE compatible compact models for coupled on-chip interconnects valid over a wide band of frequencies are not available in literature.

In this chapter, we present, for the first time, a measurement based approach for modeling the RF and time domain behavior of coupled on-chip interconnects that builds on the single line model parameter extraction methodology discussed in chapter 6. First, single interconnects are measured and modeled as cascaded multiple Γ -sections [231]. This is followed by high frequency characterization of open terminated asymmetric coupled lines. In addition to the single line model parameters, coupling resistance, capacitance and inductance between the circuit elements are extracted over a wide frequency band. The model is validated by comparing the SPICE simulation results with the measured and de-embedded S-parameters of coupled lines in the frequency domain and measured crosstalk pulse amplitude and pulse shape in the time-domain.

We have also studied the effect of low- κ dielectric on interconnect crosstalk. By using low- κ dielectrics as inter/intra metal dielectrics, mutual capacitance between the interconnects both in the lateral and vertical direction should reduce. We therefore studied the effect of ultra low- κ material (ULK) ($\kappa \sim 2.2$) on lateral reduction in coupling capacitance by using our coupling model.

8.2 TEST STRUCTURE FABRICATION AND MEASUREMENTS

Copper interconnects were formed on a film stack consisting of 10 μm thick SiO_2 and 50 nm of SiN deposited on 200 mm diameter, $\langle 100 \rangle$ oriented, p-Si substrate with resistivity of $\sim 10 \Omega\text{-cm}$. Two sets of wafers, one with undoped silicon glass (USG) with $\kappa = 4.1$, and the other with a spin on ULK dielectric with $\kappa = 2.2$ were fabricated using the single damascene process to study the effect of dielectric constant on crosstalk. The width of the copper interconnects ranged from 150 nm to 1 μm with two different line length of 500 and 1000 μm . The plan view schematic layout of a crosstalk test structure is shown in Fig.8.2.

Fig. 8.2 Plan view of the test structure for crosstalk characterization consisting of two open-ended coplanar-waveguide structures in ground-signal-ground (GSG) configuration

Fig. 8.3 (a) and 8.3 (b) show the cross-sections of the test structures for Cu/USG and Cu/ULK dielectric schemes, respectively. Table 8.1 shows the dimensions of test structures used for this study. For the coupled lines, spacing between the two lines was varied as 1, 3 and 7 times the line width. The test structures were designed in ground-signal-ground (GSG) configuration with widely separated ground bars to suppress the excitation of coplanar waveguide (CPW) modes for RF characterization.

Fig. 8.3 Cross-section of copper test structures in GSG configuration with (a) USG dielectric and (b) ULK (LKD 5109) dielectric. Ground lines are not shown

Table 8.1 Dimensions of test structure for crosstalk characterization

	All dimensions in μm											
Length (l)	500 and 1000											
Width (w)	0.15			0.25			0.50			1.00		
Spacing (s)	0.15	0.45	1.05	0.25	0.75	1.75	0.50	1.50	3.50	1.00	3.00	7.00

Thickness of the metal lines was 350 nm for the Cu/USG and 230 nm for the Cu/ULK interconnect respectively. For the Cu/ULK interconnect process, 35 nm of SiC was deposited on top of the ULK dielectric to prevent direct CMP of ULK dielectric. After formation of Cu interconnects by damascene process, 50 nm of SiN and 300 nm thick USG layers were deposited as passivation layers. To facilitate probing, tantalum and aluminum metal with a thickness of 25 nm and 750 nm respectively, were deposited and patterned on pad structures. The wafers were finally alloyed at 350 °C for 30 min. in a forming gas mixture containing H_2 and N_2 with a gas flow ratio of 1:10. Two port on-wafer S-

parameter measurement was carried out using Cascade Microtech Infinity probes and Agilent's 8510C Network Analyzer from 50 MHz to 40 GHz using the line-reflect-reflect-match (LRRM) technique for calibration. The measurement was taken on a SUMMIT 9000 analytical probe station as shown in Fig.6.6. The measured data were de-embedded by subtracting open-dummy pad admittances (Y-parameters) from the admittance of the test structures. Time domain characterization was carried out using an Agilent 81134A, 3.36 GHz pulse generator and Agilent DSO81204A, 12 GHz oscilloscope as shown in Fig. 8.4. Agilent's integrated circuit characterization and analysis program (ICCAP) was used in conjunction with SPICE 3 for modeling and simulation.

Fig. 8.4 Measurement set up for 2-port time-domain characterization

8.3 SINGLE AND COUPLED TRANSMISSION LINE MODELS

We have characterized the performance of the multiple cascaded Γ -section wide band model of a single line interconnect in chapter 6. One section of the wide-band model is shown in Fig. 8.5 (a). We used three and six Γ -sections to represent 500 μm and 1000

μm long lines, respectively. Model elements for the single line circuit are the same as the Type 1 configuration discussed in section 6.5. The equivalent wide band circuit model for the coupled lines is shown in Fig. 8.5 (b). C_m represents capacitive coupling between the two interconnect lines through the oxide and passivation layer. The coefficient of mutual inductance (K_m), which is defined as the ratio of mutual inductance between the coupled lines to the self inductance (L_1 and L_2) of each line, is incorporated to account for inductive coupling between the two lines. Resistivity of the silicon substrate has a great impact on broadband characterization of interconnects. The low-resistivity substrate that is conventionally used in silicon technology to improve latch up immunity of devices can be quite lossy for RF applications. Therefore, C_{sim} and G_{sim} are included in the equivalent circuit to represent the shunt loss of the substrate at high frequencies.

Fig. 8.5 (a) Γ -section of the single transmission line (b) Equivalent circuit model of a coupled transmission line pair where each line of the pair is represented by a single Γ -section. These sections are cascaded to represent distributed nature of transmission line

8.4 RESULTS

8.4.1 Test Structure

Single and coupled lines test structures with line width and spacing as described in Table 8.1 were formed by single copper damascene technology. Fig. 8.6 shows the TEM cross-sections of the single and coupled line structures with Cu/USG and Cu/ULK dielectric schemes for 0.15 μm wide line. Line to line spacing for the coupled lines is 0.15 μm . Plan view schematics of the single and coupled lines are shown in the inset of Fig. 8.6 (a) and (b) respectively.

Fig. 8.6 TEM cross-sections of test structures (a) Cu/USG/single line, (b) Cu/USG/coupled lines, (c) Cu/ULK/Single line and (d) Cu/ULK coupled lines. All lines are 0.15 μm wide. Line spacing is 0.15 μm for coupled lines. Insets in (a) and (b) shows schematic top views of single and coupled lines, respectively

8.4.2 Single Line Model Parameters Extraction

The extraction method used in this study is based on the optimization of single and coupled line parameters using Levenberg-Marquardt optimization technique available in modeling and simulations software ICCAP. For any optimization technique, there could be multiple solutions, with varying degrees of accuracy, depending upon the initial values used in the mathematical algorithms. Therefore, selection of initial values of model parameters is extremely important. The flow chart for the extraction of model parameters starting with measurement of S-parameters for single and coupled lines is shown in Fig. 8.7.

Fig. 8.7. Flow chart for characterization and modeling of coupled line

First, a Telegrapher's model was used to determine the values of frequency dependent line parameters $R(\omega)$, $L(\omega)$, $C(\omega)$ and $G(\omega)$ of a single line through S-parameter measurement over a frequency range of 1 to 40 GHz [228]. The frequency independent p.u.l. values of the single line wide band model parameters (R_1 , R_2 , L_1 , L_2 , C_{ox} , R_{sub} , C_{sub}) were then calculated using asymptotic techniques described in section 6.5 from the $R(\omega)$, $L(\omega)$, $C(\omega)$ and $G(\omega)$ values. The single line model parameters with initial values calculated from asymptotic techniques were further refined to improve the accuracy of the extracted parameters using the Levenberg-Marquardt optimization algorithm available in ICCAP. For the optimization, 3 and 6 sections of the wide-band model representation of the interconnect lines were cascaded for the 500 μm and 1000 μm line respectively. The objective of optimization was to extract the single line parameters that enable the best match between the measured and SPICE 3 simulated S-parameters. The optimized parameter values for the 500 μm and 1000 μm lines are shown in Table 8.2. The match between the measured and the simulated S-parameters is found to be excellent. The

Table 8.2 Optimized values of single line model parameters per section for Cu interconnects with USG as inter-metal dielectric

Single Line Parameters	Line Length							
	500 μm				1000 μm			
Linewidth (μm)	0.15	0.25	0.50	1.00	0.15	0.25	0.50	1.00
Line Height (μm)	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
R_1 (Ω)	79.87	49.17	25.63	11.77	79.44	48.93	29.23	14.31
R_2 (Ω)	1065.00	444.80	150.00	83.01	1057.00	722.90	95.42	37.59
L_1 (pH)	234.40	231.30	229.40	217.50	216.80	226.30	213.20	204.80
L_2 (nH)	1.80	1.32	0.45	0.32	0.50	0.68	0.39	0.19
C_{ox} (fF)	7.96	7.86	7.80	8.09	6.77	7.61	7.80	7.91
C_{sub} (fF)	13.69	13.35	13.70	14.33	19.85	15.33	15.32	16.22
R_{sub} (Ω)	474.70	404.00	400.00	386.10	420.30	738.10	731.20	625.20
Max. error (%)	9.78	8.16	9.61	7.89	11.29	10.52	6.41	7.89
rms error (%)	1.69	1.72	1.82	1.52	1.59	1.51	1.31	1.52

rms errors between the measured and simulated magnitude and phase of the S-parameters are below 2 percent for line width ranging from 150 nm to 1 μm , and line length of 500 μm and 1000 μm . As an example, the simulated and measured S- parameters showing a close match for two 0.15 μm wide single lines with length 500 μm and 1000 μm are shown in the Fig. 8.8 (a) and (b), respectively. The extracted series resistance of the line R_1 ,

Fig. 8.8 Measured and simulated S-parameters (a) S_{12} and (b) S_{11} for 0.15 μm wide and 0.30 μm thick single lines. The line length of 500 μm and 1000 μm are represented by (1) and (2) respectively

scales directly in proportion to the decrease in the line width as expected. However, C_{ox} increase with line width is not directly proportional to line width, indicating that fringe capacitances play a major role in determining the value of C_{ox} . L_2 decreases from 1.80 nH per cascaded section for the 0.15 μm wide line to 0.19 nH for the 1 μm wide line. This decrease in L_2 with line width indicates that skin effect starts to play a prominent role for wider lines. These extracted parameter values of a single line were used for modeling the coupled lines.

8.4.3 Coupled Lines Model Parameters Extraction for Cu/Oxide Interconnects

Though electromagnetic simulation can accurately determine interconnect line parameters, it requires a lot of computational resources. The simulation and design tools mostly rely on the use of analytical formulae for fast computation. Closed form expressions are desirable for fast simulation and circuit optimization. Although it is difficult to arrive at accurate closed form expressions for predicting the frequency dependent behaviour of interconnects on a lossy substrate, many closed form expression have been reported in literature. After a review of closed form expressions, we have selected the most appropriate closed form expressions validated by experimental data for arriving at the initial values of series and shunt parameters for coupled lines. These initial values will be used for extraction and optimization of coupled line parameters in conjunction with single line circuit element values.

(a) *Determination of coupling capacitor, C_m :*

For the coupled lines, C_m was calculated using the conformal mapping method suggested by Stellari et al. [82]. The coupling capacitance between two parallel coupled

interconnects is given by the expression:

$$C_m = \frac{0.5}{1 + \left(\frac{S}{H+T}\right)^2} C_{(BCP)}\left(\frac{T}{S/2}, \frac{2H}{S/2}\right) + \frac{0.87}{1 + \left(\frac{S/2}{H+T}\right)^2} C_{(CP)}\left(\frac{W}{S}\right) \quad (8.2)$$

where W and T are the width and thickness of each line respectively. S is the spacing between the lines and H is the distance of the substrate from the metal line. $C_{(BCP)}(z, y)$ is the coupling capacitance between the bottom side of a horizontal plate and the ground. $C_{(CP)}(z)$ represents the coupling capacitance between two horizontal coupling plates. $C_{(BCP)}(z, y)$ and $C_{(CP)}(z)$ are expressed as:

$$C_{(BCP)}(z, y) = \frac{\varepsilon}{2} M \left(\frac{\sqrt{\sinh\left[\frac{\pi}{2}(z+y)\right] \sinh\left(\frac{\pi}{2}z\right)}}{\cosh\left[\frac{\pi}{2}\left(z + \frac{y}{2}\right)\right]} \right) \quad (8.3)$$

$$C_{(CP)}(z) = \frac{\varepsilon}{4} M \left[\sqrt{1 - \frac{1}{(1+2z)^2}} \right] \quad (8.4)$$

where ε is dielectric constant of the material.

The function $M(k)$ is given as:

$$M(k) = \begin{cases} \frac{2\pi}{\ln\left[2 \frac{1 + \sqrt[4]{1-k^2}}{1 - \sqrt[4]{1-k^2}}\right]} & 0 \leq k \leq \frac{1}{\sqrt{2}} \\ \frac{2}{\pi} \ln\left[2 \frac{1 + \sqrt{k}}{1 - \sqrt{k}}\right] & \frac{1}{\sqrt{2}} \leq k \leq 1 \end{cases} \quad (8.5)$$

(b) Determination of coefficient of mutual inductance, K_m :

The coefficient of mutual inductance is given as the ratio of mutual inductance

between the two lines and the self inductance of each line. Mutual inductance values were calculated based on the partial-element equivalent circuit approach of Ruehli [83] and the complex image method of Weisshaar et al. [80].

Weisshaar et al. proposed a complex image technique to model interconnects on lossy silicon substrate using closed form expressions applicable for single as well as coupled microstrips. Complex image technique is developed to obtain approximate solutions that describe the effect of eddy current in a lossy substrate.

To understand the complex image representation, consider a filament unit line current at a height h above a semi-infinite lossy substrate with conductivity σ as shown in Fig. 8.9. The effect of lossy substrate can be represented in terms of a real image line current representing the eddy current in the substrate, located at a complex distance

Fig 8.9 Virtual current image and image plane for a current source above a semi-infinite lossy medium

$D = 2h + d = 2h + (1 - j)\delta(\omega)$ where $\delta(\omega)$ is the skin depth in the lossy substrate.

$$\delta(\omega) = \frac{1}{\sqrt{\pi f \mu_0 \sigma}} \quad (8.6)$$

The effect of lossy substrate can be modeled as a conducting image plane centered between the source and image current, which is at a complex distance $h_{eff} = h + (1 - j)\frac{\delta}{2}$ from the current source as shown in Fig. 8.9. The eddy currents in the substrate can be represented by the currents flowing in this conducting image plane.

The complex distance image approach can be extended to a microstrip line where the conductor is separated from the lossy substrate by a dielectric as shown in Fig. 8.10. The complex effective height for a microstrip line on a silicon substrate is given as:

$$h_{eff-microstrip} = h_{ox} + (1 - j)\frac{\delta_{Si}}{2} \tanh\left[\frac{(1 + j)h_{Si}}{\delta}\right] \quad (8.7)$$

where h_{ox} is the thickness of dielectric between the metal line and substrate, h_{Si} is the thickness of silicon substrate and δ_{Si} is the skin depth of the Si –substrate with μ_{Si} and

Fig. 8.10 Virtual ground plane for a microstrip line on lossy Si substrate

σ_{Si} are permeability and conductance of Si-substrate respectively.

This value of complex effective height is used for the computation of partial mutual inductances, using closed form expressions by Ruheli [83]. From this, mutual inductance and self inductance are derived.

(c) Determination of mutual admittance parameters, C_{sim} and R_{sim} :

The values of mutual admittance parameters, C_{sim} and R_{sim} were derived from the closed form expressions for line coupling parameters given by Chiu [81]. Closed form expressions for the conductance G_{sim} and the capacitance C_{sim} are derived in an approximate manner. For the coupled lines, the total mutual conductance can be obtained by using a conformal mapping approach and written as:

$$G_{sim} = 2\sigma \frac{K(k')}{K(k)} \quad (8.8)$$

K is the complete elliptic integral of the first kind and $k' = \sqrt{1 - k^2}$. The argument k is given by:

$$k = \sqrt{\frac{(d_x + d_y + d_s)d_s}{(d_x + d_s)(d_y + d_s)}} \quad (8.9)$$

where

$$d_x = \cosh\left[\frac{\pi(s + w + jh_{ave})}{h_{ave}}\right] - \cosh\left[\frac{\pi(s + 1.5w + jh_{ave})}{h_{ave}}\right] \quad (8.10)$$

$$d_s = \cosh\left[\frac{\pi(0.5w + jh_{ave})}{h_{ave}}\right] - \cosh\left[\frac{\pi(s + w + jh_{ave})}{h_{ave}}\right] \quad (8.11)$$

$$d_y = -1 - \cosh\left[\frac{\pi(0.5w + jh_{ave})}{h_{ave}}\right] \quad (8.12)$$

w is the width of each line and s is the spacing between the lines. It is assumed that the

substrate current is distributed in the silicon substrate with height h_{ave} , which is given by:

$$h_{ave} = \delta \left(1 - e^{-h_{Si}/\delta} \right) \quad (8.13)$$

where δ is the skin depth of the Si substrate given by expression (8.6). From the value of G_{sim} , C_{sim} can be derived as:

$$C_{sim} = \frac{\epsilon_{Si}}{\sigma_{Si}} G_{sim} \quad (8.14)$$

where ϵ_{Si} and σ_{Si} are the permittivity and conductivity of Si respectively.

8.4.4 Optimization of Model Parameters of Coupled Lines

As shown in the flow chart depicted in Fig. 8.7, the initial values of single-line parameters were calculated using the wide-band model and the asymptotic technique mentioned in chapter 6. A Mathematica software code was written to calculate the initial values of the coupling parameters in accordance with the closed form expressions mentioned in the flow chart. These initial values were used to extract the optimized parameter values using the IC-CAP software. The optimized parameters were obtained by finding the best fit between the measured and simulated S-parameters of coupled lines using IC-CAP optimization routines (Levenberg-Marquardt). The values of single line parameters C_{ox} and R_1 were included in the coupled line parameter optimization, whereas other parameters retained their values for the single line model. This was due to the reason that both C_{ox} and R_1 are strongly influenced by proximity effects. The extracted values of coupled line model parameters for a set of 500 μm long coupled lines having width of 0.15 μm , 0.25 μm , 0.50 μm and 1.00 μm , and spacing equal to one, three and seven times of the line width are shown in Table 8.3. The rms error indicates the error between the measured

and simulated S-parameter values. Table 8.4 summarizes the data for a set of 1000 μm long lines. The worst case rms errors are less than 3.7 % and 9.9% for the set of 500 μm and 1000 μm long lines respectively.

The coupling capacitor C_m reduces with increasing spacing between the two lines

Table 8.3 Optimized model parameters and rms error values for 500 μm long Cu/oxide coupled lines (3-cascades)

Line width (μm)	0.15			0.25			0.50			1.00		
Line space (μm)	0.15	0.45	1.05	0.25	0.75	1.75	0.50	1.50	3.50	1.00	3.00	7.00
C_m (fF)	30.89	13.46	7.62	19.16	9.67	5.72	12.58	6.71	4.17	8.95	5.26	3.29
K_m (10^{-3})	88.19	103.20	115.90	67.20	105.50	125.60	110.50	167.40	214.90	123.00	241.00	159.50
C_{ox} (fF)	3.50	3.43	3.46	3.26	3.26	3.56	3.39	3.43	3.74	3.50	3.45	3.50
R_1 (Ω)	52.04	49.00	49.05	31.56	30.88	31.12	15.76	16.50	18.35	9.05	11.64	14.10
R_2 (Ω)	1065.00	1065.00	1065.00	444.80	444.80	444.80	150.00	150.00	150.00	83.01	83.01	83.01
L_1 (pH)	234.40	234.40	234.40	231.30	231.30	231.30	229.40	229.40	229.40	217.50	217.50	217.50
L_2 (nH)	1.80	1.80	1.80	1.32	1.32	1.32	0.45	0.45	0.45	0.32	0.32	0.32
R_{sim} (k Ω)	0.88	1.15	1.42	0.88	1.15	1.42	0.88	1.15	1.42	0.88	1.15	1.42
C_{sim} (fF)	11.90	9.15	7.44	11.90	9.15	7.44	11.90	9.15	7.44	11.90	9.15	7.44
R_{sub} (Ω)	474.70	474.70	474.70	404.00	404.00	404.00	400.00	400.00	400.00	386.10	386.10	386.10
C_{sub} (fF)	13.69	13.69	13.69	13.35	13.35	13.35	13.70	13.70	13.70	14.33	14.33	14.33
r.m.s. error (%)	1.46	1.44	1.53	1.36	1.43	1.75	1.39	1.56	2.30	1.82	2.26	3.70

Table 8.4 Optimized model parameters and rms error values for 1000 μm long Cu/oxide coupled lines (6-cascades)

Line width (μm)	0.15			0.25			0.50			1.00		
Line space (μm)	0.15	0.45	1.05	0.25	0.75	1.75	0.50	1.50	3.50	1.00	3.00	7.00
C_m (fF)	30.32	13.09	7.32	19.36	9.65	5.52	13.41	6.74	3.80	9.51	5.34	2.96
K_m (10^{-3})	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
C_{ox} (fF)	3.68	3.84	3.70	4.11	4.15	3.76	3.83	3.77	3.73	3.36	3.24	3.78
R_1 (Ω)	63.75	59.79	59.60	36.51	35.24	36.73	20.63	21.15	24.62	13.51	14.25	14.99
R_2 (Ω)	1057.00	1057.00	1057.00	722.90	722.90	722.90	95.42	95.42	95.42	37.59	37.59	37.59
L_1 (pH)	216.80	216.80	216.80	226.30	226.30	226.30	213.20	213.20	213.20	204.80	204.80	204.80
L_2 (nH)	0.50	0.50	0.50	0.68	0.68	0.68	0.39	0.39	0.39	0.19	0.19	0.19
R_{sim} (k Ω)	0.77	1.01	1.24	0.77	1.01	1.24	0.77	1.01	1.24	0.77	1.01	1.24
C_{sim} (fF)	13.60	10.50	8.50	13.60	10.50	8.50	13.60	10.50	8.50	13.60	10.50	8.50
R_{sub} (Ω)	420.30	420.30	420.30	738.10	738.10	738.10	731.20	731.20	731.20	625.20	625.20	625.20
C_{sub} (fF)	19.85	19.85	19.85	15.33	15.33	15.33	15.32	15.32	15.32	16.22	16.22	16.22
r.m.s. error (%)	1.99	1.77	3.97	2.93	4.17	5.89	6.87	7.00	6.28	9.91	6.94	6.84

as expected. It may be mentioned here that the C_{ox} value reduces for the coupled lines as compared to the single line value as shown in Table 8.4. In coupled lines, the current distribution is affected by the electric field and magnetic field, due to currents in the coupling lines. The current may be pushed either to the outer edge, in case of even mode, or to the inner edge in case of odd mode. In both cases, the effective conductor width

Fig. 8.11 Measured and simulated s-parameters (a) S_{12} and (b) S_{11} for 0.15 μm wide, 0.30 μm thick and 500 μm long coupled lines. The edge to edge line spacing of 0.15 μm , 0.45 μm and 1.05 μm are represented by (1), (2) and (3) respectively

reduces, which in turn decreases C_{ox} . Mutual inductance values show weak inductive coupling for the set of 500 μm long lines. Mutual inductance shows insignificant bearing during parameter optimization for the set of 1000 μm long lines. In this case, mutual inductance coefficient values reach the lower limit of 0.001 set during optimization for all line widths. This indicates that for long coupled lines, mutual capacitance is significantly dominant over mutual inductance. Fig. 8.11 (a) and (b) show the magnitude and phase of measured and simulated S_{12} and S_{11} parameters for a pair of coupled lines with line width of 0.15 μm and line spacing of 0.15 μm , 0.45 μm and 1.05 μm respectively. Excellent agreement between measured and simulated S-parameters is clearly brought out.

8.4.5 Coupled Lines Model Parameters Extraction for Cu/ULK Interconnects

Currently, most of the high performance ICs with gate length below 130 nm make use of low- κ dielectrics and copper for the formation of interconnects. Low dielectric-constant materials are supposed to reduce coupling capacitance and crosstalk between interconnects. Test structures with ULK material (LKD1509) as inter-metal dielectric were fabricated, for studying the effect of low dielectric-constant materials on crosstalk.

We followed the same methodology as that described for Cu/USG interconnects to optimize and extract coupling parameters for Cu/ULK interconnects. The extracted optimized parameters for a set of 500 μm long lines with various line widths and spacings are shown in Table 8.5. The rms errors between the simulated and extracted parameters for single and coupled lines were less than 3.3% for a length of 500 μm . A comparison of mutual capacitance C_m (per cascade) between the Cu/USG and Cu/ULK interconnect is shown in Table 8.6. It is observed that there is an average reduction of C_m by 30% for the

Table 8.5 Optimized model parameters and rms error values for 500 μm long Cu/ULK coupled lines (3-cascades)

Line width (μm)	0.15			0.25			0.50			1.00		
Line space (μm)	0.15	0.45	1.05	0.25	0.75	1.75	0.50	1.50	3.50	1.00	3.00	7.00
C_m (fF)	19.66	8.67	5.35	11.96	6.66	4.09	8.90	5.04	3.01	7.00	4.01	2.14
K_m (10^{-3})	1.00	1.00	1.00	46.70	49.32	47.42	102.50	189.60	174.70	126.70	208.20	159.20
C_{ox} (fF)	4.64	4.61	5.35	4.25	4.22	4.56	4.07	4.28	4.94	4.21	4.50	5.61
R_1 (Ω)	96.53	101.80	101.30	62.08	60.75	59.68	30.73	31.72	30.79	17.97	20.78	19.68
R_2 (Ω)	1340.00	1340.00	1340.00	624.10	624.10	624.10	258.20	258.20	258.20	108.50	108.50	108.50
L_1 (pH)	166.50	166.50	166.50	213.70	213.70	213.70	227.10	227.10	227.10	217.50	217.50	217.50
L_2 (nH)	0.76	0.76	0.76	1.32	1.32	1.32	0.73	0.73	0.73	0.34	0.34	0.34
R_{sim} (k Ω)	0.88	1.15	1.42	0.88	1.15	1.42	0.88	1.15	1.42	0.88	1.15	1.42
C_{sim} (fF)	11.90	9.15	7.44	11.90	9.15	7.44	11.90	9.15	7.44	11.90	9.15	7.44
R_{sub} (Ω)	1456.00	1456.00	1456.00	1322.00	1322.00	1322.00	1211.00	1211.00	1211.00	1051.00	1051.00	1051.00
C_{sub} (fF)	11.92	11.92	11.92	11.80	11.80	11.80	12.08	12.08	12.08	12.91	12.91	12.91
rms error (%)	2.11	1.85	2.24	1.29	1.39	1.76	1.33	1.58	2.37	1.52	2.23	3.28

latter, with a standard deviation of 5.06%. Another consideration is the differences in the dimensions of the fabricated Cu/USG and Cu/ULK test structures. It is observed from Fig. 8.6 that the thickness of metal lines in the case of the Cu/ULK interconnect test structure is about ~30% smaller than that of the Cu/USG interconnect test structure. Thus, reduced coupling capacitance may be attributed to both lowering of dielectric constant for ULK dielectric and reduction in thickness of metal lines.

Table 8.6 Extracted values of coupling capacitance with USG and ULK as inter-metal dielectrics for 500 μm long crosstalk test structure

Line width (μm)	Spacing (μm)	Mutual Capacitance (C_m) (fF)		Decrease in C_m (%)
		ULK	USG	
0.15	0.15	19.7	30.9	36.4
	0.45	8.7	13.5	35.6
	1.05	5.4	7.6	29.6
0.25	0.25	12.0	19.2	37.6
	0.75	6.7	9.7	31.1
	1.75	4.1	5.7	29.1
0.50	0.50	8.9	12.6	29.3
	1.50	5.0	6.7	24.8
	3.50	3.0	4.2	27.9
1.00	1.00	7.0	8.9	21.8
	3.00	4.0	5.3	23.8
	7.00	2.2	3.3	33.6

Since the electrostatic field distribution is strictly 2-dimensional in nature, we used MEDICI simulations to estimate the reduction in coupling capacitance C_m due to the reduction in (i) thickness of metal lines and (ii) dielectric constant with replacement of USG with ULK dielectric. Table 8.7 shows expected reduction in the C_m for ULK interconnects relative to USG interconnects (350 nm thick) for ULK dielectric thickness of i) 350 nm and ii) 230 nm for 0.15 μm and 0.50 μm wide lines. The κ -value of ULK is assumed to be 2.4 during simulation though as-deposited κ -value of ULK is 2.24. This is to take into account the increase in effective dielectric constant due to the deposition of a diffusion barrier capping layer of SiC ($\kappa \sim 4.9$) on top of ULK dielectric. The simulation results show that the reduction in the C_m with reduction in thickness of ULK interconnect from 350 nm to 230 nm is in the range of 8.6% to 15.5% for the various structures shown in Table 8.7. The reduction in C_m extracted from experimental data is in the range of value of 24.8% to 36.4% for similar structures (Table 8.6). Thus, reduction in thickness of ULK does not fully account for the total reduction in C_m . This additional reduction can be attributed to the lowering of the effective dielectric constant with replacement of

Table 8.7. Simulated reduction in coupling capacitance C_m of ULK interconnects relative to USG interconnects (thickness 350 nm) due to thickness effect

Width (μm)	Space (μm)	Simulated reduction in coupling capacitance C_m of ULK interconnects relative to USG (350 nm) (%)		
		ULK Thickness=230 nm (A)	ULK Thickness=350 nm (B)	Difference (A-B)
0.15	0.15	47.37	31.89	15.48
0.15	0.45	39.51	26.67	12.85
0.50	0.50	34.26	23.12	11.14
0.50	1.50	26.53	17.94	8.60
USG dielectric $\kappa=4.1$, Thickness=350 nm ULK dielectric $\kappa=2.4$, Thickness=350 nm and 230 nm				

USG with ULK dielectric. Therefore, MEDICI simulations were further carried out to find out the contribution of ULK dielectric in reducing C_m .

Table 8.8 shows the comparison of simulated and extracted value of reduction in C_m from the experimental data. The experimental values of reduction in C_m are found to be less than the simulated values for all the structures. The difference is the greatest for 0.15 μm wide coupled lines with a spacing of 0.15 μm , (11.0 %), while it is the least (1.73 %) for 0.50 μm wide coupled lines with a spacing of 3.50 μm . As a κ –value of 2.4 was used in simulations, a smaller reduction in experimental value of C_m as compared to simulation implies that effective dielectric constant of ULK should be greater than 2.4. To verify this, MEDICI simulation was carried out to extract the κ -value of the ULK dielectric at which experimental reduction in C_m equals the simulated values (within an error band of $\pm 0.2\%$). As shown in Table 8.8, the effective dielectric constant is found to be greater than 2.4 for all the structures. One of the reasons for this increase in the κ -value can be damage to the ULK dielectric during the plasma etching or cleaning processes used in the fabrication of interconnects. Also, it is found that the effective κ -value increases as line spacing is reduced. This can be explained by taking into consideration the fact that plasma

Table 8.8 Extracted κ –value for a match between the simulated and experimental reduction in coupling capacitance C_m with ULK dielectric (230 nm)

Width (μm)	Space (μm)	Simulated reduction in coupling capacitance (MEDICI simulation, $\kappa=2.4$) (%) (A)	Reduction in mutual capacitance extracted from experimental data (%) (B)	Difference (%) (A-B)	Extracted κ -value from simulations for a match between simulated and experimental data
0.15	0.15	47.37	36.35	11.02	3.28
0.15	0.45	39.51	35.56	3.95	2.78
0.50	0.50	34.26	29.30	4.96	2.93
0.50	1.50	26.53	24.80	1.73	2.63

damage is expected to mainly confine itself to the sidewalls of the dielectric since the dielectric surface is protected from plasma damage during the etching process by 50 nm of SiC cap layer. Thus, with the reduction in line spacing, the ratio of the volume of the plasma damaged dielectric at the sidewalls to the total volume of the dielectric in the spacing will increase. This would lead to the increased effective dielectric constant of the ULK dielectric for smaller spacing. Another possible reason can be the increase in line width as compared to its designed value due to process variability. This will also manifest as increase in coupling capacitance, particularly for coupled lines with smaller line spacing. However, as the increase in dielectric constant predicted by simulation is quite large; the probability of increase in the ULK dielectric constant by plasma damage is very strong.

It is necessary to take into account the effect of various processes and process integration scheme on the effective κ . By increasing porosity of materials, κ value is reduced. However, plasma effect is going to be more severe with increase in porosity and may result in degradation of κ . In the context of process integration, there is a need for development of low- κ capping layer, otherwise the electrical properties of the fabricated structure may not show as much improvement as expected with ULK dielectrics.

8.4.6 Validation of Coupled Line Model Using Time Domain Measurement

The coupled line model for crosstalk was validated in the time domain by a close match between the simulated and measured pulse shape and amplitude. A pulse with a period of 10 ns and width of 5 ns, a rise/fall time of ~65 ps, and an amplitude of 1V was applied to the aggressor line. The near end of the victim line was open ended, while its far end was terminated in a 50- Ω resistance by an oscilloscope. The input pulse was applied at

the near end of the active line and crosstalk was measured at the far end by an oscilloscope. Fig. 8.12 and Fig. 8.13 show the simulated and measured far end-of-line crosstalk at the falling edge of pulse for Cu/USG and Cu/ULK coupled line test structures with line width of 0.15 μm and 0.50 μm , spacing equal to 1 and 3 times the line width, an a line length of 500 μm . The amplitude of the waveform shows a reasonable match for all the cases. The coupled lines with ULK dielectric show a smaller crosstalk as compared to USG test structure. For the 0.5 μm line width, ringing in the simulated crosstalk waveform

Fig. 8.12. Measured and simulated far-end crosstalk for a 500 μm long victim line for Cu/USG interconnects (a) $w=s=0.15 \mu\text{m}$, (b) $w=0.15 \mu\text{m}$, $s=0.45 \mu\text{m}$ (c) $w=s=0.50 \mu\text{m}$ and (d) $w=0.50 \mu\text{m}$, $s=1.50 \mu\text{m}$. The input signal on aggressor line was a pulse with width of 5 ns, period of 10 ns, rise/fall time of 65 ps and amplitude of 1 V

Fig. 8.13. Measured and simulated far-end crosstalk for a 500 μm long victim line for Cu/ULK interconnects (a) $w=s=0.15 \mu\text{m}$, (b) $w=0.15 \mu\text{m}$, $s=0.45 \mu\text{m}$ (c) $w=s=0.50 \mu\text{m}$, and (d) $w=0.50 \mu\text{m}$, $s=1.50 \mu\text{m}$. The input signal on aggressor line was a pulse with width of 5 ns, period of 10 ns, rise/fall time of 65 ps and amplitude of 1 V

is observed due to inductive coupling. This is not observed in the measured waveforms. This could be due to two reasons. First, the response of oscilloscope used for measurement is not sufficient for detecting very fast rise/fall time signals. The oscilloscope used in this study could only detect rise and fall times greater than 36 ps. Secondly, in simulation, the effect of cable parasitics that were used for connecting the signal generator and oscilloscope to DUT was not taken into consideration. Thus, we are unable to compare the simulated rise/fall time of a few tens of picoseconds against the measurements. However, if we ignore the ringing effects, we observe a close match between the simulated and

measured pulse shape and amplitude, validating the application of the model, in time-domain circuit analysis.

8.4.7 Time Domain Characterization of Coupled lines Crosstalk

Crosstalk noise in coupled lines was characterized in the time domain. A pulse with a period of 10 ns and width of 5 ns, a rise/fall time of ~ 65 ps, and an amplitude of 1V was applied to the aggressor line. The near end of the victim line was open ended, while its far end is terminated in a $50\text{-}\Omega$ resistance by an oscilloscope. The input pulse was applied at the near end of the active line and crosstalk was measured at the far end by oscilloscope. The measurement set up is shown in Fig. 8.4.

Fig. 8.14 shows the measured crosstalk input and output waveforms for the line width of $0.15\text{ }\mu\text{m}$, $0.25\text{ }\mu\text{m}$, $0.50\text{ }\mu\text{m}$ and $1.00\text{ }\mu\text{m}$, with spacing equal to 1 and 3 times of

Fig.8.14 Crosstalk for a pair of $500\text{ }\mu\text{m}$ long Cu/oxide coupled lines, with spacing equal to one and three times the line width. The line widths are (a) $0.15\text{ }\mu\text{m}$, (b) $0.25\text{ }\mu\text{m}$, (c) $0.50\text{ }\mu\text{m}$ and (d) $1.00\text{ }\mu\text{m}$

the line width. The results show that crosstalk decreases with the increase in spacing as expected. The crosstalk magnitude was 70.6 mV, 49.1 mV, 34.4 mV and 25.2 mV for equal line width and spacing of 0.15 μm , 0.25 μm , 0.50 μm and 1.00 μm respectively. An increase in spacing results in a lower mutual capacitance C_m between the lines; therefore capacitive signal coupling is decreased.

Fig. 8.15 shows the dependence of crosstalk amplitude on line width and line length. In general, crosstalk increases with an increase in line length. However, the extent of increase in crosstalk with length is not uniform for lines with varying line width and spacing. If line spacing is small, increase in the peak value of crosstalk with length is not

Fig. 8.15 Crosstalk as a function of line length for lines with equal line width and spaces of (a) 0.15 μm , (b) 0.25 μm , (c) 0.50 μm and (d) 1.00 μm for Cu/oxide lines

very significant as seen in Fig. 8.15(a). For wide spacing, crosstalk amplitude increases with length and fall time changes slightly. Both the peak value and the rise/fall time of crosstalk are important, however the signal must reach a certain threshold value before it can cause logic faults. Therefore, length effect takes a secondary role for coupled lines with smaller width/space. On the other hand, line length plays a primary role when width/spaces are large. Crosstalk increases significantly with line length as shown in Fig. 8.15(d).

Fig. 8.16 shows crosstalk wave form for Cu/oxide and Cu/ULK interconnect test structures. The line width and spacing between the lines are 0.15 μm and 1.00 μm as shown in Fig. 8.16 (a) and (b) respectively. In both cases, the Cu/ULK test structure shows less crosstalk as compared to the Cu/oxide test structure. As mentioned earlier in section 8.4.3, the decrease in crosstalk can arise from both the decreased height of the Cu/ULK interconnect as well as the decrease in the dielectric constant.

Fig. 8.16 Crosstalk Cu/oxide and Cu/ULK interconnects for a line length of 500 μm . The line width and spacing are equal to (a) 0.15 μm , and (b) 1.00 μm

8.4.8 Coupling and AC Power Loss

The signal coupling $|S_{21}|$ and AC power loss $(1 - |S_{11}|^2 - |S_{21}|^2)$ as a function of line width, spacing, line length and intra-metal dielectric were measured for the coupled lines [266].

(a) Coupling Loss $|S_{21}|$

Fig. 8.17 shows the coupling loss for lines with equal line width and spacing of 0.15 μm , 0.50 μm and 1 μm as a function of line length of 500 μm and 1000 μm . It is observed that coupling increases with frequency. This is expected as coupling susceptance $1/j\omega C_m$ will decrease with frequency. The coupling loss keeps increasing till coupling

Fig. 8.17 Coupling loss $|S_{21}|$ as a function of line lengths of 500 μm and 1000 μm for lines with equal widths and spacing of (a) 0.15 μm , (b) 0.50 μm and (c) 1.00 μm

susceptance becomes so low that there is no further impact of increase in frequency on the coupling loss. It is also observed that coupling loss increases with line length till a cross-over frequency is reached beyond which shorter lines have higher loss. Increase in coupling with line length is due to increase in C_m . However, at the same time input signal also gets attenuated both due to increase in frequency and length. This increased attenuation will reduce the coupling for longer lines. As lines get wider, cross-over frequency is found to be increased. This is due to lower attenuation of signal with wide lines. The crossover frequency for line widths of 0.15 μm , 0.50 μm and 1.0 μm were found to be 4.4 GHz, 19.1 GHz and 25.8 GHz, respectively.

Fig. 8.18 shows coupling loss as a function of line width and spacing. The coupling

Fig. 8.18 Coupling loss $|S_{21}|$ for a 500 μm long line at a spacing of 1, 3 and 7 times of its linewidth of (a) 0.15 μm , (b) 0.25 μm (c) 0.50 μm and (d) 1.00 μm

loss reduces with spacing. This is explained by a reduction in C_m . The coupling loss saturates to a peak value as frequency is increased independent of line spacing. $|S_{21}|$ at 40 GHz was found to be -8.1 dB, -5.7 dB, -3.8 dB and -2.1 dB for 0.15 μm , 0.25 μm , 0.50 μm and 1.0 μm wide lines with spacing equal to line width, respectively.

Fig. 8.19 shows the impact of ULK dielectric on coupling loss. ULK dielectric reduces signal coupling by about 3.3 dB, 2.0 dB and 1.3 dB at 40 GHz for equal line width and spacing of 0.15 μm , 0.50 μm and 1.0 μm respectively.

Fig. 8.19 Coupling loss $|S_{21}|$ for a 500 μm long line with a USG or ULK intra-metal dielectric for a linewidth of (a) 0.15 μm , (b) 0.50 μm and (c) 1.00 μm

(b) **AC Power Loss** $\left(1 - |S_{11}|^2 - |S_{21}|^2\right)$

Fig. 8.20 shows AC power loss for coupled lines with equal line width and spacing of 0.15 μm , 0.50 μm and 1 μm as a function of line length. It is observed that AC power loss increases with frequency. Similar to line coupling loss, power loss also decrease with length till a cross-over frequency is reached. The crossover frequencies for a linewidth of 0.15 μm , 0.50 μm and 1.0 μm were found to be 9.5 GHz, 24.7 GHz and 29.3 GHz, respectively.

(a)

(b)

(c)

Fig. 8.20 AC power loss as a function of line lengths of 500 μm and 1000 μm for lines with equal widths and spacing of (a) 0.15 μm , (b) 0.50 μm and (c) 1.00 μm

Fig. 8.21 shows the effect of ULK dielectric on AC power loss. It is observed that use of ULK dielectric does not improve the overall AC power loss. In our test structure, ULK is used only as intra-metal dielectric while the dielectric between the metal line and the substrate is USG. AC power loss is mainly due to attenuation and coupling to the substrate and therefore, it does not change with intra-line dielectric.

Fig. 8.21 AC power loss for a 500 μm long line with a USG or ULK intra-metal dielectric for a linewidth of (a) 0.15 μm, (b) 0.50 μm and (c) 1.00 μm

8.5 SUMMARY

We developed a modeling methodology for coupled interconnects based on measured S-parameters. First, a set of single transmission lines in ground-signal-ground

configuration is measured and modeled as multiple Γ -sections. A pair of coupled lines is then modeled as two single lines interconnected by coupling capacitance, mutual inductance and mutual resistance. Asymptotic techniques and closed form analytical expressions are used to determine the initial estimates for optimization of the model parameters of single and coupled lines. It is found that in extending the single line model to the coupled lines, only a couple of model parameters need to change due to the proximity effect. Further, time-domain crosstalk is measured for Cu/oxide and Cu/ultra low- κ interconnects and analyzed using the proposed model. Good agreement is found between the simulated and measured results in both the frequency and the time domains for different lengths, widths and spacing (for coupled-lines) confirming the accuracy of the modeling methodology. The compact modeling approach presented here facilitates accurate characterization and modeling of coupled interconnects based on measured data. To the best of our knowledge, this is the first attempt in modeling coupled lines in both frequency and time domains with the same set of model parameters. Further, AC power loss and signal coupling dependence on the width, spacing and length of the interconnect, and intra-line dielectric material is analyzed using S-parameters.

Chapter 9

Conclusions and Future Work

9.1 CONCLUSIONS

There were two main areas of contribution of this thesis. The first contribution is in the area of copper interconnect fabrication and the second relates to simulation, modeling and experimental characterization of interconnects. Firstly, process issues related to the fabrication of copper interconnects with porous ultra low- κ dielectrics were investigated and resolved. Resolution of 248 nm DUV tools for patterning of isolated or semi-isolated interconnect structures was enhanced by design of mask with alternating phase shifted sub-resolution assist features. Issues of reflection control and DUV resist contamination in a copper damascene process were solved by design of dual layer dielectric antireflection schemes and process control. Effect of plasma on the structure, composition and electrical properties of an ultra low- κ dielectric and the microstructure of barrier layer deposited on it were investigated. This would help in choosing appropriate process conditions and integration schemes for processing of porous low- κ dielectrics.

The second part experimentally investigates the high frequency electrical properties of a large set of test structures by S-parameter measurement up to 40GHz. The signal propagation modes were found to be as slow-wave at low frequencies and quasi TEM wave at high frequency (>35GHz), consistent with earlier theoretical predictions. A fully frequency independent lumped element model is developed for wideband on-chip interconnects, and its scalability is verified for line length up to 8000 μm , and line width down to 100 nm. We show that both the series and shunt lumped elements of the model can

be determined based on the frequency asymptotic technique without any optimization. The equivalent lumped circuit is derived and verified to efficiently recover the frequency-dependent parameters up to 40 GHz. A wide band equivalent circuit with frequency independent lumped elements is used for interconnect modeling by standard circuit simulators such as SPICE. Model predictions are experimentally validated in both the frequency and time domains. We show that the wide-band model accurately represents the dispersive behaviour of copper interconnects and can predict both propagation delay and signal rise time.

The modeling methodology is applied to coupled interconnects based on measured S-parameters. In the coupled line model, single line model parameters extracted from the wide-band model are extended for modeling of the coupled lines. Time-domain crosstalk is measured for Cu/oxide and Cu/Ultra low- κ interconnects and analyzed. A good agreement is found between the simulated and measured results in both the frequency and the time domains for different lengths, widths and spacing confirming the accuracy of the modeling methodology. Using this approach, reduction of crosstalk with use of ULK dielectrics was experimentally verified. The compact modeling approach presented here facilitates accurate characterization and modeling of coupled interconnects based on measured data.

9.2 RECOMMENDATIONS FOR FUTURE WORK

The ULK dielectric electrical properties degrade with plasma treatment during processing. It was found that for polymer based porous ULK dielectrics, the dielectric breakdown does not follow a conventional Schottky or Poole-Frenkel conduction mechanism. This needs to be further investigated. From experimental data, it was observed that crosstalk reduction is slightly higher than that expected from simulation with

decrease in κ . The reason for this discrepancy is attributed to an increase in κ during processing of test structures. One solution to prevent degradation of κ is to develop low- κ etch stop layers and integration schemes that will prevent direct exposure of ULK dielectrics to process chemistries. Another solution is the sealing of pores to prevent plasma chemistry interaction and barrier metal penetration into the porous material. These areas require further study to enable designers reap real benefits of ULK dielectrics for next generation of ICs

We have reported measurement results and validated our model for a single metallization layer. There is a need to investigate the propagation characteristics for multi layer metallization with low- κ dielectrics to study interaction among various layers as well as effect of lossy substrate. The effect of ground planes or finite impedance ground return path for multilayer metallization can also be investigated. That would enable a more realistic estimates of interconnect performance and reduce the iterations in a design cycle.

The crosstalk measurements were done using open ended lines with 2-port S-parameter measurements. This could impact measurement accuracy due to imperfect termination of open ended lines. Use of 4-port network analyzer with corresponding test structures would provide details of signal propagation in coupled interconnects.

Low cost silicon technology is fast replacing III-V compounds for emerging applications in wireless communication, radar, and imaging, operating between 0.8 GHz and 100 GHz. Therefore, modeling and characterization of interconnects need to be extended to 100 GHz and beyond.

Appendix A

Direct Current (DC) Resistivity of Copper Interconnects

The electrical resistivity of Cu interconnects is expected to rise with the continuous scaling of interconnect dimensions due to surface and grain boundary scattering effects. This can become a major concern for interconnect performance as it leads to excessive RC delays. Fuchs [267] in 1938 developed a theory that resistivity of thin films of alkali metals are always higher than in the original bulk as thickness decreases. If the electron mean path in the thin film is smaller than the film thickness then surface and interface scattering lead to increase in the film resistivity. Mayadas et al. [268] in 1970 concluded that in addition to surface scattering, the major portion of the total resistivity in polycrystalline films comes from electron scattering at grain boundaries. An additional factor that adds to the resistivity of Cu interconnects is contribution of high resistivity Cu diffusion barrier films such as Ta which is used in the fabrication of interconnects.

We have measured the resistance of the copper interconnects at DC using I-V measurements. The resistivity was computed from line resistance and cross sectional area were measured using high resolution TEM images. The average DC resistivity data as a function of line width with a line height of 214 nm is shown in Fig. A.1.

The resistivity is found to increase with decrease in line width for lines smaller than 500 nm. The resistivity data for 100 nm and 150 nm wide lines is tabulated and compared with experimental data reported in the literature in Table A.1. Our resistivity data follows a similar trend as other published data and differences in the resistivity values can be

attributed to differences in the structural dimensions, thickness of the barrier material and the structural tolerances depending on the fabrication methodology.

Fig A.1 Average resistivity of Cu Interconnects with line width

Table A.1 Resistivity of of nanoscale copper interconnects

Line width (nm)	Line thickness (nm)	Average Resistivity $\mu\Omega\text{-cm}$	Reference
116	214	2.53	This work
153	214	2.35	This work
100	230	2.60	[105]
150	230	2.45	[105]
100	230	3.10	[106]
150	230	2.80	[106]
200	200	2.40	[269]

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1. R. Kumar, T.K.S. Wong and N. Singh, “Inorganic and organic bottom anti-reflection coatings for the patterning of copper dual damascene interconnects,” Advanced Metallization Conference, October 29-30, 2002, Tokyo, Japan.
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