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**NANYANG
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**LOW-VOLTAGE GHZ-RANGE FREQUENCY
SYNTHESIZER**

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SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING
2008**

LOW-VOLTAGE GHZ-RANGE FREQUENCY SYNTHESIZER

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School of Electrical and Electronic Engineering

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in fulfillment of the requirement for the degree of
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2008

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other university or institution.

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Summary

The design of a fully-integrated low-noise frequency synthesizer with low supply voltage is one of the greatest challenges in integrating an RF CMOS transceiver on a single-chip. The trend towards low-cost system-on-chip solutions has resulted in an increasingly noisy environment which perturbs the operations of frequency synthesizers. Large reference spurs will mix with the signals from adjacent channels and hence degrade the SNR and other performances in a wireless transceiver. The problem becomes more severe when the power supply is scaled down along with the scaling of CMOS technology. Therefore, frequency synthesizer design with low reference spurs and low noise is becoming very crucial.

This thesis describes design techniques for reducing reference spurs while maintaining fast settling time, through improvements in system architectures as well as the design of charge pump circuit. A spur-reduction technique, which incorporates a high-performance charge pump design with an adaptive PLL architecture, is proposed. The proposed PLL architecture smoothly adapts the loop parameters according to different operating modes, so as to reduce the loop bandwidth in the locked state to further attenuate the reference spurs. The proposed architecture allows the loop filter components to be integrated on chip with a reasonable chip area.

Charge pump is the dominant building block causing reference spurs in the output spectrum of PLLs due to non-ideal effects such as current mismatch, leakage current, charge sharing and timing mismatch. The proposed charge pump circuit improves

current matching in a wide output range by applying a replica biasing technique with an improved feedback structure that provides stable operation. The percentage current mismatch for the output range from 0.1 V to 1.1 V under a supply voltage of 1.2 V is less than $\pm 0.5\%$. By employing differential current-steering switches with one side connected to a DC reference voltage, this charge pump circuit also minimizes feed-through of the input pulses, charge sharing effect and timing mismatch of input clocks.

To verify the proposed spur-reduction techniques, a fully-integrated frequency synthesizer is designed for 5-GHz WLAN applications using a 0.18- μm CMOS process with a supply voltage of 1.2 V. To accelerate the design process and shorten the simulation time, behavioral models represented in the Verilog-AMS language have been developed to facilitate a hierarchical design approach which comprises a top-down design process followed by a bottom-up verification process. Design considerations and techniques required for each building block, especially low-voltage design techniques are described in details. Post-layout simulation shows that the synthesizer, operating with a supply voltage of 1.2 V in a 0.18- μm CMOS process, is able to achieve a low reference spur level of -60 dBc and fast settling time of less than 30 μs for a frequency jump of 220 MHz from 5.14 GHz to 5.36 GHz. The total chip area is about 1.1 mm by 1.1 mm including the pad frame.

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TABLE OF CONTENTS

Summary.....	I
Acknowledgments	III
List of Abbreviations	VII
List of Figures.....	IX
List of Tables	XIV
Chapter 1 Introduction	1
1.1 Motivation.....	1
1.2 Objectives	4
1.3 Major contribution of the thesis.....	5
1.4 Organization of the thesis	6
Chapter 2 Fundamentals of the PLL frequency synthesizer	8
2.1 Phase-locked loop overview	8
2.2 Noise characteristics	12
2.3 Key performance parameters of frequency synthesizer.....	15
2.3.1 Frequency tuning range	15
2.3.2 Phase noise.....	16
2.3.3 Spurious tone	18
2.3.4 Settling time.....	20
2.4 Synthesizer architectures	21
Chapter 3 Adaptive PLL architecture and behavioral simulation.....	26
3.1 Existing spur-reduction techniques and limitations.....	26
3.2 Proposed PLL architecture.....	28

3.3 Behavioral simulation	32
3.3.1 Design methodology	32
3.3.2 Design of loop filter	35
3.3.3 Phase-domain behavioral models	40
3.3.4 Voltage-domain behavioral models	42
3.3.5 Simulation results	48
Chapter 4 Design of a high-performance charge pump for low-voltage PLLs	53
4.1 Charge pump design considerations	53
4.2 Previous state-of-the-art design techniques	54
4.3 Design of the proposed charge pump circuit	59
4.4 Simulation results and comparison	64
Chapter 5 A 1.2 V fully integrated CMOS PLL frequency synthesizer for 5-GHz WLAN	68
5.1 Design specifications	68
5.1.1 WLAN 802.11a overview	68
5.1.2 Output frequency range	69
5.1.3 Supply voltage	70
5.1.4 Phase noise and spurious suppression	70
5.1.5 Summary of design specifications	71
5.2 Synthesizer architecture	71
5.3 Circuit implementation	74
5.3.1 PFD	74
5.3.2 Charge pump	77
5.3.3 Lock detector	81

5.3.4 Programmable frequency divider.....	82
5.3.5 VCO.....	94
5.3.6 Output buffer.....	100
5.4 Layout considerations	101
5.5 Closed-loop simulation results.....	105
Chapter 6 Conclusion and recommendation	109
6.1 Conclusion	109
6.2 Recommendations for future research	110
Author's Publications	112
Bibliography	113

List of Abbreviations

64-QAM	64-Level Quadrature Amplitude Modulation
AC	Alternating Current
AMS	Analog Mixed-Signal
BER	Bit-Error-Rate
CMOS	Complementary Metal-Oxide-Semiconductor
CP	Charge Pump
CPPLL	Charge-Pump Phase-Locked Loop
CSM	Chartered Semiconductor Manufacturing
DC	Direct Current
E-TSPC	Extended True Single-Phase Clock
FFT	Fast Fourier Transform
IF	Intermediate Frequency
LD	Lock Detector
LO	Local Oscillator
MIM	Metal-Insulator-Metal
NMOS	N-channel Metal-Oxide-Semiconductor
OFDM	Orthogonal Frequency Division Multiplexing
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PMOS	P-channel Metal-Oxide-Semiconductor
PSRR	Power Supply Rejection Ratio
PVT	Process, (supply) Voltage and Temperature

RF	Radio Frequency
SCL	Source-Coupled Logic
SNR	Signal-to-Noise Ratio
SOC	System-On-Chip
TSPC	True Single-Phase Clock
U-NII	Unlicensed National Information Infrastructure
VCO	Voltage-Controlled Oscillator
WLAN	Wireless Local-Area Network

List of Figures

Figure 1.1 Block diagram of a single-chip CMOS transceiver [1] for IEEE 802.11a/b/g	4
Figure 2.1 Block diagram of a PLL	9
Figure 2.2 Block diagram of a CPPLL	10
Figure 2.3 Characteristic of the PFD	11
Figure 2.4 Linear time-invariant phase-domain model of a CPPLL	11
Figure 2.5 Linear phase-domain noise model of a CPPLL.....	13
Figure 2.6 Transfer function of noise sources. (a) Transfer function of in-band noise sources (b) Transfer function of VCO noise.....	15
Figure 2.7 Power spectrum of PLL output signal with phase noise and spurious tones	16
Figure 2.8 Effect of phase noise of LO signal	17
Figure 2.9 Effect of spurs of LO signal	18
Figure 2.10 Identical I_{up} and I_{down} generating zero average current to the loop filter.	19
Figure 2.11 Block diagram of an integer- N frequency synthesizer	22
Figure 2.12 Block diagram of pulse-swallow frequency divider.....	23
Figure 2.13 Block diagram of a fractional- N frequency synthesizer.....	25
Figure 3.1 Block diagram of the proposed PLL architecture	29
Figure 3.2 Linear model of the proposed PLL architecture.....	30
Figure 3.3 The hierarchical design flow	33
Figure 3.4 Dual-path third-order passive loop filter	36
Figure 3.5 Phase-domain behavioral model of the proposed PLL architecture.....	41

Figure 3.6 Simulation setup for an AC analysis	42
Figure 3.7 Voltage-domain behavioral model of the proposed PLL architecture	44
Figure 3.8 Finite state machine of a PFD	44
Figure 3.9 PFD transfer function (a) without dead zone, (b) with dead zone	44
Figure 3.10 Block diagram of a dead-zone-free PFD	46
Figure 3.11 Block diagram of a lock detector	47
Figure 3.12 Bode plots of the adaptive loop during frequency jump (solid lines) and in the locked state (dashed lines)	50
Figure 3.13 Transient simulation results of the adaptive PLL using the behavioral model	51
Figure 3.14 Transient response of the control voltage, V_c , during locking in a conventional single-loop PLL using the behavioral model	51
Figure 3.15 Output spectrum of the synthesizer using the behavioral model.....	52
Figure 4.1 Conventional charge pump model and PLL output spectrum with reference spurs due to non-ideal effects of the charge pump	54
Figure 4.2 Charge pump with unity-gain buffer	55
Figure 4.3 Charge pump with unity-gain buffer and feedback network.....	56
Figure 4.4 Charge pump with an active loop filter	57
Figure 4.5 Charge pump with NMOS current steering switches	58
Figure 4.6 Simplified circuit diagram of the proposed charge pump	60
Figure 4.7 Bode plot of the feedback loop in the charge pump reported in [44].....	62
Figure 4.8 Bode plot of the feedback loop in the proposed charge pump	62
Figure 4.9 Schematic of the error amplifier used in the proposed charge pump	63
Figure 4.10 Simulation setup for the transient analysis of the charge pump.....	64

Figure 4.11 Output waveforms of the up and down currents. Transient current at (a) the source node of M8, and (b) the drain node of M12	65
Figure 4.12 Simulation results for the mismatch of up and down currents as a function of the output voltage	66
Figure 4.13 (a) The plot of average up and down output currents as a function of input pulse width (b) Zoom-in view of the plot near the origin	67
Figure 5.1 Frequency allocation of IEEE 802.11a standard	69
Figure 5.2 Block diagram of the proposed synthesizer architecture.....	74
Figure 5.3 Block diagram of a PFD combined with a charge pump	75
Figure 5.4 Circuit implementation of a PFD without dead zone	76
Figure 5.5 Output waveforms of the PFD when the PLL is locked.....	77
Figure 5.6 Circuit diagram of charge pump CP1	78
Figure 5.7 Circuit diagram of the charge pump CP2.....	79
Figure 5.8 Comparison of pre-layout and post-layout simulation results for charge pump current mismatch.	79
Figure 5.9 (a) Plot of the average charge pump output current as a function of input phase error of the PFD (b) Zoom-in view of the PFD gain curve in (a).....	80
Figure 5.10 Circuit diagram of the lock detector.....	81
Figure 5.11 Conceptual operation of the lock detector (a) when the PLL is out of lock (b) when the PLL is locked.....	82
Figure 5.12 Frequency divider architecture	82
Figure 5.13 Divide-by-2 Circuit (a) Block diagram (b) SCL latch	84
Figure 5.14 Sensitivity curve of the divide-by-2 circuit.	85
Figure 5.15 Schematic of high-speed clock buffer	86

Figure 5.16 Block diagram of the dual-modulus divide-by-8/9 prescaler	87
Figure 5.17 Timing diagrams of the divide-by-8/9 prescaler	88
Figure 5.18 TSPC divide-by-2 circuit.....	89
Figure 5.19 E-TSPC divide-by-2/3 circuit.....	90
Figure 5.20 Simulated waveforms of the dual-modulus divide-by-8/9 prescaler.....	91
Figure 5.21 Simulated maximum operating frequency of the prescaler versus power supply voltage	91
Figure 5.22 Simulated power consumption of the prescaler at maximum operating frequency, F_{max} , versus power supply voltage.....	92
Figure 5.23 Block diagram of the programmable pulse-swallow frequency divider .	92
Figure 5.24 Schematic diagram of the programmable pulse-swallow counter.....	94
Figure 5.25 Conceptual illustration of negative skewed delay scheme	96
Figure 5.26 Three-stage ring oscillator with dual-delay paths	97
Figure 5.27 Delay cell with both coarse and fine frequency tunings	98
Figure 5.28 Frequency tuning characteristics of the ring-VCO. (a) Pre-layout simulation results of frequency vs. fine-tuning voltage with coarse-tuning voltage ranging from 0 V to 1 V at 0.1 V intervals (b) Post-layout simulation results of the frequency tuning characteristics	99
Figure 5.29 The high-speed output buffer	100
Figure 5.30 Overall layout view of the frequency synthesizer	103
Figure 5.31 Layout of the 3-stage ring-VCO.....	104
Figure 5.32 Layout of the charge pump.....	104
Figure 5.33 Post-layout transient waveforms of the adaptive-PLL synthesizer	105
Figure 5.34 Frequency synthesizer output spectrum at 5.36 GHz.....	106

Figure 5.35 Simulated total phase noise of the frequency synthesizer along with noise contributions from building blocks.....107

List of Tables

Table 3.1: Design parameters for the loop filter	38
Table 3.2 Component values in the loop filter for various c and fixed value of $r = 140$	
Table 3.3 Simulated settling time versus c with $r = 1$ using behavioral models	50
Table 5.1 Design specifications for the experimental prototype	71
Table 5.2 Summary of layout considerations and techniques	101
Table 5.3 Performance summary of the proposed frequency synthesizer	108

Chapter 1

Introduction

1.1 Motivation

Radio frequency (RF) wireless communication has undergone an incredible development over the past few decades. With the proliferation of IEEE 802.11a/b/g standards for wireless local-area network (WLAN), the widespread use of mobile wireless terminals in the last decade indicates a great opportunity for adoption of wireless technology at a mass-market level, and it has led to growing demand for wireless transceivers with low cost, small form factor, and low power. The most effective way to save production cost and to minimize form factor is to implement the entire wireless transceiver on a single chip with the aid of improving large-scale low-cost integration technology. CMOS technology is more feasible and more promising due to the possibility to offer the lowest cost solution as well as the potential to realize the highest integration of digital functions with the front-end circuits.

Although the aggressive scaling of CMOS technology has provided faster and smaller transistors to increase operation frequency and to reduce chip area, it poses other design considerations in single-chip transceiver integration. As CMOS technology scales to deep-submicron or further to nano-scale dimensions, the supply voltage must also be scaled down so as to avoid gate oxide breakdown. The threshold voltages of CMOS transistors are reduced as well, but they are not scaled in the same proportion as the channel length and the supply voltage because the threshold voltage

must be high enough to overcome the effect of leakage. For digital circuits, the dynamic power is proportional to the square of the supply voltage, and that is why lowering the supply voltage has been an efficient method to save power and to extend battery life. However, to maintain compatibility with digital circuits in single-chip wireless transceiver systems, it is necessary that the analog parts are designed to operate at the same low supply voltage. This is challenging as such a low-voltage constraint significantly degrades the performance of traditional analog circuits unless large currents are used, which will result in undesirably large power consumption. Therefore, novel circuit techniques need to be developed to maintain the same performance with an acceptable power consumption level under the low supply voltage. Moreover, due to the high frequency parasitic effects and high noise property of standard digital CMOS process, real single-chip CMOS transceivers [1, 2] were only recently implemented. One of the greatest challenges in single-chip CMOS transceiver integration is the design of a fully-integrated low noise frequency synthesizer with low supply voltage and low power consumption.

Figure 1.1 [1] shows the architecture of a direct conversion transceiver that has been integrated on a single chip. Local oscillators (LOs) are required to down-convert or up-convert RF signals with minimum signal-to-noise ratio (SNR) degradation. The LO signals are generated by integrated frequency synthesizer, which is one of the most critical building blocks in any wireless transceiver systems. Generally, there are three types of frequency synthesizers, including the table-look-up synthesizer, the direct synthesizer, and the phase-locked loop (PLL) synthesizer [3]. The PLL-based synthesizer has the distinct advantage of lower power consumption with a smaller

chip area over the other types of synthesizers, and it is most suitable for low-voltage single-chip CMOS transceiver systems.

There are many challenges in the design of fully integrated CMOS PLL-based frequency synthesizer. First of all, the synthesizer should have very good phase noise and spurious performance, so that the output frequency of the synthesizer is stable and accurate. The trend towards low-cost system-on-chip (SOC) radio transceivers has resulted in an increasingly noisy environment which perturbs the operations of sensitive circuit blocks, such as frequency synthesizers. At the same time, digital modulation techniques employed in new generations of wireless standards pose stringent requirements on the spectral purity of LO signals. To avoid SNR degradation of the radio receiver due to reciprocal mixing of adjacent channels, frequency synthesizer design with low reference spurs is highly desired. Second, the synthesizer should provide a sufficiently wide frequency tuning range to cover the entire frequency band of interest, and at the same time, to compensate for any frequency deviation due to process variation. Under a low supply voltage, the control voltage of the voltage-controlled oscillators (VCO) becomes limited, resulting in a large VCO gain, and worse phase noise and spurious performance. Moreover, due to the fact that the tuning characteristics of VCOs exhibit nonlinearity, i.e. the gain of VCO is not a constant, phase noise can vary dramatically over the tuning range of a VCO. It is challenging to obtain simultaneously a large tuning range, low phase noise and small phase noise variation in low-voltage low-power synthesizer design. Finally, for SOC applications, fluctuations in the internal power supply voltage can be a major cause of jitter for integrated frequency synthesizer. Therefore, it is crucial to

develop circuit techniques to improve power supply rejection ratio (PSRR) for the PLL.

Figure 1.1 Block diagram of a single-chip CMOS transceiver [1] for IEEE 802.11a/b/g

1.2 Objectives

The objective of this project is to design a low-voltage fully-integrated CMOS frequency synthesizer for WLAN 802.11a application. Assuming a direct-conversion transceiver with the LO frequency equal to the RF frequency, this frequency synthesizer is targeted for indoor communication with the output frequency ranging from 5.14 GHz to 5.36 GHz. The focus of this research is on the design techniques for reducing reference spurs while maintaining acceptable settling time, through improvements in system architecture as well as the charge pump circuit design.

1.3 Major contribution of the thesis

A major challenge in fully-integrated frequency synthesizer design is to meet stringent and conflicting requirements posed by different performance aspects, such as spectral purity and settling time. In this work, various circuit techniques to reduce reference spurs and phase noise of the PLL are extensively explored. Design for optimal spectral purity performance often causes the settling performance to be traded off, due to different requirements on the loop bandwidth and on the location of the zeros and poles of the closed-loop transfer function. A spur-reduction technique has been proposed to accomplish low reference spurs while maintaining fast settling time for a fully integrated 5-GHz frequency synthesizer. The proposed PLL architecture smoothly adapts the loop parameters according to different operating modes, so as to reduce the loop bandwidth in the locked state to further attenuate the reference spurs. In addition, a charge pump circuit, which has superior current matching performance, is incorporated with the adaptive PLL. The proposed charge pump circuit achieves current mismatch of less than $\pm 0.5\%$ for the output voltage range from 0.1 V to 1.1 V under a supply voltage of 1.2 V, by applying a replica biasing technique with an improved feedback structure that provides more stable operation. The percentage current mismatch of $\pm 0.5\%$ is based on systematic mismatch, which excludes effects such as process and temperature variations. The charge pump is able to operate under a low supply voltage of 1.2 V in a 0.18- μm CMOS process. Other non-ideal effects, which also cause spurs, such as feed-through of the input pulses, charge sharing and timing mismatch of input signals are also significantly reduced in the proposed charge pump design. A fully integrated PLL-based frequency synthesizer has been designed to verify the effectiveness of the

proposed spur-reduction techniques. To accelerate the design process, with the aid of voltage-domain behavioral models built using Verilog-AMS language, a hierarchical design approach, which comprises a top-down design process followed by a bottom-up verification process, is adopted in the frequency synthesizer design. Post-layout simulation proves that the synthesizer, operating with a supply voltage of 1.2 V in a 0.18- μm CMOS process, achieves a low reference spur level of -60 dBc and a fast settling time of less than 30 μs for a frequency jump from 5.14 GHz to 5.36 GHz. A prototype chip of the synthesizer is to be fabricated using Chartered Semiconductor Manufacturing (CSM) 0.18- μm one-poly six-metal CMOS process.

1.4 Organization of the thesis

This thesis is composed of six chapters. In Chapter 2, the fundamentals of the PLL-based frequency synthesizer including its basic theory of operation, noise characteristics, and key performance parameters such as frequency tuning range, phase noise, spurs and settling time, are reviewed. Various synthesizer architectures and their pros and cons are discussed. Chapter 3 starts with a brief analysis on the existing spur-reduction techniques, followed by the demonstration of the proposed adaptive synthesizer architecture. The hierarchical design approach is briefly explained before elaborating on system-level design aspects, including derivation of synthesizer specifications for WLAN 802.11a application, loop filter design, behavioral modeling and system simulations of the proposed frequency synthesizer. Chapter 4 concentrates on analysis and design of the charge pump circuit. Design considerations and state-of-the-art design techniques are reviewed. After that, the design of a low-voltage high-performance charge pump circuit suitable for PLL-

based frequency synthesizer with low spurious tone requirement is presented. Circuit simulations results and comparisons are included. In Chapter 5, the design of a low-voltage fully-integrated CMOS frequency synthesizer, which adopts adaptive PLL architecture with high-performance charge pump design, is described. The circuit implementation of other building blocks is also elaborated. It includes the phase-frequency detector (PFD), the lock detector, the programmable frequency divider, the VCO and the output buffer. Besides circuit simulations results, layout considerations are also discussed. Finally, Chapter 6 concludes the thesis with a summary of research achievements and some recommendations for further research.

Chapter 2

Fundamentals of the PLL frequency synthesizer

The wireless transceivers employ LOs to down-convert or up-convert RF signals. In order to generate high frequency and stable LO signals, and to vary the output frequency in small and precise steps, frequency synthesis is important. Among many choices, the PLL-based frequency synthesizer is the most popular one, particularly for CMOS RF transceiver systems. This chapter reviews some fundamentals of the PLL frequency synthesizer.

2.1 Phase-locked loop overview

A PLL is a negative feedback system that locks the output phase or frequency to an accurate reference. A typical block diagram of a PLL is shown in Figure 2.1. Basically, a PLL system consists of a phase detector, a loop filter, a VCO and a frequency divider. The basic operation of a PLL is as follows. The phase detector acts as a ‘phase-error amplifier’ to sense the phase difference between the output signal of the divider and the reference clock. The error signal is then low-pass filtered and drives the oscillator. The filtered error signal acts as a control signal of the oscillator and adjust the frequency of oscillation. The frequency of oscillation is divided down to the feedback clock by a frequency divider. Over time, the phase difference, $\Delta\theta$, between the feedback clock and the reference clock tends to be minimized. The loop is considered locked if $\Delta\theta$ becomes constant with time, and the

frequency of the VCO is equal to the frequency of the reference clock multiplied by N .

Figure 2.1 Block diagram of a PLL

In the presence of a large frequency difference, a simple phase detector does not always generate the error signals in the correct direction, as the linear range of phase detector characteristic is only $\pm 180^\circ$ from the center. The average phase detector output contains little frequency information, so the phase detector is insensitive to frequency difference at the input. This will limit the acquisition range of the PLL. Upon start-up, if the frequency of the feedback signal is far from the reference frequency, the PLL may fail to lock. This problem can be solved by incorporating a PFD and a charge pump instead of a simple phase detector in the PLL architecture. This type of PLL is called the charge-pump PLL (CPPLL). Figure 2.2 shows the block diagram of a CPPLL. The combination of a PFD and a charge pump offers two important advantages over the simple phase detector approach. First, since the PFD is able to detect both phase and frequency difference, it significantly increases the acquisition range and lock speed of PLLs. Thus, the capture range is only limited by the VCO output frequency range. Second, the static phase error is zero if mismatches and offsets are negligible [4].

Figure 2.2 Block diagram of a CPPLL

The CPPLL is often analyzed using a linear time-invariant model shown in Figure 2.4. This type of model is useful in analyzing loop stability and the noise contributed by individual building blocks to the output of the PLL. The PFD produces *up* and *down* signals to drive the charge pump to charge or discharge the loop filter so as to generate the control voltage for the VCO. As illustrated in Figure 2.3, the linear range of the PFD characteristic is from -2π to $+2\pi$. The actual phase response is not linear since phase is cyclical, and in reality the phase information is discrete, sampled at the reference frequency. Therefore, the linear time-invariant model is an approximation, the error due to which is negligible if the PLL bandwidth is $1/10^{\text{th}}$ or smaller than the reference frequency [5]. This model is also referred to as the phase-domain model as the input and output are phases rather than voltages.

Figure 2.3 Characteristic of the PFD

Figure 2.4 Linear time-invariant phase-domain model of a CPPLL

Suppose the loop begins with a phase error, θ_e , then with a linear time-invariant approximation, the average current charging the loop filter is given by

$$I_{cp-out} = I_{cp} \frac{\theta_e}{2\pi} \quad (2.1)$$

Therefore, the PFD in a CPPLL has a gain of $K_\phi = \frac{I_{cp}}{2\pi}$, where I_{cp} is the charge pump current. The VCO is modeled as an integrator with a gain of K_{vco} in rad/V; this is to convert output frequency of the VCO into a phase. The loop filter is modeled with $Z(s)$. The order of the PLL system is defined by the number of poles in the loop filter transfer function, plus the fundamental pole of the VCO.

The forward gain transfer function of the linear time-invariant model can be written as

$$G(s) = \frac{K_{\phi} \cdot K_{vco} \cdot Z(s)}{s} \quad (2.2)$$

The frequency divider divides the output frequency (and phase after integration) by a factor of N such that the feedback gain is

$$H = \frac{\theta_{fb}}{\theta_{out}} = \frac{1}{N} \quad (2.3)$$

Then the open loop transfer function can be expressed as

$$G(s) \cdot H = \frac{K_{\phi} \cdot K_{vco} \cdot Z(s)}{s \cdot N} \quad (2.4)$$

The closed loop transfer function of the PLL involves an output phase divided by an input phase, and is shown below

$$\frac{\theta_{out}}{\theta_{ref}} = \frac{G(s)}{1 + G(s) \cdot H} \quad (2.5)$$

2.2 Noise characteristics

The overall PLL output noise is determined by the noise contributions of all blocks in a PLL. The transfer functions from different noise sources to the output can be derived based on the linear phase-domain model [6, 7] of a PLL with additive noise sources as shown in Figure 2.5. In this model, θ_{ref} denotes the noise in $rad/\sqrt{Hz}$ that appears at the reference input to the PFD. θ_{div} is the noise due to the frequency divider in $rad/\sqrt{Hz}$. θ_{pfd} represents the noise of PFD in $rad/\sqrt{Hz}$. θ_{vco} models the phase noise of the VCO in $rad/\sqrt{Hz}$. $v_{n, cnt}$ is the noise appears at the VCO control voltage in $V/\sqrt{Hz}$, and $i_{n, cp}$ is the noise of the charge pump current in $A/\sqrt{Hz}$. The noise transfer functions can be written as:

$$T_{ref}(s) = \frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{G(s)}{1 + G(s) \cdot H} \quad (2.6)$$

$$T_{div}(s) = \frac{\theta_{out}(s)}{\theta_{div}(s)} = \frac{G(s)}{1 + G(s) \cdot H} \quad (2.7)$$

$$T_{pfd}(s) = \frac{\theta_{out}(s)}{\theta_{pfd}(s)} = \frac{G(s)}{1 + G(s) \cdot H} \quad (2.8)$$

$$T_{cp}(s) = \frac{\theta_{out}(s)}{i_{n,cp}(s)} = \frac{1}{K_\phi} \cdot \frac{G(s)}{1 + G(s) \cdot H} \quad (2.9)$$

$$T_{vco}(s) = \frac{\theta_{out}(s)}{v_{n,vco}(s)} = \frac{K_{VCO}}{s} \cdot \frac{1}{1 + G(s) \cdot H} \quad (2.10)$$

$$T_{vco}(s) = \frac{\theta_{out}(s)}{\theta_{vco}(s)} = \frac{1}{1 + G(s) \cdot H} \quad (2.11)$$

Figure 2.5 Linear phase-domain noise model of a CPPLL

It is shown that the closed loop responses to reference, divider, PFD and charge pump noise signals, all contain a common factor in their transfer functions. The common factor is given below

$$\frac{G(s)}{1 + G(s) \cdot H} \quad (2.12)$$

All of these noise sources are known as in-band noise sources. Using the Equations (2.2) and (2.3), and the fact that $G(s)$ has a low-pass characteristic, the following transfer function yields

$$\frac{G(s)}{1 + G(s) \cdot H} \approx \begin{cases} N & \text{for } \omega \ll \omega_c \\ G(s) & \text{for } \omega \gg \omega_c \end{cases} \quad (2.13)$$

where ω_c is the loop bandwidth. It is defined by the cross-over frequency at which the loop gain is equal to 1, that is

$$|G(j \cdot \omega_c) \cdot H| = 1 \quad (2.14)$$

The transfer functions of VCO and VCO control line noise sources have a different common factor, which is

$$\frac{1}{1 + G(s) \cdot H} \quad (2.15)$$

It can be approximated that

$$\frac{1}{1 + G(s) \cdot H} \approx \begin{cases} \frac{N}{G(s)} & \text{for } \omega \ll \omega_c \\ 1 & \text{for } \omega \gg \omega_c \end{cases} \quad (2.16)$$

Based on Equations (2.14) and (2.16), the transfer functions of in-band noise sources and VCO noise can be plotted as in Figure 2.6(a) and 2.6(b) respectively. It can be seen that the VCO noise is high-passed to the PLL output, whereas that of the in-band noise sources exhibits low-pass characteristic. Inside the loop bandwidth, the output noise of the PLL is dominantly contributed by the reference, divider, PFD and charge pump noises. The VCO and the control line noises are suppressed at lower frequencies, and the VCO noise dominants beyond the loop bandwidth. Thus, the choice of loop bandwidth has a great impact on the total PLL noise shape.

Theoretically, for optimal noise performance, the loop parameters should be chosen at the intersection of in-band noise and VCO noise [6].

Figure 2.6 Transfer function of noise sources. (a) Transfer function of in-band noise sources

(b) Transfer function of VCO noise

2.3 Key performance parameters of frequency synthesizer

2.3.1 Frequency tuning range

According to the usage models and the regulations of governing body, each communications standard utilizes a specific frequency band in the spectrum of electro-magnetic waves. For example, the IEEE 802.11a standard specifies operation over a 300-MHz allocation of spectrum in the 5-GHz unlicensed national information infrastructure (U-NII) band [8].

In the PLL-based frequency synthesizer, the tuning range of the VCO determines the limit on the tuning range of the overall system. The tuning range of the VCO should be much larger than the frequency band of interest to compensate for process variations and modeling inaccuracy. Besides, the linear output voltage range of the charge pump could further limit the tuning range of the synthesizer. Therefore, to ensure the synthesizer can operate properly, both the tuning range of the VCO and the charge pump output range must be accounted for in the synthesizer design.

2.3.2 Phase noise

In the time domain, the PLL output signal $V(t)$ with timing jitter can be expressed as

$$V(t) = V_o \sin(\omega_o t + \theta(t)) \quad (2.17)$$

where ω_o is the fundamental frequency, and $\theta(t)$ is the phase variation.

The phase variation, $\theta(t)$, has a random part and a deterministic part as shown below

$$\theta(t) = \theta_r(t) + \theta_d \sin(\omega_d t) \quad (2.18)$$

The random part, $\theta_r(t)$, accounts for phase noise and the deterministic part, $\theta_d \sin(\omega_d t)$, for spurious tones.

Phase noise is a measure of the spectral purity of a signal and is one of the most important parameters for characterization of the synthesizer. As shown in Figure 2.7, phase noise is exhibited as a skirt around the carrier frequency in the power spectrum.

Figure 2.7 Power spectrum of PLL output signal with phase noise and spurious tones

By definition, it is the ratio of the noise power, in a bandwidth of 1 Hz at a certain offset frequency Δf from the carrier, to the total carrier power, as shown in Equation (2.19).

$$L(\Delta f) = 10 \log \left(\frac{P_{noise} \text{ in 1Hz bandwidth at } \Delta f \text{ offset}}{P_{carrier}} \right), \quad (2.19)$$

where $L(\Delta f)$ is the phase noise in units of decibels per hertz (dBc/Hz).

The higher the required SNR of an RF system is, the better the phase noise for an LO is expected. As shown in Figure 2.8, if the LO signal has a phase noise skirt, both the desired RF signal and the interference will be mixed down to the intermediate frequency (IF). After mixing, the interferer can fall directly in the same band as that of the desired signal. Since the power of the interferer is quite large, the noise down-converted to the frequency of the desired signal can significantly degrade the SNR of the desired signal.

Figure 2.8 Effect of phase noise of LO signal

To fulfill the required SNR of an RF system, the phase noise of the frequency synthesizer should satisfy the following condition

$$L(\Delta f) < S_{RF} - S_{block} - 10 \log_{10}(BW) - SNR \quad (2.20)$$

where S_{RF} is the desired RF signal power, S_{block} denotes the blocking signal power, and BW refers to the channel bandwidth of the desired RF signal.

In the PLL-based frequency synthesizer, the phase noise of the output signal comes from various noise sources, such as reference signal, PFD, charge pump, frequency divider, VCO active device noise, etc. The noise characteristics are as illustrated in Section 2.2.

2.3.3 Spurious tone

Other than phase noise, the output signal of the synthesizer can also be modulated by some periodic phase variations resulting in pairs of spurious tones, i.e. spurs, as illustrated in Figure 2.7. It is measured by the difference between powers of the carrier and the spurs at some frequency offset in the unit of dBc. There are several types of spurious tones with different causes. The most common type of spur is the reference spur, appearing at frequencies of $f_o \pm f_{ref}$. Suppose the LO signal is a pure sinusoid with unwanted spurious tones at offset frequencies equal to the channel spacing. As shown in Figure 2.9, as the LO carrier mixes with the desired RF signal, the spurious tones may also mix with the interference at the adjacent channel and translate the interference to the same IF as the desired channel. As a result, the SNR of the desired channel is degraded.

Figure 2.9 Effect of spurs of LO signal

The spur specification, S_{spur} , can be derived based on the specifications of the desired signal power ($S_{desired}$), blocking signal power (S_{block}) and SNR requirement of the system.

$$S_{spur} \leq S_{desired} - S_{block} - SNR \quad (2.21)$$

Reference spurs are generated due to the sampled nature of the CPPLL. Non-ideal effects in the charge pump design, such as leakage and mismatch, are the dominant causes. As illustrated in Figure 2.10, when the PLL is in the locked condition, equal minimum delay pulses of the *up* and *down* signals are generated by the PFD to eliminate the dead zone problem [4], while most of the time the charge pump is in the high impedance state. However, there will be some parasitic leakage through the charge pump, loop filter and VCO. Of these leakage sources, the charge pump leakage tends to be the dominant one, which causes ripples on the VCO control line and results in spurs.

Figure 2.10 Identical I_{up} and I_{down} generating zero average current to the loop filter.

As shown in Figure 2.10, if the currents I_{up} and I_{down} are well matched, the charge pump generates zero average current and zero net charge to the loop filter. However, if there are mismatches between I_{up} and I_{down} , the current pulse widths will become unequal as the following condition must be fulfilled in the locked condition.

$$I_{up} \cdot t_{up} = I_{down} \cdot t_{down} \quad (2.22)$$

Moreover, timing mismatches of *up* and *down* signals from the PFD also affect the current pulse widths and charge pump turn on time. All these cause ripples on the VCO control line so as the spurs.

2.3.4 Settling time

The settling time, also known as locking time, is defined as the time required for a synthesizer to switch from one output frequency to another output frequency within certain frequency accuracy specified by the system requirement. For example, for IEEE 802.11a standard, the frequency accuracy of the output signal must not exceed ± 60 kHz with respect to the desired center frequency.

Loop bandwidth has a direct impact on settling time. The relationship between settling time and loop parameters was shown as [9]

$$t_{lock} = \frac{\ln\left(\frac{f_{step}}{f_{error}}\right)}{f_c \cdot \xi_e(\phi_m)} \quad (2.23)$$

in which,

t_{lock} is the settling time (or locking time)

f_{step} is the amplitude of the frequency jump

f_{error} is the maximum frequency error at t_{lock}

f_c is the loop bandwidth

ϕ_m is the phase margin

ξ_e is the effective damping coefficient at a specified phase margin.

2.4 Synthesizer architectures

The distinct feature that differentiates the PLL frequency synthesizer from other PLLs is the frequency divider. Based on different principles of frequency division, there are two types of synthesizer architectures, namely integer- N and fractional- N frequency synthesizers. Depending on different applications, the choice of synthesizer type is usually made based on criteria such as channel spacing specification, phase noise, settling time, power, complexity, etc.

An integer- N frequency synthesizer, as depicted in Figure 2.11, has an integer division ratio of N , such that $f_{out} = N \cdot f_{ref}$ under the locked condition. Since N is an integer, the reference frequency has to be equal to the desired frequency step or the channel spacing. For narrow-band systems, this implies a lower loop bandwidth and thus longer settling time, because the loop bandwidth is typically much less than one-tenth of the reference frequency to ensure a proper linear operation of the PLL [5]. Moreover, integer- N architecture could incur a large division ratio for narrow-band high-frequency applications, and gives rise to larger power consumption for the divider and higher phase noise at the synthesizer output. For high frequency of operation, it is impractical to build the programmable frequency divider of Figure 2.11 directly at the RF frequency. Instead, the most popular implementation of the programmable frequency divider is using dual-modulus prescaler incorporated with pulse-swallow counters [10, 11], as illustrated in Figure 2.12. The prescaler is capable of dividing either by N_p or N_p+1 according to the state of the modulus control bit. Upon system reset, the prescaler starts to perform divide-by- (N_p+1) operation while both counter P and swallow counter S start counting the output pulses of the prescaler simultaneously. Swallow counter S keeps counting until a number S is

reached, at which moment the modulus control bit changes its status to switch the prescaler from dividing-by- (N_p+1) to dividing-by- N_p . At the same time, counter P continues to count the output pulses of the prescaler. Once the overflow of counter P is reached, both counters will be reset and the whole operation cycle is repeated.

Therefore, the overall division ratio, N , can be expressed as

$$N = S \cdot (N_p + 1) + (P - S) \cdot N_p = P \cdot N_p + S \quad (2.24)$$

It should be noted that for proper reset by counter P , P must be larger than the largest value of S .

Figure 2.11 Block diagram of an integer- N frequency synthesizer

Figure 2.12 Block diagram of pulse-swallow frequency divider

Since integer- N architecture suffers from limited reference frequency and a high division ratio, it is not suitable for systems with narrow channel spacing and fast settling time requirements. Fractional- N synthesizer is preferred in such systems, as it allows smaller division ratio and wider loop bandwidth. In a fractional- N frequency synthesizer, the division ratio can be a fractional number, and the frequency step can be a fraction of the reference frequency. As a result, the reference frequency can be chosen to be much larger than the frequency step or the channel spacing. As depicted in Figure 2.13, fractional- N architecture incorporates a dual-modulus programmable divider controlled by an accumulator [12]. The reference input provides the clock signal for the accumulator. In every clock cycle of the reference frequency, the accumulator output is incremented by K , which is controlled by the channel selection input. Once the accumulator reaches its overflow, the modulus control bit changes the division ratio from N to $N+1$. So on average, the divider divides the VCO output frequency by $N+1$ for K times and N for $(2^k - K)$ times, assuming a k -bit accumulator. Hence, the average division ratio, N_{ave} , can be calculated as

$$N_{ave} = K \cdot (N + 1) + (2^k - K) \cdot N = N + \frac{K}{2^k} \quad (2.25)$$

Although the fractional- N architecture solves the problem of limitation on the reference frequency, and at the same time offers advantages of smaller N value, improved phase noise and settling time, it does have disadvantages. The most significant one is the generation of spurs in the synthesizer output spectrum. Although the average division is correct, the instantaneous division is incorrect. This causes ripples on the VCO control line in trying to correct for instantaneous phase errors, and therefore spurious tones are generated. A popular solution is to replace the accumulator with higher-order digital Sigma-Delta (Σ - Δ) modulator [12-14] to randomize the channel selection input bits and effectively push the spurious tones to higher frequency offsets for more noise suppression by the loop filter. However, this solution greatly increases the complexity of the synthesizer, and may cause the system to become unstable.

Figure 2.13 Block diagram of a fractional- N frequency synthesizer

The channel spacing for IEEE 802.11a standard is 20MHz, which is considered to be quite wide. For such a system, fractional- N synthesizer would require a reference frequency in hundreds of MHz frequency range. However, fundamental modes of inexpensive quartz crystals are limited to approximately 35MHz [15], and it is impractical to use quartz crystals operating at larger-order overtone modes. Therefore, it is not cost effective and advantageous to design a fractional- N synthesizer for this type of system. Integer- N frequency synthesis is adopted in this research work.

Chapter 3

Adaptive PLL architecture and behavioral simulation

3.1 Existing spur-reduction techniques and limitations

In the PLL-based frequency synthesizer, current mismatch and other imperfections of the charge pump circuit cause periodic ripples on the control line of VCO. As a result, a pair of spurious tones appear at a frequency offset, f_{ref} , from the carrier. By applying narrow-band frequency modulation theory with the small angle approximation, the reference spur level in dBc can be expressed as

$$P_r = 20 \log(i_{out}(f_{ref}) \cdot |Z(f_{ref})| \cdot K_{VCO} / (2f_{ref})), \quad (3.1)$$

where f_{ref} is the reference frequency, i_{out} is the amplitude of ac current component with frequency f_{ref} , $|Z(f_{ref})|$ is the impedance of the loop filter at f_{ref} , and K_{VCO} represents the VCO gain in Hz/V [6].

Equation (3.1) implies three common strategies to achieve good spurious performance. The first strategy is to alleviate non-ideal effects of the charge pump circuit through designing high-performance charge pump [8, 16-20] or calibrating the PFD with a variable delay in its reset path to minimize the PFD turn-on time in the locked state while maintaining dead-zone-free operation [21]. This strategy is crucial for PLL frequency synthesizer design as charge pump imperfection is the major cause of reference spurs. However, to apply this strategy alone may not be sufficient to fulfill low spurs requirement unless the loop filter is also carefully designed for

further spur suppression [9], which is the second strategy. The third strategy is to design the synthesizer with smaller VCO gain so as to reduce noise sensitivity. Many approaches have been reported to achieve a small VCO gain and a wide tuning range simultaneously for a frequency synthesizer. One approach is by dividing a single wide-range tuning curve into several narrow-range subbands with sufficient frequency overlap [22]. In a PLL frequency synthesizer, this is often realized by employing both discrete and continuous tuning controls. Automatic switched-capacitor tuning loop [23, 24] or other digital auto-calibration techniques [25] are incorporated to assign the proper subband for a given channel frequency so that the PLL can be locked within the desired tuning range. However, due to the complex digital frequency calibration that is employed, this approach may suffer from much increased settling time. Another approach to combine a low VCO gain with a wide tuning range is to use dual-path loop filter together with dual-control VCO [26-29]. Even though dual-path loop filter is advantageous to solve the problem of integrating a large loop capacitor on chip [30, 31], the reported techniques may suffer from a worsened spur performance [26, 30], a tradeoff between phase noise and tuning range [27], a tradeoff between noise and speed [28], or increased noise and power [31]. Moreover, the dual-control techniques [26, 27, 29], which are mainly used together with LC VCOs, are not easily applied to ring oscillators.

In this work, a spur-reduction technique, which incorporates high-performance charge pump design with adaptive PLL architecture, is proposed to accomplish low reference spur with fast settling time in a fully integrated CMOS frequency synthesizer for 5GHz WLAN SOC applications. The proposed PLL architecture is

described in the following sections, while the design of high-performance charge pump circuit is presented in Chapter 4.

3.2 Proposed PLL architecture

Equation (3.1) implies that lower loop-filter impedance level at reference frequency offset is required to achieve the desired reference spur level. In practice, this means a smaller loop bandwidth and a higher loop filter order. On the contrary, wider loop bandwidth is desired for faster settling time, which often conflicts with the requirements posed by phase noise and spurious performance. For the abovementioned reasons, it is advantageous to adapt the loop bandwidth according to different operating modes to achieve spur reduction while maintaining a fast settling time. In order to maintain stability for different operating modes, the location of the zero in the transfer function must also be shifted accordingly.

The proposed adaptive PLL architecture is shown in Figure 3.1. The synthesizer comprises two charge pump blocks, CP1 and CP2; with current ratio of $I_{cp2}/I_{cp1} = c$. The two charge pump circuits have their outputs connected to the loop filter in a similar manner to [9], but are controlled in a much simpler way. Only one PFD block and one VCO control line is required in this architecture. Third-order passive loop filter is employed with the additional pole to improve the spur suppression.

Figure 3.1 Block diagram of the proposed PLL architecture

The linear model of the proposed synthesizer is depicted in Figure 3.2. When the PLL is far from locked state, both CP1 and CP2 are active, and the control voltage V_C can be expressed as

$$V_C(s) = c \cdot I_p \cdot \frac{R_a C_2 s + 1}{s(A_2 s^2 + A_1 s + A_0)} + I_p \cdot \frac{(R_a + R_b) C_2 s + 1}{s(A_2 s^2 + A_1 s + A_0)} \quad (3.2)$$

where A_0 , A_1 and A_2 are the loop filter coefficients, and

$$\begin{aligned} A_0 &= C_1 + C_2 + C_3 \\ A_1 &= (R_a + R_b) \cdot C_2 \cdot (C_1 + C_3) + R_3 \cdot C_3 \cdot (C_1 + C_2) \\ A_2 &= (R_a + R_b) \cdot R_3 \cdot C_1 \cdot C_2 \cdot C_3 \end{aligned}$$

The open-loop transfer function, $G_{OL}(s)$, of the synthesizer after a frequency jump is derived as

$$\begin{aligned}
 G_{OL}(s) &= \frac{\theta_{out}(s)}{\theta_e(s)} \\
 &= \frac{(1+c) \cdot I_p \cdot K_{VCO}}{N \cdot s^2} \\
 &\quad \times \frac{\left(\frac{(R_a + R_b) \cdot C_2 + c \cdot R_a \cdot C_2}{1+c} \right) \cdot s + 1}{A_2 s^2 + A_1 s + A_0}
 \end{aligned} \tag{3.3}$$

where N is the division ratio of the frequency divider.

Figure 3.2 Linear model of the proposed PLL architecture

When the phase error becomes small enough and the PLL is nearly in the locked state, the lock detector generates a control signal, LD , to power down the CP2 block, while CP1 remains active. In this manner, the frequency synthesizer makes a smooth transition from wide-bandwidth mode to narrow-bandwidth mode, without switching of loop components which often causes hazardous glitch problems on the VCO control line. Another advantage of the proposed architecture is that the overall power consumption of the synthesizer is not much increased compared to the conventional single-loop architecture, thanks to the power-down feature of the high-current CP2 block.

The open-loop transfer function of the synthesizer in the locked state can be derived by setting $c = 0$ in the expression of $G_{OL}(s)$, so

$$G_{OL}(s)' = \frac{I_p \cdot K_{VCO}}{N \cdot s^2} \times \frac{((R_a + R_b) \cdot C_2 \cdot s + 1)}{(A_2 s^2 + A_1 s + A_0)} \quad (3.4)$$

The shift of the loop bandwidth and the zero location can be studied from the following relationships. First, the total loop filter capacitance, C_T , can be found by setting the magnitude of the open-loop gain equal to one at the cross-over frequency, ω_c . The open-loop transfer function of the proposed PLL can be expressed as

$$\begin{aligned} G_{OL} &= \frac{(1+c) \cdot K_\phi \cdot K_{VCO} \cdot Z(s)}{s \cdot N} \\ &= \frac{(1+c) \cdot K_\phi \cdot K_{VCO} \cdot (1+s \cdot \tau_z)}{N \cdot C_T \cdot s^2 \cdot (1+s \cdot \tau_{p1}) \cdot (1+s \cdot \tau_{p2})} \end{aligned} \quad (3.5)$$

where τ_z is the time constant of the zero, τ_{p1} and τ_{p2} are the time constants of the poles.

From Equation (3.5), we can get

$$C_T = \frac{(1+c) \cdot I_p \cdot K_{VCO}}{N \cdot \omega_c^2} \cdot \sqrt{\frac{1+\omega_c^2 \cdot \tau_z^2}{(1+\omega_c^2 \cdot \tau_{p1}^2) \cdot (1+\omega_c^2 \cdot \tau_{p2}^2)}} \quad (3.6)$$

Then, by assuming $\omega_c \tau_{p1} \ll 1$ and $\omega_c \tau_{p2} \ll 1$, the value of the loop bandwidth can be approximated by

$$\omega_c \approx ((1+c) \cdot I_p \cdot K_{VCO} \cdot \tau_z) / (C_T \cdot N) \quad (3.7)$$

When the loop is in the locked state, the change of zero location is obtained by inspecting the zero in Equation (3.3) and (3.4), that is

$$\tau_z' = \tau_z \cdot (1+c)(1+r)/(1+c+r) \quad (3.8)$$

where $r = R_b/R_a$.

It is evident that the zero of the loop filter moves to a lower frequency without the switching of loop filter components. The low-frequency zero is helpful to increase the phase margin of the PLL in the locked state. Also, the change of loop bandwidth can be derived as

$$\omega_c' \approx \omega_c \cdot (1+r)/(1+r+c) \quad (3.9)$$

Equation (3.9) implies that a smaller value of r is preferred for more effective shift of the loop bandwidth to a lower frequency. For a fixed value of r , the larger the current ratio c is, the greater the loop bandwidth reduction is resulted in when the LD signal is activated, and therefore higher degree of spur suppression can be accomplished. However, the total loop filter capacitance value also increases with the value of c . Too large of a current ratio will result in huge capacitors that are difficult to be integrated. Hence, there exists a range of c , for a constant value of r , which exhibits a good tradeoff between spectrum purity and settling time while maintaining stability for fully integrated synthesizers.

3.3 Behavioral simulation

3.3.1 Design methodology

For a complex mixed-signal system such as a PLL-based frequency synthesizer, transistor-level transient simulation is quite time-consuming. Consequently, it is inefficient or even impractical to verify the synthesizer performance following the traditional bottom-up design approach, in which one starts with the design and verification of the individual blocks before combining the blocks together to form the

system. Alternatively, a hierarchical design methodology [32-34] is promising for accelerating the design process for a PLL-based frequency synthesizer. Illustrated in Figure 3.3 is the hierarchical design approach, which consists of two complementary design processes: top-down design and bottom-up verification.

Figure 3.3 The hierarchical design flow

The top-down process begins with the specification definition, in which all the critical parameters are determined, including architecture, output frequency, reference frequency, division ratio, VCO gain, charge pump current and loop bandwidth. After defining the specifications, behavioral model simulation and optimization can be used for each building block and the whole synthesizer to evaluate different architectures as well as to verify the overall loop performance at the system level. From the system-level simulation, requirements for the individual

circuit blocks are derived. Circuits are then designed individually at the transistor level to meet the specifications, followed by the layout implementation.

Once a block is implemented, bottom-up verification should be followed. To reduce the chance of errors, it is best done with mixed-level simulation procedure, which consists of three steps. First, the proposed block functionality is verified by including an idealized model of the block in system-level simulations. Then, the functionality of the block as implemented is verified by replacing the idealized model with the transistor-level schematic. In this manner, the individual block can be verified in the context of the system, and it allows the effect of imperfections of each block on the system performance to be easily observed. Mixed-level simulation requires that both the system-level simulation and the transistor-level simulation are to be done using the same simulator on the same platform. After the layout implementation, the transistor-level schematic of the block is replaced by an extracted netlist. By comparing the results obtained from simulations that involved the schematic and the extracted netlist, the functionality and accuracy of the extracted view can be verified. From then on, mixed-level simulations of other blocks are carried out more effectively by replacing the idealized model with the extracted view of the block that has just been verified.

In the following sections, design aspects of the loop filter are discussed first before behavioral modeling and system simulations of the proposed PLL architecture are presented.

3.3.2 Design of loop filter

Loop filter is a very crucial component in any PLL, as it determines most of the PLL's key performance parameters, such as loop stability, settling time, phase noise, spurious suppression, etc. Passive loop filters are more popular than active loop filters, because active devices add phase noise, complexity and cost. Nevertheless, in some cases an active filter may be necessary; for example, when the maximum charge pump output range is smaller than the tuning voltage range required for the VCO.

Design of the loop filter begins with a thorough understanding of the system specifications, followed by choosing the proper loop filter topology and loop filter order. Then, by specifying phase margin, loop bandwidth and pole ratios, the time constants of the poles and zeros of the transfer function can be determined. From these, the values of loop filter components can be calculated. Many methods for the calculation of loop filter components have been reported. The time constants can be calculated based on general rule of thumb [3], or by introducing approximations and writing down a closed form approximation solution [35, 36], or using numerical methods to solve more precisely for the time constants [36].

As illustrated in Figure 3.1, a third-order passive loop filter topology is chosen for the proposed adaptive PLL architecture as it provides an additional pole to improve the spur suppression. The configuration of the proposed dual-path third-order loop filter is redrawn in Figure 3.4. As loop filter is designed for a specific loop bandwidth, phase margin, VCO gain, charge pump current and division ratio, the values of these parameters need to be determined first.

The reference frequency of the synthesizer is 10 MHz and the target frequency jump is from 5.14 GHz to 5.36 GHz. Therefore, the maximum and minimum division ratios are

$$N_{\max} = \frac{f_{out,\max}}{f_{ref}} = \frac{5.36\text{GHz}}{10\text{MHz}} = 536 \quad (3.10)$$

$$N_{\min} = \frac{f_{out,\min}}{f_{ref}} = \frac{5.14\text{GHz}}{10\text{MHz}} = 514 \quad (3.11)$$

In order to keep the loop gain relatively constant over the whole frequency span, the division ratio is chosen to be the geometric mean of the maximum and minimum values when designing the loop filter. That is,

$$N_{design} = \sqrt{N_{\max} \cdot N_{\min}} \approx 525 \quad (3.12)$$

Figure 3.4 Dual-path third-order passive loop filter

The required VCO gain is dependent on the required frequency tuning range and the range of the VCO control voltage. As the VCO tuning range is required to be larger than 10% for IEEE 802.11a standard [37], the target of the VCO in this work is to tune from 5.14 GHz to 5.74 GHz, corresponding to a tuning range of 11%. Assuming

a VCO control voltage range over 83% of a supply voltage of 1.2 V, the estimated VCO gain is

$$K_{vco} = \frac{600\text{MHz}}{0.83 \times 1.2\text{V}} = 600\text{MHz/V} \quad (3.13)$$

For the wide-bandwidth mode, the loop bandwidth is set to 500 kHz, *i.e.* 1/20 of the reference frequency. Phase margin is typically chosen from 40 to 55 degrees. Study [9] showed that a phase margin of about 50 degrees yields the optimal locking time. For the charge pump current, I_p , 50 to 100 μA is typical for WLAN applications. As a summary, the values of the above derived parameters are listed in Table 3.1.

Since the reference frequency is more than ten times the loop bandwidth, a third-order passive loop filter can provide the benefit of further reference spurs suppression without significant increase on the die area. Recall that the open-loop transfer function of the 4th – order CPPLL including the dual-path third-order passive loop filter as shown in Figure 3.2 is

$$G_{OL} = \frac{(1+c) \cdot K_\phi \cdot K_{vco} \cdot (1+s \cdot \tau_z)}{N \cdot C_T \cdot s^2 \cdot (1+s \cdot \tau_{p1}) \cdot (1+s \cdot \tau_{p2})} \quad (3.14)$$

where:

$$\tau_z = \frac{(R_a + R_b) \cdot C_2 + c \cdot R_a \cdot C_2}{1+c}, \text{ is the time constant that provides a stabilizing}$$

zero to the loop.

$$\tau_{p1} \approx \frac{(R_a + R_b) \cdot C_1 \cdot C_2}{C_T}, \text{ and}$$

$\tau_{p2} \approx R_3 \cdot C_3$ are the time constants of the poles that suppresses the tone of the reference input and its higher harmonics.

$C_T = C_1 + C_2 + C_3$, is the total loop filter capacitance.

Table 3.1: Design parameters for the loop filter

Symbol	Description	Value
f_c	Loop bandwidth	500 kHz
ϕ	Phase margin	50 °
I_p	Charge pump current	100 μ A
K_{VCO}	VCO gain	600 MHz/V
N	Divider ratio	525

The procedure of determining the time constants is explained as follows. The phase margin of the loop is expressed as

$$\phi = \tan^{-1}(\omega_c \cdot \tau_z) - \tan^{-1}(\omega_c \cdot \tau_{p1}) - \tan^{-1}(\omega_c \cdot \tau_{p2}) \quad (3.15)$$

where $\omega_c = 2\pi f_c$.

If the maximum phase margin is obtained at the cross-over frequency, the locking time of the PLL can be minimized. By setting the derivatives of the phase margin with respect to ω_c equal to zero, the following relationship is obtained

$$\tau_z \approx \frac{1}{\omega_c^2 \cdot (\tau_{p1} + \tau_{p2})} \quad (3.16)$$

By defining the pole ratio, $\tau_{p21} = \tau_{p2} / \tau_{p1}$, and substituting Equation (3.16) into Equation (3.15), the phase margin expression becomes

$$\phi = \tan^{-1}\left(\frac{1}{\omega_c \cdot \tau_{p1}(1 + \tau_{p21})}\right) - \tan^{-1}(\omega_c \cdot \tau_{p1}) - \tan^{-1}(\omega_c \cdot \tau_{p1} \cdot \tau_{p21}) \quad (3.17)$$

To avoid tedious numerical calculations, Equation (3.17) is solved approximately by assuming $\tan(x) \approx x \approx \tan^{-1}(x)$, and thus we have

$$\tau_{p1} \approx \frac{\sec(\phi) - \tan(\phi)}{\omega_c \cdot (1 + \tau_{p21})} \quad (3.18)$$

Once τ_{p1} is known, τ_{p2} and τ_z can be easily found.

$$\tau_{p2} = \tau_{p1} \cdot \tau_{p21} \quad (3.19)$$

$$\tau_z \approx \frac{1}{\omega_c^2 \cdot \tau_{p1} \cdot (1 + \tau_{p21})} \quad (3.20)$$

Next, the component values for the capacitors and resistors are determined. Recall that the total loop filter capacitance, C_T , can be found by setting the magnitude of the open-loop gain equal to one at the cross-over frequency, that is

$$C_T = \frac{(1+c) \cdot I_p \cdot K_{VCO}}{N \cdot \omega_c^2} \cdot \sqrt{\frac{1 + \omega_c^2 \cdot \tau_z^2}{(1 + \omega_c^2 \cdot \tau_{p1}^2) \cdot (1 + \omega_c^2 \cdot \tau_{p2}^2)}} \quad (3.21)$$

Then, the component C_I can be calculated as

$$C_1 \approx \frac{C_T \cdot \tau_{p1}}{(R_a + R_b) \cdot C_2} \cong \frac{C_T \cdot \tau_{p1} \cdot (1 + r + c)}{(1 + r) \cdot (1 + c) \cdot \tau_z} \quad (3.22)$$

The value of the capacitor C_3 needs to be considered carefully. The VCO input capacitance adds to the capacitor C_3 , so this component should be at least four times the VCO input capacitance to minimize the impact of the VCO capacitance variation. In addition, a larger C_3 results in a smaller R_3 , which is desirable to reduce the thermal noise generated from the resistor. On the other hand, the value of C_3 should be kept a few times smaller than C_1 to keep the desired phase margin.

After determining C_1 and C_3 , the value of the rest can be obtained easily.

$$\begin{aligned} C_2 &= C_T - C_1 - C_3 \\ R_a &= \frac{(1+c) \cdot \tau_z}{(1+r+c) \cdot C_2} \\ R_b &= r \cdot R_a \\ R_3 &\approx \frac{\tau_{p2}}{C_3} \end{aligned} \quad (3.23)$$

Lastly, Bode-plot analysis is performed based on the calculated component values to check for loop stability. If enough phase margin and loop bandwidth are achieved, the design is complete, otherwise return to Equation (3.18) to finetune the value of

τ_{p1} and repeat the rest of the steps. For a fixed parameter of $r = 1$, the component values for various c are summarized in Table 3.2.

Table 3.2 Component values in the loop filter for various c and fixed value of $r = 1$

Component parameter	Value						
c	0	3	5	6	7	8	15
τ_{p21}	0.6						
τ_z	8.75×10^{-7}						
τ_{p1}	7.24×10^{-8}						
τ_{p2}	4.34×10^{-8}						
C_T (pF)	32.7	130.8	196.2	228.9	261.6	294.3	523.2
C_1 (pF)	2.7	6.8	10.8	10.8	12.2	13.5	23
C_2 (pF)	29	123	184.4	216.6	248	279.3	498.2
C_3 (pF)	1	1	1	1.5	1.5	1.5	2
R_a (k Ω)	15	5.7	4.1	3.5	3.1	2.8	1.6
R_b (k Ω)	15	5.7	4.1	3.5	3.1	2.8	1.6
R_3 (k Ω)	43.4	43.4	43.4	29	29	29	21.7

3.3.3 Phase-domain behavioral models

As explained in Section 2.1, phase-domain model of the PLL frequency synthesizer provides a linear time-invariant approximation of the system behavior. Based on the block diagram of the synthesizer shown in Figure 3.1, the phase-domain behavioral model is depicted in Figure 3.5.

The behavioral model consists of a voltage-controlled voltage source, with a gain equal to $1/2\pi$, to model the PFD. The two charge pump blocks, CP1 and CP2, are realized by a voltage-controlled current source with a gain of I_p and another voltage-controlled current source with a gain of $c I_p$, respectively. The loop filter is constructed using resistors and capacitors, followed by the VCO modeled by using a voltage-controlled current source together with a 1 F capacitor for integration. The gain of the voltage-controlled current source is equal to the VCO gain, K_{vco} , in rad/Hz.

After the VCO, another voltage-controlled voltage source with a gain equal to $1/N$ is used to model the divider.

The phase-domain behavioral model is simulated using an AC analysis as it is a fast simulation process to verify the stability of the PLL system in the phase domain. The simulation setup is illustrated in Figure 3.6.

Figure 3.5 Phase-domain behavioral model of the proposed PLL architecture

Figure 3.6 Simulation setup for an AC analysis

3.3.4 Voltage-domain behavioral models

Phase-domain behavioral model is efficient in predicting the loop stability of the synthesizer by assuming a linear time-invariant behavior of the system. However, the actual loop behavior is non-linear, and phase-domain model cannot accurately estimate the settling time, and is not suitable to predict the loop dynamic behavior in the time domain. The other approach models the system in terms of voltage, and so is referred to as voltage-domain model. With voltage-domain models, the settling behavior of the loop and several non-ideal effects such as current mismatch of the charge pump and jitter of the VCO can be predicted by transient analysis using Spectre or AMS simulator. Another advantage of voltage-domain model is that mixed-level simulation procedure can be applied during bottom-up verification process as mentioned previously. As the design process reaches the verification stage, the abstract behavioral models can be replaced with detailed transistor-level models in order to verify the synthesizer as implemented. Consequently, design effort in

identifying the building block that may cause malfunction of the system can be greatly reduced.

A block diagram of voltage-domain behavioral model for the synthesizer is shown in Figure 3.7. Each building block is presented in the Verilog-AMS language [32], and can be integrated into Cadence AMS design environment along with Spice models and transistor-level schematics. Verilog-AMS offers powerful statements for efficiently describing event-driven behaviors, which greatly shorten the model development time as well as the simulation time.

A simple PFD model can be built based on the finite state machine [4] as illustrated in Figure 3.8. Such a PFD is likely to have a dead-zone problem as it produces very narrow pulses for small phase errors. Due to the finite rise time and fall time, the pulses may not find enough time to reach the required logic level, failing to turn on the charge pump switches. As a consequence, when the input phase error, θ_e , falls below a certain value, θ_0 , the output of the PFD and charge pump combination is no longer a function of θ_e , and the PLL suffers from a dead zone equal to $\pm \theta_0$ around $\theta_e = 0$ as illustrated in Figure 3.9. Therefore, the VCO will accumulate random phase error of θ_0 with respect to the reference input while receiving no feedback control action, resulting in high jitter in the PLL output.

The actual circuit implementation is based on the block diagram shown in Figure 3.10. It is constructed with two D-type flip-flops and an AND gate in the feedback path for the reset. A delay cell is inserted after the AND gate in the feedback path to ensure that, when the PLL is in steady state, the reset function has sufficient time to maintain *up* and *down* pulses, so that the dead-zone problem can be eliminated. The proposed PFD behavioral model based on the operation of this dead-zone-free PFD

is described by the Verilog-AMS code as shown in List 1. This model is also helpful in studying the dead-zone effect by varying the value of reset pulse delay, td_reset .

Figure 3.7 Voltage-domain behavioral model of the proposed PLL architecture

Figure 3.8 Finite state machine of a PFD

Figure 3.9 PFD transfer function (a) without dead zone, (b) with dead zone

List 1 Proposed behavioral representation of PFD in Verilog-AMS

```

module pfd (ref, fb, up, dn);

    output up, dn; electrical up, dn;
    input ref, fb; electrical ref, fb;
    electrical reset;
    parameter real VDD=1.2;           // Supply voltage
    parameter real vth=VDD/2;         // threshold voltage at input
    parameter integer dir=1 from [-1:1] exclude 0; // dir=1 for positive edge trigger
    parameter real tt=50p from (0:inf); // transition time of output signal
    parameter real td=100p from [0:inf]; // average delay from input to output
    parameter real td_reset=580p from [0:inf];
    integer event_up, event_dn;
    real reset_val;

    analog begin

        @(initial_step)begin
            event_up=0;
            event_dn=0;
        end

        @(cross(V(ref) - vth, dir))
            event_up=1;
        @(cross(V(fb) - vth, dir))
            event_dn=1;
        if(event_up && event_dn)
            reset_val=VDD;
        else
            reset_val=0;
        @(cross(V(reset) - vth, dir))
        begin
            event_up=0;
            event_dn=0;
        end

        V(up) <+ transition((event_up==+1)? VDD:0.0, td, tt);
        V(dn) <+ transition((event_dn==+1)? VDD:0.0, td, tt);
        V(reset) <+ transition(reset_val,td_reset,tt);
    end

endmodule

```

Figure 3.10 Block diagram of a dead-zone-free PFD

For simplicity, the PFD and the charge pump are often modeled together in a single behavioral module [32]. However, in order to facilitate mixed-level simulation, a separate behavioral model for the charge pump is created. The output is modeled as current source, such that when the *up* (*dn*) signal is active, the source current flows into (out of) the loop filter, and therefore the output voltage of the loop filter rises up (drops down). Non-idealities are represented by mismatch of the source and sink currents, similar as the behavioral model in [33]. Following the charge pump module is the loop filter which is constructed using resistors and capacitors.

The lock detector model is built based on the implementation in [38]. As shown in Figure 3.11, it senses the positive rising edge of the *up* and *dn* signals from the PFD, and outputs logic 1 when the PLL is near to the locked state. To make this circuit work properly, the delay time, Δt , needs to be smaller than the minimum pulse width of the PFD outputs. In this work, $\Delta t = 120$ ps is used.

Figure 3.11 Block diagram of a lock detector

The behavioral model for the VCO is constructed using three step operations. First, the desired output frequency is computed by implementing an ideal linear transformation from voltage to frequency based on the following relationship:

$$f_{out} = f_{min} + K_{VCO} \cdot (V_{in} - V_{min}) \quad (3.24)$$

where f_{min} and f_{max} are the minimum and maximum output frequency respectively, V_{min} and V_{max} correspond to minimum and maximum input voltages, and V_{in} represents the input voltage of the VCO. Then, the frequency is integrated to compute the output phase using $idtmod()$ function [32]. Finally, periodic output sine wave is generated using the phase information. Jitter is modeled as a random variation in the frequency of the VCO, converted from the variation in the period which is modeled by dithering the time at which clock switching occurs by random Gaussian variation. As it simply changes the time when existing activity occurs rather than creating additional activity, this model with jitter can run as efficiently as the one without.

The behavioral model of the frequency divider operates by counting input transitions and generating a reset when the correct ratio is reached, and then outputs a 50% duty cycle square-wave signal. In addition, at a point of time, T_{change} , the division ratio is

changed from N_{min} to N_{max} in order to measure the settling time of the output frequency jumping from f_{min} to f_{max} , which is the worst case condition for frequency acquisition.

3.3.5 Simulation results

The parameters and component values used for the synthesizer are given in Table 3.1 and Table 3.2 respectively. By using these parameters, the behavioral simulation results for various values of c and constant parameter of $r = 1$ are summarized in Table 3.3. The loop bandwidth, f_c' , and the phase margin, PM' , in the narrow-bandwidth mode are simulated by AC analysis using the phase-domain behavioral model. As mentioned, the reference frequency of the synthesizer is 10 MHz and the target frequency jump is from 5.14 GHz to 5.36 GHz. The settling time indicates how long a settling takes within frequency accuracy of ± 60 kHz. Transient analysis is performed using the voltage-domain behavioral model to compare the settling time of the proposed PLL architecture and that of the conventional single-loop PLL with CP1 only. It can be seen from Table 3.3 that the settling time is shortened using the proposed PLL architecture, regardless the value of c , while the loop bandwidth is reduced in the locked state by cutting off CP2.

Based on the above analysis and comparison, $c = 7$ is chosen for the synthesizer to accomplish lower reference spurs with fast settling time. It is still feasible to integrate a total capacitance of 261.6 pF on chip without occupying unreasonably large area. Figure 3.12 shows the Bode plots of the proposed PLL architecture for $c = 7$, and with the component values of $C_1 = 12.2$ pF, $C_2 = 248$ pF, $C_3 = 1.5$ pF, $R_a = R_b = 3.1$ k Ω and $R_3 = 29$ k Ω in the loop filter. During frequency jumps both CP1 and CP2

are active. The loop bandwidth in this wide-bandwidth mode is 506 kHz, and the phase margin is 48° . After the frequency jump only CP1 is active, and the PLL is switched to the narrow-bandwidth mode, in which the loop bandwidth is reduced to 135 kHz. The zero of the loop filter moves to a lower frequency, without the switching of loop filter components. The low-frequency zero helps to maintain a phase margin of 46° in the locked state.

Transient waveforms during the frequency jump from 5.14 GHz to 5.36 GHz are illustrated in Figure 3.13. Lock detector output signal, LD , indicates when the transition from the wide-bandwidth mode to the narrow-bandwidth mode takes place. The transient waveform of the VCO control voltage, V_c , shows a smooth transition during the mode changing. When the LD signal stays always as logic 1, the synthesizer is with a lower loop bandwidth and finally settles. As given in Table 3.3, the behavioral simulation shows a settling time of 30 μ s in response to a 220-MHz frequency step. Compared to the case when $c = 0$ (i.e. with CP1 only) as shown in Figure 3.14, the settling time in Figure 3.13 is 33% shorter. With a division ratio of 536 and a reference clock operating at 10 MHz, the output frequency becomes 5.36 GHz. By performing Fast Fourier transform (FFT) analysis of the transient output data, the output spectrum of the synthesizer using the behavioral model without charge-pump imperfection and VCO jitter is displayed in Figure 3.15.

Table 3.3 Simulated settling time versus c with $r = 1$ using behavioral models

c	C_T (pF)	f_c' (kHz)	PM' (deg)	Settling Time with CP1 only (μ s)	Settling Time for proposed architecture (μ s)
0	32.7	500	45	7.5	7.5
3	130.8	223	52	22	15
5	196.2	167	49	36	18
6	228.9	148	48	42	25
7	261.6	135	46	46	30
8	294.3	128	44	55	40
15	523.2	88	36	100	56

Figure 3.12 Bode plots of the adaptive loop during frequency jump (solid lines) and in the locked state (dashed lines)

Figure 3.13 Transient simulation results of the adaptive PLL using the behavioral model

Figure 3.14 Transient response of the control voltage, V_c , during locking in a conventional single-loop PLL using the behavioral model

Figure 3.15 Output spectrum of the synthesizer using the behavioral model

Chapter 4

Design of a high-performance charge pump for low-voltage PLLs

4.1 Charge pump design considerations

In the PLL-based frequency synthesizer, a charge pump is used to charge and discharge the loop filter according to the outputs of the PFD, so that the phase error is converted to a control voltage to adjust the frequency of the VCO. As illustrated in Figure 4.1, when the PLL is in locked condition, equal minimum delay pulses of the *up* and *down* signals are generated by the PFD to eliminate dead-zone problem [4]. If the currents I_{up} and I_{down} are perfectly matched, the charge pump generates zero average current and zero net charge to the loop filter. In reality, nonidealities of the charge pump circuit cause periodic ripples on the VCO control line. As a result, a pair of spurious tones will appear at frequencies of $f_o \pm f_{ref}$ in the output spectrum, which is known as reference spurs. Thus it is clear that charge pump is the dominant block causing reference spurs due to leakage current, current mismatch, and timing mismatch. The total phase offset due to these non-ideal effects can be approximated by [16]

$$\begin{aligned}\Delta\phi_{tol} &= 2\pi(\Delta\phi_{leakage} + \Delta\phi_{mismatch} + \Delta\phi_{timing}) \\ &= 2\pi\left(\frac{I_{leak}}{I_{cp}} + \frac{\Delta i}{I_{cp}} \cdot \frac{t_{on}}{T_{ref}} + \frac{\Delta t_{delay} \cdot t_{on}}{T_{ref}^2}\right)\end{aligned}\quad (4.1)$$

where I_{cp} is the charge pump current, I_{leak} is the leakage current, T_{ref} is the reference clock period, t_{on} is the PFD turn-on time, Δi and Δt_{delay} are the current and timing

mismatches. It is crucial to minimize these non-ideal effects in the charge pump design.

As the switches are connected near to the output node, the conventional charge pump shown in Figure 4.1 also suffers from charge sharing and charge injection problems. The switches are driven by the *up* and *down* output signals of the PFD. When both switches are turned off, the voltages at nodes s1 and s2 are pulled to V_{DD} and ground respectively. After the switches are turned on again, charge distribution occurs between the output load capacitor and the parasitic capacitors of the switching transistors due to the voltage differences between the output of the charge pump and the voltages at nodes s1 and s2. The charge distribution causes ripples at the output of the loop filter, resulting in spurs at the synthesizer output spectrum.

Figure 4.1 Conventional charge pump model and PLL output spectrum with reference spurs due to non-ideal effects of the charge pump

4.2 Previous state-of-the-art design techniques

In order to avoid charge sharing, the voltages of nodes s1 and s2 should be held at the same level as the output voltage. Figure 4.2 shows an improved charge pump

topology [39], in which a dummy branch consisting of switches M1b and M2b are added to prevent nodes s1 and s2 from being discharged and charged. In addition, with a unity-gain buffer, the voltages at nodes s1 and s2 are maintained at the same potential of the output node. Although the charge sharing effect can be suppressed, the input common mode and output of the buffer must be able to achieve a sufficiently wide dynamic range so that the available tuning range of the VCO is not sacrificed. Therefore, a rail-to-rail buffer needs to be designed and this greatly increases the design complexity of the charge pump. Another drawback of this design is the feed-through of the *up* and *dn* switching signals which is unavoidable since the switching transistors are connected to the output node directly. In addition, current mismatch is present due to channel length modulation effect, impedance mismatch between PMOS and NMOS transistors, and process variations.

Figure 4.2 Charge pump with unity-gain buffer

The charge pump topology shown in Figure 4.3 [8] improves on better matching of *up* and *down* currents. Through replica bias and a feedback network, the output

voltage is tracked to be equal to V_r , and I_{up} is adjusted to be equal to I_{dn} by the feedback error amplifier. Again, a rail-to-rail buffer needs to be designed, and the input dynamic range of the op amp should be sufficiently wide as well. This greatly increases the power consumption as well as design complexity of the charge pump circuit. Besides, adding transistors, operating in deep triode region, between the switches and the output is insufficient to eliminate feed-through of up and down currents.

Figure 4.3 Charge pump with unity-gain buffer and feedback network

Another improved design implements the charge pump together with an active loop filter [40] as illustrated in Figure 4.4. The rail-to-rail unity-gain buffer is not needed in this design because the output of the charge pump is isolated from the control path of the VCO. Hence, the tuning range of the VCO depends on the output stage of the

op amp in the active loop filter rather than the output of the charge pump. As the output of the charge pump is biased at a reference voltage, V_{ref} , the current mismatch can be reduced. Dummy switches M1c, M1d, M2c and M2d are added to provide complementary charges so as to minimize the error at the loop filter due to clock feed-through and charge injection. However, the mismatch in output impedance seen by the drain nodes of M1a and M1b may deteriorate current matching. Moreover, the active loop filter could introduce more phase noise due to the active devices.

Figure 4.4 Charge pump with an active loop filter

Another popular type of charge pump circuits makes use of NMOS current steering switches only, whereby the inherent mismatch of PMOS and NMOS switches can be avoided. An example of such a configuration is illustrated in Figure 4.5. A few modifications have been made based on this configuration. In [19], a wide-swing current mirror is used at the charge pump output to boost the output impedance, but it suffers from output headroom limitations. Recently, charge pump with nearly rail-to-

rail operation and leakage-current cancellation has been reported [41] using techniques such as replica bias and feedback network, however, the problem of mismatch between up and down currents is not well solved.

Figure 4.5 Charge pump with NMOS current steering switches

In addition to single-ended charge pumps discussed so far, fully differential charge pumps [20, 42, 43] have also been reported. Generally speaking, a fully differential charge pump has several advantages over a single-ended charge pump, including improved current matching, leakage current cancellation, wider output voltage range, and better suppression of timing mismatch and power supply noise. However, these advantages are achieved at the cost of two loop filters, common-mode feedback circuit and more power dissipation.

From the above investigation, a charge pump circuit based on a technique disclosed in [44] is considered attractive to alleviate current mismatch, charge sharing and charge injection problems. Feed-through of the input pulses can be eliminated by using differential current-steering switches with one side biased by DC reference voltage. With a replica biasing using feedback, the mismatch of *up* and *down*

currents can be greatly reduced. However, this circuit was found to have a feedback stability problem.

In this work, an improved charge pump circuit is proposed to solve the stability problem. It can operate with a supply voltage of as low as 1.2 V in a 0.18- μm CMOS process. The design of the proposed charge pump circuit is described in the next section.

4.3 Design of the proposed charge pump circuit

The proposed charge pump circuit includes a charge pump core circuit, a replica bias circuit and a feedback network whose inverting input terminal is connected to the output of the charge pump core. The non-inverting input terminal is connected to the output of the replica bias circuit, and the output of the error amplifier is used to bias the discharging current source of the charge pump. Figure 4.6 shows the simplified schematic of the proposed charge pump circuit, in which in actual, the current mirrors for generating I_{up} , I_{dn} and I_{ref} are implemented using wide-swing cascode current mirrors. Current-steering switches are used to enhance the switching speed. The inherent mismatch of PMOS and NMOS can be avoided by using only NMOS switches. One side of the switch pairs is connected to the ubp/dnb input signal, and the other side is connected to a reference voltage, V_{ref} , which is set to about half of the supply voltage. Transistor M0, which has the same aspect ratio and gate bias as transistors M2 and M4, is included so that the drain-source voltages of the current source M6, M5a and M6a are better matched. If the $up(dnb)$ input signal is low, the tail current flows into transistor M2(M4), while very little or no current flows into transistor M1(M3) due to the differential structure. When transistor M2 is on and

transistor M4 is off, the current flows into transistor M8 and nearly no current flows into transistor M12, so the capacitors in the loop filter are being charged. Similar principle applies to the discharge cycle.

Figure 4.6 Simplified circuit diagram of the proposed charge pump

This charge pump design provides several advantages over the conventional topology. Firstly, feed-through of the input pulses to the output terminal during the transition of upb/dnb signals can be avoided by connecting one side of the differential switches to a constant DC voltage, V_{ref} , rather than to the inversion of upb/dnb signals. For example, when the current is steered to the output through M2, M2 operates in the active region if V_{ref} is set to about half of the supply voltage, such that M2 and M5a effectively form a cascode current source when they drive current to the output hence blocking the input pulse at upb terminal from reaching the output terminal. Therefore, no spiking current appears at the output of the charge pump. Secondly, charge sharing effect is not obvious in this configuration. As transistor M2 and M4 are connected to the reference voltage, they are not completely off when the

upb/dnb input signal is high. Therefore, the charge redistribution effect is reduced when current flows again in transistors M8 and M10. Thirdly, as the NMOS switches, M1 and M3 are driven by upb and dnb , both from complementary output terminals of the PFD, timing mismatch between up and upb (or, dn and dnb) as in the conventional design is avoided. Fourthly, mismatch of up and $down$ currents is significantly reduced in a wide output voltage range by applying a replica biasing using feedback.

In the original configuration [44], the output of feedback error amplifier is used to bias the charging current sources M5a and M5b, which gives rise to a serious stability problem. There are two major poles in this feedback network, one at the output of the feedback error amplifier and the other one at node V_r of the replica bias circuit. If the output of the op amp is connected to the gates of M5a and M5b, the two poles are separated across a non-inverting gain stage. Consequently, Miller pole splitting technique cannot be applied for effective frequency compensation, resulting in an unstable loop. From the Bode plot in Figure 4.7, the existence of a right-hand-plane zero is evident. Hence, the charge pump may not be able to work properly due to the poor stability of the feedback loop.

In this design, the output of the feedback error amplifier is connected to the gates of M6a and M6b to bias the discharging current sources instead. As the two poles are separated across an inverting gain stage, Miller compensation capacitor, C_c , can be connected between output node of the amplifier and node V_r of the replica bias circuit. With the compensation capacitor, $C_c = 1$ pF, a phase margin of 67° and a loop bandwidth of 48 MHz is achieved, as seen from the Bode plot in Figure 4.8. Thus, the feedback stability problem does not exist in this charge pump design.

Figure 4.7 Bode plot of the feedback loop in the charge pump reported in [44]

Figure 4.8 Bode plot of the feedback loop in the proposed charge pump

The error amplifier in the feedback network should be able to deal with common-mode input voltages at least from V_{dsat} to $V_{dd}-V_{dsat}$. By placing an NMOS and a PMOS differential input pairs in parallel, the input stage operates for the desired

common-mode input range as long as the supply voltage requirement specified by Equation (4.2) is fulfilled.

$$V_{DD} \geq |V_{gsp}| + V_{gsn} + 2V_{dsat} \quad (4.2)$$

where V_{gsp} and V_{gsn} are the gate-source voltage of a PMOS and the gate-source voltage of an NMOS transistor, respectively. V_{dsat} is the over-drive voltage of the tail current source. Therefore, the amplifier design as depicted in Figure 4.9 is used in this charge pump circuit with a supply voltage as low as 1.2 V in a 0.18- μm CMOS process.

Figure 4.9 Schematic of the error amplifier used in the proposed charge pump

4.4 Simulation results and comparison

The proposed charge pump circuit was designed using a 0.18- μm CMOS technology. Transient analysis was performed to evaluate the performance of the charge pump, which is to be used in a PLL-based frequency synthesizer with a reference frequency of 10 MHz and a charge pump current of 100 μA . Identical voltage pulses with pulse width of 50 ns and pulse period of 100 ns are applied to the *upb* and *dnb* input terminals. As illustrated in Figure 4.10, a third-order passive loop filter in parallel with a DC voltage source is connected to the output node as an equivalent load of the charge pump in locked condition. The transient current waveforms at the source node of M8 and the drain node of M12 in Figure 4.6 are displayed in Figure 4.11. It shows that there is no spike appearing at the source and sink current outputs. It also verifies that the feedback network in the charge pump circuit is stable.

Figure 4.10 Simulation setup for the transient analysis of the charge pump

(a)

(b)

Figure 4.11 Output waveforms of the up and down currents. Transient current at (a) the source node of M8, and (b) the drain node of M12

Figure 4.12 compares the simulated systematic mismatch between the *up* and *down* currents as a function of the output voltage for the proposed charge pump and the conventional current-steering charge pump without replica bias and feedback. For the output voltage range from 0.1 V to 1.1 V, the current mismatch is $\pm 6.5 \mu\text{A}$ ($\pm 6.5 \%$) for the conventional design, and within $\pm 0.5 \mu\text{A}$ ($\pm 0.5 \%$) for the proposed design. Thus, the replica biasing technique using feedback demonstrates its effectiveness in improving current matching of the charge pump circuit.

When the PLL is in the locked state, identical minimum pulses of the *up* and *down* signals are generated by the PFD. Equation (4.1) tells that shorter turn-on time of the PFD helps to reduce the in-band noise contribution of the PLL to the output. Therefore, it is important to design the charge pump with faster speed, so that shorter delay pulse width from the PFD is allowed to turn on the charge pump current. As long as the amount of charge injected to the loop filter is linearly proportional to the phase error, the dead zone can be eliminated. Figure 4.13 shows that input pulse width must be greater than 400 ps in order to avoid dead-zone problem in the proposed charge pump circuit.

The average power consumption for the charge pump in the locked condition including replica bias circuit and the feedback error amplifier is around 0.85 mW. For a charge pump current of 100 μA , the power consumption of the proposed charge pump circuit is much lower than other reported designs [42].

Figure 4.12 Simulation results for the mismatch of up and down currents as a function of the output voltage

(a)

(b)

Figure 4.13 (a) The plot of average up and down output currents as a function of input pulse width (b)

Zoom-in view of the plot near the origin

Chapter 5

A 1.2 V fully integrated CMOS PLL frequency synthesizer for 5-GHz WLAN

This chapter demonstrates a frequency synthesizer designed for WLAN 802.11a transceivers using a 0.18- μm CMOS process with a supply voltage of 1.2 V. The experimental prototype adopts adaptive PLL architecture with high-performance charge pump design as discussed in Chapter 3 and Chapter 4.

5.1 Design specifications

5.1.1 WLAN 802.11a overview

IEEE 802.11a [37] is a new WLAN standard specifying operation in the 5 GHz U-NII band. A high data rate of up to 54 Mbps can be offered between portable devices. As illustrated in Figure 5.1, IEEE 802.11a standard covers a frequency spectrum of 300 MHz, which is separated into three bands, each with a bandwidth of 100 MHz. The lower band (5.15 GHz to 5.25 GHz) and middle band (5.25 GHz to 5.35 GHz) are specified for indoor communications, and the maximum transmit powers are 40 mW and 200 mW, respectively. The upper band (5.725 GHz to 5.825 GHz) permits a larger transmit power of up to 800 mW to support outdoor communications. To minimize the multipath effect in an indoor environment and support higher data rates at the same time, orthogonal frequency division multiplexing (OFDM) modulation scheme is employed in this standard. OFDM subdivides a carrier into several individually modulated orthogonal subcarriers, all of which can be transmitted at the

same time. In IEEE 802.11a, each band contains four channels, i.e. four carriers. Each carrier occupies 20 MHz bandwidth with 52 subcarriers, 48 of which are used for data and the rest for error correction.

Figure 5.1 Frequency allocation of IEEE 802.11a standard

The detailed specifications for the transistor-level design of frequency synthesizers are not readily available from the standard, but are embedded within the description of the requirements for the communication system. The RF system designer needs to translate these standard-compliance requirements into system-level specifications, which are easier to test. The derivation of the critical specifications for the experimental prototype is explained in the following sections.

5.1.2 Output frequency range

For output frequency range, it is sufficient to cover only the lower and middle bands as the upper band is not universally available yet. Assuming a direct-conversion receiver with the LO frequency equal to the RF frequency, this frequency synthesizer

is aimed at indoor communication with the output frequency ranging from 5.14 GHz to 5.36 GHz.

5.1.3 Supply voltage

If the supply voltage is around 40% to 60% of the maximum allowed supply voltage for a particular process while not exceeding three times the threshold voltages of the devices, the design is considered a low-voltage design [40]. Thus, in a 0.18- μm CMOS process with a maximum supply of 1.8 V and a threshold voltage of around 0.5 V, a design with a supply voltage of around 1.0 V to 1.2 V is considered a low-voltage design. In this work, the supply voltage is set to be 1.2 V.

5.1.4 Phase noise and spurious suppression

As IEEE 802.11a standard adopts OFDM as the modulation scheme, the phase noise and the spurs requirements of the synthesizer are stringent.

Considering that the receiver achieves the highest data rate of 54 Mbps with a minimum sensitivity of -65 dBm [37], and an adjacent interferer which is 40 dB stronger than the desired carrier, while the SNR is assumed to be 19 dB for a bit-error-rate (BER) of 10^{-6} in a 64-level quadrature amplitude modulation (64-QAM) system, the phase noise is calculated based on Equation (2.20). The phase noise requirement at 20 MHz offset from the carrier should be lower than -132 dBc/Hz.

$$\begin{aligned} L(20 \text{ MHz}) &\leq S_{RF} - S_{block} - 10\log_{10}(BW) - SNR \\ &\leq -40 - 10\log_{10}(20 \times 10^6) - 19 \\ \therefore L(20 \text{ MHz}) &\leq -132 \text{ dBc/Hz} \end{aligned} \tag{5.1}$$

The spurious specification can be derived based on Equation (2.21). As the maximum blocking signal is -30 dBm, and a desired signal level of -65 dBm must still be detectable with a BER of 10^{-6} , the resulting spurious specification is about -54 dB.

$$\begin{aligned}
 S_{spur} &\leq S_{desired} - S_{block} - SNR \\
 &\leq -65 - (-30) - 19 \\
 \therefore S_{spur} &\leq -54 \text{ dB}
 \end{aligned} \tag{5.2}$$

5.1.5 Summary of design specifications

Table 5.1 Design specifications for the experimental prototype

Parameter	Condition	Min	Typ	Max	Unit
Output frequency range		5.14	-	5.36	GHz
Channel Spacing			20		MHz
Reference frequency			10		MHz
Phase noise	@ 20MHz			- 132	dBc/Hz
Spurious tone				- 54	dBc
Settling time	± 60 kHz accuracy			70	μ s
Supply voltage			1.2		V
Power (excluding output buffer)			50		mW

5.2 Synthesizer architecture

Figure 5.2 shows the system block diagram of a frequency synthesizer designed for WLAN 802.11a transceivers. The system implements adaptive PLL architecture as introduced in Chapter 3, and comprises a PFD, a lock detector, two charge pumps, a third-order dual-path loop filter, a ring VCO and a programmable frequency divider. As discussed in Section 2.4, since the channel spacing of IEEE 802.11a is relatively

wide compared with other standards such as Bluetooth, integer- N architecture is more advantageous and simpler compared with other topologies, and it is adopted for this design. The programmable divider employs the pulse-swallow architecture with dual-modulus prescaler, as depicted inside the dashed box in Figure 5.2. A fixed-ratio divide-by-2 circuit is used to divide the VCO frequency by half first in order to relax the speed constraints of the prescaler. This forces the reference frequency to be reduced to half of the channel spacing, i.e. 10 MHz. The divide-by-2 circuit is followed by a divide-by-8/9 dual-modulus prescaler and a 5-bit pulse swallow counter. The 5-bit selection word allows to change the overall division ratio from 514 to 574, and to tune the output frequency from 5.14 GHz to 5.74 GHz with a reference frequency of 10 MHz and a frequency step of 20 MHz. The division ratio can be expressed by

$$N = 2 \times [9 \times S + 8 \times (32 - S)] = 512 + 2 \times S \quad (5.3)$$

where $S = 1 \sim 31$.

As presented in Section 3.3, the charge pump current of CP1 is 100 μA , while the current of CP2 is set to seven times that of CP1. With the component values of $C_1 = 12.2 \text{ pF}$, $C_2 = 248 \text{ pF}$, $C_3 = 1.5 \text{ pF}$, $R_a = R_b = 3.1 \text{ k}\Omega$ and $R_3 = 29 \text{ k}\Omega$ in the loop filter, the loop bandwidth is reduced from 500 kHz to 135 kHz to further suppress reference spurs when the PLL is automatically switched from wide-bandwidth mode to narrow-bandwidth mode near the locked state. The phase margin of the PLL is maintained at about 46° .

For the integrated loop filter components, the variation of the absolute values due to process variations will affect the loop bandwidth and phase margin of the PLL. As a result, the settling time, phase noise and spurs will also be affected. The process

variation of MIM capacitor value is about $\pm 10\%$, and that of poly resistor value is about $\pm 20\%$. AC analysis based on phase-domain behavioral model shows that the loop bandwidth varies within $\pm 7.4\%$ and the phase margin varies within $\pm 7^\circ$. The loop bandwidth and phase margin of the PLL can be adjusted by changing the charge pump current in fine steps. Therefore, the biasing circuit of the charge pump circuit is designed such that the charge pump current can be programmed using two digital control bits. As such, the variations of the capacitors and resistors values can be overcome.

As this frequency synthesizer is specified to operate with a 1.2-V supply, the high frequency building blocks, such as VCO and dividers face many design challenges. Some special circuit techniques must be employed to prevent failure when the supply voltage varies, as will be demonstrated in the following sections.

Figure 5.2 Block diagram of the proposed synthesizer architecture

5.3 Circuit implementation

5.3.1 PFD

As illustrated in Figure 5.3, a PFD is usually implemented together with a charge pump, represented by two current sources here, in the PLL. Its primary function is to compare the phase of the reference clock signal, ref , and the divider output signal, div , and generate up and dn output pulses that correspond to the phase difference between these two inputs. The two outputs from the PFD control the two current sources in the charge pump to either charge up or discharge the loop filter. Not only does a PFD detect phase difference, but it gives some information about the

frequency as well when the loop is out of lock. Therefore, a PFD is able to offer a wider acquisition range than a simple phase detector. The finite state machine and the operation principle of the PFD have been discussed in Section 3.3.4. As illustrated in Figure 3.9, a PFD can be constructed with two D-type flip-flops and an AND gate in the feedback path for reset.

Figure 5.3 Block diagram of a PFD combined with a charge pump

The PFD in this design adopts the conventional topology [39] based on two RS flip-flops as shown in Figure 5.4. The most important issue related to the PFD design is the dead-zone problem, as mentioned in Section 3.3.4. The simplest solution to this problem is to insert a fixed delay in the reset path of the PFD [3], providing a fixed minimum width to both the *up* and *dn* output pulses. The delay block after the OR gate in Figure 5.4 determines the minimum width of the output pulses. The net difference between *up* and *dn* pulse width is proportional to the phase difference between the two PFD inputs, and determines the total change in charge pump output voltage. Assuming an ideal charge pump, when the *ref* and *div* inputs are in phase under the locked condition, both the *up* and *dn* signals are simultaneously active for a

fixed short duration in each cycle, resulting in zero net charge injected into the loop filter. Complementary pass gates are used to equalize the delays of the differential output signals to drive the differential inputs of the current-steering charge pumps. Figure 5.5 shows the output waveforms of the PFD when the PLL is locked. The minimum pulse width to eliminate the dead-zone problem is about 668 ps.

Figure 5.4 Circuit implementation of a PFD without dead zone

Figure 5.5 Output waveforms of the PFD when the PLL is locked.

5.3.2 Charge pump

There are two CP blocks in this synthesizer, CP1 and CP2. It is crucial to minimize non-ideal effects of CP1, since it dominates the synthesizer performance in the locked state. As elaborated in Chapter 4, the proposed CP design as shown in Figure 5.6 provides several advantages over the conventional topology [16]. Firstly, as one side of the differential switches is connected to a fixed DC voltage, feed-through of the input pulses can be avoided by blocking pulses from reaching the output terminal during the transition of *upb/dnb* signals. Secondly, charge sharing effect is not obvious in this design. Thirdly, as the switches, M1 and M3, are driven by *upb* and *dnb*, both from complementary output terminals of the PFD, timing mismatch between *up* and *upb* (or, *dn* and *dnb*) as in the conventional design is avoided. Fourthly, the mismatch of *up* and *down* currents is less than $\pm 0.5\%$ for $0.1\text{ V} < V_{out}$

< 1.1 V, by applying a replica biasing using feedback. This is also confirmed by post-layout simulation as shown in Figure 5.8. Furthermore, the stability problem associated with the previously reported design [44] is solved by connecting the output of feedback op amp to the discharging current sources M6a and M6b instead of the charging current sources, so that Miller pole splitting technique can be applied easily between the op amp output and the node V_r of the replica bias circuit. The high-current charge pump CP2 is a scaled-up version of CP1, without the replica bias and feedback op amp. As shown in Figure 5.7, a power-down circuitry is also included in CP2. When the signal PD goes high, the drain current of transistor M15 will flow to ground instead of flowing into M5. Meanwhile, M13 is turned on to discharge the drain node of M5, ensuring a fast power-down of CP2.

Figure 5.6 Circuit diagram of charge pump CP1

Figure 5.7 Circuit diagram of the charge pump CP2

Figure 5.8 Comparison of pre-layout and post-layout simulation results for charge pump current mismatch.

With the PFD and charge pump connected together, transient simulation is performed to plot the PFD gain curve. By keeping the frequency of two inputs same at 10 MHz while sweeping the input phase differences from -400° to $+400^\circ$, the average output current of the charge pump is plotted as in Figure 5.9 (a). It is verified

that the linear range of the PFD gain curve is from -2π to $+2\pi$. The zoom-in view in Figure 5.9 (b) shows that there is no dead-zone issue.

(a)

(b)

Figure 5.9 (a) Plot of the average charge pump output current as a function of input phase error of the PFD (b) Zoom-in view of the PFD gain curve in (a)

5.3.3 Lock detector

The lock detector generates a control signal, LD , to switch the frequency synthesizer between the wide-bandwidth mode and the narrow-bandwidth mode. The operation of the lock detector as shown in Figure 5.10 [38] can be illustrated by the diagrams in Figure 5.11. When the PLL is far from the locked condition, the time difference between the positive edges of Up and $Down$ signals is larger than the delay time, t_d , in the delay cell. $Q1$ and $Q2$ are not able to become high at the same time, so the LD signal remains low indicating the PLL is configured in the wide-bandwidth mode. When the PLL is near to the locked condition, the time difference between the positive edges of Up and $Down$ signals is smaller than t_d . Both $Q1$ and $Q2$ jump to high, and the LD signal becomes high indicating the PLL switches to the narrow-bandwidth mode. To make this circuit work properly, the delay time, t_d , must be smaller than the minimum pulse width of the PFD outputs. In this design, t_d is about 120 ps.

Figure 5.10 Circuit diagram of the lock detector

Figure 5.11 Conceptual operation of the lock detector (a) when the PLL is out of lock (b) when the PLL is locked

5.3.4 Programmable frequency divider

The architecture of the programmable frequency divider as shown in Figure 5.12 has been discussed in Section 5.2. In this section, the design considerations for low-voltage operation and the design techniques used for critical building blocks are presented.

Figure 5.12 Frequency divider architecture

Figure 5.13 (a) shows the first divider stage architecture, a high-speed divide-by-two block based on two D-type flip-flops. This block is usually the speed-bottleneck for the frequency divider as it operates at the highest frequency. The two D flip-flops are connected in a master/slave configuration, and each D flip-flop is clocked by two complementary clock signals, CLK and CLKB. When the input clock signal is high, one of the D flip-flops senses the data at its D input to its Q output, while the other D flip-flop latches and holds the previous output. When the input clock signal becomes low, the D flip-flops switch their operating modes, one from the sensing mode to the latching mode, while the other one from the latching mode to the sensing mode. Through this mechanism, the output frequency is divided down to half of the input frequency.

At high operating frequencies, the D flip-flop is typically realized using source-coupled logic (SCL) latch [45, 46] as depicted in Figure 5.13 (b). When the latch is in the sensing mode, M5 is ON and M6 is OFF, the latch behaves as a differential sensing amplifier with M1, M2 and the resistive loads. When the latch is in the latching mode, M6 is ON and M5 is OFF, and the latch behaves as a differential pair with positive feedback formed by M3 and M4. The current source between the source of M5, M6 and the ground in the conventional SCL topology [46] is omitted to achieve higher operating frequency under a low supply of 1.2 V. The DC biasing of M5 and M6 is set by I_{bias} , and the high-frequency input clock signals are AC-coupled to the gates of M5 and M6 through coupling capacitors C_{c1} and C_{c2} . In this manner, the SCL latch is properly biased, and it can work well below 1.2 V without being affected by the common-mode voltage of the preceding VCO stage. The speed

of the circuit is determined by the bias current and the load capacitance seen at the output nodes, Q and QB.

(a)

(b)

Figure 5.13 Divide-by-2 Circuit (a) Block diagram (b) SCL latch

Although the operating principle of this divider can be easily understood based on standard digital circuit behaviors, its behavior at high frequencies is actually far more complex. It is important to characterize the performance of the divide-by-2 circuit by its sensitivity curve [47], which gives the minimum required amplitude of the input

clock for the divider to function properly, versus the frequency of the applied input clock. Figure 5.14 compares the pre-layout and post-layout simulation results of the divide-by-2 circuit realized in a 0.18- μm CMOS process. It is observed that the divider has a self-oscillation frequency, f_{so} , which can be measured when the input clock amplitude and the clock's differential dc voltage are both set to zero. It is desirable to design f_{so} to be slightly higher than half of the input frequency, so that very low input clock amplitude is needed for proper divide-by-2 operation. In this design, the self-oscillation is designed to be about 3 GHz. The average power consumption of this divide-by-2 circuit is about 1.9 mW.

Figure 5.14 Sensitivity curve of the divide-by-2 circuit.

The divide-by-8/9 prescaler is realized in true-single-phase-clock (TSPC) logic [48]. TSPC logic offers advantage over the traditional SCL logic in terms of power consumption due to the reduced capacitive loads, especially in low-voltage designs. It is also a more suitable architecture than traditional static CMOS logic for a divider working at high frequency. However, it is not suitable for the first divide-by-2 circuit

because of its single-ended operation. Moreover, TSPC dividers require rail-to-rail voltage swing for input signals in order to achieve high-frequency operation. If the voltage swing of the input signal is not sufficient, the dividers may fail to function correctly. Therefore, clock buffer is needed to provide rail-to-rail input signal to TSPC divide-by-8/9 prescaler.

The high-speed clock buffer as illustrated in Figure 5.15 overcomes the speed limitation of the conventional inverter-chain buffer. Through AC-coupling capacitors, pull-up device M3 and pull-down device M4, the input DC level of transistors M6 is shifted close to VDD, and that of M5 close to GND, so as to prevent the transistors M5 and M6 from operating in the cut-off region. By using this technique, a rail-to-rail voltage swing is provided to drive the TSPC dividers at high frequency under low supply voltage. The inverters INV1 and INV2 are used to reduce the input loading of the clock buffer, as well as to balance the loads to the differential outputs of the preceding divide-by-2 circuit.

Figure 5.15 Schematic of high-speed clock buffer

The structure of the dual-modulus prescaler is shown in Figure 5.16. It consists of a divide-by-2/3 synchronous divider and two asynchronous divide-by-2 dividers. As illustrated in the timing diagram in Figure 5.17, when MC is low, the value of q_2 is always high, AND2 and D2 are inactive, and AND1 functions as an inverter. D1 functions as a divide-by-2 circuit, and the whole prescaler performs divide-by-8 function. When MC is high, the value of q_2 becomes low when q_1 , q_3 and q_4 are all equal to 1, so D1 performs a divide-by-3 operation after every three consecutive divide-by-2 cycles. As a result, the prescaler performs a divide-by-9 function.

Figure 5.16 Block diagram of the dual-modulus divide-by-8/9 prescaler

Figure 5.17 Timing diagrams of the divide-by-8/9 prescaler

The divide-by-2 blocks D3 and D4 are implemented in TSPC logic as shown in Figure 5.18. The TSPC divide-by-2 circuit is built based on TSPC D-type flip-flop in which the output is fed back to the D input and the clock terminal is connected to the input signal. The operation of the TSPC divide-by-2 circuit consists of two operating modes, namely the evaluation mode and the hold mode. When *In* is low, the value at node *a1* becomes the inverted value of D input. Node *a2* is precharged to high through M4, and transistors M6 and M8 are off so that the output value is held. When *In* is high, it works in the evaluation mode, and the value at node *a1* is transferred to node *Outb*. As the output node *Outb* is fed back to D input, the output will toggle its own state every two clock cycles. Hence, it performs the divide-by-2 function.

Figure 5.18 TSPC divide-by-2 circuit

The most critical block in the prescaler is the divide-by-2/3 block as it operates at the highest frequency. It is realized using the extended true-single-phase-clock (E-TSPC) logic [49]. E-TSPC logic allows higher operating frequencies compared with the conventional TSPC logic, because it avoids using the cascode structure which causes the body effect of the transistors and slows down the switching speed. The disadvantage of E-TSPC logic is the static power consumption. However, the increase in total power consumption is small since the dynamic power consumption dominates at the frequencies of interest. Another advantage is that the logic functions can be embedded easily within the latches. This results in more compact circuits and reduced power consumption. As illustrated in Figure 5.19, the AND gates are realized by adding only one more transistor each.

Figure 5.19 E-TSPC divide-by-2/3 circuit

Figure 5.20 displays the simulated waveforms of the dual-modulus prescaler driven by the SCL divide-by-2 outputs at 3 GHz. The simulated maximum input frequency versus the supply voltage, as well as the corresponding power consumption, is shown in Figure 5.21 and 5.22 respectively. According to the post-layout simulation results, at 1.2-V power supply, 3.5-GHz operating frequency is achieved, consuming only 408.3 μA . The high-speed clock buffer consumes 750 μA .

Figure 5.20 Simulated waveforms of the dual-modulus divide-by-8/9 prescaler

Figure 5.21 Simulated maximum operating frequency of the prescaler versus power supply voltage

Figure 5.22 Simulated power consumption of the prescaler at maximum operating frequency, F_{max} , versus power supply voltage.

The divide-by-8/9 prescaler is followed by a programmable pulse-swallow counter as illustrated in Figure 5.23. In general, if the counter is programmed with an input count of M and the swallow counter with an input count of S (where $M \geq S$), then in each output cycle, the division ratio of the prescaler is $P+1$ for S times, and P for the remaining $M-S$ times. Therefore, the total division ratio is given by

$$N = S(P+1) + (M-S)P = M \cdot P + S \quad (5.4)$$

Figure 5.23 Block diagram of the programmable pulse-swallow frequency divider

As seen in Equation (5.4), once the prescaler modulus, $P/(P+1)$, has been determined in the design, various N division ratios can be realized by changing the input count setting for M and S for the programmable and swallow counters respectively. In this work, the prescaler modulus is chosen to be 8/9, and the M and S counters share a 5-bit synchronous counter. The M counter is fixed to divide the frequency by 32, while the S counter can be programmed by a 5-bit selection word. Thus, by taking into account of the divide-by-2 circuit in front of the prescaler, the total division ratio of the frequency divider used in this work can be expressed as

$$N = 2 \times [9 \times S + 8 \times (32 - S)] = 512 + 2 \times S \quad (5.5)$$

where $S = 1 \sim 31$.

The schematic diagram of the programmable pulse-swallow counter is shown in Figure 5.24. The 5-bit synchronous counter counts from 0 to 31 before the counter resets and starts to count from 0 again. Meanwhile, the modulus control signal, MC , is set to high upon reset of the synchronous counter. The MC signal remains high until the counter output $q4:q0 = S4:S0$, where $S4:S0$ is the 5-bit channel selection code of the swallow counter. This causes the comparison logic block of the swallow counter to reset the SR flip-flop, and MC changes to low. The MC signal remains low for the rest of the clock cycles until the counter resets and at the same time MC changes to high again. The duty cycle of MC signal is proportional to the length of channel selection code $S4:S0$ and it is used to control the prescaler modulus.

The static CMOS logic is used to implement the programmable pulse-swallow counter. Post-layout simulation shows that the overall power consumption of the frequency divider is about 3.5 mW under a supply voltage of 1.2 V.

Figure 5.24 Schematic diagram of the programmable pulse-swallow counter

5.3.5 VCO

VCO is one of the most crucial building blocks in a frequency synthesizer as it determines the output frequency range that the synthesizer is able to support. Since the VCO operates at the highest frequency within the synthesizer, it usually consumes a large portion of the total power consumption, and its phase noise is dominant in the whole system at frequency offsets beyond the PLL loop bandwidth. Two common categories for VCO designs are LC-tank oscillators and ring oscillators. LC VCO is more popular in applications that require higher frequency with lower phase noise and lower power consumption, such as in a mobile cellular telephone system. However, it also has its disadvantages such as larger die area due to the on-chip inductors and narrower frequency tuning range. Complicated calibration techniques [22, 25, 50] are usually applied to ensure sufficient frequency coverage as well as to overcome tuning range variation due to process, supply voltage and

temperature (PVT) variations. Moreover, before designing any LC VCO circuit, accurate characterization of both the inductors and varactors must be performed, but it is not practical for this project due to the limited resources and restrained time-frame.

In this research, a ring-oscillator-based VCO is designed, as it does not require passive components such as inductors and varactors, and takes better advantages of technology scaling and low-cost SOC solutions. The disadvantage of poorer phase noise compared to LC oscillators is overcome by adopting 3-stage dual-delay-path architecture and saturated gain stage, which follows the design in [51].

The oscillation frequency of conventional single-loop ring oscillators is determined as

$$f_o \approx \frac{1}{2 \cdot N \cdot t_d} \quad (5.4)$$

where N is the number of stages and t_d is the unit delay time of a delay cell. Hence the frequency of the oscillator is limited by the smallest possible delay of a basic inverter cell. To solve the speed limitation problem of the ring oscillators, various architectures have been reported [52-55], and most of them are based on the same concept of negative skewed delay scheme [56] as illustrated in Figure 5.25. The concept is to ensure that the PMOS transistors are switched on ahead of the low-to-high output transitions and switched off ahead of the high-to-low output transitions. Therefore, the speed limitation owing to the lower mobility of p-type carrier is alleviated, and the oscillation frequency is greatly improved. In actual implementations, ring oscillators with dual-delay-path [54] or multiple-pass architectures [51-53] are proposed to realize this concept.

Figure 5.25 Conceptual illustration of negative skewed delay scheme

Illustrated in Figure 5.26 is the ring oscillator structure used in this work. It is based on dual-delay scheme which contains two delay paths. The primary delay path, as represented by the thick lines, is the normal delay path, and the secondary delay path represented by the thin lines is the negative skewed delay path which is formed by adding a set of secondary inputs V_{s+} and V_{s-} , to each stage and switching these inputs earlier than the primary inputs using feedforward technique. Three-stage ring oscillator with dual-delay paths, which uses the minimum number of stages required for this structure, is implemented to obtain higher oscillation frequency. All of the three stages are loaded with identical output buffers to ensure equal rise and fall times, and hence better jitter performance.

Figure 5.26 Three-stage ring oscillator with dual-delay paths

Each stage employs saturated-type delay cell with both coarse and fine tuning capability, as shown in Figure 5.27 [51]. Ring oscillators usually provide much wider frequency tuning range than LC-tank oscillators. This is advantageous for accommodating PVT variations; however, as the supply voltage scales with technology in deep-submicron CMOS process, a very large VCO gain will be incurred and the sensitivity to noise at its control input will be increased, which will degrade the noise performance of the PLL. To achieve both a lower VCO gain and a wide tuning range, a new delay cell, which is equipped with both coarse and fine tuning, has been proposed [51]. The idea is to break a single whole-range tuning curve into a set of sub-range tuning curves with sufficient frequency overlap, by using both discrete coarse-tuning and continuous fine-tuning. As shown in Figure 5.27, NMOS transistors M1 and M2 form the input pair of the primary loop, while PMOS transistors M5 and M6 serve as the input pair of the secondary loop. It is important to note that the secondary input pair needs to be weaker than the primary

input pair for proper operation. PMOS transistors M3 and M4 are the load of the delay cell, with their gates tied to the coarse-tuning voltage. In this delay cell, the tail current source is removed so as to reduce the $1/f$ noise. Extra PMOS loads, M7 and M8 with their gates connected to the ground node, are added to avoid the loss of oscillation at the extreme cases of frequency tuning [51]. Since these two transistors are biased in the triode region of operation, this design may be more susceptible to supply noise. Coarse tuning is realized by varying the load through changing the gate voltage of M3 and M4, while fine tuning is done by adjusting the amount of tail current flowing through the cross-coupled transistors M10 and M11, which provide positive feedback and help to reduce the sensitivity to the common-mode noise.

Figure 5.27 Delay cell with both coarse and fine frequency tunings

This ring VCO is designed with a supply voltage of 1.5 V in a 0.18- μm CMOS technology. Simulations in SpectreRF are used to extract frequency tuning characteristics. Figure 5.28 compares the pre-layout and post-layout simulation results for fine-tuning characteristics of the VCO, with the coarse-tuning voltage, V_{coarse} , ranging from 0 V to 1 V at a 0.1 V interval. Post-layout simulation results

show that the fine-tuning VCO gain varies from 500 MHz/V to 750 MHz/V in the fine-tuning voltage range from 0.5 V to 0.9 V.

(a)

(b)

Figure 5.28 Frequency tuning characteristics of the ring-VCO. (a) Pre-layout simulation results of frequency vs. fine-tuning voltage with coarse-tuning voltage ranging from 0 V to 1 V at 0.1 V intervals (b) Post-layout simulation results of the frequency tuning characteristics

5.3.6 Output buffer

In order to drive bond pads and even off-chip loads at higher speed, the output buffer adopts two-stage design with the second stage configured as an f_t doubler [57] as shown in Figure 5.29. For output buffers using differential pairs in a cascade of stages, large input capacitance is the limiting factor in achieving high speed as wide transistors must be employed in order to steer the large tail current to the differential outputs. The problem is solved by using a relatively lower tail current for the first stage and an f_t doubler as the second stage, which is able to provide the same voltage gain as the conventional differential pair but with a lower input capacitance. The bias voltage, V_b , is chosen to be the common-mode level of V_{inp} and V_{inn} , allowing the differential pairs to operate with minimum systematic offset. With $R3 = R4 = 50\ \Omega$, a tail current of $2 I_2$ equal to 20 mA is used to generate a differential output voltage swing of 1 V_{pp}.

Figure 5.29 The high-speed output buffer

5.4 Layout considerations

The frequency synthesizer is fully integrated in a 0.18- μm CMOS technology with 6 metal layers and 1 poly layer. The overall layout view is shown in Figure 5.30. The total area including pad frame occupies 1.1 mm by 1.1 mm. The active region occupies only 770 μm by 770 μm , dominated by the capacitors of the loop filter. The design will be taped out to Chartered Semiconductor Manufacturing for fabrication. The measurement is to be done by wafer probing on bare silicon dies.

Advanced layout techniques must be applied throughout this work to minimize device mismatches, parasitic components, cross-talk and substrate coupling. These techniques at different hierarchical levels are summarized in Table 5.2.

Table 5.2 Summary of layout considerations and techniques

Level of design	Layout technique	Purpose
Floor planning	Critical analog and RF blocks, such as charge pump and VCO, are placed far from digital elements	Reduce interference between analog and digital signals
Power line	Separate power lines and pads for analog, digital and VCO blocks	Reduce noise coupling
	Wide power lines using the top metal	Reduce parasitics
	Use as many contacts/vias as possible when two power lines are connected	Reduce parasitics
	Tree structure of circuit power line planning	Reduce noise coupling
General	Add shielding for critical path, and increase the spacing to other signal lines	Reduce noise coupling and parasitic capacitance
	Always use multiple contacts and vias	- Reduce parasitic resistance - Improve reliability
	Surround digital, analog and VCO blocks with guard rings	Improve isolation
VCO (See Figure 5.31)	Use ground lines in between the parallel output signal lines	Reduce noise coupling
	Use alternating metal layers rather than same metal layer for side-by-side parallel signal lines	Reduce parasitics and cross-talk
	Separate N-well for each delay cell	Improve isolation

VCO (See Figure 5.31)	Symmetrical placement of layout for each delay cell	Improve matching
	Adopt interdigitated layout for differential pairs	- Reduce parasitics - Improve matching
	Use wider metal width and stacked multiple metal layers for drain and source connections	- Accommodate 1.5~2 times current limit of design to cover process variation. - Reduce parasitics
Charge pump (See Figure 5.32)	Symmetrical placement of layout for charge pump core and its replica	Improve matching
	Adopt interdigitated layout and add dummy devices for current mirrors and differential pairs	- Reduce parasitics - Improve matching
	Adopt common-centroid layout for input pairs of the error amplifier	- Improve matching - Minimize systematic offset
Divider and others	Symmetrical placement of layout for SCL divide-by-2	Improve matching
	Adopt interdigitated layout for differential pairs	- Reduce parasitics - Improve matching
	Adopt interdigitated layout and add dummies on both sides for resistors	Improve matching
	Avoid crossing of input line with output line	Avoid undesired return path or feedback path
	Matched and short bus lengths wherever possible	- Reduce parasitics - Reduce mismatches of signals between the stages

Figure 5.30 Overall layout view of the frequency synthesizer

Figure 5.31 Layout of the 3-stage ring-VCO

Figure 5.32 Layout of the charge pump

5.5 Closed-loop simulation results

Post-layout simulations are carried out for the closed-loop frequency synthesizer to verify the functionalities. A reference clock of 10 MHz is supplied to the PFD input and the channel selection code is set to a division ratio of 536. The transient waveforms of lock detector output, LD , and VCO fine-tuning voltage, V_c , are displayed in Figure 5.33. The frequency synthesizer settles into the locked state after 20 μs , which is shorter than the settling time of 30 μs predicted by behavioral simulations in Section 3.3.5 because simulated VCO gain is higher than the specification.

Figure 5.33 Post-layout transient waveforms of the adaptive-PLL synthesizer

In order to evaluate the reference spur amplitude, FFT analysis of the transient output data is performed. To speed up the simulation time, a mixed-level simulation is carried out, in which the layout extracted views of PFD, LD, charge pump and divider are co-simulated with the behavioral model of the VCO with jitter parameter included. Also, ideal loop filter components are used in this simulation. The

spectrum of the synthesizer output at 5.36 GHz is shown in Figure 5.34. The spur level being extracted from the FFT analysis is -60 dBc, which is 14 dB lower than the case with charge pump current ratio $c = 0$. Hence, the simulation results show that the proposed synthesizer is able to accomplish a significant reduction in reference spurs while maintaining a fast settling time. The total power consumption of the synthesizer excluding the VCO output buffers is 37.7 mW, dominated by the ring-VCO.

Figure 5.34 Frequency synthesizer output spectrum at 5.36 GHz

The closed-loop noise of the PLL synthesizer can be calculated by using the linear phase-domain noise model developed in Section 2.2. The noise characteristics of individual PLL blocks are obtained by post-layout simulations first, and then analyzed with the aid of MATLAB program. The total phase noise of the PLL can be calculated by adding all the block noise contributions. Figure 5.35 plots the individual noise contribution of main building blocks together with the total phase

noise for the whole synthesizer system. At 20 MHz offset from the carrier frequency, the phase noise at the synthesizer output depends on the noise of the VCO, which is about - 131.5 dBc/Hz. At 10 kHz offset from the carrier frequency, the total phase noise is dominated by charge pump and divider noise, which is about - 95 dBc/Hz. However, due to the higher noise of the ring-VCO, the in-band noise from 10 kHz offset to 500 kHz offset is also dominated by VCO noise.

Figure 5.35 Simulated total phase noise of the frequency synthesizer along with noise contributions from building blocks.

As a summary, the simulated circuit performance of the proposed frequency synthesizer is given in Table 5.3.

Table 5.3 Performance summary of the proposed frequency synthesizer

Technology	0.18- μ m CMOS
Supply Voltage	1.2 V (1.5 V for VCO)
Power consumption	37.7 mW (excluding output buffer)
Phase noise	- 91 dBc/Hz @ 10 kHz offset
	- 132.5 dBc/Hz @ 20 MHz offset
Reference spurs	- 60 dBc
Tuning range	5.14 GHz ~ 5.74 GHz
Settling time	< 30 μ s

Chapter 6

Conclusion and recommendation

6.1 Conclusion

In this thesis, various circuit techniques employed in low-voltage fully-integrated CMOS frequency synthesizers are presented. The key contributions are on spur-reduction techniques to accomplish low reference spurs while maintaining fast settling time. It is challenging to fulfill these two conflicting requirements concurrently because of different preferences on the loop bandwidth and on the location of the poles and zeros of the closed-loop transfer function. Existing spur-reduction techniques and limitations are discussed. An adaptive PLL architecture is proposed to smoothly adapt the loop parameters according to different operating modes. During frequency jumps, the architecture allows wider bandwidth for fast acquisition time. When the loop is locked, the loop bandwidth is reduced to further attenuate the reference spurs. Another advantage of the proposed architecture is that it allows the loop filter components to be integrated on chip with a reasonable chip area.

In addition, a high-performance charge pump circuit is incorporated with the adaptive synthesizer to alleviate non-ideal effects that cause spurs. Charge pump is the dominant block causing reference spurs in the output spectrum of PLLs due to non-ideal effects such as current mismatch, leakage current, charge sharing and timing mismatch. The proposed charge pump circuit solves the feedback stability problem associated with the originally reported design. By employing differential

current-steering switches with one side connected to a DC reference voltage, this charge pump circuit minimizes feed-through of the input pulses, charge sharing effect and timing mismatch of input clocks. More importantly, with a replica biasing technique and a feedback network, the proposed charge pump circuit demonstrates superior current matching in a wide output voltage range. It is designed in a 0.18- μm CMOS process with a supply voltage of 1.2 V. The percentage current mismatch for the output range from 0.1 V to 1.1 V is less than $\pm 0.5\%$.

An experimental prototype of fully-integrated frequency synthesizer is designed for 5-GHz WLAN SOC applications using a 0.18- μm CMOS process with a supply voltage of 1.2 V. The synthesizer adopts the proposed adaptive PLL architecture with high-performance charge pump circuit. A hierarchical design approach, comprising a top-down design process followed by a bottom-up verification process, is adopted to accelerate the design process and shorten the simulation time. Behavioral models represented in the Verilog-AMS language have been developed to facilitate this design process. Design considerations and techniques required for each building block to meet the stringent specifications of the 5-GHz synthesizers as the supply voltage is lowered are intensively discussed. Post-layout simulation shows that the synthesizer is able to achieve a low reference spur level of -60 dBc and fast settling time of less than 30 μs for a frequency jump of 220 MHz from 5.14 GHz to 5.36 GHz, with a power consumption of 37.7 mW. The total chip area is about 1.21 mm^2 .

6.2 Recommendations for future research

In this work, separate supply pins are allocated for critical PLL blocks, such as charge pump, dividers and VCO. Each supply pin is to be connected to a clean

external power supply during wafer-probing measurements. However, for SOC applications, fluctuations in the internal power supply voltage can be a major cause of phase noise or jitter for integrated frequency synthesizer. This problem becomes more significant as the supply voltage is lowered because the relative supply fluctuation becomes larger. Therefore, it is crucial to improve PSRR of the frequency synthesizer. On-chip regulating circuitries are recommended to be included in future research. A high level of supply noise rejection can be achieved with a high-bandwidth voltage regulator that provides a clean supply to the sensitive blocks in a PLL, such as charge pump, frequency divider and VCO. Moreover, the phase noise of the ring-VCO can be improved with on-chip supply regulations. The major challenge relevant to this approach is to design a low-noise regulator with low power consumption and small area.

Another recommendation for future research is on loop filter topologies that allow smaller capacitor values. The loop filter is usually the integration bottleneck of narrow-band PLL frequency synthesizers. Although the chip size of this work is only 1.21 mm^2 , almost 70% of the active area is dominated by loop filter components. Therefore, capacitor scaling techniques may become future research topics. The main issues of the state-of-the-art approaches [58, 59] are noise and accuracy.

Author's Publications

1. Y. Sun, P. Y. Song, and L. Siek, "Design of a high performance charge pump circuit for low voltage phase-locked loops," *2007 IEEE International Symposium on Integrated Circuits*, pp 295-298, September 26-28, 2007.
2. Y. Sun and L. Siek, "A spur-reduction technique in a fully integrated CMOS frequency synthesizer for 5-GHz WLAN SOC," *2007 IEEE International SOC conference*, pp

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