The multi-step dynamic reference analog-to-digital converter

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**THE MULTI-STEP DYNAMIC REFERENCE
ANALOG-TO-DIGITAL CONVERTER**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2008

THE MULTI-STEP DYNAMIC REFERENCE ANALOG-TO-DIGITAL CONVERTER

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The Multi-Step Dynamic Reference Analog-to-Digital Converter

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Abstract

Abstract

The thesis presents the research work on high-speed analog-to-digital converter (ADC), with a design specification of 8 bits of resolution under static operating condition and an effective number of bits (ENOB) of 7 bits at 100 MSample/s. A group of novel Multi-Step Dynamic Reference topologies is proposed in this work, which includes a Two-Step design and a Pipelined one. These converters have built-in digital-to-analog converters (DAC) implemented in the feedforward path to establish the reference voltages dynamically. High-speed conversion is achieved with the same number of comparators as the intended number of bit resolutions. The built-in DACs are realized using simple current steering circuits and R-2R resistor networks. Several techniques such as auto zero, two-step operation, and pipelining are used to achieve the high-speed high-accuracy performance.

The Two-Step Dynamic Reference design can achieve a conversion rate of one sample/clock. Compared with the conventional two-step ADC, it does not need to generate residue voltage for the operation of fine stage. The Pipelined design can achieve even higher speed at the expense of more S/H amplifiers and longer latency than the Two-Step one. Residue voltage production is also eliminated, which is a performance limitation in conventional Pipelined ADC.

The two proposed topologies use the same basic building blocks. The high-speed comparator is designed using auto-zero technique to realize high accuracy. The effect of channel charge injection is also eliminated by employing proper clock scheme. The

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sample-and-hold amplifier uses two pair of feedback capacitors, and the interleaving technique is not used for holding the output for a full clock cycle. Folded-cascode structure with gain boosting is utilized for the op-amp to achieve high speed and high accuracy. The R-2R resistor network and current steering circuit employ feedback amplifier to establish accurate reference voltages. The clock generator and bias circuit are also properly designed.

An 8-bit Two-Step Dynamic Reference ADC and an 8-bit Pipelined Dynamic Reference ADC are both implemented using the 0.18 μ m 1P6M CMOS process. The layout of the Pipelined design has also been done. The pre-layout simulation shows that the Two-Step design has a Differential Nonlinearity (DNL) of 0.36LSB and an Integral Nonlinearity (INL) of 0.58LSB; the Signal-to-Noise-and-Distortion Ratio (SNDR) and Spurious Free Dynamic Range (SFDR) are 41.13dB and 53.62dB when the input frequency is 20MHz. The post-layout simulation has been carried out for the Pipelined design. It has a DNL of 0.12LSB and an INL of 0.25LSB. The dynamic performance indicates a SNDR of 41.93dB and a SFDR of 56.03dB when the input frequency is 24MHz. The evaluation of SNDR and SFDR with respect to the sampling frequency variation and the input frequency variation were also characterized. The Pipelined Dynamic Reference ADC implemented in this work achieves a comparable performance as the state-of-the-art high speed ADC designs in literature.

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Chapter 1 Introduction

This chapter gives an introduction of analog-to-digital converter (ADC). First, the background is presented such as the role played by data conversion circuitry in modern electronic system and the classification of A/D converters. Then the objective of the research work is illustrated with the design specification. After that the major contribution of this research work is described. Finally the organization of the thesis is stated.

1.1 Background

In the 1960s, Intel's co-founder Gordon Moore, predicted that the number of transistors per square millimeter of silicon would double every one and half years. This prediction, which is called Moore's law, has been proven to be very visionary. In the past two decades, integrated circuit density and complexity have gone through an amazing revolution as a result of the rapid development of semiconductor fabrication technology. The speed of digital integrated circuit also becomes faster and faster because of the continuous device minimization. The clock rates have moved into hundreds of MHz or even GHz range while consuming acceptable power. At the same time, digital signal processing has also developed very rapidly in the past few decades, with more complex algorithm realized by using new DSP architectures.

Because of the advancement in integrated circuit fabrication technology and digital signal processing algorithm, many functions that were traditionally performed by analog circuit have shifted into the digital signal processing domain. However, the

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real world is analog in nature. Transducers pick up physical parameters such as pressure, temperature, strain or position and convert to analog signal for further processing. As a result, there must always be some linkage between the real analog world and the digital world of signal processing, irrespective of how advanced the integrated circuit fabrication technology and the DSP algorithm would develop in the future.

For that reason, different data converters (analog-to-digital converters and digital-to-analog converters) of various topologies, which provide different speed, resolution, SFDR, SNDR and power consumption performance, have been developed to make the interface. Figure 1.1 shows the typical processing cycle of natural signal. First, the weak analog signal is amplified to a sufficient level for the subsequent circuitry to process. Then the anti-aliasing filter removes the unwanted, out-of-band interferers. After that, the ADC (analog-to-digital converter) digitizes the continuous analog signal so that it would be ready to be processed by the DSP core. At the backend, the DAC (digital-to-analog converter) reproduces the analog signal and the re-construction filter removes the sharp corners or the high frequency content. Finally, another amplifier stage boosts the power of the analog signal to the wanted level.

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Figure 1.1 Processing Cycle of Natural Signal

Nowadays, the ever-growing speed and resolution of DSP and digital integrated circuits, as well as modern communication systems, make data conversion interface the bottleneck of the whole system. The vital roles that are played by data converters make them continually a challenging and hot research topic currently and in the future.

Basically, to realize the A/D converter implementation is much more difficult than to implement the D/A converter. There are plenty of ADC topologies for different applications. In general, low-to-medium-speed and high-accuracy ADCs are needed for the applications such as audio signal processing, instrumentation and measurement (I&M), whereas the advances of imaging, video, and digital communication systems are the main driving forces for the development of high-speed and low-to-medium-accuracy ADC. Table 1.1 shows the classification of ADC architectures and Figure 1.2 gives more examples of ADC applications.

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Table 1.1 Different A/D converter architectures [1]

Low-to-Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low-to-Medium Accuracy
Integrating	Successive approximation	Flash
Oversampling	Algorithmic	Two-step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

Figure 1.2 ADC applications [2]

Normally the transceivers of modern high-speed wireline and wireless communication systems require high-speed ADCs with medium resolution realized in deep-submicron CMOS [3], [4]. Standards such as the 1000BASE-T Ethernet

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protocol usually require a resolution of 7-9 bits under a conversion rate of more than 80 MSample/s. Besides that, low power ADCs are highly preferred in the transceiver applications with digital signal processors and in the portable systems. So the motivation of this research work is directed towards the design of high-speed ADC architectures for such applications.

1.2 Objective

This research work is directed towards the design of high-speed and low-power analog-to-digital converter, with 8 bits of resolution under static operating condition and an effective number of bits (ENOB) of 7 bits at 100 MSample/s. Conventional ADCs for high-speed applications employ flash, folding and interpolating, subranging, and pipelined architectures, whereas in this work, two novel ADC architectures, which are named Two-Step Dynamic Reference ADC and Pipelined Dynamic Reference ADC, are proposed and implemented.

The objectives of the research work are as follows:

- 1) Investigate the topologies of high speed CMOS A/D converter, as well as the basic building blocks of ADC such as low-offset high-speed comparator and high performance sample-and-hold circuit.
- 2) Design ADC architectures which make optimum tradeoff among speed, accuracy, and power consumption using a top-down methodology. The optimum tradeoff is quantified by the Figure of merit (FOM), which would be defined in Section 2.9 of the thesis. The FOM of the implemented design would be compared

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with those of the state-of-the-art high-speed ADCs in literature. Various circuit techniques could be employed in order to improve the FOM of the design.

3) Conduct transistor level design of the fundamental building blocks such as the high-speed low-offset comparator and the sample-and-hold amplifier, for the proposed topologies to achieve the required specification.

4) Construct, simulate, optimize and layout the implemented A/D converter circuit.

5) Compare the performance of the ADC circuit with other state-of-the-art high-speed design in the literature and give recommendations for future work.

1.3 Major Contribution

The two ADC designs in this work are the novel Multi-Step (Two-Step and Pipelined) Dynamic Reference topologies proposed by improving several aspects of the previous work in [5], which is named Unclocked Dynamic Reference A/D Converter. It can achieve high speed as the conversion time is limited only by the propagation time of its internal signals. The chip area and power consumption are small. Furthermore, since no internal clock signal is used, control lines can be minimum.

However, there are also a few aspects of the Unclocked Dynamic Reference ADC that deserve further improvements. First, due to the sequential nature of the dynamic reference A/D conversion algorithm and varying input, there are glitches presented in the output of the ADC. Second, because offset compensation technique cannot be

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used, the comparator circuits become the performance bottleneck of the whole converter by limiting the output accuracy severely. In this work, the Multi-Step Dynamic Reference topologies are proposed to overcome those drawbacks and to improve the performance.

The author adopts several techniques by using internal clock signal. First, the clock signal may be utilized to define the output sampling time, so that the glitches that are generated due to the serial nature of internal operation can be removed. Second, switched-capacitor circuit technique is used to reduce comparator offset voltage. So the accuracy of the converter can be improved tremendously. Finally, the one-step conversion of the original design is divided into multiple steps, enabling the use of pipelining operation, so that higher throughput can be achieved without increasing the hardware complexity.

The first proposed topology is the Two-Step Dynamic Reference ADC design. Using only one sample-and-hold amplifier, the conversion is divided into two steps. This topology has less number of comparators (the same as the intended bits of resolution) compared with conventional two-step ADC. So more power budget can be allocated to reduce settling time and hence ensures high conversion speed. Furthermore, the hardware simplicity of the proposed design leads to low power consumption.

The other topology is the Pipelined Dynamic Reference ADC, which is to be implemented in silicon. By using one sample-and-hold amplifier for each stage, it achieves a pipelined conversion of 1 bit per stage. Compared with conventional

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Pipelined ADC, it eliminated the usage of residue amplifiers, which may limit the ADC performance.

The disadvantage of the proposed ADC topologies is mainly due to the mismatch effects between a large number of current sources and resistor strings, which would cause inaccuracy in voltage reference. The author tried to address it in the latter part of the thesis.

1.4 Organization of the Thesis

The thesis is organized as follows. Chapter 1 gives the background of the project, including the role played by data converters in modern electronic system and the classification of analog-to-digital converters. The objective as well as the major contribution of the research work is also presented. Chapter 2 reviews high-speed ADC design on the aspects of performance characterization and architectures. The advantages and drawbacks of them are described in detail. The state-of-the-art high-speed designs in the literature are also reviewed in the last section. Chapter 3 proposed a novel Two-Step Dynamic Reference ADC topology and a Pipelined one. This group of architectures has several key advantages over the conventional high-speed ADCs and the Unclocked Dynamic Reference converter design in [5]. Chapter 4 gives the transistor level design of the fundamental building blocks of both architectures, such as comparator, sample-and-hold amplifier, resistor network, current steering circuit, clock generator and bias circuit. Chapter 5 shows the layout of an 8-bit Pipelined Dynamic Reference ADC. After that, the post-layout simulation

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results of some basic building blocks are presented. The pre-layout simulation results of the Two-Step design and post-layout simulation results of the Pipelined one are also shown. The comparison with some state-of-the-art high-speed ADCs is presented. Finally, Chapter 6 states the conclusion of the report and gives recommendations for future work.

Chapter 2 Review of High-Speed A/D Converter

In this chapter, a literature review of high-speed ADC topologies is conducted. In the first section, the performance characterization of ADC is introduced. Then the design problems of high-speed ADC are briefly listed. The subsequent sections describe the working principles of various high-speed ADC structures such as the full Flash, Two-Step, Subranging, Pipelined, Folding and Interpolating, and Time-Interleaved ones. The last section talks about the state-of-the-art high-speed A/D converters in the literature. The performances of various topologies that are implemented with the latest technologies are compared. The tradeoff between speed, accuracy and power consumption is also stated.

2.1 ADC Performance Characterization

The performance of A/D converter is often characterized using two major categories of parameters: the static parameters and the dynamic ones. As its name implies, a static parameter is related to the DC operating condition of the converter. In contrast, the dynamic parameters are measured with an analog input signal that varies with time. The dynamic performance of the ADC is dependent on the frequency of the input signal.

2.1.1 The Static Parameters

Of the static performance, the offset is the difference between the ideal and actual input voltages required to obtain the code 000....00. And the gain error is the

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difference of the slopes between the lines connecting the ideal and actual transitions for the full scale range, i.e. from code 000...00 to code 111...11. Figure 2.1 illustrates both the offset and gain error for a 2-bit A/D converter.

Figure 2.1 The offset and gain error for a 2-bit ADC [1]

Assuming the transfer curve is a straight line, the ideal and actual relationships between the input and the output of the converter can be described by the following equations:

$$V_{out,ideal} = G_{ideal} \cdot V_{in,ideal} \quad (2.1)$$

$$V_{out,actual} = G_{actual} \cdot V_{in,actual} + V_{os} \quad (2.2)$$

where V_{in} is the input voltage of the converter and V_{out} is the output voltage. V_{os} is the offset voltage. The gain error can be considered as the deviation between G_{ideal} and G_{actual} .

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The absolute accuracy is related to the difference between the theoretical and the actual input voltages required to convert a particular output code, which includes the offset, gain, and linearity errors. However, in actual situation, the offset and gain error can be calibrated by subtracting the offset and dividing the gain. Thus, the relative accuracy is defined after this normalization.

The Integral Nonlinearity Error (INL) is defined as the largest deviation of codes from a straight line connecting the two ends of the full scale. In contrast, the Differential Nonlinearity Error (DNL) is defined as the actual difference between two adjacent codes minus 1 Least Significant Bit (LSB), which can also be described by the following equation

$$DNL_i = (V_{i+1} - V_i) - 1LSB \quad (2.3)$$

where V_i is the actual value of the i^{th} transition level.

In actual measurement, both INL and DNL are evaluated after removing the offset and gain error to obtain the relative accuracy, which is used to characterize the static performance of the converter. A slow linear input voltage generated from the ramp synthesizer could be utilized for the test of static performance. A digital-to-analog conversion would also be included to re-construct the analog signal from the digital output bits of the device under test (DUT), which can be captured by an oscilloscope.

2.1.2 The Dynamic Parameters

The Dynamic parameters are related to the performance of the converter using AC input signal, i.e. under input transient condition, which is a consequence of limited

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bandwidth, slew-rate limitation, and accuracy etc. The dynamic performance is dependent upon the frequency of the input signal.

Total harmonic distortion (THD) is the ratio of the square root of the sum of the squares of the most significant harmonics (usually from the second to the fifth ones) to the magnitude of the input fundamental (usually the input is a pure sine wave).

$$THD = \frac{\sqrt{(V_2^2 + V_3^2 + \dots)}}{V_1} \quad (2.4)$$

where V_1 is the fundamental component; V_2 , V_3 , and so on are the magnitudes of the second, third harmonics etc. THD represents the distortion of the output waveform caused by INL, DNL and other non-linearity.

Signal-to-Noise Ratio (SNR) is the ratio of the power of input signal to the noise floor, which is usually the remaining harmonics (those excluding the second to the fifth ones). The noise mainly originates from the quantization error of the input signal and the device noise. The quantization noise is due to the finite resolution of the converter, whereas the device noise is from the internal circuitry such as current sources, amplifiers, resistors and so on.

For example, an ideal N-bit ADC has a SNR of

$$SNR = 6.02 \times N + 1.76 \text{ dB} \quad (2.5)$$

The device noise manifests itself as the deviation from the theoretical SNR value that is mainly due to the quantization noise.

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SNDR is actually the power of input to the combined noise floor and distortion, which is a more realistic figure than THD and SNR. Some manufacturers specify a parameter called Effective Number of Bits (ENOB) based on the value of SNDR.

$$ENOB = \frac{(SNDR - 1.76)}{6.02} \text{ bits} \quad (2.6)$$

The equation is obtained from equation 2.5 with SNR replaced by SNDR and N replaced by ENOB. This parameter measures the actual accuracy of the converter using input voltage of certain frequency.

Another dynamic parameter is the Spurious Free Dynamic Range (SFDR), which is the ratio of the Root-Mean-Square (RMS) value of the input signal to the RMS value of the largest harmonics. In communication applications, the SFDR is one of the most important parameters to characterize the performance of a system.

To evaluate the dynamic performance of the A/D converter, the FFT (Fast Fourier Transform) test and the Code Density Test (CDT) are widely employed. By doing FFT for the output signal using software tools such as Matlab, the frequency spectrum can be obtained, and subsequently the SFDR, SNDR and ENOB can be calculated based on the spectrum. The Code Density Test is an alternative method to get dynamic parameters. In the CDT, the converter performance is inferred from the histogram of the output code when the input of the converter is produced from a high-purity sine wave generator.

Chapter 2 Review of High-Speed A/D Converter

2.2 Design Problems for High-Speed ADC

After describing the performance characterization of A/D converters, let's look more closely to the design problems particularly related to high-speed ADC. They can normally be classified into two categories: timing errors and distortion.

There are 4 main sources of timing errors in designing ADC [6]:

- 1) Limited rise and fall time of the sampling clock;
- 2) Signal-dependent delay;
- 3) Clock jitter;
- 4) Clock skew.

The distortion of a quantized signal can be caused from the following reasons [6]:

- 1) Aperture time of sampling comparators;
- 2) Distortion in the input buffer or input signal amplifier;
- 3) Offset in input amplifiers and comparators;
- 4) Changes in the reference voltage values;
- 5) Delays of analog signal and clock signal.

All the above-mentioned design problems must be carefully handled in high-speed ADC design in order to achieve high accuracy.

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2.3 Full Flash ADC Architecture

From this section onwards, the architectures of high-speed A/D Converters are reviewed. First, let's look at the flash A/D converter.

Full Flash ADC has the simplest topology among all the high-speed A/D converters. It is also the fastest design, as seen in some publications [7], [8]. The Flash technique is also known as the parallel-approximation technique. It uses the most straightforward way to achieve A/D conversion.

Figure 2.2 A Typical 3-bit Flash ADC Topology

The Flash converter uses a parallel array of comparators to sample the analog input and reference voltages simultaneously to attain high conversion speed. Figure 2.2 shows a typical flash ADC topology.

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Since for each quantization level one comparator is needed, an N -bit Flash converter requires an array of $(2^N - 1)$ comparators. The analog input voltage is connected to one input of each comparator while the other input is connected to a fixed reference voltage established by a resistor string. These references represent equidistant voltage levels corresponding to the $(2^N - 1)$ switching points between the voltage extremes of the A/D converter input range. Any comparator connected to a resistor string node where the voltage is larger than V_{in} will have a “0” output while those connected to nodes with voltage less than V_{in} will have a “1” output.

Flash ADC has a processing rate of 1 sample/cycle. The highly parallel structure makes the sampling rate of several GS/s to be possible [9], [10]. However, the number of comparators and other hardware components is doubled for each additional bit. So the drawback of the technique is a significant increase in power dissipation for high resolution. As a result, ADCs with resolution of higher than 8 bits are rarely based on the Flash architecture. Besides that, matching of resistors beyond 10 bits of accuracy is difficult to achieve in current technology.

2.4 Two-Step ADC Architecture

The high power consumption and large chip area of the full Flash topology, which result from its hardware complexity, restrict the resolution of the output. For many high-speed applications, resolution of 10 bits or more is required, which is not realistic to be implemented using full flash design (e.g. more than 1000 comparators

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would be required for a 10-bit full Flash ADC). The Two-Step ADC architecture is developed to overcome this problem.

Figure 2.3 A Two-Step ADC architecture [1]

The topology of the Two-Step ADC is more sophisticated than that of the full Flash ADC. In a simplified architecture without digital error correction, two $N/2$ -bit Flash ADCs, one $N/2$ -bit DAC, one analog subtractor, one gain amplifier, several S/H amplifiers and some latch circuits are needed for the basic operation. First, the coarse ADC in the first stage generates the $N/2$ MSBs from the held output of the S/H amplifier. Subsequently, the $N/2$ MSBs are converted back to equivalent analog voltage by the $N/2$ -bit DAC. Then the subtractor subtracts the analog voltage from the held output of the S/H amplifier to produce the residue, which would be used to estimate the LSBs in the second stage. Before processing by the second stage ADC, the residue is amplified by a gain of $2^{N/2}$ to ease the requirement of the circuitry of the fine ADC stage. Finally the fine stage produces the $N/2$ LSBs.

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Since only two Flash converters with resolution of $N/2$ bits are used, the hardware complexity is significantly reduced as compared to an N -bit full Flash design. For example, about 1023 ($2^{10}-1$) comparators are needed for a full Flash architecture with 10-bit resolution. Whereas for a Two-Step ADC, only 62 ($2 \times (2^5-1)$) comparators are needed.

However, in the above-mentioned topology, the coarse ADC should be at least N -bit accurate, which is hard to be realized in high-speed application. To solve this problem, normally digital error correction logic would be incorporated to ease the requirement. Figure 2.3 shows a typical Two-Step ADC with digital error correction circuit. It would correct an error of up to half LSB of the coarse stage ($N/4$ LSBs of the whole converter), so that the linearity and accuracy of it only need to be $N/2$ -bit. However, the range of the fine stage should be expanded to $(N/2+1)$ bits for accommodating the maximum error. Gain of the residue amplifier is also reduced accordingly. So after incorporating the digital error correction technique, neither of the two ADCs needs to be N -bit accurate.

Compared with the full Flash topology, the Two-Step architecture occupies smaller silicon area, consumes less power and has less capacitive loading for the input S/H amplifier. Besides that, since the two internal ADCs used need not to be N -bit accurate, the voltages that the comparators need to resolve are less stringent.

However, the gain amplifier before the second stage is one of the major limitations, which is required to be high-speed as well as highly accurate. The S/H amplifier is also difficult to realize, which will limit the dynamic performance. Furthermore, as

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the fine stage can only start to process until the coarse ADC finish conversion, two clock cycles are needed for processing one input sample. As a result, the processing rate of it is half of that of the full flash one. To double the speed of the two-step ADC to realize a conversion rate of one sample/cycle, Another S/H amplifier is often used between the first and the second stages. In this way, a pipelined conversion is achieved.

2.5 Subranging ADC Architecture

Broadly speaking, Subranging ADC is also one kind of “Two-Step” architecture [11]. It consists of coarse conversion and fine conversion banks. However, the residue amplification circuitry is eliminated from the conventional Two-Step design.

Figure 2.4 A Subranging ADC architecture

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The Subranging topology has a resistive ladder that provides both the coarse and fine reference voltages. Figure 2.4 shows its topology. First, the coarse ADC generates the $N/2$ MSBs using the coarse reference voltages. Then the analog multiplexer (AMUX) chooses the appropriate subrange of the resistive ladder as the fine voltage reference based on the MSBs' values. After that, the fine ADC starts to process and generates the $N/2$ LSBs.

Compared with the Two-Step topology, the Subranging ADC eliminates the high-speed high-accuracy residue amplifier, which is the major limitation for the performance of the Two-Step converter. This enables potentially faster conversion.

However, there are also some drawbacks associated with this topology. First, the number of resistors of the reference ladder is the same as that of the full Flash design, which creates heavy input loading. Besides that, it also introduces component matching problem and restricts accuracy and linearity of the converter. Second, the AMUX may limit the speed of the conversion as the maximum output swing is large and output loading is heavy. Techniques like interpolation and averaging can be used to reduce the number of resistors of the voltage reference, and absolute value signal processing can be used to reduce maximum output voltage swing of the AMUX.

By expanding the range of the fine voltage reference, digital error correction can be incorporated to the architecture similar to the Two-Step design, which relaxes the accuracy requirement of the coarse conversion stage. Two clock cycles are also needed for processing one input sample for this topology.

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2.6 Pipelined ADC Architecture

The idea of Two-Step conversion can be generalized to a multi-step design. Pipelined ADC is the most popular multi-stage architecture for high-speed application [1]. Figure 2.5 shows the block diagram.

Figure 2.5 A Pipelined ADC architecture

For the Pipelined ADC architecture, multiple conversion stages are cascaded, which are separated by sample-and-hold amplifiers. The structure of each stage as well as the operating principle is similar to that of the Two-Step ADC. To achieve pipelined operation, one sample-and-hold amplifier per stage is required for memorizing the data processed by each stage, and shift registers are needed to reconfigure the correct output data membership. Consequently, the conversion rate is determined by the time needed to transfer data from one stage to the next, not from the input to the output of the converter.

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Pipelined operation allows the increasing of resolution without sacrificing too much conversion time, chip area or power consumption. The architecture is very efficient in terms of hardware complexity, which is only linearly proportional to the number of bits.

However, in the first few stages, maximum accuracy is required. As a result, the settling of the residue amplifier becomes the speed bottleneck of the whole converter for high resolution conversion. Besides that, the input sample-and-hold amplifier is another critical component, which determines the linearity of the converter. Due to these limitations, although the processing rate of Pipelined ADC can achieve 1 sample/cycle, its sampling frequency is not as high as that of the full Flash design. However, it can achieve higher resolution and occupy much smaller area.

2.7 Folding and Interpolating ADC Architecture

The A/D converter of the folding topology also has a coarse stage and a fine stage as the Two-Step design. But a folding A/D converter determines the LSB separately from the MSB using analog processing technique. The LSB is generated at the same time as the MSB. Compared with the Two-Step architecture, internal D/A converter and residue amplifier are eliminated.

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Figure 2.6 A 4-bit Folding ADC and the waveform with a ramp input

Figure 2.6 shows a 4-bit folding ADC as well as the waveform of the output of the folding block when the input is a ramp voltage. The folding blocks have different groups of folding points, which cover all the voltage taps of a 4-bit voltage reference. In this manner, the LSBs are produced without the prior knowledge of the MSBs.

As shown in section 2.3, the flash ADC has a large number of comparators that introduce plenty of input capacitance. This drawback severely limits the performance of the flash architecture at high resolution application, besides occupying a large silicon area. To alleviate the limitation, usually interpolation technique is used to reduce the reference voltage taps and hence, the input capacitance. Figure 2.7 is the topology of a flash converter with interpolation (single ended). Each interpolation for

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the preamplifiers of the comparator array reduces the number of voltage taps by half.

So totally a $4\times$ reduction of input capacitance and reference taps is achieved.

Figure 2.7 Interpolations ($4\times$) inside the flash ADC architecture (single-ended)

Since interpolation is a very effective technique to reduce the input capacitance and hardware complexity, it is also frequently used inside the folding ADC architecture, by interpolating at the interface between the folding blocks and latches. The Folding and Interpolating ADC is another popular method to realize high-speed A/D conversion.

2.8 Time-Interleaved ADC Architecture

To perform high-speed conversion at very high sampling rate (e.g. tens of GSample/s) with large analog bandwidth, a single A/D converter is normally not

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enough. For such application, multiple analog-to-digital converters are used in a time-interleaved mode [1]. Figure 2.8 shows a typical Time-Interleaved ADC architecture. In this design, the type of basic converter used is not important. As the individual converter can process in lower speed, the performance of each of them is improved, especial on the aspect of Bit-Error-Rate (BER).

Figure 2.8 A Time-Interleaved ADC architecture

However, there are also some disadvantages associated with the design. First, because not all converters have the same offset voltage, offset trimming is needed. Second, the gain of each converter must be trimmed too. Third, the converters used have different INL and DNL specifications, which introduce distortion components. However, with a careful design, high performance can still be achieved using the Time-Interleaved architecture.

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2.9 The State-of-the-Art High-Speed ADCs

The design of high-speed ADC always leads to a tradeoff between conversion speed, accuracy and power consumption. To compare the performance, a figure of merit is often used so that those important parameters could be considered together [17]:

$$FOM = \frac{2^{ENOB} f_{smp}}{P_{diss}} \quad (2.7)$$

where P_{diss} is the total power dissipation of the converter and f_{smp} is the sampling frequency. This definition of FOM is to be used in the subsequent part of the thesis.

Figure 2.9 Speed vs. resolution tradeoff for state-of-the-art high-speed ADC [20]

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Table 2.1 Performace of the state-of-the-art high-speed ADC

Author/Year	Architecture	$ENOB$ (bit)	P_{diss} (mW)	f_{samp} (MS/s)	Technology (μm)	FOM
Mulder/04 [18]	Subranging	7.6	21	125	0.13	1.15×10^{12}
Limotyarakis/05 [19]	Time- Interleaved	7.48	71	150	0.18	0.38×10^{12}
Taft/04 [20]	Folding and Interpolating	7.26	774	1600	0.18	0.32×10^{12}
Srinivas/06 [21]	Flash	5.29	50	160	0.35	0.13×10^{12}
Park/07 [22]	Flash	3.48	78	4000	0.18	0.57×10^{12}
Lee/07 [23]	Time- Interleaved	10.89	909	125	0.18	0.26×10^{12}
Ginsburg/07 [24]	Time- Interleaved	3.93	1.67	125	0.18	1.14×10^{12}
Zjajo/03 [25]	Two-Step	9.7	100	80	0.18	0.67×10^{12}
Ning/06 [26]	Two-Step	7.93	85	250	0.35 (Si-CMOS)	0.72×10^{12}
Ploeg/01 [27]	Two-Step	10.34	295	54	0.25	0.24×10^{12}
Grace/05 [28]	Pipelined	11.8	755	80	0.25	0.38×10^{12}
Xia/06 [29]	Pipelined	9.67	20.2	44	0.25 (BiCMOS)	1.78×10^{12}
Lizuka/06 [30]	Pipelined	10.41	72.8	40	0.18	0.75×10^{12}
Ray/07 [31]	Pipelined	10.84	268	40	0.18	0.27×10^{12}
Honda/07 [32]	Pipelined	8.89	33	100	0.09	1.44×10^{12}
Wu/07 [33]	Pipelined	6.60	30	100	0.18	0.32×10^{12}

Figure 2.9 shows the speed versus resolution tradeoff of the state-of-the-art high-speed ADCs. Table 2.1 summarizes the performance of some typical high-speed converters with different topologies in literature. Obviously, for resolution of less than 6-7 bits, the Flash architecture is preferred, which is the fastest one that provides a

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conversion rate of up to several GHz using latest CMOS technology. In the other hand, the pipelined topology is used in a wide range of resolution (6b to 15b in published literature). Since the hardware complexity of the pipelined design is only linearly proportional to the number of output bits, the penalty to realize a relatively high resolution is not severe. However, the settling time of the sample-and-hold amplifier as well as that of the residue amplifier becomes the speed bottleneck of the pipelined design.

Both the Folding ADC and the Subranging ADC do not need precise subtraction and amplification to generate residue voltage, which makes them to be faster than the two-step topology. However, the frequency of the signal inside the folding blocks is several times that of the input signal for the folding ADC. So it cannot achieve a comparable conversion rate as that of the Flash one. For the subranging converter, the large number of voltage taps connected to the analog multiplexer often introduces a significant capacitance, which limits the conversion speed severely.

As we can see, all the conventional high-speed ADC topologies have their own merits and drawbacks. It leaves motivation for researchers to explore for new ADC architecture that can balance the performance tradeoff better than the conventional ones in certain applications.

Chapter 3 The proposed Multi-Step Dynamic Reference ADC Architectures

This chapter is mainly focused on the proposed architectures in the research work. First, section 3.1 introduces the Unclocked Dynamic Reference topology. An implementation of the architecture using R-2R resistor network and current steering circuit is also introduced. Based on the topology, a Two-Step Dynamic Reference design is proposed in section 3.2 and a Pipelined Dynamic Reference one is proposed in section 3.3. These two architectures can be classified as the “Multi-Step” Dynamic Reference ADC, which has higher conversion speed and accuracy than the original unlocked design.

3.1 The Unclocked Dynamic Reference ADC and the Implementation

Conventional ADC structure (e.g. the Flash converter or the Two-Step one) has a fixed reference voltage ladder. Normally the number of comparators is exponentially proportional to the resolution of the ADC. However, for the Unclocked Dynamic Reference ADC topology, it has the same number of comparators as the intended bits of resolution. In addition, its voltage reference is dynamic in nature and is established by built-in DACs in the feedforward path. Since this type of converter has its output sequence that emerges naturally from the internal operation (not imposed from an external clock), it operates with minimum control lines, so that the use of clock, reset,

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end-of-conversion and chip enable etc. could be eliminated. The general architecture of the Unlocked Dynamic Reference ADC is shown in Figure 3.1.

Figure 3.1 The general architecture of the Unlocked Dynamic Reference ADC

From the figure it can be seen, V_{in} is the output of the S/H amplifier (not shown) that is fed to all 4 comparators. At the input of the first comparator, it is compared with a fixed reference voltage which is half of the full-scale voltage (V_{FS}) and the MSB (B_3) is produced. Immediately the MSB is sent to the reference voltage regulators of all the subsequent stages. The value of the reference voltage of the second stage (V_{ref2}) is dependent on the MSB value.

If the MSB value is “1”:

$$V_{ref2} = \frac{1}{4}V_{FS} + MSB \cdot \left(\frac{1}{2}V_{FS}\right) = \frac{1}{4}V_{FS} + (1) \cdot \left(\frac{1}{2}V_{FS}\right) = \frac{3}{4}V_{FS} \quad (3.1)$$

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If the MSB value is “0”:

$$V_{ref2} = \frac{1}{4}V_{FS} + MSB \cdot \left(\frac{1}{2}V_{FS}\right) = \frac{1}{4}V_{FS} + (0) \cdot \left(\frac{1}{2}V_{FS}\right) = \frac{1}{4}V_{FS} \quad (3.2)$$

Then based on the input value and V_{ref2} , the second bit (B_2) is generated. It is again fed to the reference voltage regulators of all the subsequent stages. Both the MSB and the second bit are used to determine the reference voltage of the third comparator and the third bit (B_3) is obtained. In this way, the value of the reference voltage of each bit is determined by the values of all previous bits. The digital output bits are generated in a sequential way until finally the LSB is obtained. The voltage regulators function as built-in DACs with offset voltages.

The design uses a serial technique with comparators in its speed limiting path. The conversion is unlocked and one-step in nature. The decision path is always feedforward, therefore it is unconditionally stable and does not suffer from local minima which one might expect from a configuration with direct or indirect feedback. It belongs to a class of converters known as the type 1 equilibrium encoder [12]-[16], also known as stage-by-stage A/D converter or cascaded-stage A/D converter.

One possible realization of the Unlocked Dynamic Reference architecture is shown in Figure 3.2. By eliminating the switches, a “tug-of-war” situation occurs at every input of the comparators. In this figure we assume the input signal range is from 0V to 16V. For the output of the comparator, a digital “1” represent DC voltage of 0V and a digital “0” represent DC voltage of -1V. The rectangular boxes represent resistors and the respective numbers are the normalized conductance.

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Figure 3.2 Unlocked Dynamic Reference ADC using comparators and passive elements

To give an example for the detailed operation, we assume an input voltage value of 10V. Then the current summation at the input of the MSB comparator is

$$I_{i3} = 8V_{ref} + 1V_{in} = -8 + 10 = 2A$$

Since $V_{i3} \geq 0$, the comparator output gives a voltage of -1V, or $\overline{B_3} = 0$.

Subsequently at the input of the second comparator, the current summation is

$$I_{i2} = 4V_{ref} + 1V_{in} + 8V_{o3} = -4 + 10 - 8 = -2A$$

Since $V_{i2} < 0$, the comparator output gives a voltage of 0V, or $\overline{B_2} = 1$.

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Then at the input of the third comparator, the current summation is

$$I_{i1} = 2V_{ref} + 1V_{in} + 8V_{o3} + 4V_{o2} = -2 + 10 - 8 + 0 = 0A$$

Since $V_{i1} \geq 0$, the comparator output gives a voltage of -1V, or $\overline{B_1} = 0$.

Finally at the input of the LSB comparator, the current summation is

$$I_{i0} = 1V_{ref} + 1V_{in} + 8V_{o3} + 4V_{o2} + 2V_{o1} = -1 + 10 - 8 + 0 - 2 = -1A$$

Since $V_{i0} < 0$, the comparator output gives a voltage of 0V, or $\overline{B_0} = 1$.

The final digital output is 1010, which is an expected value. However, for this design, linearity and monotonicity depend on the matching of the resistors in the array. So accurate matching is impossible for high-resolution conversion.

Another possible realization of the concept introduced in Figure 3.1 is the topology proposed in [5]. The intuitive working principle of it is shown in Figure 3.3. By using switches, the value of each reference voltage (except that of the MSB stage) is adjusted according to the decisions made from all the previous bits. The switches together with the voltage sources act as the internal DACs.

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Figure 3.3 Unlocked Dynamic Reference ADC using switches to control voltage reference [5]

During this research work, a 3-bit Unlocked Dynamic Reference ADC is implemented. Figure 3.4 only shows the single-ended circuit for the purpose of simplicity. The generation of reference voltages is actually realized by steering current into the R-2R resistor network, which acts as internal DAC blocks with offset voltages. The reason to use this method to establish the reference voltages is based on two facts: First, the current steering circuit is fast; second, only two resistor values are used so the total number of "root resistors" is reduced.

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The overall response time of a serial chain of comparators is approximately equal to $\sqrt{N}t_s$ [5], where N is the number of stages or bits, and t_s is the settling time per stage. Input must not be faster than the overall response time, which determines the conversion speed.

Figure 3.4 3-bit Unlocked Dynamic Reference A/D converter implemented using R-2R resistor network and current steering circuit

Verilog-AMS language is used to model the behavior of the comparators. By using these models to do a top-down design, the construction and simulation time of the architecture design are much shorter than using the SPICE transistor models. From the simulation result in Figure 3.5, the architecture is proved to function correctly to achieve A/D conversion.

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Figure 3.5 Simulation result of the 3-b design with a ramp input

There are several advantages associated with the design in Figure 3.4. First, it can achieve high speed as the conversion time is limited only by the propagation time of its internal signals. Second, the current steering circuit is fast, which can further ensure high-speed performance. Third, because of the resistor values used in the R-2R network, the matching is good. Last, this ADC design has minimum control lines, so that it can be incorporated into a VLSI chip with minimum interfacing interconnections or could be used together with a sensor at a remote end as in a data-logger.

The disadvantages of the topology are also obvious. First, due to the sequential nature of the dynamic reference A/D conversion algorithm and the varying input, there are glitches presented in the output transfer curve of the ADC (as can be seen from Figure 3.5). Second, since offset compensation technique cannot be used, the

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comparators become the performance bottleneck of the whole converter by limiting the output accuracy severely.

3.2 The Proposed Two-Step Dynamic Reference ADC

To overcome the limitations of the Unclocked Dynamic Reference topology, a novel two-step dynamic reference ADC architecture is proposed. By introducing internal clock signal, the conversion is divided into two steps and pipelined so that higher conversion speed could be achieved. Furthermore, glitches are eliminated by defining appropriate output sampling time using clock signal and offset compensation is performed for the comparator array to enhance conversion accuracy.

3.2.1 The Architecture

A 4-bit diagram in Figure 3.6 (a) is used to explain the working principle of the two-step dynamic reference architecture. The single-ended representation is used for analysis. In real implementation, the structure is fully differential.

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(a)

(b)

Figure 3.6 (a) A 4-bit Two-Step Dynamic Reference ADC (b) the clock scheme of the CBANK

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The structure of the whole converter is divided into the coarse conversion bank (CBANK) and the fine conversion (FBANK) bank. The generation of the reference voltages is actually realized by steering current into the R-2R resistor network, which acts as internal DAC blocks with offset voltages. The coarse bank conducts a rough estimation and generates two MSBs. The two MSBs are used to control the switches of the current steering circuit in the fine bank, so that the corresponding reference voltages could be generated. Then the fine bank produces the two LSBs based on the output voltage of the sample-and-hold amplifier and the reference voltages. After generating the output bits, the coarse stage as well as the fine stage proceeds to perform conversion of next sample immediately by proper clock arrangement. In this way, the pipelined operation is enabled.

Figure 3.6(b) is the clock scheme of the CBANK, which is employed for the internal operation of the comparators. Using this timing arrangement, offset cancellation is able to be performed. The clock scheme of the FBANK is similar but with a delay of one clock interval. The details of it would be explained in the next chapter when introducing the comparator design.

The conversion rate of this ADC design is one sample/cycle. Because the structure is divided into two banks, the number of comparators through which the signal propagates during each conversion cycle is half of that of the unclocked design.

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3.2.2 The timing arrangement

Figure 3.7 presents the timing arrangement of the proposed two-step ADC design. The internal clock generates two pairs of non-overlapped phases, with Φ_1 and Φ_2 for the coarse bank (CBANK) and Φ_2 and Φ_3 for the fine bank (FBANK). The detailed timing shown in the figure is explained as follows:

- Interval 1: the S/H amplifier samples the input voltage while the inputs of the CBANK and the FBANK comparators are disconnected.
- Interval 2: the S/H amplifier outputs the first voltage sample $V_{in}(1)$ to drive the CBANK. The FBANK comparators are still disconnected.
- Interval 3: the CBANK samples its own reference voltages. The differences of $V_{in}(1)$ and the CBANK reference voltages are amplified by the preamplifiers of the comparators in the CBANK. At the same time, the S/H amplifier samples $V_{in}(2)$ (the second input sample) and drives the FBANK with $V_{in}(1)$. The output latches of the comparators of the CBANK strobe at the end of this interval to generate the MSBs once the amplifications in the preamplifiers are completed.
- Interval 4: During the fourth interval, the S/H drives the CBANK using $V_{in}(2)$. The FBANK samples its reference voltages, of which the values are determined by the MSBs produced by the CBANK. Similarly, the differences of $V_{in}(1)$ and the FBANK reference voltages are amplified by the preamplifiers of the comparators in the FBANK. At the end of this interval, the latches of the comparators of the FBANK

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strobe and the LSBs are generated, which are combined with the MSBs generated at the end of the third interval to produce the digital output of the A/D converter.

Figure 3.7 Timing Diagram of the Two-Step Dynamic Reference ADC

By the above timing arrangement, it can be seen that the S/H amplifier needs to hold for both intervals during a clock cycle to drive both the coarse bank and the fine bank. The SHA (sample-and-hold amplifier) design proposed in [34] is adopted, which does not use interleaving techniques. As the first output is generated at the end of the fourth interval, the initial latency of this proposed design is two clock cycles. After this latency, a conversion rate of 1 sample/cycle is achieved.

The duration of one clock interval must not be smaller than the overall response time of the serial chain of the comparators of either the CBANK or the FBANK. The overall response time of a serial chain of comparators or amplifiers is approximately equal to the square root of the number of stages times the individual setting time [5]

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$$t_{conv} = \sqrt{N} t_s \quad (3.3)$$

where t_{conv} is the overall response time, N is the number of stages or bits and t_s is the individual setting time. This is only true when the cascaded stages are identical. However, it is not the case for either the coarse stage or fine stage of the proposed design. Of both banks, the MSB comparators are required to control all subsequent stages and hence the output loading decreases from the MSB comparator to the LSB comparator. Because of this, the overall conversion time of each bank of an N -bit ADC of the proposed topology is:

$$t_{conv,CBANK} = \sqrt{t_{s,N}^2 + t_{s,(N-1)}^2 + \dots + t_{s,(N/2+2)}^2 + t_{s,(N/2+1)}^2} \quad (3.4)$$

$$t_{conv,FBANK} = \sqrt{t_{s,(N/2)}^2 + t_{s,(N/2-1)}^2 + \dots + t_{s,2}^2 + t_{s,1}^2} \quad (3.5)$$

where $t_{s,n}$ is the setting time of the n^{th} stage. So the duration of half a clock cycle (one clock interval) should be:

$$t_{interval} \geq \text{MAX} [t_{conv,CBANK}, t_{conv,FBANK}] \quad (3.6)$$

where $t_{interval}$ is the duration of one clock interval. Because the number of comparators is only N and less than that of other high-speed ADC topologies, more power budget can be allocated to each comparator, so that the settling time and the duration of one clock interval can be reduced to increase the conversion speed.

From the above analysis, the total number of comparators on the internal signal path during each conversion cycle is only half of that of the unclocked design with the same resolution. This feature makes the two-step topology possible to achieve a higher processing speed. Furthermore, since output latches are used to sample the

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digital output from the comparators, glitches are totally removed. Finally, the clock-controlled comparator can achieve a higher accuracy by using the auto-zero technique, which would be explained in the next chapter.

3.3 The Proposed Pipelined Dynamic Reference ADC

The Two-Step design in the last section uses only one sample-and-hold amplifier. For the second architecture proposed in the research work, there is one SHA for each conversion stage. By proper arrangement and timing of the internal building blocks, it can achieve a conversion of a one bit per stage and a conversion rate of one sample/clock. Although the hardware complexity and power consumption of the proposed pipelined converter are larger than the two-step one, it can achieve a higher conversion speed.

3.3.1 The Architecture

A 3-bit Pipelined design is shown in Figure 3.8. Similarly, the single-ended representation is used for the purpose of the analysis.

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Figure 3.8 A 3-bit Pipelined Dynamic Reference ADC

The working principle of the 3-bit design is similar to the unlocked ADC in Figure 3.4. However, with an S/H amplifier for each stage and the use of internal clock, the sampled input signal is processed in a pipelined manner. All the S/H amplifiers act as delay elements except for the one at the MSB stage.

The internal clock scheme of the pipelined design is similar to that shown in Figure 3.6(b). But there is one clock delay between every two consecutive stages.

This novel Pipelined Dynamic Reference topology has several advantages over conventional Pipelined ADC design. First, since the DAC operation is inherent in the reference voltage generating circuitry that includes the current steering circuit and the R-2R network, no dedicated D/A converter is needed for each stage. Second, as the reference voltages are dynamically generated, all the residue amplifiers are eliminated. Because for conventional Pipelined ADC, maximum accuracy is required in the first

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few stages, the residue amplifier settling becomes the speed bottleneck of the whole converter for high resolution conversion [1]. By eliminating them, potentially higher conversion speed can be achieved.

One of the major drawbacks of this design is that the accuracy of comparators must be higher than that of the conventional one especially for those of the first few stages, since digital error correction technique is not used. This problem can be solved by using offset-compensated high-speed comparator. The other drawback is that N number of S/H amplifiers is needed for an N -bit Pipelined topology. However, only the S/H amplifier of the first stage needs to have high performance, since for all the subsequent S/H amplifiers the input signal has been sampled by the first SHA already. This greatly relaxes the circuit requirement.

3.3.2 The timing arrangement

The timing arrangement of the 3-bit Pipelined Dynamic Reference ADC in Figure 3.8 is shown in this part. With a dedicated S/H amplifier for each stage, a pipelined operation of 1 bit per stage is realized. Φ_1 is one of the non-overlapping control signals of the first stage. In the block diagram of Figure 3.8, Φ_i is a $(i-1)$ -interval delayed version of Φ_1 . For simplicity, only signal Φ_1 is shown in the timing diagram.

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Figure 3.9 Timing diagram of the proposed Pipelined design

At the input of comparator, the sampling sequence between the input voltage and the reference voltage is different from that of the Two-Step design. For the Pipelined topology, the reference voltage is sampled one interval earlier than the input voltage, whereas the sequence for the Two-Step ADC is reverse as revealed in the timing diagram of Figure 3.7.

The explanation of the timing arrangement in Figure 3.9 is as follows:

- Interval 1: the 1st SHA (the S/H amplifier connected to the MSB comparator) samples the first input voltage ($V_{in}(1)$) and the 1st comparator (the MSB comparator) tracks its own reference voltage.
- Interval 2: the 1st SHA drives the 1st comparator with $V_{in}(1)$. The difference between $V_{in}(1)$ and the MSB reference voltage is amplified by the preamplifier of the

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MSB comparator. The latch circuit of the 1st comparator strobes at the end of this interval and the first MSB is generated.

- Interval 3: During the third interval, the 2nd SHA (the S/H amplifier connected to the comparator of the second bit) leaves the reset state and starts to sample $V_{in}(1)$. The 1st S/H amplifier samples the second input voltage ($V_{in}(2)$) as well as enters the 2nd S/H amplifier with $V_{in}(1)$ at the same time. Both the 1st comparator and the 2nd comparator (the comparator of the second bit) sample their own reference voltages. The reference voltage of the 2nd comparator is determined by the value of the MSB generated at the end of the previous interval.

- Interval 4: the 1st SHA drives the 1st comparator with $V_{in}(2)$. The difference between $V_{in}(2)$ and the MSB reference voltage is again amplified by the preamplifier of the 1st comparator. At the same time, the 2nd S/H drives its respective comparator with $V_{in}(1)$. The difference between $V_{in}(1)$ and the 2nd stage reference voltage is also amplified by the preamplifier of the 2nd comparator. The latch circuits of the 1st comparator and the 2nd comparator strobe at the end of the interval. The second MSB and the first bit of the second stage are generated.

- Interval 5 and 6: During these two intervals, the first and second stages repeat to function in the same way. The third stage starts the pipelined operation. At the beginning of interval 7 (end of interval 6), the first LSB is generated from the latch circuit of the 3rd comparator. The third MSB and the second bit of the second stage are produced as well. The first digital word output is available as soon as the first LSB appears. So the latency of the conversion is 3 clock cycles, of which the number is

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equal to the number of stages (bits). After this initial latency a conversion rate of 1 sample/cycle is achieved.

From this timing arrangement, it can be seen that the S/H amplifiers also need to hold for both intervals during a clock cycle as that of the Two-Step design. One of the major drawbacks is N number of S/H amplifiers are needed for an N-bit Pipelined topology, whereas for the Two-Step ADC, only one S/H amplifier is present. The other disadvantage is that the design has a higher latency compared to the Two-Step ADC with the same resolution.

However, for the Pipelined topology only the S/H amplifier of the first stage needs to have high performance, since the inputs to all the subsequent S/H amplifiers are already sampled signals. This greatly relaxes the circuit requirement. Furthermore, to process only one bit per stage can enhance the speed of the conversion. By examining equations 3.4-3.6 that determine the minimum duration of one clock interval of the Two-Step design, it can be seen that the speed of it is restricted by the signal propagation time of the serial chain of comparators of either the CBANK or the FBANK. In the other hand, the minimum duration of one interval of the Pipelined one is equal to the largest delay of one comparator. In mathematical form

$$t_{interval} \geq MAX[t_{s,N}, t_{s,N-1}, \dots, t_{s,2}, t_{s,1}] \quad (3.7)$$

where $t_{s,n}$ is the setting time of the n^{th} comparator stage and $t_{interval}$ is the duration of one clock interval. Equation 3.7 reveals that the proposed design can achieve high conversion speed since pipelining technique is employed.

Chapter 4 The Basic Building Blocks

In this chapter, the basic building blocks of the Multi-Step Dynamic Reference A/D converters such as the comparator, the sample-and-hold amplifier, the R-2R resistor network, the current steering circuit, the clock generator and the biasing circuit are presented. Both proposed topologies, the two-step and the pipelined ADCs in this work use the same basic building blocks.

4.1 The Comparator

Comparator is a widely used electronic component which is employed to detect whether a signal is greater or smaller than another. In high-speed A/D converters, it is a key building block that determines the speed, accuracy and power consumption. So to design high-speed and low-offset comparators is an important issue for implementing the proposed architectures.

4.1.1 Op-amp Used as Comparator

A simple approach to achieve the function of comparison is to use open-loop op-amp. Figure 4.1 is a two-stage op-amp implemented as comparator. The two-stage comparator does not have compensation capacitor, since it is mainly utilized for nonlinear and open-loop applications.

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Figure 4.1 Two-stage op-amp used as comparator

There are two poles in the transfer function of the above comparator, one is from the first stage and the other is from the second stage. The frequency response of it can be expressed as the following equation:

$$A_v(s) = \frac{A_{v0}}{\left(1 + \frac{s}{p_1}\right) \cdot \left(1 + \frac{s}{p_2}\right)} \quad (4.1)$$

where p_1 is the first pole and p_2 is the second pole; A_{v0} is the DC gain of the comparator and $A_v(s)$ is the frequency response in the form of Laplace Transformation. Because the compensation capacitor is removed, the outputs of the two stages are isolated from each other. As a result, the two poles are simply expressed as

$$p_1 = \frac{-1}{C_1(r_{o2} \parallel r_{o4})} \quad (4.2)$$

$$p_2 = \frac{-1}{C_2(r_{o5} \parallel r_{o6})} \quad (4.3)$$

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where C_i is the total capacitance at the output of the i^{th} stage and r_{oi} is the output resistance of the transistor “ M_i ” as shown in the above figure. From the equations, it can be seen that the first pole is further from the origin than that of the compensated two-stage op-amp. So the frequency response is much faster. Equation 4.3 is still valid when a load capacitance is included.

However, this simple design has a few serious drawbacks. First, since the output of comparator has to slew a large voltage, it often settles too slowly. The other problem is due to the input-offset voltage, which would limit the accuracy of the comparator. As a result, this design is seldom used in modern high-speed medium-accuracy applications.

4.1.2 The Comparator in the Unclocked Design

To solve the slew-rate limitation problem of the comparator in Figure 4.1, the circuit in the following figure can be employed. This comparator is used in the 3-bit unclocked design in the research work.

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Figure 4.2 The comparator used in the 3-bit unclocked design

The two inverters at the output stage can produce rail-to-rail voltage swing and do not suffer from slew-rate limitation. The aspect ratio is increased gradually to achieve a minimum delay time. PMOS input transistors (M1 & M2) are used to achieve a ground-compatible design.

However, this circuit also cannot alleviate the problem of input-offset voltage, which restricts the accuracy of the Unclocked Dynamic Reference A/D converter in Figure 3.4.

4.1.3 The Auto-Zeroed High-Speed Comparator

High-speed comparison requires that the small difference at the comparator input should be amplified to rail-to-rail value in a short time. This requires the comparator to have a fast small-signal response as well as a large slew rate.

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Figure 4.3 shows the output responses of a preamplifier and a regenerative latch respectively when a small differential input voltage is being applied at time 0 (the origin of the time axis). For a simple regenerative latch employing two back-to-back connected transistors, the input port and the output port actually coincide, this provides a positive feedback with feedback factor of 1. It is observed from the figure that a preamplifier has a negative exponential response and a latch has a positive exponential response in time domain. So the preamplifier has a quick response at the beginning of the amplification but cannot settle to the desired output level. On the other hand, the latch circuit is fast only when the voltage is large.

Figure 4.3 Preamplifier and Latch step response [35]

Modern high-speed comparators usually combine the advantages of both preamplifier and latch to achieve a faster amplification rather than using either of

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them on its own. The working principle could be explained with the aid of the above figure when the output of the preamplifier is applied to the input of the latch. First, a small voltage difference at the input is amplified to a larger value V_x in a time of t_1 . During this time the differential output voltage of the latch is zero because of some reset mechanism used. At the end of t_1 , the latch circuit gets out of the reset state and the voltage V_x starts to be amplified. Since the input port and the output port are the same for the simple latch, this voltage appears directly as the differential output voltage. Subsequently a fast buildup occurs because of the positive feedback, until it achieves the value of V_{OH} in a time of t_2 . So the total conversion time is $(t_1 + t_2)$. If the latch circuit is used alone with the same small input voltage, the comparison time is larger than $(t_1 + t_2)$.

However, to apply the above-mentioned technique we need a clock to realize a proper timing arrangement so that the signal would be amplified to a sufficient level before the latch starts to work. Since in our proposed architectures the internal clock is introduced, we are capable to adopt this technique for fast comparison.

Now let's look at the speed of the preamplifier in detail. For a preamp with a single-pole response (or with only one dominant pole), the unity gain frequency is equal to:

$$\omega_u = \frac{g_m}{C_L} \quad (4.4)$$

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C_L is the load capacitance, which is usually the junction capacitance plus the gate-source capacitance of the input transistor of next stage. To achieve a DC gain of A^n , the time constant is obtained from the following equation:

$$\tau_{total1} = \frac{A^n}{\omega_u} = \frac{A^n \cdot C_L}{g_m} \quad (4.5)$$

where τ_{total} is the time constant and g_m is the transconductance of the input transistor.

If instead, n identical amplifiers with a DC gain of A for each are cascaded to achieve the same amplification, its frequency response in the form of Laplace Transformation can be expressed as

$$A_{total}(s) = \prod^n A_i(s) \quad (4.6)$$

$A_i(s)$ is the frequency response of the i^{th} amplifier. The detailed expression can be found by using the following equations

$$A_i(s) = \frac{A}{1 + \frac{s}{\omega_{pi}}} \quad (4.7)$$

$$\omega_{pi} = \frac{\omega_u}{A} = \frac{g_m}{C_L \cdot A} \quad (4.8)$$

Substituting Equation 4.7 and 4.8 into Equation 4.6 we can obtain:

$$A_{total}(s) = \prod^n A_i(s) = \frac{A^n}{\left(1 + \frac{s}{\omega_{pi}}\right)^n} \cong \frac{A^n}{1 + n \cdot \frac{s}{\omega_{pi}}} = \frac{A^n}{1 + \frac{nA \cdot C_L}{g_m}} \quad (4.9)$$

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The above approximation is valid when $s \ll \omega_{pi}$. From Equation 4.9 it can be seen, when having the same DC gain of A^n , the time constant of the cascaded amplifiers is equal to:

$$\tau_{total2} = \frac{n}{\omega_p} = \frac{nA \cdot C_L}{g_m} \quad (4.7)$$

The loading capacitance C_L is similar to the one in Equation 4.5, since both of them represent the output capacitance of the amplifier (junction capacitance) plus the input capacitance of the next stage (gate-source capacitance). Compared Equation 4.7 with Equation 4.5, it is observed that the cascaded amplifiers have a much smaller time constant than that of a single amplifier when achieving the same DC gain. As a result, to realize a fast response in the preamp stage of the comparator, the cascaded topology is preferred.

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Figure 4.4 (a) The comparator design in Pipelined topology; (b) the clock scheme

Figure 4.4(a) shows the comparator design that is utilized in the Pipelined topology. For the two-step converter, the comparator is almost the same as this one, except V_{ref} is entered at phase ϕ_2 and $V_{S/H}$ is entered at phase ϕ_{1d} in the former. It is due to the different timing arrangements of the two topologies.

Based on the earlier analysis, we employed three preamplifiers instead of one and with a latch circuit to achieve a fast comparison. The timing shown in Figure 4.4(b) is explained as follows. During clock phase ϕ_1 (auto-zero phase), the switches on the feedback paths of the preamplifiers are closed. The reference voltage is sampled into

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the left plate of the input capacitor. If the input-offset voltage of the preamplifier stage is considered, the expression of the total charge stored inside the capacitor is

$$Q_C = (V_{REF} - V_{os}) \cdot C \quad (4.8)$$

Figure 4.5 The comparator at (a) the auto-zero phase; (b) the comparison phase.

Figure 4.5(a) shows the circuit configuration of the comparator during the auto-zero phase. The value of the input-offset voltage is stored inside the input capacitor together with the reference voltage. Subsequently during phase ϕ_2 (comparison phase), all the feedback switches are opened (Figure 4.5(b)). The value of the input voltage (which is from the S/H Amplifier) is entered into the left plate of the capacitor. Since the right plate is floating, no discharge path exists and the charge inside the capacitor is preserved. As a result, the voltage at the right plate of the capacitor, which is also the negative input voltage of the preamplifier stage (V_{in-}), can be calculated based on the charge conservation principle.

$$(V_{S/H} - V_{in-}) \cdot C = Q_C = (V_{REF} - V_{OS}) \cdot C$$

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$$\Rightarrow V_{in-} = V_{S/H} - V_{REF} + V_{OS} \quad (4.9)$$

Hence, the voltage difference amplified by the preamp stage is

$$V_{in,preamp} = V_{in+} - V_{in-} = V_{OS} - (V_{S/H} - V_{REF} + V_{OS}) = V_{REF} - V_{S/H} \quad (4.10)$$

It is actually the difference between the reference voltage and the input voltage. The offset voltage has been “auto-zeroed” because it is stored inside the input capacitor during the first clock phase. This technique is called Input Offset Storage (ISS). At the end of the comparison phase, the latch circuit produces the digital output based on the amplified difference.

From Figure 4.4(b), it is observed that the feedback switches that are controlled by signal ϕ_1 open slightly ahead of the one connected to the reference voltage (which is controlled by signal ϕ_{1d}). This timing arrangement is to get rid of the effect of channel-charge injection. After the feedback switch is off, the negative input of the first preamplifier becomes floating. If the charge injected by the switch connected to V_{REF} is Δq , then the voltage change at the left plate of the input capacitor is $\Delta q/C$. However, when the “ ϕ_2 ” switch is on, the voltage at this point changes to $V_{S/H}$. Thus, the overall voltage change is equal to $(V_{REF} - V_{S/H})$. The key point is that, as long as the voltage goes from one fixed voltage V_{REF} to another one $V_{S/H}$, the intermediate fluctuation due to the charge injection of the switch has no effect on the output since the total charge is preserved inside the capacitor.

Of course, there is also charge injection due to the feedback switch. The value is equal to

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$$\Delta q = WLC_{ox}(V_{CK} - V_{TH}) \quad (4.11)$$

V_{CK} is the voltage of the clock signal at level high. The charge value is fixed and not dependent on signal. So its effect is largely removed when fully differential operation is employed as shown in Figure 4.6. However, in practice with the use of differential circuit, charge-injection mismatch error of the feedback switches due to process variation still exists. It is therefore necessary to reduce this error to achieve high accuracy.

Figure 4.6 Fully Differential implementation of the preamp stage

When using differential implementation as shown in Figure 4.6, there is another observation that we can make from the timing scheme in Figure 4.4(b). The feedback switches of the first preamp (which are controlled by signal ϕ_{1a}) open slightly ahead of the rest. When the charges are injected, the offset voltage due to the charge-injection mismatch is stored inside the output capacitors of the first stage, which are also the input capacitors of the second stage. So this offset voltage is “auto-zeroed” by the second preamp since its feedback loops are still closed. The second and the third preamps do not need to employ this technique, because the offset error due to the charge-injection mismatch of their feedback switches (which are

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$$A_v = g_{m1} / g_{m3} = g_{m2} / g_{m4} = \sqrt{\frac{K'_N(W/L)_1 I_1}{K'_p(W/L)_3 I_3}} = \sqrt{\frac{K'_N(W/L)_1}{K'_p(W/L)_3}} \quad (4.12)$$

In order to enhance the voltage gain A_V in equation 4.12, the current sources are used in parallel with the diode-connected load transistors M3 and M4. Thus, A_V is increased to

$$A_v = g_{m1} / g_{m3} = \sqrt{\frac{K'_N(W/L)_1 I_1}{K'_p(W/L)_3 I_3}} = \sqrt{\frac{K'_N(W/L)_1}{K'_p(W/L)_3}} \sqrt{1 + \frac{I_5}{I_3}} \quad (4.13)$$

The gain is enhanced by the square root of 1 plus the ratio of I_5 to I_3 . At the same time, the load resistance is not increased so that the large bandwidth could be retained.

When the latch stage starts to build up the output, kickback noise is generated and dumped to the driving circuitry. The function of the transistors M7 and M8 in Figure 4.7 is to isolate the noise from latch output. Furthermore, these two transistors could reduce the input capacitance due to Miller effect.

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Figure 4.8 Transistor level implementation of the Latch

The latch of the comparator is shown in Figure 4.8, which is adopted from [36]. The differential input voltage is converted to current and mirrored to the cross-coupled transistors M3 and M4. When the $\phi_{2\text{latch}}$ signal is low, the differential output ports are shorted to ground by transistors M9 and M10. At the end of the comparison phase, $\phi_{2\text{latch}}$ goes high and the output is released. The positive feedback regenerates the differential signal to almost rail-to-rail swing. The current mirrors formed by transistors M5-M8 provide isolation between the preamplifier stage and the output latch, so that the kickback noise would be further reduced.

4.2 The Sample-and-Hold Amplifier

As its name implies, sample-and-hold amplifier is used to sample an analog signal and hold it for a length of time. It is a crucial building block in high-speed A/D converters, which can greatly minimize errors due to slight difference in delay time within the internal operation of the converter.

Figure 4.9 A simple open-loop sample-and-hold amplifier

A simple sample-and-hold amplifier is shown in Figure 4.9. When the ϕ_1 signal is high, the voltage at the top plate of the capacitor follows V_{in} . When ϕ_1 goes low, the

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charge in the capacitor is preserved. V_{out} is equal to the value of V_{in} at the instance when the switch is opened. Because this topology has a “track” phase of which the duration is comparable to that of the “hold” phase, it is frequently referred as a “track-and-hold” amplifier.

This simple S/H amplifier has a serious drawback due to the channel-charge injection effect of the input switch. The total channel charge when the switch is closed is equal to:

$$\Delta q = WLC_{ox}(V_{CK} - V_{in} - V_{TH}) \quad (4.14)$$

Assuming half of it is injected into the capacitor, the output error is equal to

$$\Delta V = \frac{\Delta q}{2C} = \frac{WLC_{ox}(V_{CK} - V_{in} - V_{TH})}{2C} \quad (4.15)$$

The value is dependent on the input voltage. Hence, its negative influence on accuracy cannot be eliminated. So this simple design cannot achieve a high accuracy.

4.2.1 The SHA Used in the Proposed Topologies

There are various topologies of S/H amplifier in literature which have different advantages and drawbacks. Some of these are open-loop structures while others are closed-loop structures. To realize the timing arrangement of the proposed topologies shown in Figure 3.7 and Figure 3.9, the SHA design needs to hold the output for a full clock cycle. Traditionally interleaving technique is used to achieve the function [37].

The proposed topologies employ the SHA structure in Figure 4.10, which is similar to the design in work [34]. This S/H amplifier uses the same op-amps to process the

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input sample so that the matching could be better than that of the conventional interleaving SHAs. Furthermore, the SHA in the figure can realize single-to-differential conversion, which is very useful as all the subsequent stages are fully differential.

Two non-overlapping clock signals ϕ_1 and ϕ_2 are employed for the operation of the SHA. ϕ_1 is the sample phase which coincides with the second hold phase. During this phase, all the switches controlled by ϕ_1 are closed. The sample network is isolated from the hold network. The input voltage is tracked by the upper sampling capacitor (C_1) and the common-mode voltage (the value of it is equal to half of the power supply voltage) is tracked by the lower sampling capacitor. These two capacitors are identical in value. The right plates of these capacitors are also connected to V_{CM} (the common-mode voltage). At the same time, the right plates of the “ C_2 ” capacitors are connected to V_{CM} . Thus, they are discharged and at the reset state. At the end of ϕ_1 phase, the switches connected to the right plates of the sampling capacitors open slightly ahead of the rest. By this arrangement, the signal-dependent channel-charge-injection error due to the input switches is eliminated. This technique is similar to that used in the comparator circuit in Figure 4.4.

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Figure 4.10 SHA in the proposed topologies

During the first hold phase (ϕ_2), the left plates of the two sampling capacitors are shorted together. The charge stored inside the sampling capacitors is dumped out. The capacitors C_2 are connected between the input and output of the op-amp to form a close loop. All the charge from the capacitors C_1 is forced into the capacitors C_2 . Since the two inputs of the op-amp are at virtual ground due to the effect of the negative feedback, the value of V_{in} is established differentially at the output. The

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value of C_2 is half of that of C_1 , hence the amplitude of the output is twice of that of V_{in} . At the same time, the right plates and left plates of the capacitors C_3 are connected to V_{CM} . So they are discharged and at the reset state.

During the second hold phase (ϕ_1), the capacitors C_2 are reset. At the same time, the C_3 capacitors are connected to the C_2 capacitors. The charges stored inside both C_2 capacitors are forced into the C_3 capacitors, which continue to hold the differential voltage at the output. At the same time the sampling capacitors C_1 track the next sample of input voltage. In this way, the SHA performs three operations in 2 clock phases without using the interleaving technique.

4.2.2 The Problem due to Offset Voltage of SHA

According to literature [34], the SHA design in Figure 4.10 does suffer from offset voltage problem. The authors claimed that by using large devices for the OTA the value could be only a few millivolts. However, if the actual measurement results are not satisfactory, it should be replaced in future design.

During the sample phase (ϕ_1), because of the negative feedback formed by capacitors C_3 , the following relationship holds

$$V_+ - V_- = V_{OS} \quad (4.16)$$

where V_+ and V_- are the positive and negative terminals' input voltages of the op-amp; V_{OS} is its input offset voltage. At the same time, the right plates of capacitors C_2 are connected to the DC voltage V_{CM} . Hence, the input offset voltage V_{OS} is stored inside

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these two capacitors. As a result, subsequently during the first hold phase (ϕ_2) V_{OS} is successfully cancelled.

However, the offset voltage still causes a change in the output of the SHA during the second hold phase, which may introduce unacceptable error to the ADC.

Figure 4.11 Using two normal SHA to realize the same operation

We observe that the operation of holding the output for a full clock cycle can still be achieved by using two normal SHAs connected in series. The above figure shows the circuit configuration and the timing scheme. It can be seen that “S/H1” holds the first input voltage during clock interval 2 and “S/H2” holds it during interval 3.

The SHA in Figure 4.10 can also be used as a normal SHA (such as the one in Figure 4.11) by simply ignoring the hold operation during the second hold phase.

Using the above timing scheme, the offset cancellation can be successfully achieved.

But the active area occupied by the SHAs is also doubled.

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4.2.3 The Precision and Speed of the SHA

First, let's look at the gain of the SHA in Figure 4.10 during the first hold mode (ϕ_2). The equivalent circuit configuration is shown in Figure 4.12. For the ease of analysis, we used single-ended representation.

Figure 4.12 SHA During the first hold mode

The input and output relationship can be obtained from the following equations

$$(V_{in} - V_-) \cdot sC_1 = V_- \cdot sC_{in} + (V_- - V_{out}) \cdot sC_2 \quad (4.17)$$

$$V_- \cdot A_v = -V_{out} \quad (4.18)$$

where V_- is the voltage at the negative terminal of the op-amp and A_v is the gain of the op-amp. From Equations 4.17 and 4.18 we can obtain

$$\begin{aligned} \left(V_{in} + \frac{V_{out}}{A_v} \right) \cdot sC_1 &= -\frac{V_{out}}{A_v} \cdot sC_{in} + \left(-\frac{V_{out}}{A_v} - V_{out} \right) \cdot sC_2 \\ \Rightarrow \frac{V_{out}}{V_{in}} &= -\frac{C_1}{C_2 + \frac{C_1 + C_2 + C_{in}}{A_v}} \end{aligned} \quad (4.19)$$

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For large value of A_v , the gain is equal to $-C_1/C_2$, which is an expected value. To calculate the error due to the finite gain of the op-amp, the following relationship is derived from Equation 4.19

$$\frac{V_{out}}{V_{in}} \cong -\frac{C_1}{C_2} \left(1 - \frac{C_1 + C_2 + C_{in}}{A_v \cdot C_2} \right) \quad (4.20)$$

So the SHA suffers from a gain error of $(C_1/C_2) \cdot (C_1 + C_2 + C_{in}) / (C_2 A_v)$. Since the nominal ratio between C_1 and C_2 is a fixed value of 2 and C_{in} is a relative small value, the gain error mainly depends on the gain of the op-amp.

The error introduced at the second hold phase is mainly due to the mismatch between C_2 and C_3 .

To estimate the speed of the SHA, the small signal equivalent circuit during the first hold phase can be used, which is shown in Figure 4.13.

Figure 4.13 Small signal model of the SHA during the first hold mode

Using KCL, the following two equations can be obtained from the above figure

$$(V_{in} - V_-) \cdot sC_1 = V_- \cdot sC_{in} + (V_- - V_{out}) \cdot sC_2 \quad (4.21)$$

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$$(V_- - V_{out}) \cdot sC_2 = G_m V_- + \frac{V_{out}}{R_0} + V_{out} \cdot sC_L \quad (4.22)$$

The expression of V_- can be derived from Equation 4.21

$$V_- = \frac{C_1 V_{in} + C_2 V_{out}}{(C_1 + C_2 + C_{in})} \quad (4.23)$$

Substitute V_- to equation 4.22 with the above expression, we can obtain

$$\frac{V_{out}}{V_{in}} = \frac{-C_1(G_m - sC_2) \cdot R_0}{C_2 G_m R_0 + C_1 + C_2 + C_{in} + R_0 \cdot s[C_L(C_1 + C_2 + C_{in}) + C_2(C_1 + C_{in})]} \quad (4.24)$$

From the transform function, the time constant could be calculated

$$\tau_{SHA} = \frac{R_0 \cdot [C_L(C_1 + C_2 + C_{in}) + C_2(C_1 + C_{in})]}{C_2 G_m R_0 + C_1 + C_2 + C_{in}} \quad (4.25)$$

Because $G_m R_0$ is the gain of the op-amp, which is supposed to be a large value, we have $C_2 G_m R_0 \gg (C_1 + C_2 + C_{in})$. Equation 4.25 is simplified to

$$\tau_{SHA} \cong \frac{C_L(C_1 + C_2 + C_{in}) + C_2(C_1 + C_{in})}{C_2 G_m} \quad (4.26)$$

Again since the nominal ratio between C_1 and C_2 is a fixed value of 2 and C_{in} is a relative small value, the time constant is further simplified to

$$\tau_{SHA} \cong \frac{3C_L + C_1}{G_m} \quad (4.27)$$

G_m is equal to the transconductance of the input transistor of the op-amp. The equation is valid as long as the amplifier has only one dominant pole and a reasonable phase margin. Hence, to ensure high speed, large input g_m as well as small input and loading capacitance should be used.

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During the second hold phase (ϕ_2), the charge is transferred from C_2 to C_3 . The time constant is obtained simply by replacing C_1 with C_2 and C_2 with C_3 in Equation 4.26. Since the value of C_2 is only half of that of C_1 and C_3 is equal to C_2 , the speed of the SHA in the second hold phase is faster than that in the first phase.

4.2.4 The Op-amp Design

From the precision and speed considerations shown in the previous part, we can decide the op-amp structure to be used in the proposed topologies. To achieve a high gain, two-stage or gain boosting amplifier should be used. However, for the two-stage op-amp, compensation is usually needed to obtain sufficient phase margin, which slows down the amplifier. On the other hand, the gain boosting design maintains the “one stage” nature when achieving a comparable voltage gain. This property makes gain boosting amplifier to have enough speed for the SHA design in the proposed ADC topologies.

The peak-to-peak amplitude of the output voltage of the SHA should be 1V in the proposed topologies when a 1.8V power supply is used. The large voltage-swing requirement makes the telescopic structure not feasible to be used as the main amplifier. As a result, we choose the folded-cascode structure although it consumes more power. NMOS input transistors are used in order to minimize the input capacitance. The schematic diagram of the folded-cascode OTA with gain boosting is shown in Figure 4.14. The voltage swing of the design is equal to

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$(V_{DD} - V_{eff7} - V_{eff5} - V_{eff3} - V_{eff9})$. Since the overdrive voltage (V_{ov} or V_{eff}) is chosen at around 100mV, we have enough margin to accommodate the 1V swing at the output.

Figure 4.14 The op-amp used in the SHA

The gain of the op-amp is calculated using the following equation:

$$A_V = \frac{V_{out}}{V_{in}} = g_{m1} \{ [(g_{m5} + g_{mb5})r_{o5}(r_{o7} \parallel r_{o2})A_1] \parallel [(g_{m3} + g_{mb3})r_{o3}r_{o9}A_2] \} \quad (4.28)$$

where A_1 is the gain of the auxiliary amplifier “AMP1” and A_2 is the gain of the auxiliary amplifier “AMP2”. Their values are large so that the gain error in equation 4.20 is made sufficiently small.

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The value of g_{m1} influences the time constant and hence the settling speed of the whole SHA. The step response in time domain is expressed as

$$V_{out} = V_{in} \left(1 - e^{-\frac{t}{\tau_{SHA}}} \right) \quad (4.29)$$

In order to settle to the required accuracy, the settling time during the hold phase needs to be at least 6 to 7 times of the time constant.

The fully differential implementation in Figure 4.14 requires a common-mode feedback to define the common mode level of the output voltages. Since the clock signals are used in the SHA, a typical switched-capacitor design [38] is utilized as shown in Figure 4.15.

Figure 4.15 The switched capacitor in the op-amp

The C_S capacitors store the difference between V_{CM} and V_{b4} during the first clock phase ϕ_1 . V_{CM} is the output common-mode voltage, which is also equal to half V_{DD} . V_{b4} is the nominal bias voltage of the bottom NMOS transistors in Figure 4.14 (M9 &

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M10). In the second clock phase ϕ_2 , charge sharing between C_s and C_c occurs if $(V_{out+} + V_{out-})/2$ is not equal to V_{CM} . Later during the next few clock cycles the charge transfer would continue until the outputs settle to the nominal common-mode voltage. At the steady state, V_{b4_1} would be equal to V_{b4} due to effect of the internal feedback mechanism.

The absolute value and matching of the capacitors are not critical. Hence the value should be small. Otherwise the outputs of the op-amp would be overloaded. Transmission gates are used to implement the switches as they are capable of handling wide output swing.

This switched capacitor CMFB has two advantages over the normal one. First, there is no resistive loading introduced to the op-amp. Second, the output swing is not limited by the CMFB used.

Figure 4.16 shows the auxiliary amplifiers employed in the op-amp. The same CMFBs are used as the one in Figure 4.15. The gains of AMP1 of AMP2 are expressed as

$$A_{V1} = \frac{V_{out1}}{V_{in1}} \cong g_{m1} \{[(g_{m5} + g_{mb5})r_{o5}(r_{o7} \parallel r_{o2})] \parallel [(g_{m3} + g_{mb3})r_{o3}r_{o9}]\} \quad (4.30)$$

$$A_{V2} = \frac{V_{out2}}{V_{in2}} \cong g_{m1} \{[(g_{m3} + g_{mb3})r_{o3}(r_{o9} \parallel r_{o2})] \parallel [(g_{m5} + g_{mb5})r_{o5}r_{o7}]\} \quad (4.31)$$

The unity gain frequency of both auxiliary amplifiers ($\omega_{u,aux}$) should be

$$\beta\omega_{u,main} < \omega_{u,aux} < \omega_{p2,main} \quad (4.32)$$

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β is the feedback factor, $\omega_{u,main}$ is the unity gain frequency of the main amplifier, and $\omega_{p2,main}$ is the frequency of the second pole of the main amplifier. Equation 4.32 defines a safe region in which the stability of the op-amp is not destroyed by the auxiliary amplifiers [39].

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4.3 The Resistor Network and the Current Steering circuit

The R-2R resistor network functions together with the current steering circuit to establish the reference voltages. Figure 4.17 is the schematic diagram of the current source with current steering switches.

Figure 4.17 The current source with current steering switches

V_{ctrl} is the control voltage from the outputs of the previous comparator stages in the proposed ADC topologies. V_{th} defines the threshold value of V_{ctrl} to steer current into the R-2R resistor network. It is on half way between voltage “high” and voltage “low” of the digital signals. If V_{ctrl} is low, all the current is injected into the R-2R network. If V_{ctrl} is high, the current goes into the digital ground. The current steering technique is fast and suitable for the high-speed applications. To generate accurate current, large output resistance are required for the current source. Cascode structure (M1 & M2) is employed and transistors use non-minimum channel length.

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However, this technique introduces mismatch problem between a large number of current sources and resistor strings. The accuracy of the voltage sources could be influenced severely.

4.3.1 Problem due to Global Mismatch

The first issue to be handled is the tolerances of the transistors in the current sources and the poly resistors due to manufacturing spread. To fulfill the requirement as a voltage reference, the product of the current value I and resistance value R in the resistor network should be an accurate value that is equal to

$$I \cdot R = \frac{V_{FS}}{2} \quad (4.33)$$

where V_{FS} is the full scale range of the input. The absolute value of poly resistor normally has a process variation of about $\pm 10\%$. The MOS transistors also have variations in μ , W , L and V_{th} , which deteriorate the accuracy of the current source.

To lessen the effects due to this global mismatch, in the proposed design the current value and the resistance value are correlated to achieve a process-invariant product, rather than to achieve an accurate value for I or R alone. The circuit in Figure 4.18 utilizes an op-amp in feedback loop to regulate the correlation.

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Figure 4.18 To establish accurate voltage using op-amp

In the above circuit, the op-amp is employed to regulate the current in each branch to compensate the variation of the value of the poly resistor so that equation 4.33 can be realized with satisfactory accuracy. The open loop gain is equal to $A_v g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2}$, where A_v is the gain of the amplifier. Since the feedback factor is equal to one, the error due to the finite gain can be calculated

$$\text{as } \frac{V_R}{V_{FS}/2} = \frac{A_v g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2}}{1 + A_v g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2}} \quad (4.34)$$

$$\Rightarrow \frac{V_R}{V_{FS}/2} = \frac{1}{1 + \frac{1}{A_v g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2}}} \cong 1 - \frac{1}{A_v g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2}} \quad (4.35)$$

$$\Rightarrow \text{error} = \frac{1}{A_v g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2}} \quad (4.36)$$

This error is negligible with the current circuit parameters and condition.

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However, practical devices in the op-amp suffer from random variations, which introduce input offset voltage. This offset produces gain error for the whole ADC. According to literature [1], it can be removed by dividing with the gain. But in the proposed design no calibration circuit was implemented for this purpose. Instead, a bond pad is employed to monitor the voltage $V_{FS}/2$ of the prototype chip. An externally applied reference DC voltage can be connected to the negative input port of the op-amp. The reference voltage would be manually tuned to cancel the offset during measurement.

4.3.2 Problem due to Local Mismatch

Besides the global mismatch problem, the resistors and transistors on the same piece of silicon also suffer from random variation. From literature [40], a moderate matching, i.e. approximately $\pm 0.1\%$ mismatch for poly resistor can be achieved by using appropriate layout technique, which is equivalent to 9 to 10 bits of resolution. It is sufficient for the 8-bit ADC theoretically. In this design, common-centroid layout techniques such as the one-dimensional interdigitation and the two-dimensional cross-coupling are extensively used. Dummy resistors are also added to create similar environment for resistors at the edges.

To achieve a drain current mismatch of less than $\pm 0.1\%$, i.e. resolution of more than 10 bits, usually trimming is involved [40]. But in the proposed design, we did not apply this technique to the transistors in the current sources. Instead, layout technique similar to that for the poly resistors is employed and non-minimum channel length is

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used, assuming a resolution of more than 8 bits can be achieved. However, the final results can only be verified from measurement.

The accuracy of the current upon the variation of the output voltage of the current sources was also verified by simulation. When the terminal voltage changes from 0.4V to 1.4V (the full-scale reference voltage), the variation of the drain current is only $\pm 0.2\%$, which is more than sufficient for the 8-bit application. The small variation is due to the cascode structure and non-minimum channel length utilized.

4.3.3 The Op-amp design and the differential implementation

The transistor level implementation of the op-amp used in Figure 4.17 is shown below.

Figure 4.19 Transistor level implementation of the op-amp

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Its gain can be obtained using the following equation

$$A_v = g_{m1} \{ [(g_{m3} + g_{mb3})r_{o1}r_{o3}] \parallel [(g_{m5} + g_{mb5})r_{o5}r_{o7}] \} \quad (4.37)$$

In actual implementation, fully differential implementation is used for the resistor network and current steering circuit, which brings several benefits to the ADC performance.

Figure 4.20 Differential R-2R network and current sources versus single-ended one

Figure 4.20 shows the differential R-2R resistor network and current steering circuit as well as their single-ended counterpart. For the single-ended implementation, during the switching event current is injected to or extracted from the ground through the R-2R network. This event introduces noise to the ground, and causes substrate “bounce”. However, for the differential implementation, the upper switches (those without the dots) and the lower switches (those with the dots) are controlled by

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complementary clock signals. Hence the total currents that enter the bias point remain unchanged and hence very little noise is introduced.

In addition, the differential implementation removes the influence of common mode noise. Although the chip area is increased, it is worthwhile because higher accuracy is attained.

4.4 The Clock Generator

Non-overlapping clocks are essential for the operation of comparator and sample-and-hold amplifier. The following simple circuit (Figure 4.21) is used for the generation of internal control signals.

The ϕ_1 signal should fall to zero before the ϕ_{1d} signal reaches the falling edge in order to avoid signal-dependent channel charge injection in the comparator circuits. The small differences among all the other “in phase” signals are due to similar reasons. On the other hand, the ϕ_1 signal and the ϕ_2 signal should be non-overlapping to allow complete charge settling. However, the clock edges need only be moderately controlled. Likewise, as long as the signal inside the preamp stages has been amplified to a sufficient level, the rising edge of the ϕ_{2Latch} signal does not need to be precise. The only requirement is that its duration should be long enough to allow the output to be regenerated to rail-to-rail value. As a result, inverter chains with non-inverting property are employed as the delay elements.

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Figure 4.21 (a) Circuit diagram of the clock generator; (b) the generated signals

4.5 The Biasing Circuit

The Biasing circuit utilized in the proposed topologies is a conventional one (Figure 4.22). Since the supply voltage is quite low, two pairs of wide-swing current

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mirrors are used to generate the bias voltages ($V_{b1} - V_{b4}$). The biasing of the cascoded devices is established by the diode-connected transistors M5 and M14. The resistor R is used to define the current in the loop and the transconductance of transistors. This circuit is also frequently referred as “constant-transconductance” voltage bias.

For the bias loop, the start-up problem does exist when the power supply is turned on. Transistors M15-18 are included to function as the start-up circuitry. At the event of zero current, the transistor M17 is off. Since the gate-source voltage of transistor M18 is always equal to the power supply voltage, it works like a resistor. As a result, the voltages at the gates of transistors M16 and M15 are pulled high, which inject current into the bias loop. Hence the bias circuitry starts up. Because the biasing current in the loop keeps on increasing, the gate-source voltage of M17 goes high. It sinks more and more current from M18 until M15 and M16 turn off. After that, the circuit enters the steady state. Large capacitors (not indicated in the Figure) are also connected to decouple noise from the outside circuitry.

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Figure 4.22 The biasing circuit used in the ADC designs

Chapter 5 The Layout Implementation and the Simulation results

An 8-bit Two-Step Dynamic Reference ADC and an 8-bit Pipelined ADC are constructed in the research work using the 0.18 μ m 1-poly 6-metal CMOS process. In this chapter, first the layout implementation of the Pipelined Dynamic Reference A/D converter is presented. Then the performance of some basic building blocks is shown. After that, the pre-layout simulation results of the Two-Step Dynamic Reference ADC and the post-layout simulation results of the Pipelined Dynamic Reference ADC are stated. Finally the performance comparison with the state-of-the-art high-speed ADC design is illustrated.

5.1 Layout Implementation

Since the Pipelined Dynamic Reference ADC is to be realized in real silicon chip, its layout was constructed in the research work. Figure 5.1 is the floor plan. The digital blocks are allocated at the right side of the chip. In this way, the noisy part and the quiet part are separated in order to alleviate the influence of noise to the analog circuitry. Because the comparator circuits are blended with analog and digital signals, it is put besides the digital blocks. In addition, every analog functional block is enclosed with substrate ties and n-well, which function as guard rings for the purpose of noise isolation. N-well guard rings are also used in the digital blocks. Figure 5.2 presents the idea of using guard ring for isolation.

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The clock generator is placed close to the comparators and the digital blocks. Thus the clock skew error due to long routing is minimized. The bias circuit is allocated at the centre of the layout so that the routing distance would be short to all the analog blocks.

Figure 5.1 The Layout floor plan for the Pipelined dynamic reference ADC

Figure 5.2 Use of guard ring for noise isolation

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The layout uses two pairs of power supply and ground. Hence the large transient current inside the digital blocks would not introduce noise to the V_{DD} and G_{ND} of the analog blocks. The substrate can be connected to either the digital ground or the analog one. If the former is used, the large voltage swing at the outputs of the digital circuits could couple to the substrate through the junction capacitance. This effect makes the threshold voltage of the NMOS transistors fluctuate, which contributes noise to the analog part. Based on this consideration, analog ground is connected to the substrate as the chip ground. Although substrate noise is introduced to the analog G_{ND} , it is not so problematic since the substrate voltage and the analog ground are bouncing together.

Figure 5.3 Cross-coupled transistors with dummies to improve matching

To minimize the error due to device mismatch, symmetrical layout is required for the analog circuitry. Common-centroid layout techniques such as the one-dimensional

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interdigitation and the two-dimensional cross-coupling are extensively used. Figure 5.3 is an example of cross-coupling employed for the input transistors of the preamplifiers inside the comparator. Dummy transistors are added to create similar environment for the transistors on the left side and the right side.

To match the routing paths, the wires with differential signals are in parallel. Lower and upper ground planes are usually used as shield for sensitive lines.

Figure 5.4 Layout of the implemented 8-bit Pipelined Dynamic Reference ADC

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The layout of the prototype chip is shown in Figure 5.4. It has been sent out for fabrication. There is extra chip area consumed due to two reasons. First, the active area occupied by the routing is too large because of the inherent complexity of the interconnects. Second, the extensive use of common-centroid layout technique for the blocks such as the current steering circuit and the resistor network consumes plenty of space and requires complex routing. The total chip area including pads is $2.0 \times 1.9 \text{ mm}^2$.

5.2 The Simulation Results of Some Basic Building Blocks

In this section, the post-layout simulation results of some basic building blocks are presented. First, Figure 5.5 shows the gain and phase plot of the preamplifier when the respective loading capacitance is included.

Figure 5.5 Gain and phase plot of the preamplifier

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The simulation results indicate that a single preamp achieves a gain of more than 10 (20dB) with a phase margin of near 90 degree. The unity gain frequency is about 2.5GHz. As a result, with three preamp cascaded together, a small signal of 0.5mV (equal to 1/8 LSB of an 8-bit ADC) is amplified to about 500mV, which is more than enough for the latch circuit to build up the digital output in a short time.

The op-amp in Figure 4.13 needs to have large gain as well as high speed to establish an accurate output for the sample-and-hold amplifier. To obtain a satisfactory frequency response, the phase margin and the gain of the main amplifier as well as those of the auxiliary amplifiers must be carefully designed. The simulation results in Figure 5.6 show that the op-amp achieves a gain of 81.38dB and a unity gain frequency of more than 700MHz. The first pole is at 65kHz and the second pole is at 900MHz. The phase margin is about 55 degree.

Figure 5.6 Gain and phase plot of the op-amp in the SHA

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From Equation 4.19, the gain error is found to be 0.026% (Less than 0.1LSB) if the input capacitance is ignored. The time constant in equation 4.26 is calculated using the unity gain frequency of the op-amp

$$\tau_{SHA} \cong \frac{3C_L + C_1}{G_m} \cong \frac{2}{2\pi f_u} = 0.45ns \quad (5.1)$$

If the total settling time for the SHA is 4ns (which is less than half of a clock cycle), the error is calculated to be

$$error = e^{-\frac{t}{\tau_{SHA}}} = e^{-\frac{4}{0.45}} = 1.51 \times 10^{-4} \quad (5.2)$$

It is less than 0.05LSB for the 8-bit converter.

We can see that the amplifiers have plenty of margins on the design parameters according to the AC simulation results. However, in real situation, factors such as non-linearity would worsen the performance.

Figure 5.7 is the output waveform of the clock generator. Using digital buffers at the output, the sharp clock edges are maintained even with the loading capacitances included. The timing of this clock generator ensures the correct function of the internal building blocks of the A/D converters.

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Figure 5.7 The output waveform of the clock generator

5.3 Pre-layout Simulation Results of the Two-Step Topology

An 8-bit two-step dynamic reference ADC is implemented and simulated using the 0.18 μ m CMOS process in this research work, with 4-bit conversions for both the course bank and the fine bank. The input sampling rate of the converter is 100MSample/s. The power supply voltage is 1.8V. The pre-layout simulation results of the implemented design are presented in this section.

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Figure 5.8 Simulated DC performance of the Two-Step Topology

Figure 5.8 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) errors. We can see the DNL is within $\pm 0.36\text{LSB}$ and the INL is within $\pm 0.58\text{LSB}$. Figure 5.9 presents the FFT frequency spectrum of the output when the input signal frequency is 20MHz with peak-to-peak amplitude of 1V. The signal-to-noise and distortion ratio (SNDR) is 41.13dB. The spurious free dynamic range (SFDR) is 53.81dB. Finally, the total power consumption of the ADC under this operating condition is 9.1mW.

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Figure 5.9 FFT spectrum for the Two-Step Topology

5.4 Post-layout Simulation Results of the Pipelined Topology

The 8-bit pipelined dynamic reference ADC was also implemented using the 0.18 μ m CMOS technology, with a power supply voltage of 1.8V and maximum input voltage swing of 1.0V. The nominal sampling frequency of the converter is 100MSample/s. The post-layout simulation results are presented in this section.

Fig. 5.10 shows the differential nonlinearity and the integral nonlinearity errors. We can see the DNL is within ± 0.12 LSB and the INL is within ± 0.25 LSB. The maximum value for both INL and DNL occurs at the middle point, which is determined by the MSB stage. Since the output of this stage controls the dynamic voltage references of all subsequent ones, its performance is the most critical.

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Figure 5.10 Simulated DC performance of the Pipelined Topology

Figure 5.11 presents the FFT spectrum of the ADC at the sampling frequency of 100MS/s when the input is a sinusoidal signal of 24MHz. From the frequency spectrum it can be seen that, the Spurious-Free Dynamic Range is 56.03dB. The Signal-to-Noise-and-Distortion Ratio is 41.93dB. The power consumption under this operating condition is 15mW.

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Figure 5.11 FFT spectrum for the Pipelined topology

From the above simulation results, we can see that the pipelined design achieves better performance than the two-step one, because the comparator stages in the former have more time to settle due to the different timing arrangement from the latter, although these two designs use the same basic building blocks. However, the Pipelined converter consumes more power and occupies larger silicon area because more SHA blocks are used than the two-step one.

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Figure 5.12 SNDR & SFDR versus input frequency at sampling rate of 100MS/s

Figure 5.12 shows the simulated SNDR and SFDR when the input frequency is changing from a low value to the maximum frequency allowable for Nyquist sampling rate of 100MS/s. The SNDR drops to 37.14dB at the input frequency of 48MHz (near the half of Nyquist sampling rate). And the SFDR changes from 57.84 dB to 53.25dB.

Figure 5.13 is the simulated SNDR and SFDR when the sampling frequency is changed from 60MS/s to 130MS/s with the input frequency remaining at 24MHz. The SNDR drops from 43.88dB to 39.75dB. And the SFDR changes from 57.92dB to 54.41dB.

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Figure 5.13 SNDR & SFDR versus sampling frequency

The Performance summary of the Pipelined Dynamic Reference ADC is presented in Table 5.1 based on the post-layout simulation results. The comparison with the state-of-the-art high-speed ADC designs is shown in Table 5.2. Using the definition of Figure of Merit in Equation 2.7, we can see the proposed Pipelined Design achieves a comparable performance as the state-of-the-art ADCs in literature.

However, the measurement results would be worse than the simulation results due to noise and mismatch effect etc. Although the implemented ADC only has 8-bit resolution, the influence of noise from the internal devices such as poly resistors can only be known after the measurement.

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Table 5.1 Performance summary of the pipelined design

Technology	0.18 μ m CMOS process
Supply Voltage	1.8V
Resolution	8-bit
Sampling Rate	100MS/s
DNL	0.12LSB
INL	0.25LSB
SNDR ($F_{in} = 24\text{MHz}$)	41.93dB
SFDR ($F_{in} = 24\text{MHz}$)	56.03dB
Chip Area (including pads)	2.0 $\times$ 1.9mm ²
Power Consumption	15mW

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Table 5.2 Performance comparison with the state-of-the-art high-speed ADC design

Author/Year	Architecture	$SNDR$ (dB)	P_{diss} (mW)	f_{samp} (MS/s)	Technology (μm)	FOM
Mulder/04 [18]	Subranging	47.51	21	125	0.13	1.15×10^{12}
Srinivas/06 [21]	Flash	33.61	50	160	0.35	0.13×10^{12}
Honda/07 [32]	Pipelined	55.28	33	100	0.09	1.44×10^{12}
Wu/07 [33]	Pipelined	41.49	30	100	0.18	0.32×10^{12}
This work	Pipelined Dynamic Reference	41.93	15	100	0.18	0.85×10^{12}

Chapter 6 Conclusion and Future Works

6.1 Conclusion

In the thesis, first the background knowledge of data converters was presented. Then the performance characterization and design problems of high-speed A/D converters were stated. After that, a thorough literature review of various high-speed medium-accuracy ADC topologies was carried out, including the full Flash, Two-Step, Subranging, Pipelined, Folding and Interpolating, and Time-Interleaved architectures. The advantages and drawbacks were compared. Then some state-of-the-art high-speed A/D converters in the literature were introduced.

A study of a new topology, named the Unclocked Dynamic Reference ADC, was also carried out. A 3-b converter of such topology was implemented and simulated for functional verification. The top-down design methodology was adopted and the Verilog-AMS language was used to build the behavioral models.

After studying the disadvantages of the Unclocked Dynamic Reference design, a group of novel Multi-Step Dynamic Reference ADC topologies which includes a Two-Step converter and a Pipelined one was proposed by introducing internal clock signals. They are able to achieve higher speed and better accuracy than the unclocked ADC due to the following reasons. Firstly, the auto-zero technique is employed to reduce the comparator offset voltage tremendously. Secondly, by proper timing arrangement, the pipelining operation is enabled to realize a conversion rate of 1 sample/cycle. Thirdly, Multi-Step implementation reduces the number of comparators

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through which the internal signals need to propagate during each conversion cycle. Fourthly, by defining sampling instance using internal clock signal, glitches are totally removed from the ADC output. Finally, the fully differential implementation reduces the odd harmonic distortion and the noise due to channel charge injection. For the two topologies proposed in this work, the Two-Step converter has less hardware complexity and shorter conversion latency than the Pipelined one, whereas the latter can achieve higher accuracy.

For the Two-Step Dynamic Reference ADC, the number of comparators is the same as the intended number of bit resolutions. Because of the much less hardware complexity than the conventional two-step ADC, more power budget can be allocated to the individual comparator, so that the settling time can be reduced to increase the conversion speed.

Compared with the conventional Pipelined ADC, the Pipelined Dynamic Reference design also can potentially achieve higher speed and better accuracy as the dedicated D/A converter and the residue amplifier are eliminated from each stage. One of the major drawbacks of this design is that the accuracy of the comparator must be high since the digital error correction technique is not utilized. This problem can be solved by using offset-compensated high-speed comparator. The other drawback is that N S/H amplifiers are needed for an N -bit Pipelined topology. However, only the S/H amplifier of the first stage needs to have high performance, because for all subsequent S/H amplifiers the input signal has already been sampled. This greatly relaxes the circuit requirement.

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The major disadvantage of the proposed architectures is due to the global and local mismatch of the current sources and resistors, which may result in inaccurate reference voltages. The author tried to address it using circuit and layout techniques. However, the effect can only be verified from measurement of the prototype chip.

The basic building blocks are also designed for the proposed architectures. The Pipelined topology and the Two-Step one use the same building blocks although the configurations and timing arrangements are different. For the comparator, auto-zero technique is utilized to reduce offset voltage. It has preamplifier stage followed by latch circuit to realize high-speed comparison. Channel-charge-injection errors are eliminated by using proper clock scheme. The sample-and-hold amplifier uses two pair of feedback capacitors to hold the output for a full clock cycle, so that the interleaving technique could be abandoned for better matching. The op-amp in the SHA employs a folded-cascode structure with gain boosting to achieve large gain and fast response. Common-mode feedbacks are applied for proper operation. R-2R resistor network and the current steering circuit are used to establish the dynamic reference for the proposed topologies. Amplifier is employed in feedback loop to ensure reference voltages are produced accurately. The clock generator and the bias circuit are also designed properly for the function of the converters.

An 8-bit Two-Step Dynamic Reference ADC was implemented using the 0.18 μ m CMOS 1P6M process. The pre-layout simulation indicates that it can achieve a DNL of 0.36LSB and an INL of 0.58LSB. On the aspect of dynamic performance, the SNDR and SFDR are 41.13dB and 53.42dB using input with a frequency of 20MHz.

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An 8-bit Pipelined Dynamic Reference ADC was also implemented using the same process. The layout of the converter has been completed. From the post-layout simulation, it was found to have a DNL of 0.12LSB and an INL of 0.25LSB. Its SNDR and SFDR are 41.93dB and 56.03dB when using input with a frequency of 24MHz. The dynamic performance for different input frequency and sampling frequency was also characterized. The Pipelined design is found to have comparable performance with the state-of-the-art high-speed ADCs in literature.

6.2 Future Works

The layout of the 8-bit Pipelined Dynamic Reference ADC has been sent out for fabrication. An on-wafer testing would be conducted for static and dynamic performance characterization when the prototype die returns.

The layout area in Figure 5.4 is large due to the large routing space required. It could be revised in the future to reduce the active area that is occupied by metal wires. Local matching of resistors is believed to be one of the major factors to restrict the ADC performance. More layout technique should be used to reduce the errors due to resistor matching. Calibration might also be employed to enhance the accuracy of resistor network and current steering circuit.

Digital error correction is an effective method to reduce the hardware requirement and improve the accuracy of modern high-speed ADC. In the proposed Multi-Step Dynamic Reference ADC topologies, we could try to include it so that a better tradeoff between speed and accuracy can be achieved to realize a higher performance.

Author's Publications

Author's Publications

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IEEE European Conference on Circuit Theory and Design 2007, pp. 232-235,
Seville, Spain, Aug. 2007.

- [2]. Li Danping, Siek Liter, “A Pipelined Dynamic Reference A/D converter”,
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